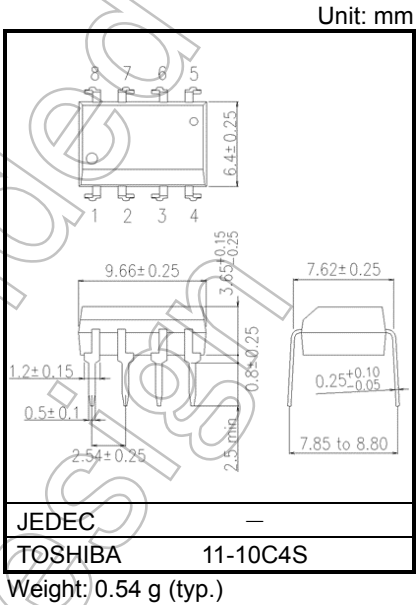


TLP554

Isolated Line Receiver
Simplex/Multiplex Data Transmission
Computer-Peripheral Interface
Microprocessor System Interfaces
Digital Isolation for A/D, D/A Conversion

The TOSHIBA TLP554 a photocoupler which combines an infrared emitting diode and an integrated high gain, high speed photodetector.
The output of the detector circuit is an open collector, Schottky Clamped transistor.
A Faraday shield integrated on the photodetector chip reduces the effects of capacitive coupling between the input LED emitter and the high gain stages of the detector. This provides an effective common mode transient immunity of 1000 V/ μ s.

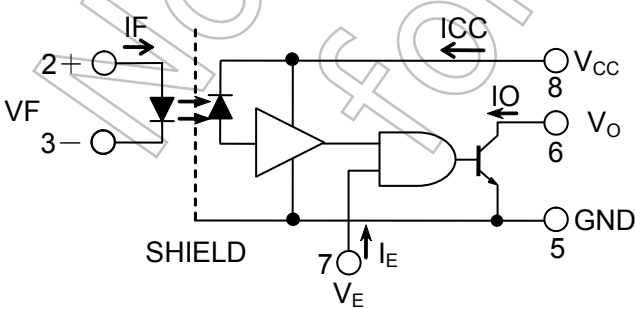
- Input Current Threshold
 - Switching Speed
 - Common mode transient immunity
 - Guaranteed Performance over Temperature
 - Isolation Voltage
 - UL-recognized
 - cUL-recognized
- : IF = 5 mA (max)
 - : 10 MBd (typ. @NRZ)
 - : ± 1000 V/ μ s (min)
 - : 0 to 70°C
 - : 2500 Vrms (min)
 - : UL 1577, File No.E67349
 - : CSA Component Acceptance Service No.5A
- File No.E67349



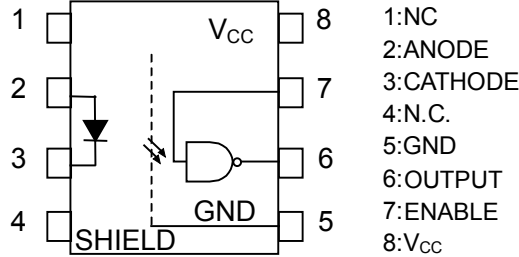
Truth Table

INPUT	ENABLE	OUTPUT
H	H	L
L	H	H
H	L	H
L	L	H

Schematic



PIN CONFIGURATION (TOP VIEW)



Start of commercial production
1985-01

Recommended Operating Conditions

Characteristic	Symbol	Min	Typ.	Max	Unit
Low Level input Voltage	V _{FL}	-3	0	1.0	V
High Level input current	I _{FH}	6.3 (Note 1)	—	20	mA
Supply Voltage (Note 2)	V _{CC}	4.5	5	5.5	V
High-Level Enable Voltage	V _{EH}	2.0	—	V _{CC}	V
Low-Level Enable Voltage	V _{EL}	0	—	0.8	V
Fan Out(TTL Load)	N	—	—	8	—
Operating Temperature	T _{opr}	0	—	70	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Note 1: 6.3 mA condition permits at least 20 % CTR degradation. Initial switching threshold is 5.0 mA or less.

Note 2: Denotes the operating range, not the recommended operating condition.

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
LED	Forward current	I _F	20	mA
	Forward current derating (Ta > 85°C)	ΔI _F /ΔTa	-1.6	mA/°C
	Reverse voltage	V _R	5	V
	Input power dissipation	P _D	100	mW
	Input power dissipation derating (Ta > 85°C)	ΔP _D /°C	-2.5	mW/°C
DETECTOR	Output current	I _O	25	mA
	Output voltage	V _O	-0.5 to 7	V
	Supply voltage (Note 1)	V _{CC}	7	V
	Enable voltage (Note 2)	V _E	5.5	V
	Output power dissipation	P _O	40	mW
	Output power dissipation derating (Ta > 85°C)	ΔP _O /ΔTa	-2.6	mW/°C
Storage temperature range		T _{stg}	-55 to 125	°C
Operating temperature range		T _{opr}	-40 to 85	°C
Lead soldering temperature (10 s) (Note 3)		T _{sol}	260	°C
Isolation voltage (AC, 60 s, R.H. ≤ 60 %) (Note 4)		BV _S	2500	V _{rms}

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: 60 s Maximum.

Note 2: Not to exceed V_{CC} by more than 500 mV.

Note 3: 2 mm below seating plane.

Note 4: Device considered a two-terminal device :Pins 1, 2, 3 and 4 shorted together, and Pins 5, 6, 7 and 8 shorted together.

Electrical Characteristics

(Unless otherwise specified $T_a = 0$ to 70°C , $V_{CC} = 4.5$ to 5.5 V , $V_{FL} \leq 1.0\text{ V}$)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Forward Voltage		V_F	$I_F = 10\text{ mA}$, $T_a = 25^\circ\text{C}$	—	1.65	1.80	V
Temperature Coefficient of Forward Voltage		$\Delta V_F / \Delta T_a$	$I_F = 10\text{ mA}$	—	-2.0	—	mV/ $^\circ\text{C}$
Input Reverse Current		I_R	$V_R = 5\text{ V}$, $T_a = 25^\circ\text{C}$	—	—	10	μA
Input Capacitance		C_T	$V_F = 0\text{ V}$, $f = 1\text{ MHz}$, $T_a = 25^\circ\text{C}$	—	45	—	pF
High-Level Output Current		I_{OH}	$V_F = 1.0\text{ V}$, $V_O = 5.5\text{ V}$ $V_E = 2.0\text{ V}$	—	10	250	μA
			$V_F = 1.0\text{ V}$, $V_O = 5.5\text{ V}$ $V_E = 2.0\text{ V}$, $T_a = 25^\circ\text{C}$	—	0.5	10	
Low-Level Output Voltage		V_{OL}	$I_F = 5\text{ mA}$, $V_E = 2.0\text{ V}$ $I_{OL} = 13\text{ mA}$ (Sinking)	—	0.4	0.6	V
High Level input current		I_{FH}	$I_{OL} = 13\text{ mA}$ (Sinking) $V_E = 2.0\text{ V}$, $V_{OL} = 0.6\text{ V}$	—	—	5	mA
Supply Current	High Level	I_{CCH}	$V_{CC} = 5.5\text{ V}$, $I_F = 0\text{ mA}$, $V_E = 0.5\text{ V}$	—	7	15	mA
	Low Level	I_{CCL}	$V_{CC} = 5.5\text{ V}$, $I_F = 10\text{ mA}$ $V_E = 0.5\text{ V}$	—	12	19	
Enable Current	High Level	I_{EH}	$V_{CC} = 5.5\text{ V}$, $V_E = 2.0\text{ V}$	—	-1.0	—	mA
	Low Level	I_{EL}	$V_{CC} = 5.5\text{ V}$, $V_E = 0.5\text{ V}$	—	-1.6	-2.0	
Enable Voltage	High Level	V_{EH}	(Note 1)	2.0	—	—	V
	Low Level	V_{EL}	—	—	—	0.8	
Resistance (Input-Output)		R_S	$V_S = 500\text{ V}$, R.H. $\leq 60\%$, $T_a = 25^\circ\text{C}$, (Note 2)	5×10^{10}	10^{14}	—	Ω
Capacitance (Input-Output)		C_S	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$, $T_a = 25^\circ\text{C}$ (Note 2)	—	0.6	—	pF

Note: All typ. values are at $T_a = 25^\circ\text{C}$

Note 1: No pull up resistor required as the device has an internal pull up resistor.

Note 2: Device considered a two-terminal device :Pins 1, 2, 3 and 4 shorted together, and Pins 5, 6, 7 and 8 shorted together.

Switching Characteristics (Ta = 25°C, VCC = 5 V)

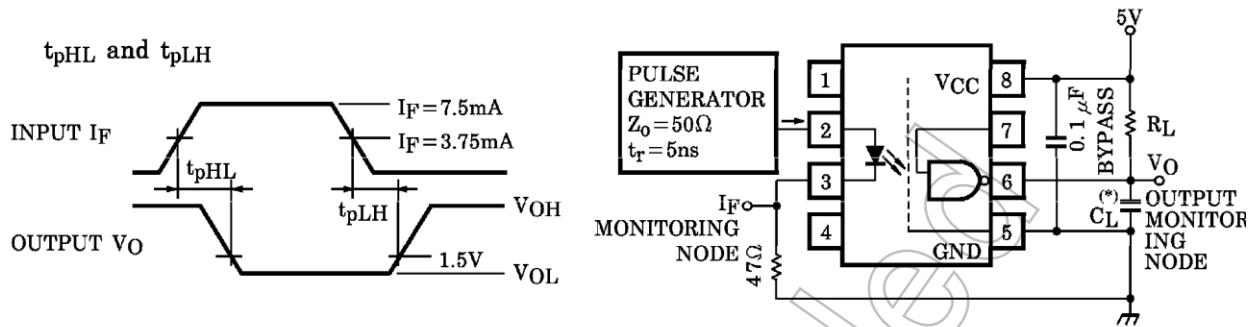
Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation Delay Time (L→H)	t _{pLH}	1	I _F = 7.5→0 mA, R _L = 350 Ω C _L = 15 pF	—	60	120	ns
Propagation Delay Time (H→L)	t _{pHL}		I _F = 0→7.5 mA, R _L = 350 Ω C _L = 15 pF	—	60	120	
Output Rise Time(10-90%)	t _r		I _F = 7.5→0 mA, R _L = 350 Ω C _L = 15 pF	—	30	—	
Output Fall Time(90-10%)	t _f		I _F = 0→7.5 mA, R _L = 350 Ω C _L = 15 pF	—	30	—	
Enable Propagation Delay Time (L→H)	t _{ELH}	2	V _E = 0.5→3.0 V, R _L = 350 Ω I _F = 7.5 mA, C _L = 15 pF	—	25	—	ns
Enable Propagation Delay Time (H→L)	t _{EHL}		V _E = 3.0→0.5 V, R _L = 350 Ω I _F = 7.5 mA, C _L = 15 pF	—	25	—	
Common Mode Transient Immunity at Hight Level Outout (Note 1)	CM _H	3	I _F = 0 mA, R _L = 350 Ω V _{CM} = 400 V, V _{O(min)} = 2 V	1000	10000	—	V/μs
Common Mode Transient Immunity at Low Level Outout (Note 2)	CM _L		I _F = 7.5 mA, R _L = 350 Ω V _{CM} = 400 V, V _{O(max)} = 0.8 V	-1000	-10000	—	

Note: A ceramic capacitor (0.1 μF) should be connected from pin 8 (V_{CC}) to pin 5 (GND) to stabilize the operation of the high gain linear amplifier. Failure to provide the bypass may impair the switching property.
The total lead length between capacitor and coupler should not exceed 1 cm.

Note 1: CM_H is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 2.0 V)

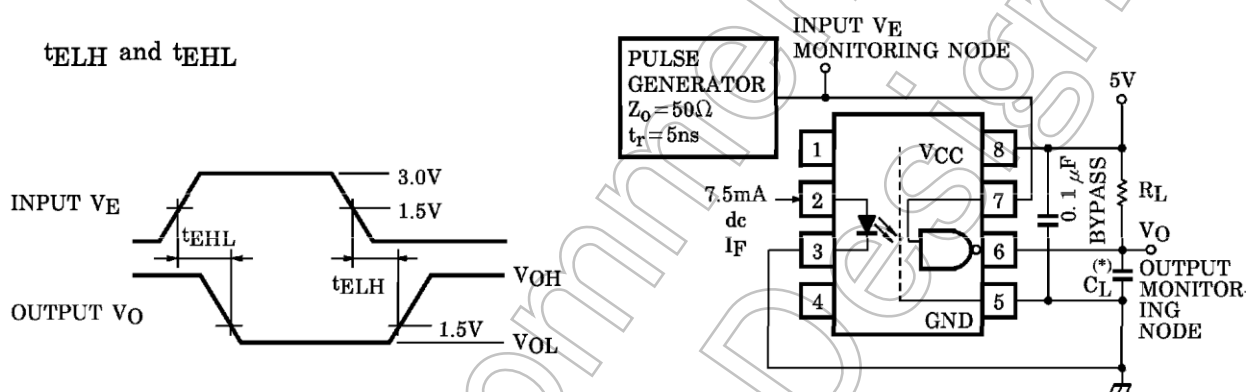
Note 2: CM_L is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8 V).

TEST CIRCUIT 1.



(*) C_L is approximately 15pF which includes probe and stray wiring capacitance.

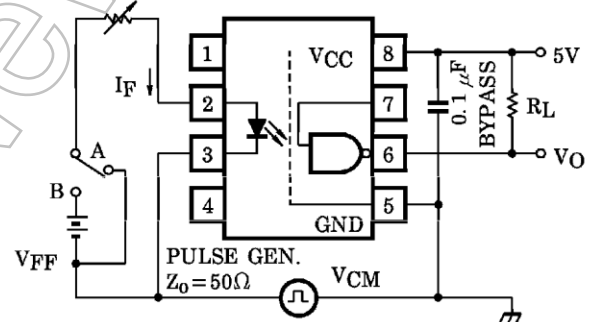
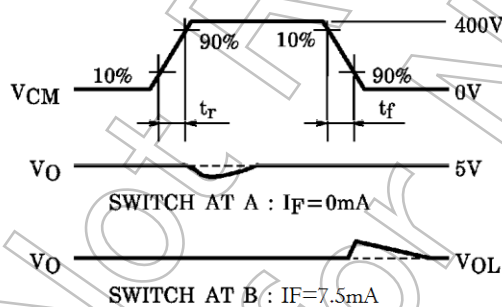
TEST CIRCUIT 2.



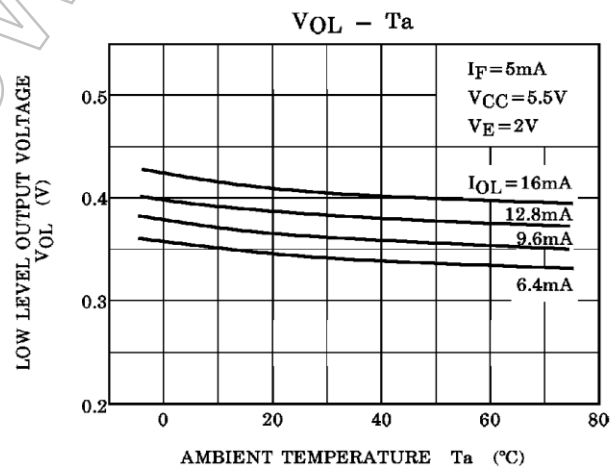
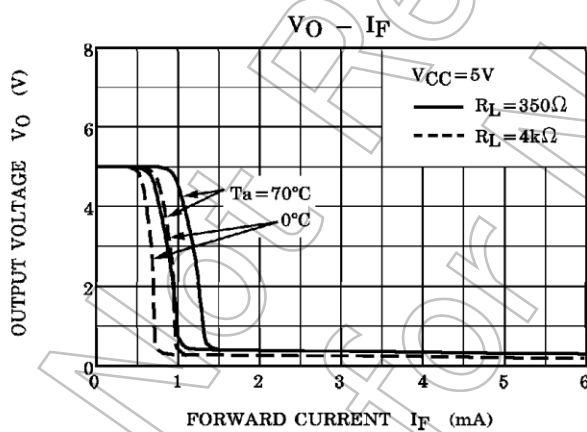
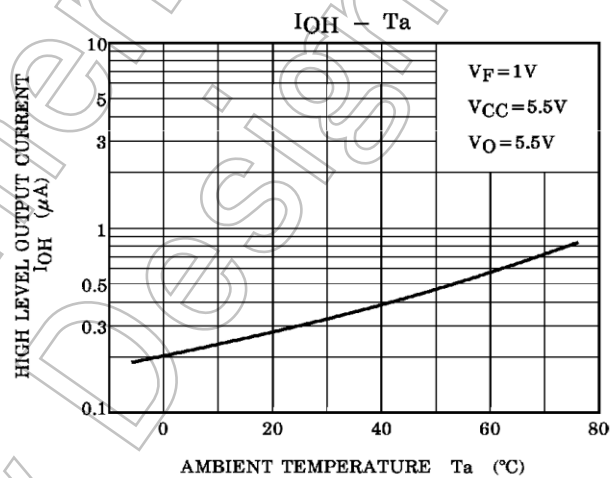
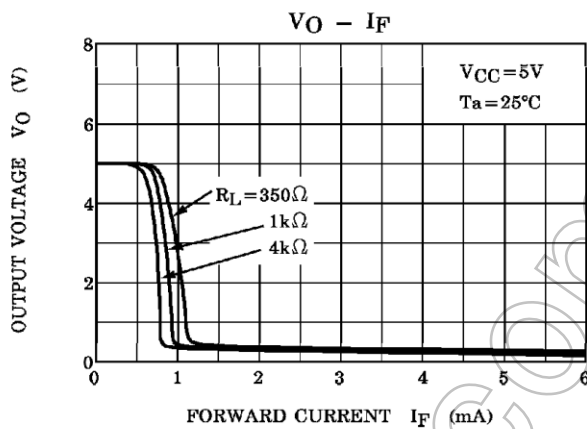
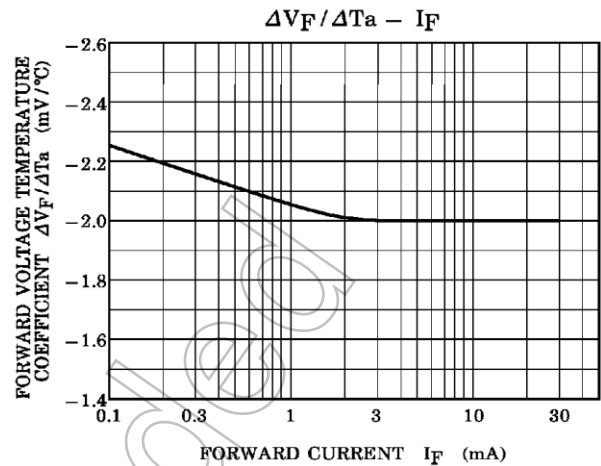
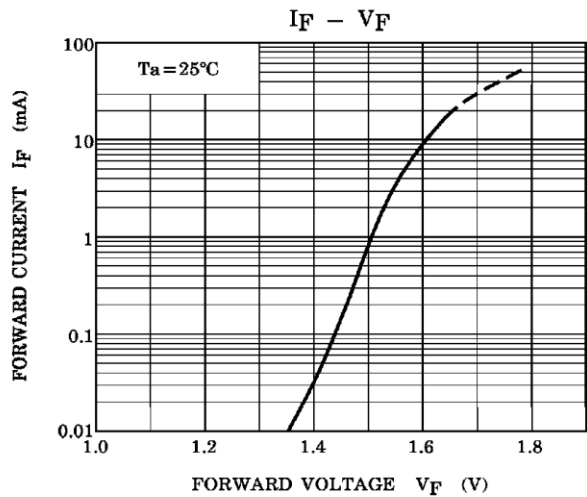
(*) C_L is approximately 15pF which includes probe and stray wiring capacitance.

TEST CIRCUIT 3.

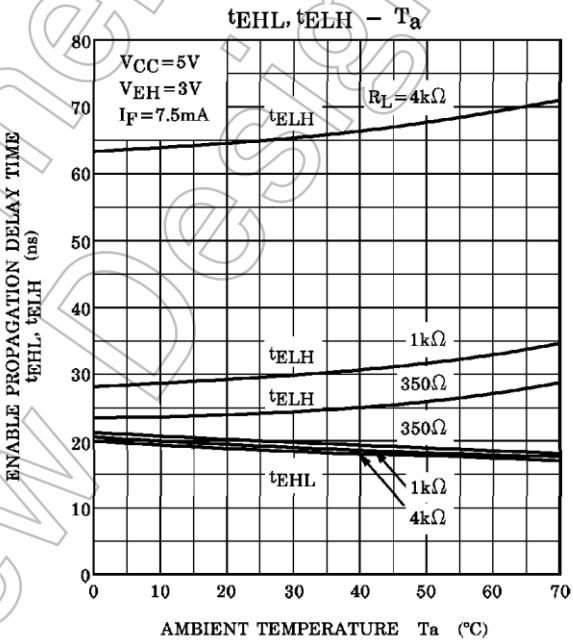
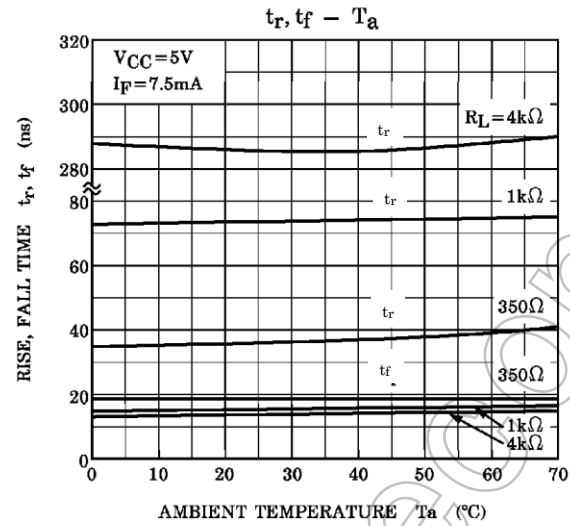
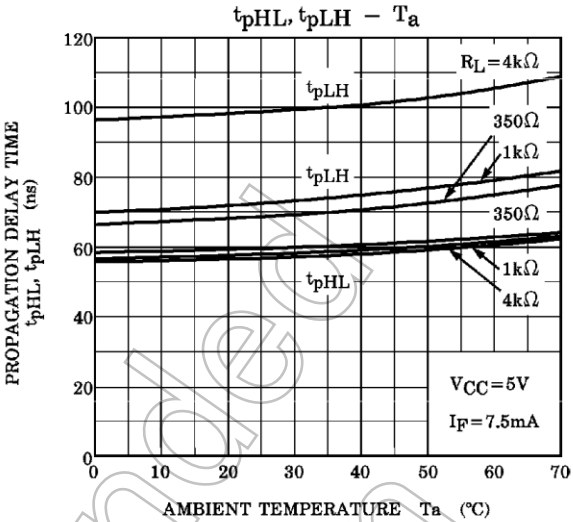
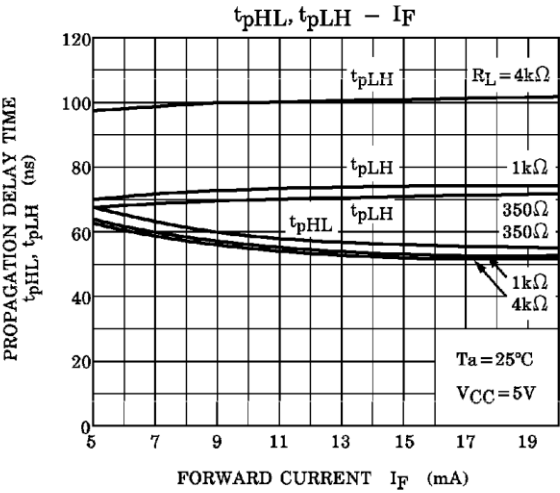
Transient Immunity and Typ. Waveforms.



$$CM_H = \frac{320(\text{V})}{t_r(\mu\text{s})}, \quad CM_L = \frac{320(\text{V})}{t_f(\mu\text{s})}$$



NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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