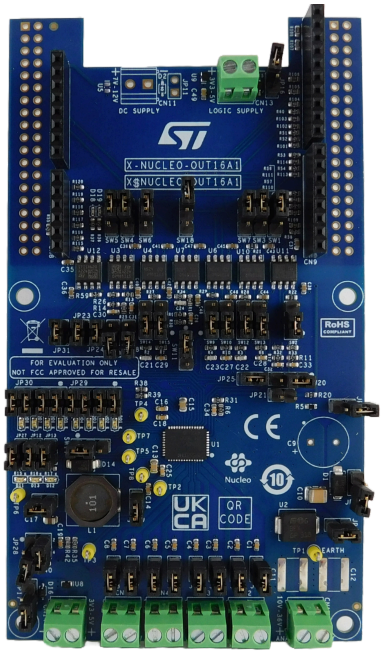
X-NUCLEO-OUT16A1

Data brief

Industrial digital output expansion board based on IPS8200HQ for STM32 Nucleo



Features

- Based on the IPS8200HQ octal high-side switch, which features:
  - Operating range 10.5 to 36 V
  - Operating output current ≤ 0.7A
  - Low power dissipation ($R_{ON(MAX)}$ = 200 mΩ)
  - Undervoltage lock-out
  - Selectable driving modes parallel or 5 MHz SPI (8 or 16 bits)
  - Embedded step-down converter
  - 4x2 LED matrix for efficient status indication
  - MCU freeze detection
  - Fast decay for inductive loads
  - Overload and overtemperature protections
  - Loss of ground protection
  - Junction Overtemperature and parity check diagnostic pin (FAULT)
  - Case overtemperature diagnostic pin (TWARN)
  - Supply voltage Level diagnostic pin (PGOOD)
  - QFN48L 8x6 mm package
- Application board voltage operating range: 12 to 33 V
- Extended voltage operating range (J9 open) up to 36 V
- Operating current: up to 0.7 A per channel
- Blue LED showing SPI mode selection
- Yellow LED showing SPI mode 16-bits selection
- Red LED for FAULT diagnostic pin (JP12 closed)
- Red LED for PGOOD diagnostic pin (JP13 closed)
- Red LED for TWARN diagnostic pin (JP27 closed)
- 4 kV_{PK} galvanic isolation guaranteed by STISO620 and STISO621
- Supply rail reverse polarity protection
- Compatible with STM32 Nucleo development boards
- Equipped with Arduino® UNO R3 connectors
- RoHS and China RoHS compliant
- CE certified

Product summary	
Industrial digital output expansion board based on IPS8200HQ for STM32 Nucleo	X-NUCLEO-OUT16A1
Software expansion for STM32Cube driving industrial digital output based on intelligent power switch (IPS)	X-CUBE-IPS
Octal high-side smart power solid-state relay	IPS8200HQ
Applications	Programmable Logic Controllers

Description

The X-NUCLEO-OUT16A1 industrial digital output expansion board, for STM32Nucleo, provides a powerful and flexible environment for the evaluation of the driving and diagnostic capabilities of the IPS8200HQ octal high-side smart power solid state relay, in a digital output module connected to 0.7 A industrial loads.

The X-NUCLEO-OUT16A1 interfaces with the microcontroller on the STM32 Nucleo via STISO620 and STISO621 and Arduino® R3 connectors. The user can select which driving mode controls the IPS8200HQ: Parallel (SEL2 = L by JP21 = open) or SPI (SEL2 = H by JP21 = closed). In the case of SPI selection, the user can select the communication protocol between 8 bits (SEL1 = L by JP22 = open) or 16 bits (SEL1 = H by JP22 = closed).

The V_{CC} supply pin of the IPS8200HQ is provided by the connector CN1, while the loads (driven by the eight output channels of the IPS8200HQ) can be connected between the connectors CN2, CN3, CN4, CN12, and the pin 2 of the connector CN1.

The on-board digital isolators (STISO620 and STISO621) feature the 2.8k V_{RMS} (4k V_{PK}) galvanic isolation between the two application sides: Logic and process sides.

The logic side is the application side of the MCU and it is supplied by the VISO_L rail (3.3 V or 5.0 V). VISO_L can be supplied by an external power supply connected to CN13 or, alternatively by the pin 4 (SW1 = close 1-2) or pin 5 (SW1 = close 2-3) of CN6.

The process side is the application side of the industrial loads and it is supplied by the VCC and VISO_P rails. The VISO_P (3.3 or 5.0 V) is usually supplied by the VREG rail (JP31 = closed) that can be generated by the step-down embedded in the IPS8200HQ (SW17 = close 1-2, JP20 = closed, JP15 = closed and JP28 = close 2-4 (VREG = 3.3 V) or JP28 = 1-3 (VREG = 5.0 V)). Alternatively, VREG can be provided by an external power supply connected to CN14 (SW17 = close 2-3, JP20 = open, JP15 = open).

In parallel driving mode (active with the default jumper and switch settings) the application board can work even without any Nucleo board: in this case, the user must provide the process side voltage (usually 24 V) by the CN1 and the VISO_L (usually 3.3 V) by the CN13. The IN_X signals, available on CN5[1, 2, 3], CN8[4] and CN9[3, 5, 7, 8], drive on/off the correspondent OUT_X connected to the loads on the process side. The IN_X pins can be driven low/high swinging between 0V and VISO_L. The activation of each OUTX (OUT1… OUT8) can be monitored by the green LEDs DOX (DO1… DO8).

The activation of the three diagnostic pins (TWARN, PGOOD, FAULT) can be visualized on the correspondent red LEDs (D11, D12, D13, respectively) or monitored by an oscilloscope on TP6, TP7, and TP5.

Note: Although the pins CN8[5], CN5[9], CN5[10] are connected to the nets FAULT_L, PGOOD_L and TWARN_L, these pins cannot correctly report the status of the corresponding signals on the process side (FAULT, PGOOD, and TWARN) due to routing mistake on the same side.

The SPI driving mode can be set by changing the default configuration (JP21 = close; SW4, SW5, SW6, SW7, SW9, SW10, SW11, SW12, SW13, SW14, SW15, and SW20 = close 2-3, SW18 = close 1-2). The SPI-8bits is the default mode (JP22 = open), while the SPI-16bits mode can be activated by JP22 = close.

In SPI driving mode it is also possible to activate the MCU freeze detection feature by setting SW3 = close 2-3.

The expansion board can be connected to either a NUCLEO-F401RE or a NUCLEO-G431RB development board. In this case the companion firmware X-CUBE-IPS detects the selected configuration (GPIO, SPI-8bits, SPI-16bits) by reading the signals SEL2_L and SEL1 from CN8[1] and CN8[6]. The activation of the MCU freeze feature is detected by WDEN(in) on CN9[4].

It is also possible to evaluate a system composed of a X-NUCLEO-OUT16A1 stacked on other expansion boards. In fact, SPI driving mode allows the daisy-chaining communication with another X-NUCLEO-OUT16A1 stacked through the Arduino connectors: the two stacked boards must be configured with SW6, SW18 = close 2-3 on one board, and SW6, SW18 = close 1-2 on the other board.

1 Schematic diagrams

Figure 1. **X-NUCLEO-OUT16A1 circuit schematic (1 of 3)**

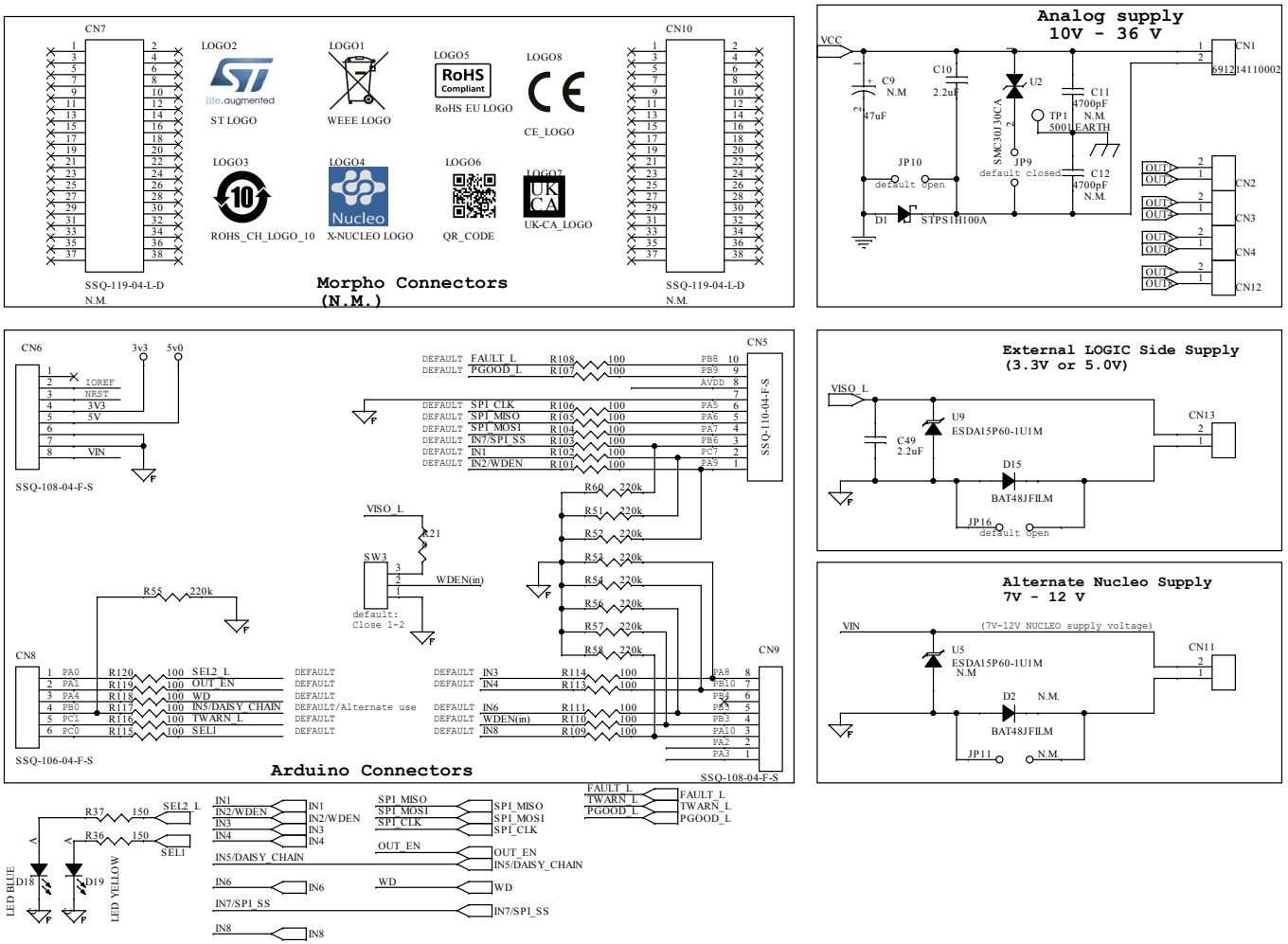


Figure 2. X-NUCLEO-OUT16A1 circuit schematic (2 of 3)

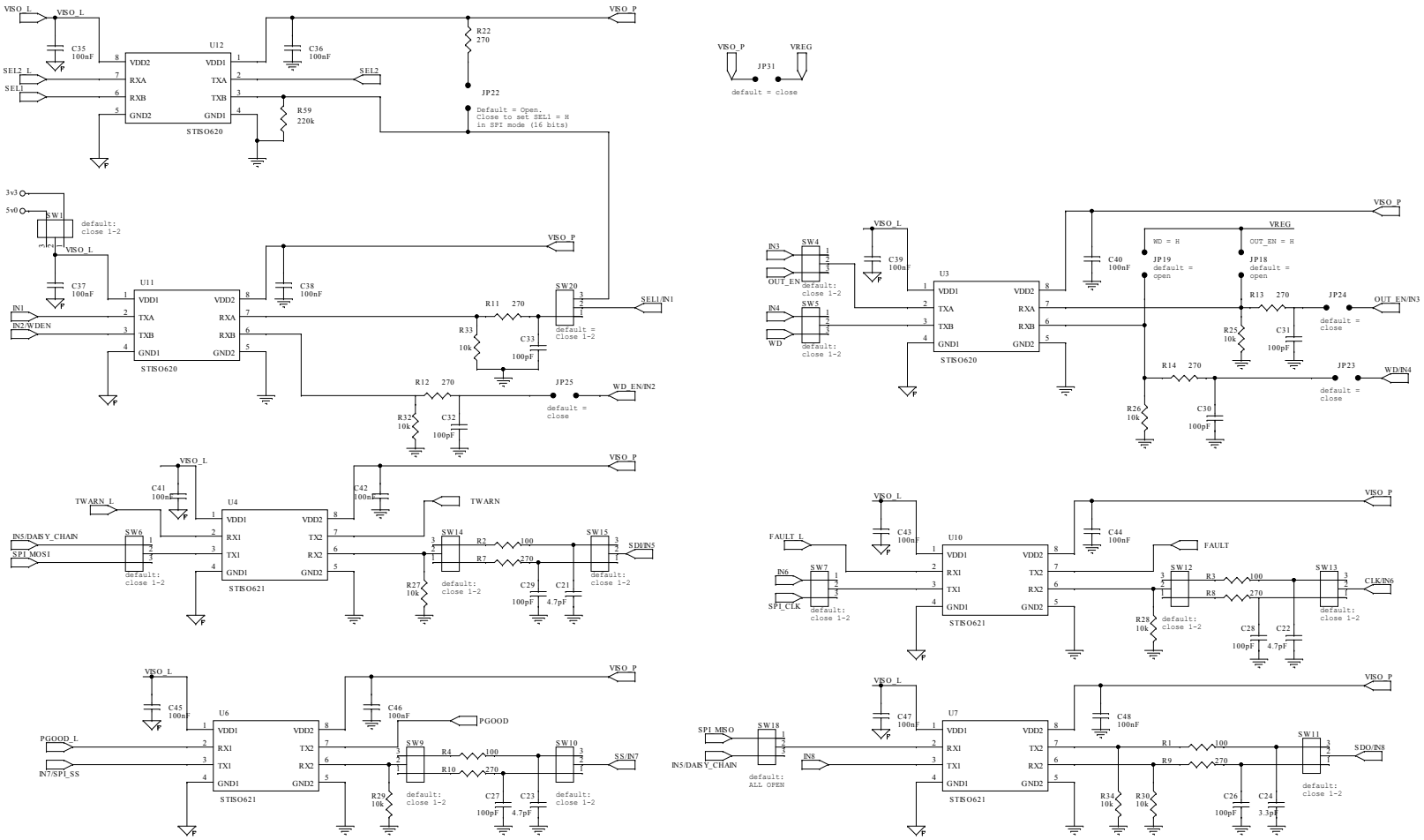
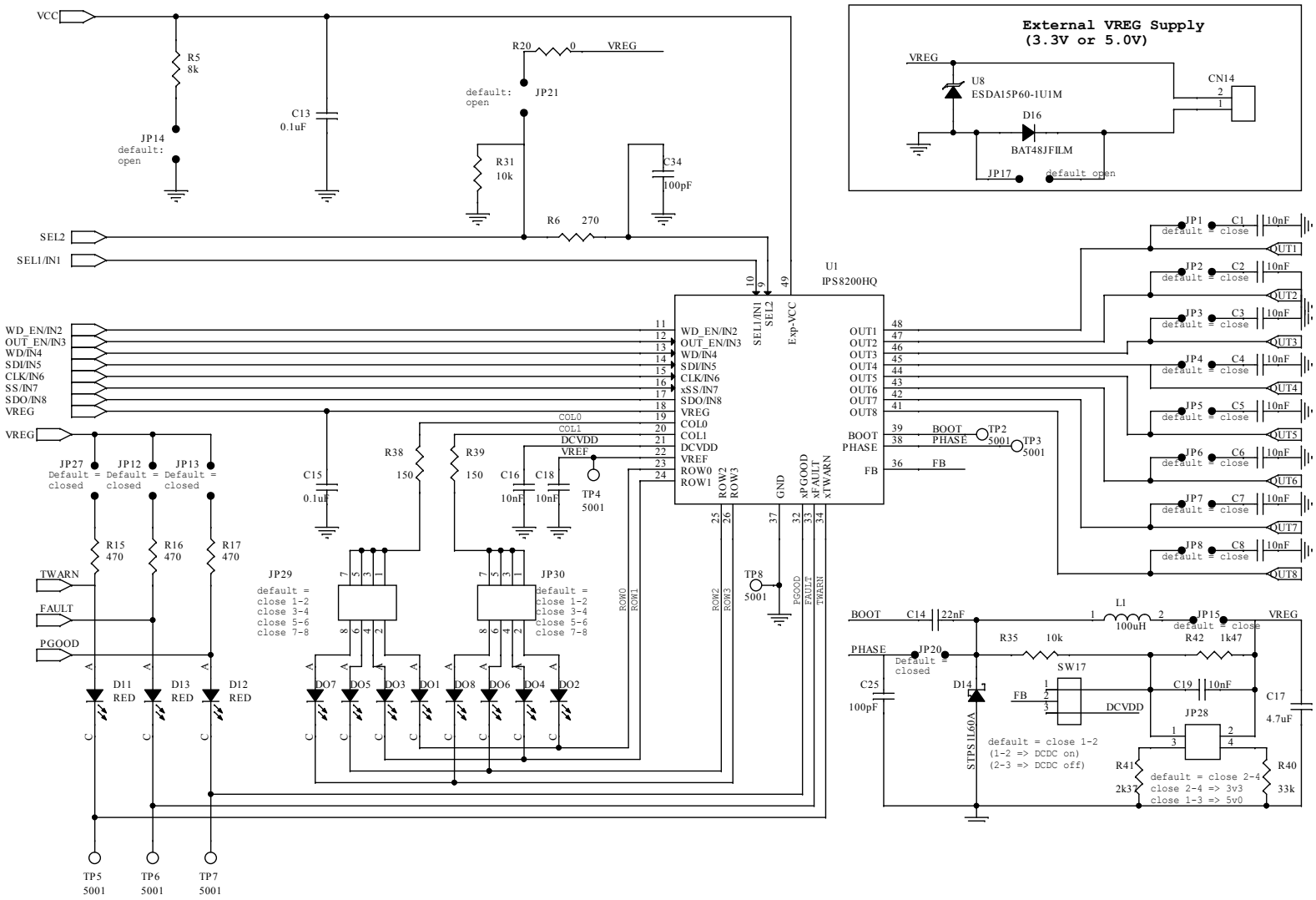


Figure 3. **X-NUCLEO-OUT16A1 circuit schematic (3 of 3)**



2 Board versions

Table 1. **X-NUCLEO-OUT16A1 versions**

Finished good	Schematic diagrams	Bill of materials
X$NUCLEO-OUT16A1 (1)	X$NUCLEO-OUT16A1 schematic diagrams	X$NUCLEO-OUT16A1 bill of materials

1. *This code identifies the X-NUCLEO-OUT16A1 evaluation board first version.*

Revision history

Table 2. **Document revision history**

Date	Revision	Changes
13-Oct-2023	1	Initial release.
24-Apr-2024	2	Updated description.