Features

This LSI has following features

RZ/G2H

- Four 1.5-GHz Arm® Cortex®-A57 MPCore™ cores,
- Four 1.2-GHz Arm® Cortex®-A53 MPCore™ cores,
- Memory controller for LPDDR4-3200 with 32 bits × 2 channels,
- 1 channel for HDMI1.4b output (*1) and 1 channel for RGB888 output and 1channel for LVDS,
- 2 channels MIPI-CSI2 Video Input, 2 channels digital Video Input,
- Serial ATA interface,
- USB3.0 × 1 channel and USB2.0 × 2 channels,

RZ/G2M V1.3 RZ/G2M V3.0

- Two 1.5-GHz Arm® Cortex®-A57 MPCore™ cores,
- Four 1.2-GHz Arm® Cortex®-A53 MPCore™ cores,
- Memory controller for LPDDR4-3200 with 32 bits × 2 channels,
- 1 channel for HDMI1.4b output (*1) and 1channel for RGB888 output and 1channel for LVDS,
- 2 channels MIPI-CSI2 Video Input, 2channels digital Video Input,
- USB3.0 × 1 channel and USB2.0 × 2 channels,

RZ/G2N

- Two 1.5-GHz Arm® Cortex®-A57 MPCore™ cores,
- Memory controller for LPDDR4-3200 with 32 bits × 1 channel,
- 1 channel for HDMI1.4b output (*1) and 1channel for RGB888 output and 1channel for LVDS,
- 2 channels MIPI-CSI2 Video Input, 2 channels digital Video Input,
- Serial ATA interface,
- USB3.0 × 1 channel and USB2.0 × 2 channels,

RZ/G2E

- Two 1.2-GHz Arm® Cortex®-A53 MPCore™ cores,
- Memory controller for DDR3L-1856 * with 32 bits × 1 channel,
- 1 channel for RGB888 output and 2 channels for LVDS,
- 1 channel MIPI-CSI2 Video Input, 2 channels digital Video Input,
- USB3.0 × 1 channel and USB2.0 × 1 channel,

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

- 800-MHz Arm® Cortex®-R7 core (*1),
- Three-dimensional graphics engines,
- Sound processing units,
- SD host interface,
- PCI Express interface,
- Video processing units,
- CAN interface, and
- EthernetAVB interface.

Note 1. In case of using this function, please contact a Renesas Electronics sales representative.

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Section 1 Overview

1.1 Outline of Specification

1.1.1 Arm Core

Item	Description
System CPU Cortex-A57 RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N	RZ/G2H • Arm Cortex-A57 Quad MPCore 1.5 GHz • L2 cache 2 Mbytes (ECC) RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N • Arm Cortex-A57 Dual MPCore 1.5 GHz • L2 cache 1 Mbytes (ECC) RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N • L1 I/D cache 48/32 Kbytes (Parity/ECC) • NEON™/VFPv4 supported • Security extension supported • Virtualization supported • Armv8 architecture
System CPU Cortex-A53 RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2E	RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 • Arm Cortex-A53 Quad MPCore 1.2 GHz • L1 I/D cache 32/32 KBytes (Parity/ECC), L2 cache 512 Kbytes (ECC) RZ/G2E • Arm Cortex-A53 Dual MPCore 1.2 GHz • L1 I/D cache 32/32 KBytes (Parity/ECC), L2 cache 256 Kbytes (ECC) RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2E • NEON™/VFPv4 supported • Security extension supported • Virtualization supported • Armv8 architecture
Debug and Trace (For All Products)	• JTAG/SWD I/F supported RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 • ETM-A57/A53 supported (each CPU) RZ/G2N • ETM-A57 supported RZ/G2E • ETM-A53 supported RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E • ETF 16 KBytes for program flow trace (each cluster)

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1.1.2 CPU Core Peripherals

Item	Description
Clock Pulse Generator (CPG) (For All Products)	• Generates the clocks from external clock (EXTAL). RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N — Maximum Cortex-A57 clock: 1.5 GHz RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2E — Maximum Cortex-A53 clock: 1.2 GHz RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E — Maximum 3DGE clock: 600 MHz RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N — Maximum AXI-bus clock: 400 MHz — Maximum SDRAM bus clock: 1600 MHz (LPDDR4-3200) — Maximum media clock: 400 MHz RZ/G2E — Maximum AXI-bus clock: 266 MHz — Maximum SDRAM bus clock: 928 MHz (DDR3L-1856) — Maximum media clock: 266 MHz RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E • System-CPU shut down mode control supported • Module-standby mode supported • Includes module reset registers to control reset operation of individual on-chip peripheral modules
System Controller (SYSC) (For All Products)	• Shuts down and restores power to target modules Target modules: RZ/G2H — Cortex-A57 (with independent shutting down of CPUs 0, 1, 2, 3, and SCU+L2 cache) * RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N — Cortex-A57 (with independent shutting down of CPUs 0, 1 and SCU+L2 cache) * RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 — Cortex-A53 (with independent shutting down of CPUs 0, 1, 2, 3, and SCU+L2 cache) * — 3DGE — VCP RZ/G2E — Cortex-A53 (with independent shutting down of CPUs 0, 1 and SCU+L2 cache) * *: SCU and L2 cache are treated as one power-domain. When CPU is working, SCU+L2 cache cannot be powered off. • Low leakage standby mode supported
RESET (For All Products)	• Includes one reset-signal external output port for external modules • Includes Boot Address Register, etc.

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Item	Description
Pin function controller (PFC) (For All Products)	• Setting multiplexed pin functions for LSI pins Function of the LSI pin selectable by setting the registers in the PFC module • Module selection Enable and disable the functions of LSI pins to which pin functions from multiple pin groups are assigned by setting the registers in the PFC module. • Pull-up/down control for each LSI pin On/off and up/down of the pull register on each LSI pin can be controlled by setting the registers in the PFC module.Control of SDIO functions SDIO functions, including the driving ability of pins for the SDIF, can be controlled by setting registers of the PFC.
General-purpose I/O (GPIO) (For All Products)	• General-purpose I/O ports • Supports GPIO interrupts
Thermal sensor / Chip Internal Voltage Monitor (THS/CIVM *) (For All Products)	RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N • 3 channels of thermal sensor RZ/G2E • 1 channel of thermal sensor RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E • Programmable 3 temperature level for the sensor, to indicate the temperature level • Interrupt when the temperature reaches programmed * : RZ/G2E does not support CIVM.

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1.1.3 External Bus Module

Item	Description
External Bus Controller for EX-Bus (LBSC) (For All Products)	• EX-BUS interface: max. 16-bit bus RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N • Frequency: 66 MHz or 44.4 MHz RZ/G2E • Frequency: 66 MHz RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E • External area divided into several areas and managed — Allocation to space of area 0, area 1 — Area 0 supports 1-MByte memory space (startup mode). — I/F settings, bus width settings, and wait state insertion are possible for each area. • SRAM interface — Wait states can be inserted through register settings. Period of waiting is set in cycle unit, and the maximum value is 15. — EX_WAIT pin can be used for wait state insertion. — Connectable bus widths: 16 bits or 8 bits • Supports external buffer enable/direction control • Supports Burst ROM interface • Supports Byte-control SRAM interface
External Flash Controller (For All Products)	• Supports RPC-IF (Reduced Pin Count interface) flash memory or QSPI flash memory RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N Max. Frequency 160 MHz (320MB/s) for RPC-IF, 80 MHz (80MB/s)* for QSPI (QSPI0) RZ/G2E Max. Frequency 150 MHz (300MB/s) for RPC-IF, 80 MHz (80MB/s) for QSPI (QSPI0) RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E Dual QSPI operation for two 4-bit serial flash memories is also available; 80 MHz (160MB/s)* for Dual QSPI (QSPI0+QSPI1). Note. *: For RZ/G2M V1.3, 40MB/s for QSPI, 80MB/s for dual QSPI. The RZ/G2M V1.3 does not support QSPI-DDR operation.

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Item	Description
External Bus Controller for LPDDR4/DDR3L SDRAM (DBSC4) (For All Products)	RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N • LPDDR4-3200 can be connected directly. Note. The LPDDR4X (JESD209-4-1) is not supported. RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 • 2 channels (32-bit bus mode) • Memory Size: Up to 8GB * RZ/G2N • 1 channel (32-bit bus mode) • Memory Size: Up to 4GB * RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N * : LPDDR4-SDRAM compliant with JEDEC JESD209-4B. (Supports memory with sizes from 4 Gbits to 16 Gbits per channel of DBSC4.) RZ/G2E • DDR3L-1856 can be connected directly. • 1 channel (32-bit bus mode) • Memory Size: Up to 2 GB RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E • Auto Refresh/Self Refresh/Partial Array Self Refresh supported • Auto Pre-charge Mode • DDR Back Up supported • Cache memory for DDR-Memory access efficiency • Memory access protection for secure/safety regions • Decompression of visual near lossless compressed image • ECC supported

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1.1.4 Internal Bus Module

Item	Description
AXI-bus (For All Products)	• On-chip main bus — Bus protocol: AXI3 with QoS control RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N — Frequency: 400 MHz — Bus width: 512 bits/256 bits/128 bits RZ/G2E — Frequency: 266 MHz — Bus width: 256 bits/128 bits/64 bits • On-chip CPU bus RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 — CoreLink™ CCI-Kipling Cache Coherent Interconnect — Bus protocol: AMBA®4 ACE™ and ACE-Lite™ — Frequency: 800 MHz — Bus width: 128 bits RZ/G2N — Bus protocol: AXI3 — Frequency: 800 MHz — Bus width: 128 bits RZ/G2E — Bus protocol: AXI3 — Frequency: 533 MHz — Bus width: 128 bits
Direct Memory Access Controller for System (SYS-DMAC) (For All Products)	• 16 channels for PeriW domain (SYDM0) • 32 channels for PeriE domain (SYDM1, 2) • Address space: 4 GBytes on architecture • Data transfer length: Byte, word (2 Bytes), longword (4 Bytes), 8 Bytes, 16 Bytes, 32 Bytes and 64 Bytes • Maximum number of transfer times: 16,777,215 times • Transfer request: Selectable from on-chip peripheral module request and auto request • Bus mode: Selectable from normal mode and slow mode • Priority: Selectable from fixed channel priority mode and round-robin mode • Interrupt request: Supports interrupt request to CPU at the end of data transfer • Repeat function: Automatically resets the transfer source, destination, and count at the end of DMA transfer (by descriptor function) • Descriptor function (each channel) supported • MMU (each channel) supported • Channel bandwidth arbiter (each channel)

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Item	Description
Boot (For All Products)	• System startup with selectable boot mode at power-on reset • Either external ROM boot (area 0) or on-chip ROM boot can be selected through MD pin on development chip. • In on-chip ROM boot, RPC-IF or QSPI serial ROM boot is supported. • Program downloaded to internal memory (System RAM) • Autorun function for the downloaded program • About detail information of BOOT, refer to Section 24 (Boot) and Appendix B (Active sequence).
Direct Memory Access Controller for Audio (Audio-DMAC) (For All Products)	RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N • 32 channels • asdm0: 16 channels • asdm1: 16 channels RZ/G2E • 16 channels • asdm0: 16 channels RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E • Address space: 4 GBytes on architecture • Data transfer length: Byte, word (2 Bytes), longword (4 Bytes), 8 Bytes, 16 Bytes, 32 Bytes and 64 Bytes • Maximum number of transfer times: 16,777,215 times • Transfer request: Selectable from on-chip peripheral module request and auto request • Bus mode: Selectable from normal mode and slow mode • Priority: Selectable from fixed channel priority mode and round-robin mode • Interrupt request: Supports interrupt request to CPU at the end of data transfer • Repeat function: Automatically resets the transfer source, destination, and count at the end of DMA transfer (by descriptor function) • Descriptor function (each channel) supported • MMU (each channel) supported • Channel bandwidth arbiter (each channel)
Audio-DMAC-Peripheral-Peripheral (For All Products)	• Audio-DMAC (for transfer from Peripheral to Peripheral) RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N • 29 channels + 29 (extended) channels for audio domain RZ/G2E • 29 (extended) channels for audio domain RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N • Data transfer length: longword (4 Bytes) • Transfer count: Transfer count is not specified (DMA transfer is made from the transfer-start to transfer-stop settings.). • Transfer request: Selectable from on-chip audio peripheral module request • Priority: round-robin mode • Interrupt request: not supports interrupt request to CPU at the end of data transfer
IPMMU (For All Products)	• An IPMMU is a memory management unit (MMU) which provides address translation and access protection functionalities to processing units and interconnect networks.

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Item	Description	
Interrupt Controller (INTC) (For All Products)	INTC-AP (For All Products; for AP-System core Cortex-A57/Cortex-A53)	— 7 interrupt pins which can detect external interrupts — Max. 480 shared peripheral interrupts supported — Fall/rise/high level/low level detection is selectable — On-chip peripheral interrupts: Priority can be specified for each module — 16 software interrupts that have been generated and 6 private peripheral interrupts supported — 32-level priority selectable — Trust Zone supported

1.1.5 Internal Memory

Item	Description
System RAM (For All Products)	RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RAM of 384 KBytes RZ/G2E RAM of 128 KBytes

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1.1.6 Graphics Units

Item	Description
3D Graphics Engine (3DGE)	RZ/G2H • Imagination Technologies PowerVR Series6XT GX6650 • Max. Frequency. 600 MHz • Drastically performance improvements for sophisticated graphics and GPU computer • Reducing power consumption even further through advanced power saving mechanisms • Lowest memory bandwidth in the industry with compression technologies • Ultra HD deep color GPU Support APIs: OpenGL ES 3.1, (OpenCL 1.2 EP) • 7.2 Gpix/s, 300 Mpoly/s, 288 GFLOPS RZ/G2M V1.3 RZ/G2M V3.0 • Imagination Technologies PowerVR Series 6XT GX6250 • Max. Frequency 600 MHz • Drastically performance improvements for sophisticated graphics and GPU computer • Reducing power consumption even further through advanced power saving mechanisms • Lowest memory bandwidth in the industry with compression technologies • Ultra HD deep color GPU Support APIs: OpenGL ES 3.1, (OpenCL 1.2 EP) • 2.4 Gpix/s, 300 Mpoly/s, 96 GFLOPS RZ/G2N • Imagination Technologies PowerVR Series 7XE GE7800 • Max. Frequency. 600 MHz • Drastically performance improvements for sophisticated graphics and GPU computer • Reducing power consumption even further through advanced power saving mechanisms • Lowest memory bandwidth in the industry with compression technologies • Ultra HD deep color GPU Support APIs: OpenGL ES 3.1, (OpenCL 1.2 EP) • 2.4 Gpix/s, 200 Mpoly/s, 38.4 GFLOPS RZ/G2E • Imagination Technologies PowerVR Series 8XE GE8300 • Max. Frequency. 600 MHz • Drastically performance improvements for sophisticated graphics and GPU computer • Reducing power consumption even further through advanced power saving mechanisms • Lowest memory bandwidth in the industry with compression technologies • Ultra HD deep color GPU Support APIs: OpenGL ES 3.1, (OpenCL 1.2 EP) • 2.4 Gpix/s, 200 Mpoly/s, 19.2 GFLOPS

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Item	Description	
Display Unit (DU) (For All Products)	Display channel	RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N 3 independently controllable channels RZ/G2E 2 independently controllable channels
	Interface	RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N • HDMI 1 channel (option) • LVDS 1 channel RZ/G2E • LVDS 2 channels RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E • Digital RGB 1 channel (8-bit precision for each RGB color)
	LVDS interface (per channel)	• Output: compliant with TIA/EIA-644; five pairs of differential output (four pairs of data and one pair of clock) • Operating frequency: Dotclk 150 MHz
	HDMI (option)	RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N • Support HDMI 1.4b class transfer rate, up to 3D format 1080p60/4Kp30 • Dotclk 297 MHz
	Screen size and number of composite planes per channel	RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N • Maximum screen size: 3840 × 2160 RZ/G2E • Maximum screen size: 1920 × 1080 (also depends on frame rate) RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E • Number of planes specifiable: 5 (VSP2 processing) • Number of planes specifiable: 1 (DU)
	CRT scanning method	Non-interlaced
	Synchronization method	Master
	Internal color palette (VSP2)	• Includes four color palette planes which can display 256 of 260 thousands colors at the same time.
	Output display numbers	RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N • Three output channels (resolutions for different displays) RZ/G2E • Two output channels RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N • Output on rising and falling edges of the synchronizing signal (resolution for the same display) RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E • 8-bit precision for each RGB color
	Blending ratio settings (VSP2)	Number of color palette planes with blending ratio: 4
	Dot clock	Switchable between external input and internal clock

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Item	Description	
Video Input Module (VIN) (For All Products)	MIPI-CSI2 interface	RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N • 2 channels (4 lane × 1 channel, 2 lane × 1 channel) • Interleaving by 4 VC (virtual channel) supported • Filtering by DT (data type) supported • YUV422 8/10bit, RGB888, Embedded 8bit, User Defined 8bit are supported • 1.5 Gbps/Lane RZ/G2E • 1 channel (2 lane × 1 channel) • Interleaving by 2 VC (virtual channel) supported • Filtering by DT (data type) supported • YUV422 8/10bit, RGB888, Embedded 8bit, User Defined 8bit are supported • 1.1 Gbps/Lane

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Item	Description	
Video Input Module (VIN) (For All Products)	digital interface	RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N • 2 channels (RGB/YCbCr) • Dotclk 100 MHz • ITU-R BT.601 interface: 8-, 10- (same size only (not scaling)), 12- (same size only (not scaling)) 16-, 20- (same size only (not scaling)) or 24-bit (same size only (not scaling)), YCbCr422, 18-bit RGB666, 24-bit RGB888 • ITU-R BT.656 interface: 8-, 10- (same size only (not scaling)), or 12-bit (same size only (not scaling)) YCbCr422 • ITU-R BT.1358 interface: 16-, 20- (same size only (not scaling)), or 24-bit (same size only (not scaling)) YCbCr422 • ITU-R BT.709 interface: 8-, 10- (same size only (not scaling)), 12- (same size only (not scaling)) 16-, 20- (same size only (not scaling)) or 24-bit (same size only (not scaling)) YCbCr422, 18-bit RGB666, 24-bit RGB888 About Digital RGB channel usage combination, Refer as follows cases. CASE1 VIN-A8bit + VIN-B8/12/16 CASE2 VIN-A12bit + VIN-B8/12/16 CASE3 VIN-A16bit + VIN-B8/12 RZ/G2E • 2 channels (RGB/YCbCr) • Dotclk 100 MHz • ITU-R BT.601 interface: 8-, 10- (same size only (not scaling)), or 12-bit (same size only (not scaling)) YCbCr422, RGB666, RGB888 • ITU-R BT.656 interface: 8-, 10- (same size only (not scaling)), or 12-bit (same size only (not scaling)) YCbCr422 • ITU-R BT.1358 interface: 16-, 20- (same size only (not scaling)), or 24-bit (same size only (not scaling)) YCbCr422 • ITU-R BT.709 interface: 8-, 10- (same size only (not scaling)), or 12-bit (same size only (not scaling)) YCbCr422, RGB666, RGB888
Video Input Module (VIN) (For All Products)	Capturing function	RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N Up to 8 input images can be captured (using VC, DT filtering) RZ/G2E Up to 2 input images can be captured (using VC, DT filtering)
	Clipping function	Up to 4096 × 4096
	Horizontal scaling	Up to two times, but only scaling down is possible for HD1080i or HD1080p data. (one input only)
	Vertical scaling	Up to three times, but only scaling down is possible for HD1080i or HD1080p data. (one input only)
	Output format	RGB-565, ARGB-1555, ARGB8888, YCbCr422, RGB888, YCbCr420 YC separation, and extraction of the Y component

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1.1.7 Video Processing

Item	Description
Video Signal Processor (VSPI) (For All Products)	RZ/G2H VSPI has the following features. 2 sets of VSPI are integrated. 500 Mpix/s process rate per 1 VSPI Supports 4K (3840 pixels × 2160 lines) processing RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N VSPI has the following features. 1 set of VSPI is integrated. 500 Mpix/s process rate per 1 VSPI Supports 4K (3840 pixels × 2160 lines) processing RZ/G2E VSPI has the following features. 1 set of VSPI is integrated. 125 Mpix/s process rate per 1 VSPI Supports Full HD (1920 pixels × 1080 lines) processing RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E (1) Supports Various Data Formats and Conversion — Supports YCbCr444/422/420, RGB, αRGB, αplane — Color space conversion and changes to the number of colors by dithering — Color keying — Supports combination between pixel alpha and global alpha — Supports generating pre multiplied alpha (2) Video Processing — Up and down scaling with arbitrary scaling ratio — Super resolution processing — Image rotation/reversal function: Reverses an image vertically/horizontally or rotates it by 90°/270° (3) Picture Quality/Color Correction with 1D/3D Look Up Table (LUT) — Hue, brightness, and saturation adjustment — 1D and 2D histogram Following functions will be supported by Renesas software portfolio. — Dynamic γ correction and gain correction — Correction of color (to adjust skin tones or colors in memory) (4) Visual near lossless image compression supported — 50% of bandwidth is diminished

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Item	Description
Video Signal Processor (VSPB) (For All Products)	RZ/G2H VSPB has the following features. 2 sets of VSPB are integrated. 500 Mpix/s process rate (output rate) per 1 VSPB. Supports 4K (3840 pixels × 2160 lines) processing RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N VSPB has the following features. 1 set of VSPB is integrated. 500 Mpix/s process rate (output rate) per 1 VSPB. Supports 4K (3840 pixels × 2160 lines) processing RZ/G2E VSPB has the following features. 1 set of VSPB is integrated. 125 Mpix/s process rate (output rate) per 1 VSPB. Supports Full HD (1920 pixels × 1080 lines) processing RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E (1) Supports Various Data Formats and Conversion — Supports YCbCr444/422/420, RGB, αRGB, αplane — Color space conversion and changes to the number of colors by dithering — Color keying — Supports combination between pixel alpha and global alpha — Supports generating pre multiplied alpha (2) Video Processing — Blending of 5 picture layers and raster operations (ROPs) — Vertical flipping (3) Picture Quality/Color Correction with 1D/3D Look Up Table (LUT) — 1D and 2D histogram Following functions will be supported by Renesas software portfolio. — Dynamic γ correction and gain correction — Correction of color (to adjust skin tones or colors in memory) (4) Visual near lossless image compression supported — 50% of bandwidth is diminished

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Item	Description
Video Signal Processor (VSPD) (For All Products)	RZ/G2H VSPD has the following features. 1 set of VSPD is integrated. Supports 4K (3840 pixels × 2160 lines) resolution. RZ/G2M V1.3 RZ/G2M V3.0 VSPD has the following features. 3 sets of VSPD are integrated. Supports 4K (3840 pixels × 2160 lines) resolution. RZ/G2N VSPD has the following features. 1 set of VSPD is integrated. Supports 4K (3840 pixels × 2160 lines) resolution. RZ/G2E VSPD has the following features. 2 sets of VSPD are integrated. Supports Full HD (1920 pixels × 1080 lines) resolution. RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E (1) Supports Various Data Formats and Conversion — Supports YCbCr444/422/420, RGB, αRGB, αplane — Color space conversion and changes to the number of colors by dithering — Color keying — Supports combination between pixel alpha and global alpha — Supports generating pre multiplied alpha (2) Video processing — Blending of 5 picture layers and raster operations (ROPs) — Vertical flipping in case of output to memory (3) Direct connection to display module RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N — Supports 4096 pixels in horizontal direction RZ/G2E — Supports 2048 pixels in horizontal direction RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E — Writing back image data which is transferred to Display Unit (DU) to memory
Video Signal Processor (VSPDL) RZ/G2H RZ/G2N	VSPDL has the following features. 1 set of VSPDL is integrated. (1) Supports various data formats and conversion — Supports YCbCr444/422/420, RGB, αRGB, αplane — Color space conversion and changes to the number of colors by dithering — Color keying — Supports combination between pixel alpha and global alpha — Supports generating pre multiplied alpha (2) Video processing — Blending of five picture layers and raster operations (ROPs) (3) Direct connection to display module — Supports two display output interfaces — Supports 2048 pixels in horizontal direction — Writing back image data which is transferred to Display Unit (DU) to memory

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Item	Description
Video Codec Processor (VCP4) (For All Products)	The VCP4 is a multi-codec module which provides encoding and decoding capabilities on the basis of multiple video coding schemes, e.g., H.265/HEVC, H.264/AVC. This IP (Intellectual Property) is a multi codec that processes the frame or each field by controlling software for VCP4 executed on host CPU. • The VCP4 has the following features: Support for multiple codecs H.265/HEVC MP (Main Profile) decoding H.264/MPEG-4 AVC HP (High Profile) and MVC SHP (Stereo High Profile) encoding and decoding • Support for up to 4K resolutions (H.265 and H.264) Multiple channel processing: RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N When iVDP1C is used: (H.264/H.265 1920 × 1080p × 120 fps) When iVDP1C is not used: (H.265 1920 × 1080p × 120 fps) + (H.264 1920 × 1080p × 120 fps) RZ/G2E When iVDP1C is not used: (H.264/H.265 1920 × 1080p × 60 fps) When iVDP1C is used: (H.264/H.265 1920 × 1080p × 30 fps) RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E Note: “1920 × 1080p × 120 fps” can be replaced as “3840 × 2160p × 30 fps”. “1920 × 1080p × 60 fps” can be replaced as “1280 × 720p × 120 fps”. “1920 × 1080p × 30 fps” can be replaced as “1280 × 720p × 60 fps”. Maximum performance will change with securable bus bandwidth. RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E • Data handling on a picture-by-picture basis Encodes/decodes data one picture (frame or field) at a time. • High picture quality Supports the H.264 high-efficiency coding tools (CABAC, 8 × 8 frequency conversion, and quantization matrix). High-efficiency motion vector detection by a combination of discrete search and trace search Optimal-mode selection by Rate-Distortion (RD) cost evaluation Picture quality control based on activity analysis results which match visual models • Low power dissipation Dynamically disables the clocks for the entire VCP4. Dynamically disables the clocks for individual submodules. • Includes its own reference data cache • Lossless image compression for reference picture is supported Use the software from Renesas to handle VCP4 functions.

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Item	Description
Video Decoding Processor for inter-device video transfer (iVDP1C) (For All Products)	• Low-latency decoder H.264/AVC, JPEG • Color format 4:2:0/4:2:2 • Bit depth 8/10/12bits • Performance: RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N 1280 pixels × 960 lines × 30 frames/second × 4 channels (regardless of when VCP4 is used or not) RZ/G2E 1280 pixels × 960 lines × 30 frames/second × 2 channels (when VCP4 is not used) 1280 pixels × 960 lines × 30 frames/second × 1 channel (when VCP4 is used) RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E • Max. resolution: 1920 pixels × 1088 lines • Includes its own reference data cache • Lossless image compression for reference picture is supported if bit depth is 8 bits Use the software from Renesas to handle iVDP1C functions.
Fine Display Processor (FDP1) (For All Products)	The FDP1 is the de-interlacing module which converts the interlaced video to progressive video, and has the following features. RZ/G2H (1) Supports 2 channels 500 Mpix/s for output performance per 1 FDP1 RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N (1) Supports 1 channel 500 Mpix/s for output performance per 1 FDP1 RZ/G2E (1) Supports 1 channel 125 Mpix/s for output performance per 1 FDP1 RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E (2) Supports various data formats — Input: YCbCr444/422/420 — Output: YCbCr444/422/420 and RGB/αRGB (3) 8190 pixels x 8190 lines video processing performance (4) High image quality de-interlacing algorithm — Motion adaptive de-interlacing — Accurate still detection — Diagonal line interpolation (DLI) (5) Visual near lossless image compression supported 50% of bandwidth is diminished

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1.1.8 Sound Interface

Item	Description	
Sampling Rate Converter Unit (SCU) (For All Products)	Overall specification	• Includes ten SRC modules — Supports the quality suitable for audio sound (High-sound-quality type) (THD+N -132dB): six modules — Supports the quality suitable for voice sound (general-sound-quality type) (THD+N -96dB): four modules • The SRC module is capable of correcting phase change and delay (timing jitter) generated during data transfer over external memories or external devices. • The channel count conversion unit (CTU), mixer (MIX), and digital mute and volume function (DVC) can be used on two fixed output channels.
	Sampling rate conversion (SRC)	• Capable of asynchronous sampling rate conversion • Supports resolutions up to 24 bits • Two kinds of filter type for SRC. — Supports the quality suitable for audio sound (High-sound-quality type) (THD+N -132dB): Realized the filter by passband -1dB@0.4575FS, cutoff -18dB@0.5FS. — Supports the quality suitable for voice sound (general-sound-quality type) (THD+N -96dB): Realized the filter by passband -1dB@0.4561FS, cutoff -72dB@0.5FS. (Characteristics of each filter is written in the equivalent/up-sampling cases.) • Automatically generates antialiasing filter coefficients • For monaural to eight-channel sound sources
Sampling Rate Converter Unit (SCU) (For All Products)	Channel count conversion unit (CTU)	• Downmixing and splitter functions — Conversion of eight input channels into four output channels — Conversion of six input channels into two output channels — Conversion of two input channels into four sets of two output channels — Conversion of one input channel into eight sets of one output channel — No conversion
	Mixer (MIX)	• Mixing (adds) two to four sources into one • Ratio for adding sources is selectable • Ratio is dynamically changeable • Mixing with volume ramp is available (ramp period is selectable)
	Digital volume and mute function (DVC)	• Volume control function including digital volume, volume ramp, and zero-crossing mute • The digital volume function is specified by a 24-bit fixed-point value within the range from 0 to 8 times (mute, or -120 to 18 dB) • The volume ramp function can be used for soft mute, fade-in, fade-out, or desired volume adjustment • The volume ramp period can be changed within the sampling range from the 0th to 23rd power of 2 • The zero-crossing mute function silences the sound at the zero-crossing point of the audio data

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Item	Description	
Serial Sound Interface Unit (SSIU) (For All Products)	Overall specification	RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E • Includes ten SSI modules functioning as interfaces with external devices. — Supports short and long formats for monaural — Supports TDM format (six modules of ten modules can be used for this function) RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N • Max. 16 independent monaural sound sources in a TDM format can be in TDM format. RZ/G2E • Max. 8 independent monaural sound sources in a TDM format can be in TDM format.
	Serial sound interface (SSI)	• 10 channels • Max. SCK frequency 15.1 MHz (for slave input) or 12.5 MHz (for master output) • Operating mode: non-compressed mode (Not support compressed mode) • Supports versatile serial audio formats (I2S/left justified/right justified) • Supports master/slave functions • Programmable word clock, bit clock generation functions • Multichannel format functions (up to four channels) • Supports 8-/16-/18-/20-/22-/24-bit data formats • Supports TDM mode • Supports WS continue mode • The DMA controller or interrupts control the transfer of data to and from the SSI module. • Supports short and long frames for monaural data (valid data lengths are 8 and 16 bits) • Up to nine independent clock signals can be input.
Audio Clock Generator (ADG) (For All Products)	Selection or division of audio clock signals	

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1.1.9 Storage

<table>
<tr><th>Item</th><th>Description</th></tr>
<tr><td>USB2.0 Host
(For All Products)</td><td>RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N
• 2 channels (Host only 1 channel/Host-Function 1 channel)
• USB Host (EHCI/OHCI) 2 LINK
RZ/G2E
• 1 channel (Host-Function 1 channel)
• USB Host (EHCI/OHCI) 1 LINK
RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N
• USB3.0 module also can be used as USB2.0
• Compliance with USB2.0
• USB Function 1 LINK
• Supports On-The-Go (OTG) function Rev2.0 complying with 2 protocols:
+ Session Request Protocol (SRP).
+ Host Negotiation Protocol (HNP).
RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E
• Compliance with USB2.0 (High-Speed)
• Interrupt request
• Internal dedicated DMA
• Compliance with Battery Charging function Rev1.2:
+ Charging Port (Host): CDP, SDP are supported (Not support DCP).
+ Portable Device (Function) is supported.</td></tr>
<tr><td>USB3.0
(For All Products)</td><td>• USB 3.0 DRD 1 channel
• This module can be use as USB2.0 as follows
<table>
<tr><th>Core</th><th>Super Speed</th><th>High Speed</th><th>Full Speed</th><th>Low Speed</th></tr>
<tr><td>Host</td><td>√</td><td>√</td><td>√</td><td>√</td></tr>
<tr><td>Peripheral</td><td>√</td><td>√</td><td>√</td><td>—</td></tr>
</table>
• Supports SS/HS/FS/LS. xHCI</td></tr>
<tr><td>Serial-ATA Gen3
RZ/G2H RZ/G2N</td><td>• Serial ATA Standard Rev3.2 supported
• 6.0-Gbps (Gen3) transfer rate supported
PHY is shared with PCIE Controller</td></tr>
</table>

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Item	Description
SD host Interface (For All Products)	RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N • 4 channels RZ/G2E • 3 channels RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E • Supports SDR104 class transfer rate Does not support CPRM • Supports SD memory/SDIO interface • Error check function: CRC7 (command/response), CRC16 (data) • Max. Frequency 200 MHz • Card detection function • Supports write protection • SD-binding function — Compliant with Content Protection for Recordable Media Specification in revision 0.92 of the SD-Binding Part of the SD Memory Card Book • SD-SD content protection — Compliant with Content Protection for Recordable Media Specification in revision 0.92 of the SD-SD part of the SD Memory Card Book
Multimedia Card Interface (MMC) (For All Products)	RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N • 2 channels • eMMC 5.0 base, Support HS400 class transfer rate RZ/G2E • 1 channel • eMMC 5.0 base, Support HS400 class transfer rate RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E • eMMC controllable • Data bus: 1/4/8-bit MMC mode (not support SPI mode) • Support block transfer (not support stream transfer) • Block size in multiple block transfer: 512 Bytes
rawNAND Controller RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E	• The NAND Flash Memory Interface controller implements the function of a high level interface to one NAND flash device. It supports the functionality of the high speed NAND Flash devices described in the ONFI 1.x specifications.

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1.1.10 Network

Item	Description
Controller Area Network Interface (CAN interface) (For All Products)	• 2 channels • Supports CAN specification 2.0B • Maximum bit rate: 1 Mbps • Message box — Normal mode: 32 receive-only mailboxes and 32 mailboxes for transmission/reception — FIFO mode: 32 receive-only mailboxes and 24 mailboxes for transmission/reception, 4-stage FIFO for transmission, and 4-stage FIFO for reception • Reception — Data frame and remote frame can be received. — Selectable receiving ID format — Selectable overwrite mode (message overwritten) or overrun mode (message discarded) • Acceptance filter — Mask can be enabled or disabled for each mailbox. • Transmission — Data frame and remote frame can be transmitted. — Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) — Selectable ID priority mode or mailbox number priority mode • Sleep mode for reducing power consumption
CAN-FD (For All Products)	• 2 channels • 8 Mbps (CAN clock 40 MHz)
PCIE Controller (For All Products)	• PCI Express Base Specification Revision 2.0 • PHY integrated RZ/G2H RZ/G2N • 1 Lane × 2 channels (one of PHY is shared with Serial ATA) RZ/G2M V1.3 RZ/G2M V3.0 • 1 Lane × 2 channels RZ/G2E • 1 Lane × 1 channel
EthernetAVB-IF (For All Products)	• Supports IEEE802.1BA, IEEE802.1AS, IEEE802.1Qav and IEEE1722 functions • Magic packet detection • Supports Reception Filtering to separate streaming frames from different sources • Supports interface conforming to IEEE802.3 PHY RGMII (Reduced Gigabit Media Independent Interface) • RGMII v1.3 • Supports transfer at 1000 Mbps and 100 Mbps.

1.1.11 Timer

Item	Description
RCLK Watchdog Timer (For All Products)	• 1 channel • Internal 16-bit watchdog timer operated by RCLK • Programmable overflow time period: more than 1 hour count capable

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Item	Description
16-Bit Timer Pulse Unit (TPU) (For All Products)	• 4-channels 16-bit timers • Each channel outputs PWM
System Watchdog Timer (For All Products)	• 1 channel • Internal 16-bit watchdog timer • Programmable overflow time period: more than 1 hour count capable initial counter value 171[s]
Compare Match Timer Type0 (CMT0) (For All Products)	• 2 channels • 32-bit timer (16 bits/32 bits can be selected) • Source clock: RCLK clock • Compare match function provided • Interrupt requests
Compare Match Timer Type1 (CMT1) (For All Products)	• 8 channels • 48-bit timer (16 bits/32 bits/48 bits can be selected) • Source clock: RCLK/system clock • Compare match function provided • Interrupt requests
Compare match timer 2 (CMT2) (For All Products)	(same as CMT1)
Compare match timer 3 (CMT3) (For All Products)	(same as CMT1)
System Timer (For All Products)	• 32-bit timer, 1 channel (16 bits/32 bits can be selected) • Compare match function provided • Interrupt requests
System up-time clock (For All Products)	• 1 channel • Internal 32-bit timer • Programmable overflow time period: maximum 24 hours
Timer Unit (TMU) (For All Products)	• 15 channels • 32-bit timer • Auto-reload type 32-bit down counter • Internal prescaler • Interrupt request • 2 channels for input capture

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1.1.12 Peripheral Module

Item	Description
IIC Bus Interface for PMIC (IIC for PMIC) (For All Products)	• 1 PMIC channel for dedicated buffer • Supports single master transmission/reception • Interrupt request • Automatic transfer by wakeup control
I2C Bus Interface (I2C) (For All Products)	RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N • 7 channels • 4 channels for buffers with a slew rate (channel 0, 3, 4, 5 for dedicated buffers) • 3 channels for LVTTL buffers (channels 1, 2, 6 for ordinary buffers) RZ/G2E • 8 channels • 2 channels for buffers with a slew rate (channel 0, 3 for dedicated buffers) • 6 channels for LVTTL buffers (channels 1, 2, 4, 5, 6, 7 for ordinary buffers) RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E • NXP I2C bus interface method supported • Master/slave functions • Multi-master functions • Transfer rate up to 400 kbps supported • Programmable clock generation from the system clock • Master and Slave function DMA supported

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Item	Description	
Serial communication interface with FIFO (SCIF) (For All Products)	Overall specification	• 6 channels • Asynchronous, clock-synchronized modes • Asynchronous serial communication mode The SCIF performs serial data communication based on a character-by-character asynchronous system. This feature enables serial data communication with standard asynchronous communication chips that support Universal Asynchronous Receiver/Transmitter (UART) or Asynchronous Communication Interface Adapter (ACIA). There is a choice of eight serial data transfer formats. — Data length: 7 bits or 8 bits — Stop bits: 1 bit or 2 bits — Parity: Even/odd/none — Receive error detection: Parity, framing, and overrun errors — Break detection: A break is detected when a framing error lasts for more than 1 frame length at Space 0 (low level). When a framing error occurs, a break can also be detected by reading the RX pin level directly from the serial port register (SCSPTR). • Clock synchronous serial communication mode The SCIF performs serial data communication synchronized with a clock. This feature enables serial data communication with other LSIs that support synchronous communication. There is a single serial data communication format for clock synchronous serial communication. — Data length: 8 bits — Receive error detection: Overrun errors • Full-duplex communication capability The SCIF has an independent transmitter and receiver that enable simultaneous transmission and reception. The transmitter and receiver both have a 16-stage FIFO buffer structure, enabling continuous serial data transmission and reception. • On-chip baud rate generator, enabling any bit rate to be selected The SCIF enables choice of a clock source for transmission/reception: a clock from the on-chip baud rate generator based on the internal clock or an external clock. • Eight interrupt sources The SCIF has eight types of interrupt sources. receive-data-ready, receive-FIFO-data-full, break, transmit-FIFO-data-empty, transmit-end, receive-error, overrun-error and time-out and enables any of them to be requested independently. • DMA data transfer When the transmit FIFO register is empty or the receive FIFO register has received data, issuing a DMA transfer request activates the DMA controller (DMAC) to execute a data transfer. • In asynchronous mode using channels 0, 1, 3, and 4, modem control functions (RTS and CTS) are stored. • RTS and CTS are not implemented for SCIF2 and SCIF5.

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Item	Description	
Serial Communication Interface with FIFO (SCIF) (For All Products)	Overall specification	• The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available. • In asynchronous mode, a receive data ready (DR) or a timeout error (TO) can be detected during reception.
Clock-Synchronized Serial Interface with FIFO (MSIOF) (For All Products)	• 4 channels • Internal 32-bit × 64-stage transmit FIFOs/internal 32-bit × 256-stage receive FIFOs • Supports master and slave modes • Internal prescaler RZ/G2H • Supports serial formats: SPI (master and slave modes) RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E • Supports serial formats: IIS, SPI (master and slave modes) • Interrupt request, DMAC request	
High Speed Serial Communication Interface with FIFO (HSCIF) (For All Products)	• 5 channels • Asynchronous serial communication mode • Capable of full-duplex communication • On-chip baud rate generator, enabling any bit rate to be selected • Eight interrupt sources • DMA data transfer • Modem control functions (HRTS# and HCTS#) are stored. • The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available. • A receive data ready (DR) or a timeout error (TO) can be detected during reception.	
PWM (For All Products)	• 7 channels • High-level width (10 bits) of PWM output can be set. • Output cycle periods (10 bits) of PWM can be set. • Periods in the range from two to 2^{24} × 1023 cycles of the Pϕ clock can be set. • Continuous pulse or single pulse output selectable	

1.1.13 Others

Item	Description
Boundary Scan (For All Products: option)	• Boundary scan based on IEEE 1149.1 via JTAG interface is supported. Note that some module pins are not available on this boundary scan.

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1.2 Block Diagram

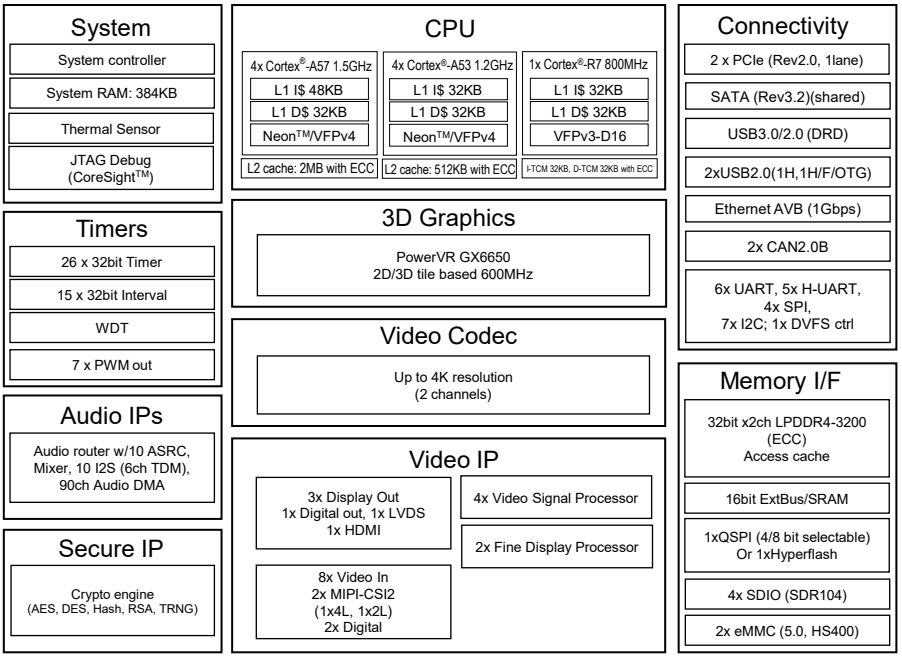


Figure 1.2-1 RZ/G2H (R8A774Ex) Block Diagram

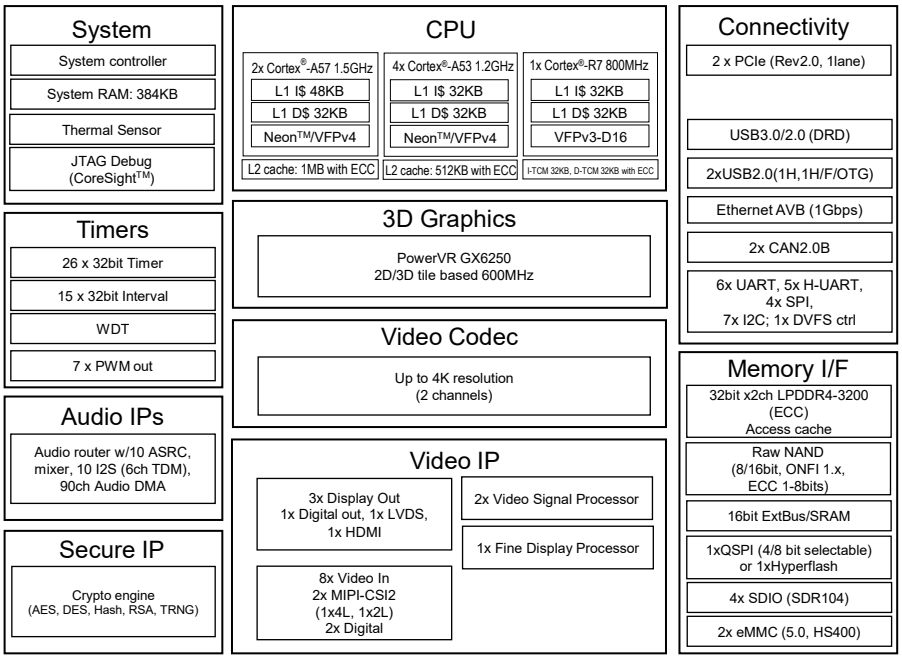


Figure 1.2-2 RZ/G2M (R8A774Ax) Block Diagram

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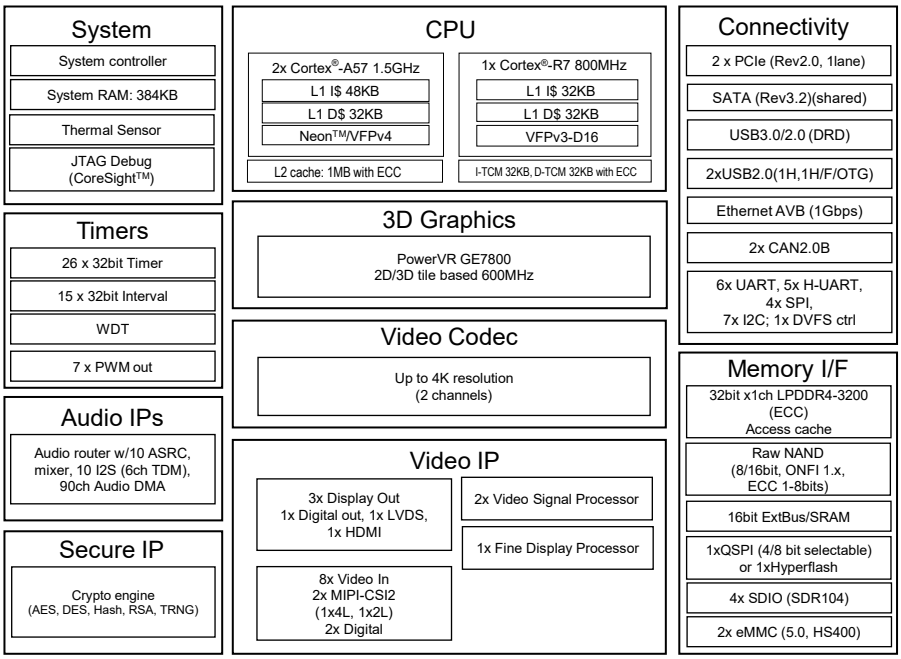


Figure 1.2-3 RZ/G2N (R8A774Bx) Block Diagram

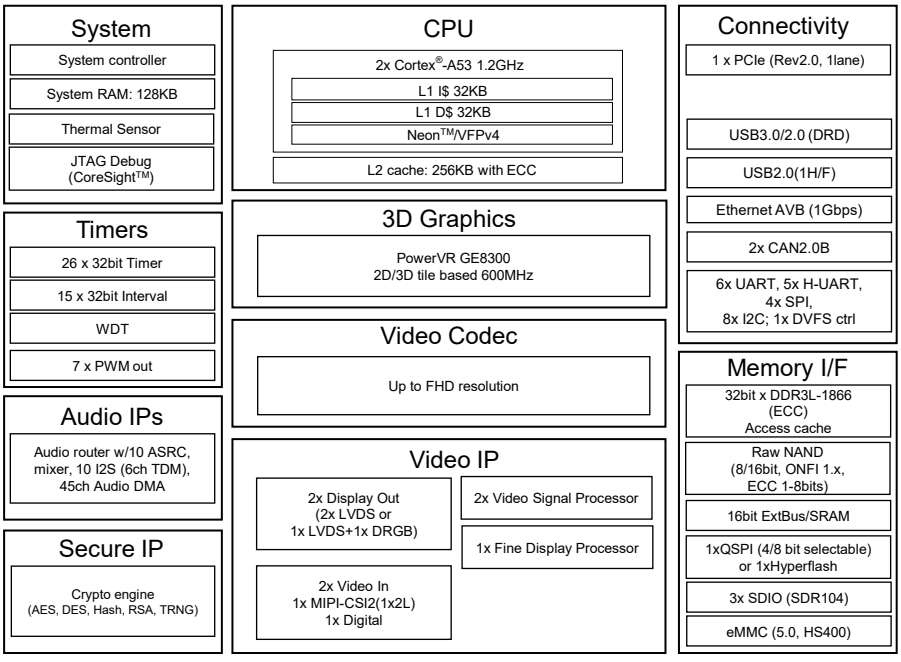


Figure 1.2-4 RZ/G2E (R8A774C0) Block Diagram

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1.3 Product Lineup

Table 1.3-1 Product lineup 【RZ/G2H, RZ/G2M V1.3,V3.0, RZ/G2N】

Group	Part Number	Core	HDMI	DDR Memory	Graphics	Stream
RZ/G2H	R8A774E0HA01BN	1.5 GHz Quad Cortex-A57, 1.2 GHz Quad Cortex-A53, 800 MHz Cortex-R7(*1)	OFF	LPDDR4 (3200)	PowerVR GX6650 (600 MHz)	H.264/H.265
	R8A774E1HA01BN		ON			
RZ/G2M	R8A774A2HA01BG		OFF		PowerVR GX6250 (600 MHz)	
	R8A774A3HA01BG		ON			
RZ/G2N	R8A774B0HA01BG	1.5 GHz Dual Cortex-A57, 800 MHz Cortex-R7(*1)	OFF		PowerVR GE7800 (600 MHz)	
	R8A774B1HA01BG		ON			

Note 1. In case of using this function, please contact a Renesas Electronics sales representative.

Table 1.3-2 Product lineup 【RZ/G2E】

Group	Part Number	Core	HDMI	DDR Memory	Graphics	Stream
RZ/G2E	R8A774C0HA01BG	1.2 GHz Dual Cortex-A53, 800 MHz Cortex-R7(*1)	—	DDR3L (1856)	PowerVR GE8300 (600 MHz)	H.264/H.265

Note 1. In case of using this function, please contact a Renesas Electronics sales representative.

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1.4 Function Comparison

Items	RZ/G2H	RZ/G2M	RZ/G2N	RZ/G2E
CPU (Cortex-A)	4× Cortex-A57 @1.5GHz 4×Cortex-A53 @1.2GHz (35.6 k DMIPS) L1, L2 Parity/ECC	2× Cortex-A57 @1.5GHz 4× Cortex-A53 @1.2GHz (23.3 k DMIPS) L1, L2 Parity/ECC	2× Cortex-A57 @1.5GHz (12.3 k DMIPS) L1, L2 Parity/ECC	2× Cortex-A53 @1.2GHz (5.5 k DMIPS) L1, L2 Parity/ECC
CPU (Cortex-R)	1 x Cortex-R7 @800MHz L1, TCM w/ECC			
DRAM I/F	32bit×2ch LPDDR4 (3200)		32bit ×1ch LPDDR4 (3200)	32bit ×1ch DDR3L (1856)
Video in	2×MIPI-CSI2, 2xDigital (RGB/YcbCr) up to 8input image can be captured			1×MIPI-CSI2, 1×Digital (RGB/YcbCr) up to 2 input image can be captured
Video Codec	Support up to 4k resolutions Decoding : H265, Encoding and Decoding : H.264			Support up to FHD resolutions Decoding : H265, Encoding and Decoding : H.264
3D GFX	PowerVR GX6650 @600 MHz	PowerVR GX6250 @600 MHz	PowerVR GE7800 @600 MHz	PowerVR GE8300 @600 MHz
Display out	1×HDMI, 1×LVDS, 1×Digital RGB			2×LVDS or 1×LVDS, 1× Digital RGB
USB	USB2.0×2ch (1×Host, 1×Host/Function/OTG) USB3.0/2.0×1ch (DRD)			USB2.0×1ch (Host/Function) USB3.0/2.0 ×1ch (DRD)
Gbit Ether	1ch			
CAN	2ch (support CAN-FD)			
PCIe	2ch (Rev.2.0 Lane×1) one of the 2ch is shared with SATA	2ch (Rev.2.0 Lane×1)	2ch (Rev.2.0 Lane×1) one of the 2ch is shared with SATA	1ch (Rev.2.0 Lane×1)
SATA	1ch (Pin Shared)	No	1ch (Pin Shared)	No
Package	1022 pin FCBGA, 29mm × 29mm, 0.8mm ball pitch			552 pin FCBGA 21mm × 21mm, 0.8mm ball pitch

Figure 1.4-1 Functional difference of RZ/G Series, 2nd Generation

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Section 2 Pin

2.1 Pin Functions of Functional Blocks

(1) RZ/G2H: Refer to attached 「RZ_G2H_pin_multiplex excel file」(Please double-click the icon on the right side)

(2) RZ/G2M: Refer to attached 「RZ_G2M_pin_multiplex excel file」(Please double-click the icon on the right side)

(3) RZ/G2N: Refer to attached 「RZ_G2N_pin_multiplex excel file」(Please double-click the icon on the right side)

(4) RZ/G2E: Refer to attached 「RZ_G2E_pin_multiplex excel file」(Please double-click the icon on the right side)

2.2 Pin Assignment

(1) RZ/G2H: Refer to attached 「RZ_G2H_pin_assignment excel file」(Please double-click the icon on the right side)

(2) RZ/G2M: Refer to attached 「RZ_G2M_pin_assignment excel file」(Please double-click the icon on the right side)

(3) RZ/G2N: Refer to attached 「RZ_G2N_pin_assignmen excel file」(Please double-click the icon on the right side)

(4) RZ/G2E: Refer to attached 「RZ_G2E_pin_assignment excel file」(Please double-click the icon on the right side)

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Section 3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3.1.1 Absolute Maximum Ratings for [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]

RZ/G2H
RZ/G2M V1.3 RZ/G2M V3.0
RZ/G2N RZ/G2E

Item	Value	Unit	Remarks
Power supply voltage (3.3 V) (VDDQ33, VDDQVA_SDn (n = 0 to 3) (except during operation through SDHI (SDR50, SDR104)), VDD33_SATA, VDD33_PCIEn (n = 0, 1), VDDQ33_USB3HSHn (n = 0, 1), VDDQ33_USB3HSn (n = 0, 1), VDD33_USB3n (n = 0, 1), VDDQ33_USB2Hn (n = 0, 1, 2), VDDQ33_USB2)	-0.3 to +3.84	V	—
Power supply voltage (2.5 V) (VDDQ25_ETH)	-0.3 to +2.9	V	—
Power supply voltage (1.8 V) (VDDQ18, VDD18_CPGPLLn (n = 0 to 4), VDDQ18_HDMIn (n = 0, 1), VDDQ18_LVDS, VDD18_LVDSPLL1, VDDQ18_CSIn (n = 0 to 3), VDDQ18_ISO, VDD18_MLBPLL, VDDQ_MDPLLn (n = 0, 1), VDD18_DUPLLn (n = 0, 1), AVDD_USB, VDDQVA_SDn (n = 0 to 3) (SDR50, SDR104))	-0.3 to +2.34	V	—
Power supply voltage (1.1 V) (VDDQVA_DDRn (n = 0, 1))	-0.3 to +1.5	V	LPDDR4
Power supply voltage (0.9 V) (VDD09_DDRPLLn (n = 0, 1), VDD09_SATA, VDD09_PCIEn (n = 0, 1), VDD09_USB3n (n = 0, 1), VDD09_USB3HSn (n = 0, 1), VDD09_USB2n (n = 0, 1 ,2), VDDQ09_HDMIn (n = 0, 1), VDDQ09_LVDS, VDD09_CSIn (n = 0 to 3)) VDD09_LVDSPLL2	-0.3 to + 1.12	V	—
Power supply voltage (0.9 V) (VDD)	-0.3 to + 1.12	V	—
Power supply voltage (0.9 V) (VDD_DVFS)	-0.3 to + 1.12	V	—
Input voltage (3.3-V I/O)	-0.3 to VDDQ33 + 0.3	V	*1
Input voltage (3.3-V I/O [SDHI])	-0.3 to VDDQVA_SDn + 0.3	V	*1
Input voltage (3.3-V I/O [SATA])	-0.3 to VDD33_SATA + 0.3	V	*1
Input voltage (3.3-V I/O [PCIE])	-0.3 to VDD33_PCIEn + 0.3	V	*1
Input voltage (3.3-V I/O [USB3])	-0.3 to VDD33_USB3n + 0.3	V	*1
Input voltage (3.3-V I/O [USB3HSH])	-0.3 to VDD33_USB3HSHn + 0.3	V	*1

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Item	Value	Unit	Remarks
Input voltage (3.3-V I/O [USB3HS])	-0.3 to VDD33_USB3HSn + 0.3	V	*1
Input voltage (3.3-V I/O [USB2H])	-0.3 to VDDQ33_USB2Hn + 0.3	V	*1
Input voltage (3.3-V I/O [USB2])	-0.3 to VDDQ33_USB2 + 0.3	V	*1
Input voltage (2.5-V I/O [ETH])	-0.3 to VDDQ25_ETH + 0.3	V	*2
Input voltage (1.8-V I/O)	-0.3 to VDDQ18 + 0.3	V	*3
Input voltage (1.8-V I/O [HDMI])	-0.3 to VDDQ18_HDMIn + 0.3	V	*3
Input voltage (1.8-V I/O [VDDQ18_LVDS])	-0.3 to VDDQ18_LVDS + 0.3	V	*3
Input voltage (1.8-V I/O [VDDQ18_CSIn])	-0.3 to VDDQ18_CSIn + 0.3	V	*3
Intput voltage (1.8-V I/O [VDDQ18_PCIEn])	-0.3 to VDDQ18_PCIEn + 0.3	V	*3
Input voltage (1.8-V I/O [VDDQVA_SDn])	-0.3 to VDDQVA_SDn + 0.3	V	*3, SDR50, SDR104
Input voltage (1.1-V I/O [VDDQVA_DDRn])	-0.3 to VDDQVA_DDRn + 0.3	V	*4, LPDDR4
Input voltage (0.9-V I/O [VDD09_SATA])	-0.3 to VDD09_SATA + 0.3	V	*5
Input voltage (0.9-V I/O [VDD09_PCIEn])	-0.3 to VDD09_PCIEn + 0.3	V	*5
Input voltage (0.9-V I/O [VDD09_USB3n])	-0.3 to VDD09_USB3n + 0.3	V	*5
Input voltage (0.9-V I/O [VDD09_USB3HSn])	-0.3 to VDD09_USB3HSn + 0.3	V	*5
Input voltage (0.9-V I/O [VDD09_USB2n])	-0.3 to VDD09_USB2n + 0.3	V	*5
Input voltage (0.9-V I/O [VDDQ09_HDMIn])	-0.3 to VDDQ09_HDMIn + 0.3	V	*5
Input voltage (0.9-V I/O [VDDQ09_LVDS])	-0.3 to VDDQ09_LVDS + 0.3	V	*5
Input voltage (0.9-V I/O [VDD09_CSIn])	-0.3 to VDD09_CSIn + 0.3	V	*5
Output voltage (3.3-V I/O)	-0.3 to VDDQ33 + 0.3	V	*1
Output voltage (3.3-V I/O [SDHI])	-0.3 to VDDQVA_SDn + 0.3	V	*1
Output voltage (3.3-V I/O [SATA])	-0.3 to VDD33_SATA + 0.3	V	*1
Output voltage (3.3-V I/O [PCIE])	-0.3 to VDD33_PCIEn + 0.3	V	*1
Output voltage (3.3-V I/O [USB3])	-0.3 to VDD33_USB3n + 0.3	V	*1
Output voltage (3.3-V I/O [USB3HSH])	-0.3 to VDD33_USB3HSHn + 0.3	V	*1
Output voltage (3.3-V I/O [USB3HS])	-0.3 to VDD33_USB3HSn + 0.3	V	*1
Output voltage (3.3-V I/O [USB2H])	-0.3 to VDDQ33_USB2Hn + 0.3	V	*1
Output voltage (3.3-V I/O [USB2])	-0.3 to VDDQ33_USB2 + 0.3	V	*1
Output voltage (3.3-V I/O [GE])	-0.3 to VDDQ25_GE + 0.3	V	*1
Output voltage (3.3-V I/O [AVB])	-0.3 to VDDQ25_AVB + 0.3	V	*1
Output voltage (3.3-V I/O [VDDQ_DU])	-0.3 to VDDQ_DU + 0.3	V	*1
Output voltage (3.3-V I/O [VDDQ_VIN01])	-0.3 to VDDQ_VIN01 + 0.3	V	*1
Output voltage (2.5-V I/O [ETH])	-0.3 to VDDQ25_ETH + 0.3	V	*2
Output voltage (2.5-V I/O [GE])	-0.3 to VDDQ25_GE + 0.3	V	*2
Output voltage (2.5-V I/O [AVB])	-0.3 to VDDQ25_AVB + 0.3	V	*2
Output voltage (1.8-V I/O)	-0.3 to VDDQ18 + 0.3	V	*3
Output voltage (1.8-V I/O [HDMI])	-0.3 to VDDQ18_HDMIn + 0.3	V	*3
Output voltage (1.8-V I/O [VDDQ18_LVDS])	-0.3 to VDDQ18_LVDS + 0.3	V	*3
Output voltage (1.8-V I/O [VDDQ18_CSIn])	-0.3 to VDDQ18_CSIn + 0.3	V	*3
Output voltage (1.8-V I/O [VDDQVA_SDn])	-0.3 to VDDQVA_SDn + 0.3	V	*3, SDR50, SDR104
Output voltage (1.8-V I/O [VDDQ18_DU])	-0.3 to VDDQ_DU + 0.3	V	*3
Output voltage (1.8-V I/O [VDDQ_VIN01])	-0.3 to VDDQ_VIN01 + 0.3	V	*3
Output voltage (1.1-V I/O [VDDQVA_DDRn])	-0.3 to VDDQVA_DDRn + 0.3	V	*4, LPDDR4

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Item	Value	Unit	Remarks
Output voltage (0.9-V I/O [VDD09_SATA])	-0.3 to VDD09_SATA + 0.3	V	*5
Output voltage (0.9-V I/O [VDD09_PCIEn])	-0.3 to VDD09_PCIEn + 0.3	V	*5
Output voltage (0.9-V I/O [VDD09_USB3n])	-0.3 to VDD09_USB3n + 0.3	V	*5
Output voltage (0.9-V I/O [VDD09_USB3HSn])	-0.3 to VDD09_USB3HSn + 0.3	V	*5
Output voltage (0.9-V I/O [VDD09_USB2n])	-0.3 to VDD09_USB2n + 0.3	V	*5
Output voltage (0.9-V I/O [VDDQ09_HDMIn])	-0.3 to VDDQ09_HDMIn + 0.3	V	*5
Output voltage (0.9-V I/O [VDDQ09_LVDS])	-0.3 to VDDQ09_LVDS + 0.3	V	*5
Output voltage (0.9-V I/O [VDD09_CSIn])	-0.3 to VDD09_CSIn + 0.3	V	*5
Operating temperature	-40 to +85	°C	Ta (ambient)
	-40 to +115	°C	Tj (junction)
Maximum rating temperature	-40 to +125	°C	Tj (junction)
Storage temperature	-55 to +125	°C	Ta (ambient)

Notes: Permanent damage to the LSI may result if absolute maximum ratings are exceeded. In normal operation, this LSI should be used within the specifications described in the following descriptions. If this LSI is not used within the specifications, the reliability of this LSI may lower.

Voltages are referenced at GND = VSS = AVSS = 0 V.

Abbreviations in the tables have the following meanings.

SDHI: SDHI does not operate through SDR50 and SDR104.

SDHI (SDR50, SDR104): SDHI operates through SDR50 and SDR104.

For details of the number of channels or available modules, refer to each manual; SDHI, DU/LVDS, SATA/PCIEC/USB3.0, DBSC4 (DDR), USB2.0, HDMI and CSI and Pin Information of Individual RZ/G Series Product.

1. Do not exceed 3.84 V.
2. Do not exceed 2.90 V.
3. Do not exceed 2.34 V.
4. Do not exceed 1.50 V.
5. Do not exceed 1.12 V.

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Table 3.1.2 Absolute Maximum Ratings for [RZ/G2E]

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N **RZ/G2E**

Item	Value	Unit	Remarks
Power supply voltage (3.3 V) (VDDQ33, VDDQ25_AVB0, VDDQ_SDn (n = 0, 1, 3), VDDQ_QSPI, VDDQ33_USB2)	-0.3 to +4.6	V	*1
Power supply voltage (2.5 V) (VDDQ25_AVB0)	-0.3 to +3.3	V	*2
Power supply voltage (1.8 V) (VDDQ18, VDD18_CPGPLLn (n = 0, 1, 3) VDDQ18_LVDS, VDD18_LVDSnPLL (n = 0, 1), VDDQ18_CSI0, VDDQ18_USB20, VDDQ18_USB30, VDDQ18_PCIE0, VDDQ18_MLBPLL, VDDQ_MAPLL, VDDQ_SDn (n = 0, 1, 3), VDDQ18_ISO, VDDQ_MDPLLn (n = 0, 1), AVDD_USB, VDDQ_QSPI)	-0.3 to +2.5	V	*3
Power supply voltage (1.35 V) (VDDQ_CK, VDDQ_DDR)	-0.3 to + 1.75	V	*4
Power supply voltage (1.0 V) (VDD, VDDD_USB30, VDDD_PCIE0)	-0.3 to + 1.26	V	
Input voltage (3.3-V I/O)	-0.3 to VDDQ33 + 0.3	V	*1
Input voltage (3.3-V I/O [AVB0])	-0.3 to VDDQ25_AVB0 + 0.3	V	*1
Input voltage (3.3-V I/O [VDDQ_SD])	-0.3 to VDDQ_SDn + 0.3 (n = 0, 1, 3)	V	*1
Input voltage (3.3-V I/O [VDDQ_QSPI])	-0.3 to VDDQ_QSPI + 0.3	V	*1
Input voltage (2.5-V I/O [AVB0])	-0.3 to VDDQ25_AVB0 + 0.3	V	*2
Input voltage (1.8-V I/O)	-0.3 to VDDQ18 + 0.3	V	*3
Input voltage (1.8-V I/O [VDDQ_SD])	-0.3 to VDDQ_SDn + 0.3 (n = 0, 1, 3)	V	*1
Input voltage (1.8-V I/O [VDDQ_QSPI])	-0.3 to VDDQ_QSPI + 0.3	V	*1
Input voltage (1.35-V I/O [VDDQ_DDR])	-0.3 to VDDQ_DDR + 0.3	V	*4
Output voltage (3.3-V I/O)	-0.3 to VDDQ33 + 0.3	V	*1
Output voltage (3.3-V I/O [AVB0])	-0.3 to VDDQ25_AVB0 + 0.3	V	*1
Output voltage (3.3-V I/O [VDDQ_SD])	-0.3 to VDDQ_SDn + 0.3 (n = 0, 1, 3)	V	*1
Output voltage (3.3-V I/O [VDDQ_QSPI])	-0.3 to VDDQ_QSPI + 0.3	V	*1
Output voltage (2.5-V I/O [AVB0])	-0.3 to VDDQ25_AVB0 + 0.3	V	*2
Output voltage (1.8-V I/O)	-0.3 to VDDQ18 + 0.3	V	*3
Output voltage (1.8-V I/O [VDDQ18_LVDS])	-0.3 to VDDQ18_LVDS + 0.3	V	*3
Output voltage (1.8-V I/O [VDDQ_SD])	-0.3 to VDDQ_SDn + 0.3 (n = 0, 1, 3)	V	*1
Output voltage (1.8-V I/O [VDDQ_QSPI])	-0.3 to VDDQ_QSPI + 0.3	V	*1
Output voltage (1.35-V I/O [VDDQ_DDR])	-0.3 to VDDQ_DDR + 0.3	V	*4
Operating temperature	-40 to +85	°C	Ta (ambient)
	-40 to +115	°C	Tj (junction)
Maximum rating temperature	-40 to +125	°C	Tj (junction)

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Item	Value	Unit	Remarks
Storage temperature	-55 to +125	°C	Ta (ambient)

Notes: Permanent damage to the LSI may result if absolute maximum ratings are exceeded. In normal operation, this LSI should be used within the specifications described in the following descriptions. If this LSI is not used within the specifications, the reliability of this LSI may lower.

Voltages are referenced at GND = VSS = AVSS = 0 V.

1. Do not exceed 4.6 V
2. Do not exceed 3.3 V
3. Do not exceed 2.5 V
4. Do not exceed 1.75 V

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3.2 Power Supply

Table 3.2.1 Power Supply for [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]

RZ/G2H
RZ/G2M V1.3 RZ/G2M V3.0
RZ/G2N RZ/G2E

Item	Symbol	Voltage			Unit	Remarks
		Min.	Typ.	Max.		
Power supply (Internal)	VDD	0.75	0.82	0.88	V	VDD for power supply and VSS for ground
Power supply (Internal)	VDD_DVFS	0.76	0.83	0.88	V	VDD_DVFS for power supply and VSS for ground.
Power supply (3.3-V I/O)	VDDQ33	3.1	3.3	3.5	V	VDDQ33 for power supply and VSS for ground
Power supply (3.3-V I/O [SDHI])	VDDQVA_SDn (n = 0 to 3)	3.1	3.3	3.5	V	VDDQVA_SDn for power supply and VSS for ground
Power supply (3.3-V I/O [SATA])	VDD33_SATA*1	3.1	3.3	3.5	V	VDD33_SATA for power supply and VSS for ground
Power supply (3.3-V I/O [PCIE])	VDD33_PCIEn (n = 0, 1)	3.1	3.3	3.5	V	VDD33_PCIEn (n = 0, 1) for power supply and VSS for ground
Power supply (3.3-V I/O [USB3HSH])	VDDQ33_USB3HSHn (n = 0, 1)	3.1	3.3	3.5	V	VDDQ33_USB3HSHn (n = 0, 1) for power supply and VSS for ground
Power supply (3.3-V I/O [USB3HS])	VDDQ33_USB3HSn (n = 0, 1)	3.1	3.3	3.5	V	VDDQ33_USB3HSn (n = 0, 1) for power supply and VSS for ground
Power supply (3.3-V I/O [USB3])	VDD33_USB3n (n = 0, 1)	3.1	3.3	3.5	V	VDD33_USB3n (n = 0, 1) for power supply and VSS for ground
Power supply (3.3-V I/O [USB2H])	VDDQ33_USB2Hn (n = 0, 1, 2)	3.1	3.3	3.5	V	VDDQ33_USB2Hn (n = 0, 1, 2) for power supply and VSS for ground
Power supply (3.3-V I/O [USB2])	VDDQ33_USB2	3.1	3.3	3.5	V	VDDQ33_USB2 for power supply and VSS for ground
Power supply (2.5-V I/O [ETH])	VDDQ25_ETH	2.4	2.5	2.6	V	VDDQ25_ETH for power supply and VSS for ground
Power supply (1.8-V I/O [VDDQ18])	VDDQ18	1.7	1.8	1.9	V	VDDQ18 for power supply and VSS for ground
Power supply (1.8-V I/O [HDMI])	VDDQ18_HDMIn (n = 0, 1)	1.7	1.8	1.9	V	VDDQ18_HDMIn (n = 0, 1) for power supply and VSS for ground
Power supply (1.8-V I/O [LVDS])	VDDQ18_LVDS	1.7	1.8	1.9	V	VDDQ18_LVDS for power supply and VSS for ground
Power supply (1.8-V I/O [CSI])	VDDQ18_CSIn (n = 0 to 3)	1.7	1.8	1.9	V	VDDQ18_CSIn (n = 0 to 3) for power supply and VSS for ground
Power supply (1.8-V I/O [SDHI (SDR50, SDR104)])	VDDQVA_SDn (n = 0 to 3)	1.7	1.8	1.9	V	VDDQVA_SDn (n = 0 to 3) for power supply and VSS for ground
Power supply (1.1-V I/O [DDR (LPDDR4)])	VDDQVA_DDRn (n = 0, 1)	1.06	1.10	1.17	V	VDDQVA_DDRn (n = 0, 1) for power supply and VSS for ground
Power supply (0.9-VI/O[SATA])	VDD09_SATA*1	0.75	0.82	0.88	V	VDD09_SATA for power supply and VSS for ground
Power supply (0.9-VI/O[PCIE])	VDD09_PCIEn (n = 0, 1)	0.75	0.82	0.88	V	VDD09_PCIEn (n = 0, 1) for power supply and VSS for ground

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Item	Symbol	Voltage			Unit	Remarks
		Min.	Typ.	Max.		
Power supply (0.9-VI/O[USB3])	VDD09_USB3n (n = 0, 1)	0.75	0.82	0.88	V	VDD09_USB3n (n = 0, 1) for power supply and VSS for ground
Power supply (0.9-VI/O[USB3HS])	VDD09_USB3HSn (n = 0, 1)	0.75	0.82	0.88	V	VDD09_USB3HSn (n = 0, 1) for power supply and VSS for ground
Power supply (0.9-VI/O[USB2])	VDD09_USB2n (n = 0, 1, 2)	0.75	0.82	0.88	V	VDD09_USB2n (n = 0, 1, 2) for power supply and VSS for ground
Power supply (0.9-VI/O[HDMI])	VDDQ09_HDMIn (n = 0, 1)	0.75	0.82	0.88	V	VDDQ09_HDMIn (n = 0, 1) for power supply and VSS for ground
Power supply (0.9-VI/O[LVDS])	VDDQ09_LVDS	0.75	0.82	0.88	V	VDDQ09_LVDS for power supply and VSS for ground
Power supply (0.9-VI/O[CSI])	VDD09_CSIn (n = 0 to 3)	0.75	0.82	0.88	V	VDD09_CSIn (n = 0 to 3) for power supply and VSS for ground
Power supply (PLL[LVDS])	VDD09_ LVDSPLL 2	0.75	0.82	0.88	V	VDD09_LVDSPLL2 for power supply and VSS for ground respectively
Power supply (PLL[CPG])	VDD18_CPGPLLn (n = 0 to 4)	1.7	1.8	1.9	V	VDD18_CPGPLLn (n = 0 to 4) for power supply and VSS_CPGPLLn (n = 0 to 4) for ground
Power supply (PLL[MLB])	VDD18_MLBPLL	1.7	1.8	1.9	V	VDD18_MLBPLL for power supply and VSS_MLBPLL for ground respectively
Power supply (PLL[DU])	VDD18_DUPLLn (n = 0, 1)	1.7	1.8	1.9	V	VDD18_DUPLLn (n = 0, 1) for power supply and VSS_DUPLLn (n = 0, 1) for ground respectively
Power supply (PLL[LVDS])	VDD18_LVDSPLL 1	1.7	1.8	1.9	V	VDD18_LVDSPLL 1 for power supply and VSS for ground respectively
Power supply (PLL[DDR])	VDD09_DDRPLLn (n = 0, 1)	0.75	0.82	0.88	V	VDD09_DDRPLLn (n = 0, 1) for power supply and VSS for ground respectively

Note: 1. Only for RZ/G2H, RZ/G2N.

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Table 3.2.2 Power Supply for [RZ/G2E]

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N **RZ/G2E**

Item	Symbol	Voltage			Unit	Remarks
		Min.	Typ.	Max.		
Power supply (Internal)	VDD	0.98	1.03	1.08	V	VDD for power supply and VSS for ground
Power supply (PLL[CPG])	VDD18_CPGPLLn (n = 0, 1, 3)	1.7	1.8	1.9	V	VDD18_CPGPLLn (n = 0, 1, 3) for power supply and VSS_CPGPLLn (n = 0, 1, 3)
Power supply (PLL[MLB])	VDD18_MLBPLL	1.7	1.8	1.9	V	VDD18_MLBPLL for power supply and VSS_MLBPLL for ground
Power supply (1.8-V I/O[VDDQ18])	VDDQ18	1.7	1.8	1.9	V	VDDQ18 for power supply and VSS for ground
Power supply (1.8-V I/O [VDDQ18_ISO])	VDDQ18_ISO	1.7	1.8	1.9	V	VDDQ18_ISO for power supply and VSS for ground
Power supply (1.8-V I/O[CSI])	VDDQ18_CSI0	1.7	1.8	1.9	V	VDDQ18_CSI0 for power supply and VSS for ground
Power supply (1.8-V I/O[LVDS])	VDDQ18_LVDS	1.7	1.8	1.9	V	VDDQ18_LVDS for power supply and VSS for ground
Power supply (PLL[LVDS])	VDD18_LVDSnPLL (n = 0, 1)	1.7	1.8	1.9	V	VDD18_LVDSnPLL (n = 0, 1) for power supply and VSS_LVDSnPLL (n = 0, 1) for ground respectively
Power supply (2.5-V I/O[AVB0])	VDDQ25_AVB0	2.3	2.5	2.7	V	VDDQ25_AVB0 for power supply and VSS for ground
Power supply (3.3-V I/O[AVB0])	VDDQ25_AVB0	3.0	3.3	3.6	V	VDDQ25_AVB0 for power supply and VSS for ground
Power supply (3.3-V I/O)	VDDQ33	3.0	3.3	3.6	V	VDDQ33 for power supply and VSS for ground
Power supply (1.35-V I/O[DDR])	VDDQ_CK, VDDQ_DDR	1.283	1.35	1.45	V	VDDQ_CK, VDDQ_DDR for power supply and VSS for ground
Power supply (1.8-V I/O[SD])	VDDQ_SDn (n = 0, 1, 3)	1.7	1.8	1.9	V	VDDQ_SDn (n = 0, 1, 3) for power supply and VSS for ground respectively
Power supply (1.8-V I/O[QSPI])	VDDQ_QSPI	1.7	1.8	1.9	V	VDDQ_QSPI for power supply and VSS for ground respectively
Power supply (3.3-V I/O[SD]	VDDQ_SDn (n = 0, 1, 3)	3.0	3.3	3.6	V	VDDQ_SDn (n = 0, 1, 3) for power supply and VSS for ground respectively
Power supply (3.3-V I/O[QSPI])	VDDQ_QSPI	3.0	3.3	3.6	V	VDDQ_QSPI for power supply and VSS for ground respectively
Power supply (PLL)	VDDQ_ MAPLL	1.7	1.8	1.9	V	VDDQ_MAPLL for power supply and VSS for ground respectively
Power supply (PLL)	VDDQ_MDPLLn (n = 0, 1)	1.7	1.8	1.9	V	VDDQ_MDPLLn (n = 0, 1) for power supply and VSS for ground respectively

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Item	Symbol	Voltage			Unit	Remarks
		Min.	Typ.	Max.		
Power supply (USB)	AVDD_USB	1.7	1.8	1.9	V	AVDD_USB for power supply and AVSS for ground respectively
	VDDQ33_USB2	3.0	3.3	3.6	V	VDDQ33_USB2 for power supply and VSS for ground respectively
	VDDQ18_USB20	1.7	1.8	1.9	V	VDDQ18_USB20 for power supply and VSS for ground respectively
Power supply (USB3.0)	VDDD_USB30	0.98	1.03	1.08	V	VDDD_USB30 for power supply and VSS for ground
	VDDQ18_USB30	1.7	1.8	1.9	V	VDDQ18_USB30 for power supply and VSS for ground
Power supply (PCIe)	VDDD_PCIE0	0.98	1.03	1.08	V	VDDD_PCIE0 for power supply and VSS for ground
	VDDQ18_PCIE0	1.7	1.8	1.9	V	VDDQ18_PCIE0 for power supply and VSS for ground

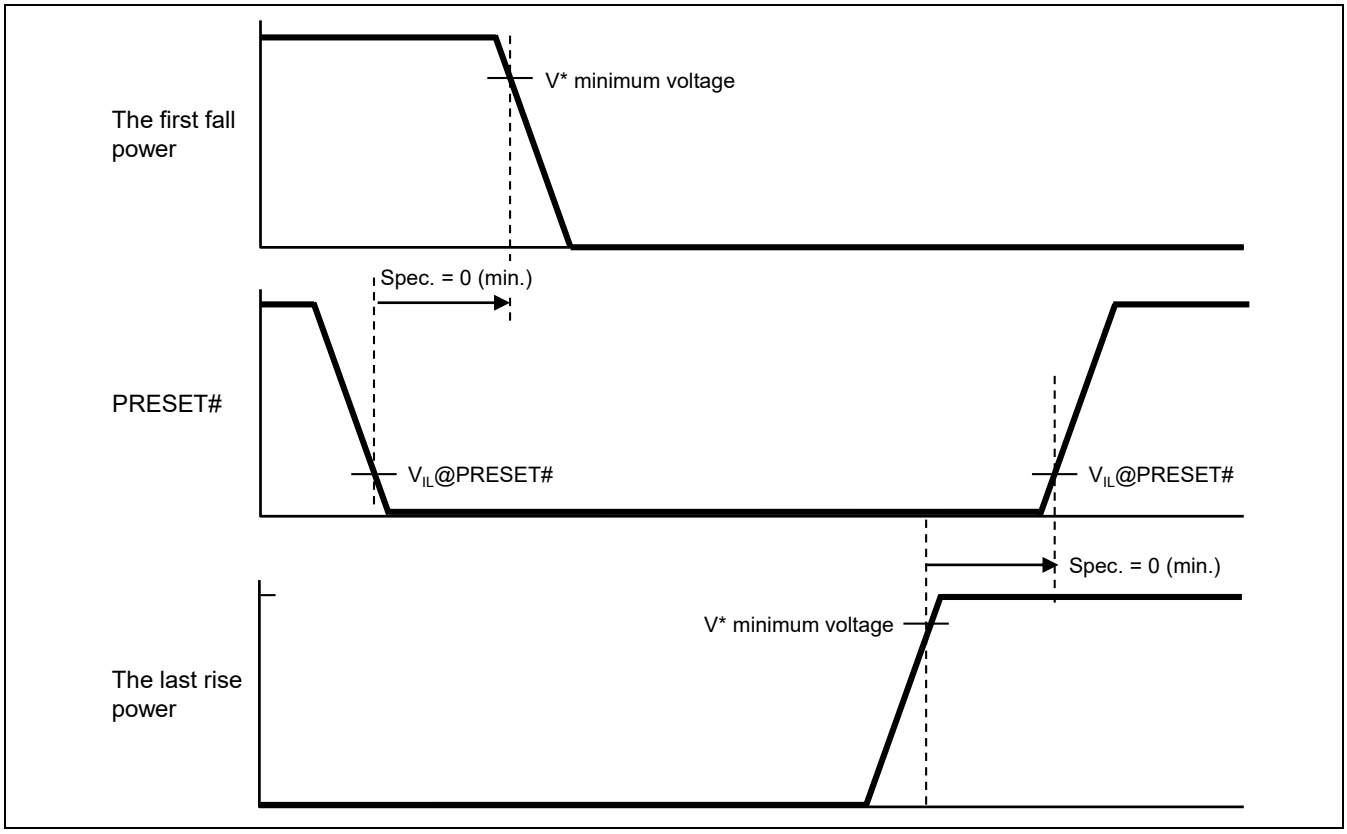
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3.3 Sequence of Turning On/Off Power Supplies

3.3.1 Sequence of Turning On/Off Power Supplies for [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]

RZ/G2H
RZ/G2M V1.3 RZ/G2M V3.0
RZ/G2N RZ/G2E

(1) PRESET# VS. Power for [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]

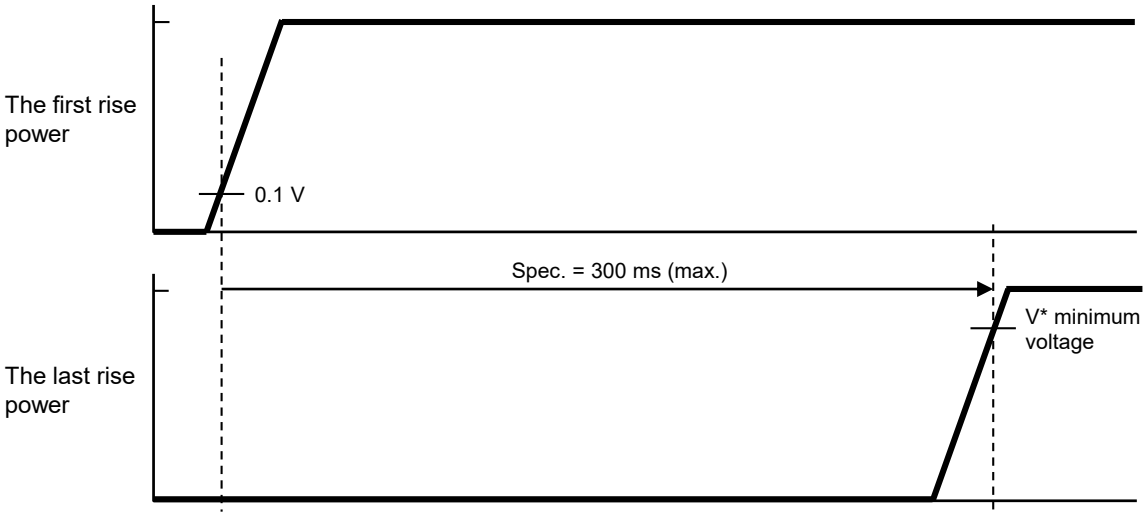


Note that power-on reset, refer to the specifications shown in section 3.5 “Clock and Reset Timings”.

Figure 3.3.1.1 PRESET# VS. Power [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]

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(2) Period for Power Rise for [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]

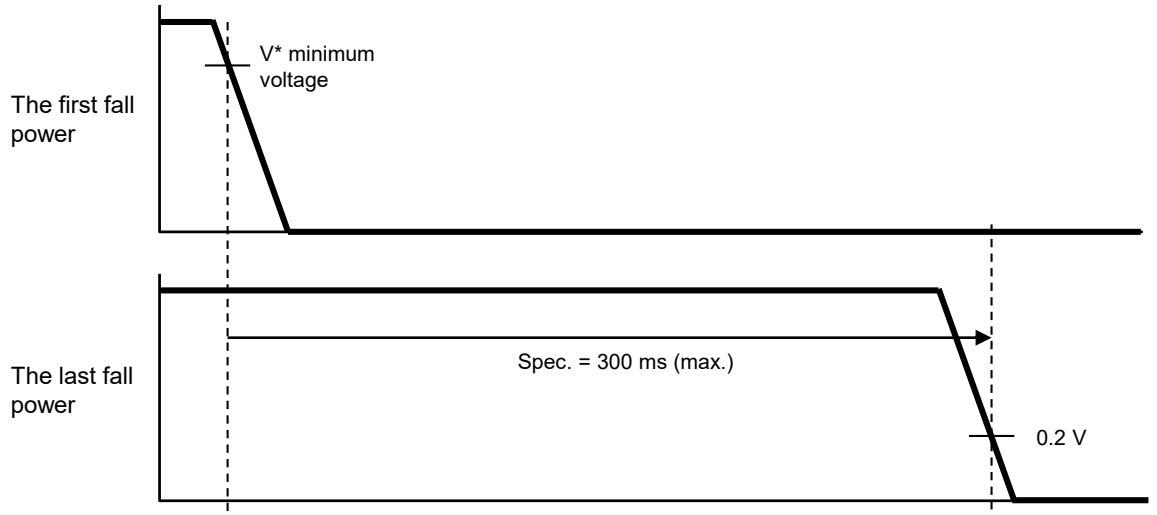


For all V*, power off state must be 0 V (GND), power rising must be started from 0 V, and end to 0 V respectively. (excluding DDR-SDRAM power-supply backup state)
Period from 0 V to 0.1V at power-on and from 0.2 V to 0 V at power-off should be shorten as much as possible.

Figure 3.3.1.2 Period for Power Rise for [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]

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(3) Period for Power Fall for [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]

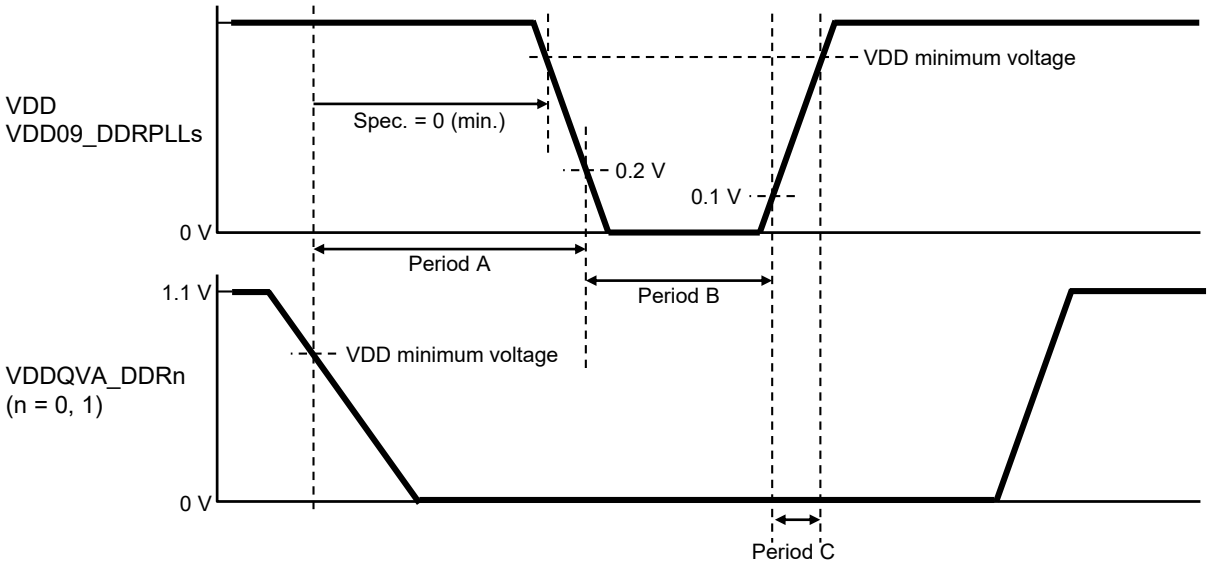


For all V*, power off state must be 0 V (GND), power rising must be started from 0 V, and end to 0 V respectively.
(excluding DDR-SDRAM power-supply backup state)
Period from 0 V to 0.1V at power-on and from 0.2 V to 0 V at power-off should be shorten as much as possible.

Figure 3.3.1.3 Period for Power Fall for [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]

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(4) VDD and VDD09_DDRPLLs vs VDDQVA_DDRn (n = 0, 1) [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]



VDD and VDD09_DDRPLLs must be greater than VDDQVA_DDRn (n = 0, 1) for Period A.
VDDQVA_DDRn (n = 0, 1) must be off for Period B.
VDD and VDD09_DDRPLLs must be greater than VDDQVA_DDRn (n = 0, 1) for Period C.
VDD09_DDRPLLs are VDD09_DDRPLLnm (n = 0-3, m = CA, DQ01, DQ23)

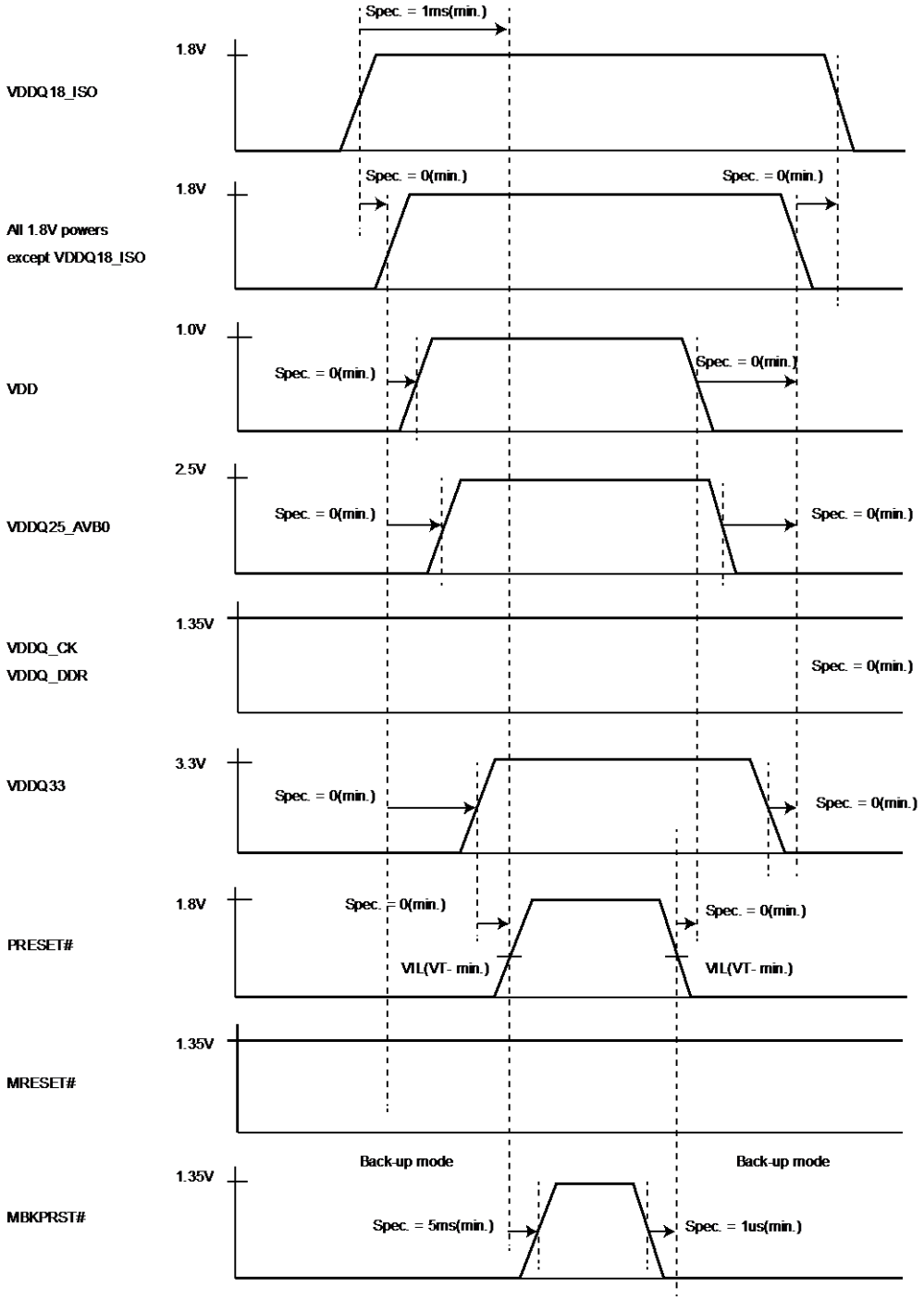
Figure 3.3.1.4 VDD and VDD09_DDRPLLs vs VDDQVA_DDRn (n = 0, 1) [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]

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3.3.2 Sequence of Turning On/Off Power Supplies for [RZ/G2E]

RZ/G2H
RZ/G2M V1.3 RZ/G2M V3.0
RZ/G2N RZ/G2E

(1) Power-up/down sequence with DDR backup [RZ/G2E]

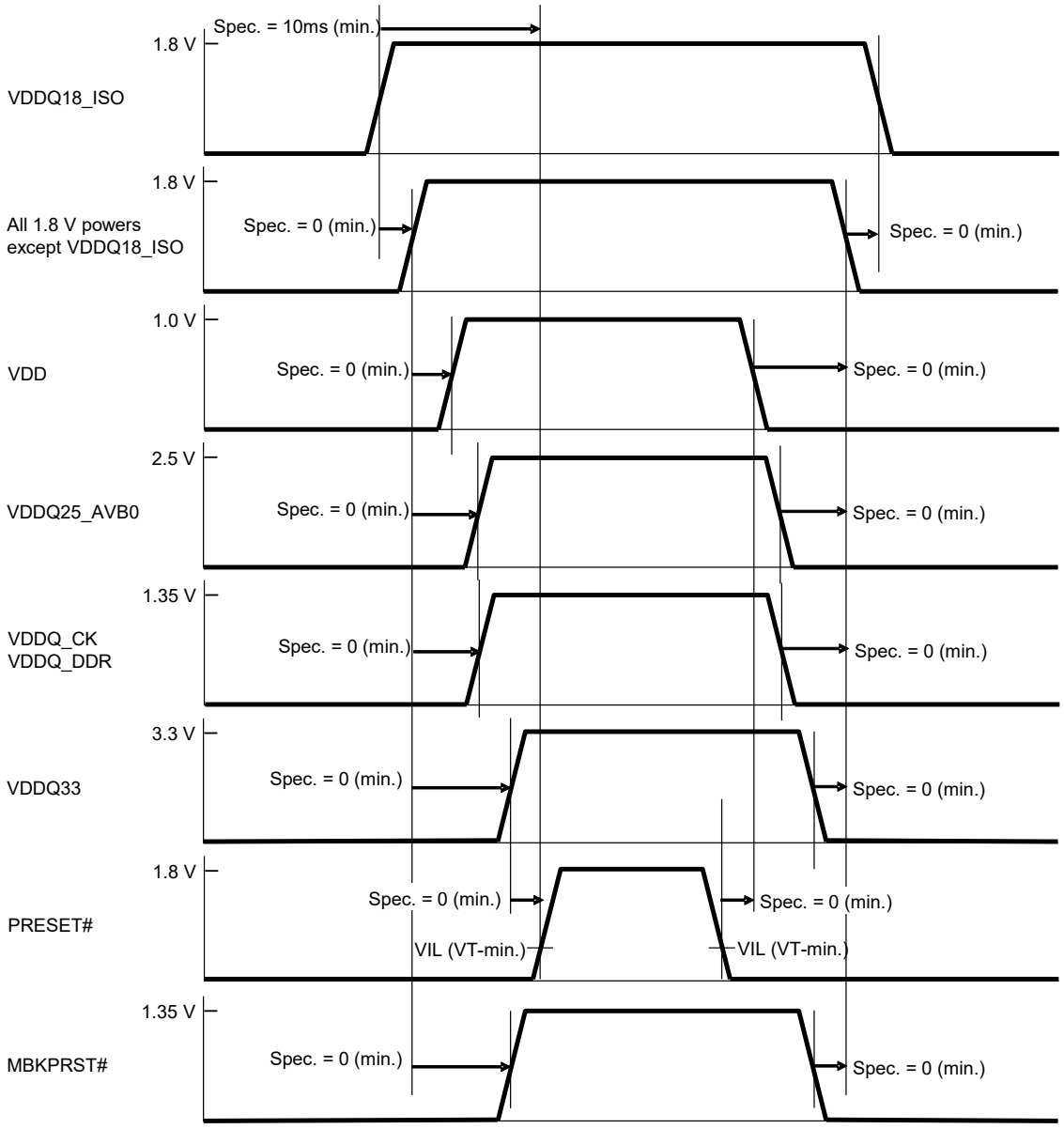


Note: Refer to Figure 3.3.4.1 for the maximum time from first power rising(falling) to last power rising(falling). Note that at power-on reset, refer to the specifications shown in section 3.5 “Clock and Reset Timings”. Even when DDR backup mode is used, the first power up sequence must keep the sequence “RZ/G2E power-up/down sequence without DDR backup”.

Figure 3.3.2.1 power-up/down sequence with DDR backup [RZ/G2E]

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(2) Power-up/down sequence without DDR backup [RZ/G2E]



Notes: 1. Refer to Figure 3.3.4.1 for the maximum time from first power rising(falling) to last power rising(falling). Note that at power-on reset, refer to the specifications shown in section 3.5 “Clock and Reset Timings”.
2. MBKPRST# input must track VDDQ_DDR/VDDQ_CK during VDDQ_DDR/VDDQ_CK power-up.

Figure 3.3.2.2 power-up/down sequence without DDR backup [RZ/G2E]

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3.3.3 Wave form definition for power sequence [RZ/G2E]

RZ/G2H
RZ/G2M V1.3 RZ/G2M V3.0
RZ/G2N **RZ/G2E**

This definition is for the different voltage power supply for example between 1.8-V and 3.3-V, it is possible to turn on or off at the same time for the same voltage power supply.

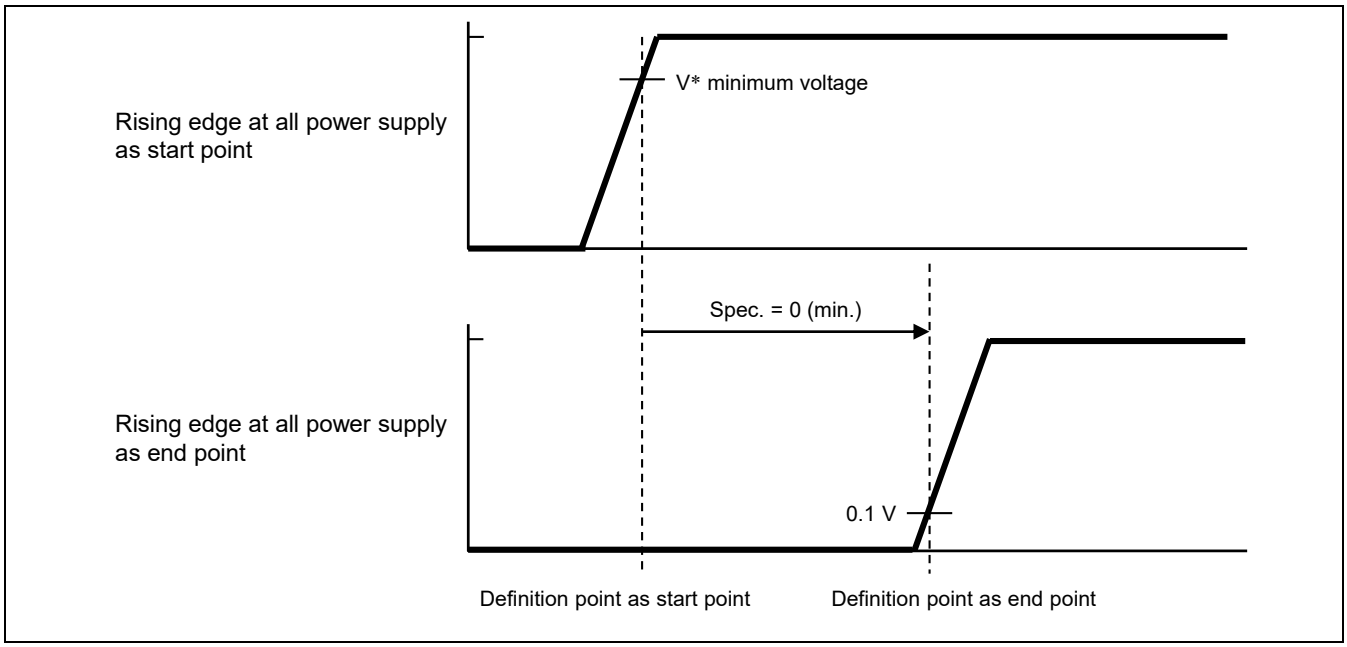


Figure 3.3.3.1 Period for Power Rise for [RZ/G2E]

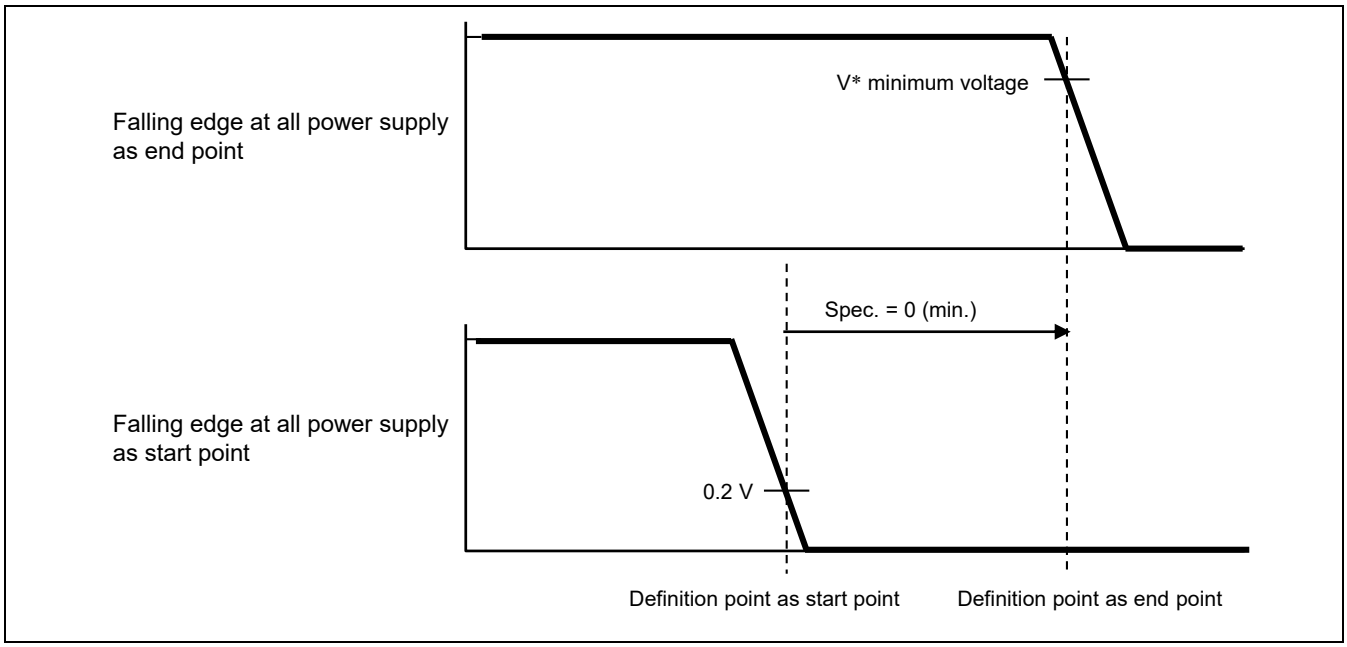
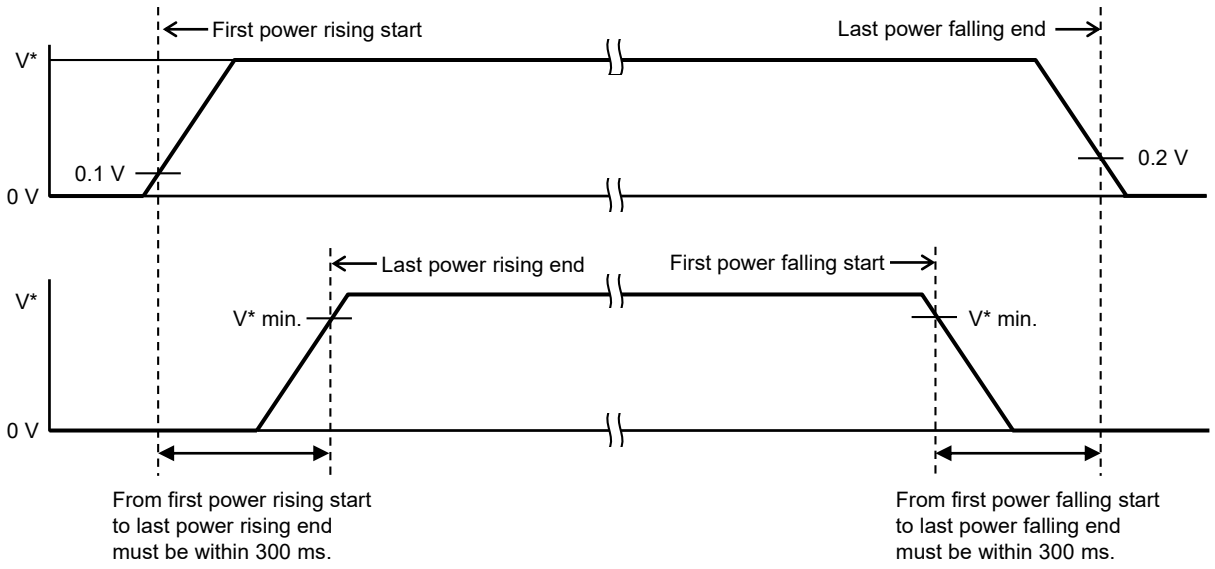


Figure 3.3.3.2 Period for Power Fall for [RZ/G2E]

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3.3.4 Power On and Power Off Wave Form [RZ/G2E]

RZ/G2H
RZ/G2M V1.3 RZ/G2M V3.0
RZ/G2N **RZ/G2E**



Note: For all V*, power off state must be 0 V (GND), power rising must be started from 0 V and power falling must be ended to 0 V (excluding DDR-SDRAM power-supply backup state).
Periods from 0 V to 0.1 V at power-on and from 0.2 V to 0 V at power-off should be shortened as much as possible.

Figure 3.3.4.1 Power On and Power Off Wave Form [RZ/G2E]

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3.4 DC Characteristics

Table 3.4.1 Supply Current for LSI

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Item	Symbol	Power Min.	Typ.	Max.	Unit	Remarks
Supply current (Internal)	IDD	—	—	8700 6846.0 6908.0 3554.9	mA mA mA mA	VDD = 0.88 V [RZ/G2H] VDD = 0.88 V [RZ/G2M V1.3] VDD = 0.88 V [RZ/G2M V3.0] VDD = 0.88 V [RZ/G2N] Condition: Cortex-A53: Dhrystone-MAX,
Supply current (Internal)	IDD_DVFS	—	—	12000 7632.9 8351.0 5554.6	mA mA mA mA	VDD_DVFS = 0.88 V [RZ/G2H] VDD_DVFS = 0.88 V [RZ/G2M V1.3] VDD_DVFS = 0.88 V [RZ/G2M V3.0] VDD_DVFS = 0.88 V [RZ/G2N] Condition: Cortex-A57: Dhrystone-MAX, GPU: Polygon fill-MAX
Supply current (3.3-V I/O)	IDDQ33	—	—	94	mA	VDDQ33 = 3.5 V [RZ/G2H], [RZ/G2M V1.3], [RZ/G2N]
Supply current (3.3-V I/O [SDHI])	IDDQVA_SDn (n = 0 to 3)	—	—	31	mA	VDDQVA_SDn = 3.5 V (n = 0 to 3) [RZ/G2H], [RZ/G2M V1.3], [RZ/G2N]
Supply current (3.3-V I/O [SATA])	IDD33_SATA	—	—	57.6	mA	VDD33_SATA = 3.5 V [RZ/G2H], [RZ/G2N]
Supply current (3.3-V I/O [PCIE])	IDD33_PCIEn (n = 0, 1)	—	—	57.6	mA	VDD33_PCIEn = 3.5 V (n = 0, 1) [RZ/G2H], [RZ/G2M V1.3], [RZ/G2N]
Supply current (3.3-V I/O [USB3HSH])	IDDQ33_USB3HSHn (n = 0)	—	—	72	mA	VDDQ33_USB3HSHn = 3.5V (n = 0) [RZ/G2H], [RZ/G2M V1.3], [RZ/G2N]
Supply current (3.3-V I/O [USB3HS])	IDDQ33_USB3HSn (n = 0)	—	—	72	mA	VDDQ33_USB3HSn = 3.5 V (n = 0) [RZ/G2H], [RZ/G2M V1.3], [RZ/G2N]
Supply current (3.3-V I/O [USB3])	IDD33_USB3n (n = 0)	—	—	57.6	mA	VDD33_USB3n = 3.5 V (n = 0) [RZ/G2H], [RZ/G2M V1.3], [RZ/G2N]
Supply current (3.3-V I/O [USB2H])	IDDQ33_USB2Hn (n = 0 to 3)	—	—	72	mA	VDDQ33_USB2Hn = 3.5 V (n = 0, 1) [RZ/G2H], [RZ/G2M V1.3], [RZ/G2N]
Supply current (3.3-V I/O [USB2])	IDDQ33_USB2	—	—	216 144	mA mA	VDDQ33_USB2 = 3.5 V [RZ/G2H] VDDQ33_USB2 = 3.5 V [RZ/G2M V1.3], [RZ/G2N]
Supply current (2.5-V I/O [ETH])	IDDQ25_ETH	—	—	40	mA	VDDQ25_ETH = 2.6 V [RZ/G2H], [RZ/G2M V1.3], [RZ/G2N]
Supply current (1.8-V I/O [VDDQ18])	IDDQ18	—	—	50	mA	VDDQ18 = 1.9 V [RZ/G2H], [RZ/G2M V1.3], [RZ/G2N]
Supply current (1.8-V I/O [HDMI])	IDDQ18_HDMIn (n = 0, 1)	—	—	10.5	mA	VDDQ18_HDMIn = 1.9 V (n = 0) [RZ/G2H], [RZ/G2M V1.3], [RZ/G2N]
Supply current (1.8-V I/O [LVDS])	IDDQ18_LVDS	—	—	110.2	mA	VDDQ18_LVDS = 1.9 V [RZ/G2H], [RZ/G2M V1.3], [RZ/G2N]

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Item		Symbol	Power Min.	Typ.	Max.	Unit	Remarks
Supply current (1.8-V I/O [CSI])		IDDQ18_CSIn (n = 0 to 2)	—	—	6.3	mA	VDDQ18_CSIn = 1.9 V (n = 0, 2) [RZ/G2H] (n = 0)
					4.5	mA	VDDQ18_CSIn = 1.9 V (n = 1) [RZ/G2H]
					6.3	mA	VDDQ18_CSIn = 1.9 V (n = 0) [RZ/G2M V1.3], [RZ/G2N]
					4.5	mA	VDDQ18_CSIn = 1.9 V (n = 1) [RZ/G2M V1.3], [RZ/G2N]
Supply current (1.8-V I/O [SDHI(SDR50, SDR104)])		IDDQVA_SDn (n = 0 to 3)	—	—	35	mA	VDDQVA_SDn = 1.9 V (n = 0 to 3) [RZ/G2H], [RZ/G2M V1.3] , [RZ/G2N]
Supply current (1.1-V I/O [DDR(LPDDR4)])	Normal	IDDQVA_DDRn (n = 0, 1)	—	—	470	mA	VDDQVA_DDRn = 1.17 V (n = 0, 1) [RZ/G2M V1.3], [RZ/G2M V3.0], [RZ/G2H]
					330	mA	VDDQVA_DDRn = 1.17 V (n = 0) [RZ/G2N]
							Condition: Driver impedance: 40Ω No termination Load capacitance: 2.5pF Write Read rate: 50%, 50% I/O Toggle rate: 100%
	DDR power supply backup		—	—	8	mA	VDDQVA_DDRn = 1.17 V (n = 0, 1) [RZ/G2H]
					4	mA	VDDQVA_DDRn = 1.17 V (n = 0, 1) [RZ/G2M V1.3]
					3	mA	VDDQVA_DDRn = 1.17 V (n = 0) [RZ/G2N]
Supply current (0.9-VI/O[SATA])		IDD09_SATA	—	—	162	mA	VDD09_SATA = 0.88 V [RZ/G2H], [RZ/G2N]
Supply current (0.9-VI/O[PCIE])		IDD09_PCIEn (n = 0, 1)	—	—	162 [RZ/G2H], [RZ/G2N]	mA	VDD09_PCIEn = 0.88 V (n = 0, 1) [RZ/G2H], [RZ/G2M V1.3], [RZ/G2N]
					90 [RZ/G2M V1.3]		
Supply current (0.9-VI/O[USB3])		IDD09_USB3n (n = 0)	—	—	162 [RZ/G2H], [RZ/G2N]	mA	VDD09_USB3n = 0.88 V (n = 0) [RZ/G2H], [RZ/G2M V1.3], [RZ/G2N]
					90 [RZ/G2M V1.3]		
Supply current (0.9-VI/O[USB3HS])		IDD09_USB3HSn (n = 0)	—	—	50.4 [RZ/G2H], [RZ/G2N]	mA	VDD09_USB3HSn = 0.88 V (n = 0) [RZ/G2H], [RZ/G2M V1.3], [RZ/G2N]
					28 [RZ/G2M V1.3]		
Supply current (0.9-VI/O[USB2])		IDD09_USB2n (n = 0 to 3)	—	—	28	mA	VDD09_USB2n = 0.88 V (n = 0, 1) [RZ/G2H], [RZ/G2M V1.3], [RZ/G2N]
Supply current (0.9-VI/O[HDMI])		IDDQ09_HDMIn (n = 0, 1)	—	—	33.7	mA	VDDQ09_HDMIn = 0.88 V (n = 0) [RZ/G2H], [RZ/G2M V1.3], [RZ/G2N]
Supply current (0.9-VI/O[LVDS])		IDDQ09_LVDS	—	—	9	mA	VDDQ09_LVDS = 0.88 V [RZ/G2H], [RZ/G2M V1.3], [RZ/G2N]

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Item	Symbol	Power			Unit	Remarks
		Min.	Typ.	Max.		
Supply current (0.9-VI/O[CSI])	IDD09_CSIn (n = 0 to 2)	—	—	28.8	mA	VDD09_CSIn = 0.88 V (n = 0) [RZ/G2H]
				18	mA	VDD09_CSIn = 0.88 V (n = 1) [RZ/G2H]
				28.8	mA	VDD09_CSIn = 0.88 V (n = 0) [RZ/G2M V1.3], [RZ/G2N]
				18	mA	VDD09_CSIn = 0.88 V (n = 1) [RZ/G2M V1.3], [RZ/G2N]
Supply current (PLL [CPG])	IDD18_CPGPLLn (n = 0 to 4)	—	—	3.0	mA	VDD18_CPGPLLn = 1.9 V (n = 0 to 4) [RZ/G2H], [RZ/G2M V1.3], [RZ/G2N]
Supply current (PLL [MLB])	IDD18_MLBPLL	—	—	3.0	mA	VDD18_MLBPLL = 1.9 V [RZ/G2H], [RZ/G2M V1.3], [RZ/G2N]
Supply current (PLL [DU])	IDD18_DUPLLn (n = 0, 1)	—	—	3.0	mA	VDD18_DUPLLn = 1.9 V (n = 0) [RZ/G2H], [RZ/G2M V1.3], [RZ/G2N]
Supply current (PLL [LVDS])	IDD18_LVDSPLL 1	—	—	12.6	mA	VDD18_LVDSPLL1 = 1.9 V [RZ/G2H], [RZ/G2M V1.3], [RZ/G2N]
Supply current (PLL [LVDS])	IDD09_LVDSPLL 2	—	—	18	mA	VDD09_LVDSPLL2 = 0.88 V [RZ/G2H], [RZ/G2M V1.3], [RZ/G2N]
Supply current (PLL [DDR])	IDD09_DDRPLL n (n = 0, 1)	—	—	50	mA	VDD09_DDRPLLn = 0.88 V (n = 0, 1) [RZ/G2M V1.3]
						VDD09_DDRPLLn = 0.88 V (n = 0) [RZ/G2N]

Note: Tc(Tt) = 115 °C (ΘJc = 0.1°C/W) [RZ/G2H], [RZ/G2M V1.3]

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Table 3.4.2 Supply current for [RZ/G2E]

RZ/G2H
RZ/G2M V1.3 RZ/G2M V3.0
RZ/G2N **RZ/G2E**

Item	Symbol	Power			Unit	Remarks
		Min.	Typ.	Max.		
Supply current (Internal)	IDD	—	—	5649.1	mA	VDD = 1.08V
Supply current (3.3V I/O)	IDDQ33	—	—	92.6	mA	VDDQ33 = 3.6V
Supply current (3.3V I/O[QSPI])	IDDQ_QSPI	—	—	21.6	mA	VDDQ_QSPI = 3.6V
Supply current (3.3V I/O[SDHI])	IDDQ_SDn (n = 0, 1, 3)	—	—	5.4	mA	VDDQ_SDn (n = 0, 1, 3) = 3.6V, Highspeed mode
Supply current (3.3V I/O[AVB0])	IDDQ25_AVB0	—	—	4.5	mA	VDDQ25_AVB0 = 3.6V, 100Mbps
Supply current (3.3V I/O[USB2])	IDDQ33_USB2	—	—	60 (30/ch)	mA	VDDQ33_USB2 = 3.6V
Supply current (2.5V I/O[AVB0])	IDDQ25_AVB0	—	—	24.4	mA	VDDQ25_AVB0 = 2.7V, 1Gbps
Supply current (1.8V I/O)	IDDQ18	—	—	25.2	mA	VDDQ18 = 1.9V
Supply current (1.8V I/O[ISO])	IDDQ18_ISO	—	—	2	mA	VDDQ18_ISO = 1.9V
Supply current (1.8V I/O[QSPI])	IDDQ_QSPI	—	—	25.7	mA	VDDQ_QSPI = 1.9V
Supply current (1.8V I/O[SDHI])	IDDQ_SDn (n = 0, 1, 3)	—	—	11.4	mA	VDDQ_SDn (n = 0, 1, 3) = 1.9V, SDR104
Supply current (1.8V I/O[SDHI])	IDDQ_SD3	—	—	67.8	mA	VDDQ_SD3 = 1.9V, HS400
Supply current (PLL[CPG])	IDDQ18_CPGPLL0	—	—	4	mA	VDD18_CPGPLL0 = 1.9V
Supply current (PLL[CPG])	IDDQ18_CPGPLLn (n = 1, 3)	—	—	2	mA	VDD18_CPGPLLn (n = 1, 3) = 1.9V
Supply current (1.8V I/O[LVDS])	IDDQ18_LVDS	—	—	100	mA	VDDQ18_LVDS = 1.9V
Supply current (PLL[LVDS])	LVDSn_PLL_ICC (n = 0, 1)	—	—	2	mA	VDD18_LVDSnPLL (n = 0, 1) = 1.9V
Supply current (1.8V I/O[CSI])	IDDQ18_CSI0	—	—	13	mA	VDDQ18_CSI0 = 1.9V
Supply current (1.8V[USB2])	IDD_AVD0+IDDQ18_USB20,	—	—	80, (40/ch)	mA	AVDD_USB = VDDQ18_USB20 = 1.9V
Supply current (1.8V I/O[USB30])	IDDQ18_USB30	—	—	13	mA	VDDQ18_USB30 = 1.9V
Supply current (1.8V I/O[PCIE0])	IDDQ18_PCIE0	—	—	13	mA	VDDQ18_PCIE0 = 1.9V
Supply current (PLL[MAPLL])	IDDQ_MAPLL	—	—	26.6	mA	VDDQ_MAPLL = 1.9V
Supply current (PLL[MDPLL])	IDDQ_MDPLLn (n = 0, 1)	—	—	26.6	mA	VDDQ_MDPLLn (n = 0, 1) = 1.9V
Supply current (PLL[MLB])	IDDQ18_MLBPLL	—	—	4	mA	VDD18_MLBPLL = 1.9V

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Item		Symbol	Power			Unit	Remarks
			Min.	Typ.	Max.		
Supply current (1.35V [DDR3L])	Normal	IDDQ_CK + IDDQ_DDR	—	—	959	mA	VDDQ_CK = VDDQ_DDR = 1.45V (total value)
	DDR power supply backup		—	—	2.9	mA	VDDQ_CK = VDDQ_DDR=1.45 V (total value)
	Normal	IDDQ_CK	—	—	63.0	mA	VDDQ_CK = 1.45V
Supply current (1.0V [PCIE])		IDDD_PCIE0	—	—	110	mA	VDDD_PCIE0 = 1.08V
Supply current (1.0V [USB30])		IDDD_USB30	—	—	110	mA	VDDD_USB30 = 1.08V

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Table 3.4.3 DC Characteristics (3.3-V I/O)

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Input high voltage	VIH	2.0	—	VDDQ33 + 0.3	V	VDDQ33 = 3.1 to 3.5 V	—
Input low voltage	VIL	-0.3	—	0.8	V		
Output high voltage	VOH	2.4	—	—	V	VDDQ33 = 3.1 to 3.5 V	IOH = -4 mA
Output low voltage	VOL	—	—	0.4	V		IOL = 4 mA
Pin capacitance	CL	—	—	10 22	pF	—	All pins
Input leakage current	ILI	—	—	10	µA	VDDQ33 = 3.1 to 3.5 V	All input pins
Output leakage current	ILO	—	—	10	µA	Without pull-up or pull-down resistor	Hi-Z output
Pull-up current	IPU	40	—	115	µA	VDDQ33 = 3.1 to 3.5 V	Vin = VSS
Pull-down current	IPD	40	—	115	µA	—	Vin = 3.1 to 3.5 V

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Table 3.4.4 DC Characteristics (3.3-V I/O)

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N **RZ/G2E**

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Input high voltage	VIH	2.0	—	VDDQ33 + 0.3	V	VDDQ33 = 3.0 to 3.6 V	—
Input low voltage	VIL	-0.3	—	0.8	V		
Output high voltage	VOH	2.4	—	VDDQ33 + 0.3	V	VDDQ33 = 3.0 to 3.6 V	IOH = -4 mA
Output low voltage	VOL	-0.3	—	0.4	V		IOL = 4 mA
Pin capacitance	CL	—	—	10	pF	—	All pins
Input leakage current	ILI	—	—	1	µA	VDDQ33 = 3.0 to 3.6 V	All input pins
Output leakage current	ILO	—	—	1	µA	Without pull-up or pull-down resistor	Hi-Z output
Pull-up current	IPU	-34	—	-360	µA	VDDQ33 = 3.0 to 3.6 V	Vin = VSS
Pull-down current	IPD	34	—	360	µA	—	Vin = 3.0 to 3.6 V

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Table 3.4.5 DC Characteristics (3.3-V I/O [SDHI])

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Input high voltage	VIH	0.625 × VDDQVA_SD	—	VDDQVA_SD + 0.3	V	VDDQVA_SDn (n = 0 to 3) = 3.1 to 3.5 V, VSS = 0 V	—
Input low voltage	VIL	VSS – 0.3	—	0.25 × VDDQVA_SD	V		—
Output high voltage	VOH	0.75 × VDDQVA_SD	—	—	V		IOH = -2 mA VDDQVA_SDn min
Output low voltage	VOL	—	—	0.125 × VDDQVA_SD	V		IOL = 2 mA VDDQVA_SDn min
Pin capacitance	CL	—	—	10	pF		—
Input leakage current	ILI	—	—	10	µA	VDDQVA_SDn (n = 0 to 3) = 3.1 to 3.5 V, VSS = 0 V Without pull-up or pull-down resistor	—
Output leakage current	ILO	—	—	10	µA		Hi-Z output

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Table 3.4.6 DC Characteristics (3.3-V I/O [AVB0])

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N **RZ/G2E**

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Input high voltage	VIH	2.0	—	VDDQ33 + 0.3	V	VDDQ33 = 3.0 to 3.6 V	—
Input low voltage	VIL	-0.3	—	0.8	V		
Output high voltage	VOH	2.4	—	VDDQ33 + 0.3	V	VDDQ33 = 3.0 to 3.6 V	IOH = -4 mA
Output low voltage	VOL	-0.3	—	0.4	V		IOL = 4 mA
Pin capacitance	CL	—	—	10	pF	—	All pins
Input leakage current high	ILIH	—	—	10	µA	VDDQ33 = 3.0 to 3.6 V	All input pins
Input leakage current low	ILIL	-10	—	—	µA	Without pull-up or pull-down resistor	—
Output leakage current high	ILOH	—	—	10	µA		Hi-Z output
Output leakage current low	ILOL	-10	—	—	µA		—
Pull-up current	IPU	-34	—	-360	µA	VDDQ33 = 3.0 to 3.6 V	Vin = VSS
Pull-down current	IPD	34	—	360	µA	—	Vin = 3.0 to 3.6 V

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Table 3.4.7 DC Characteristics (2.5-V I/O [AVB])

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Input high voltage	VIH	1.7	—	VDDQ25_ETH+ 0.3	V	VDDQ25_ETH = 2.4 to 2.6V	—
Input low voltage	VIL	-0.3	—	0.7	V		
Output high voltage	VOH	2.0	—	—	V	VDDQ25_ETH = 2.4 to 2.6V	IOH= -1 mA
Output low voltage	VOL	—	—	0.4	V		IOL = 1 mA
Pin capacitance	CL	—	—	10	pF	—	—
Input leakage current high	ILIH	—	—	15	µA	VDDQ25_ETH = 2.6 V, Vin = 2.5 V *1	—
Input leakage current low	ILIL	-15	—	—	µA	VDDQ25_ETH = 2.6 V, Vin = 0.4 V *1	—
Output leakage current high	ILOH *1	—	—	10	µA	—	Hi-Z output*1
Output leakage current low	ILOL *1	-10	—	—	µA	—	Hi-Z output*1
Pull-up current	IPU	30	—	85	µA	VDDQ25_ETH = 2.4 to 2.6 V	Vin = VSS
Pull-down current	IPD	30	—	85	µA	—	Vin = 2.4 to 2.6 V

Note: *1 Without pull-up or pull-down resistor.

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Table 3.4.8 DC Characteristics (2.5-V I/O [AVB0])

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N **RZ/G2E**

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Input high voltage	VIH	1.7	—	VDDQ25_AVB0 + 0.3	V	VDDQ25_AVB0 = 2.3 V to 2.7 V	—
Input low voltage	VIL	-0.3	—	0.7	V		—
Output high voltage	VOH	2.0	—	—	V	VDDQ25_AVB0 = 2.3 V to 2.7 V	IOH = -1 mA
Output low voltage	VOL	—	—	0.4	V		IOL = 1 mA
Input leakage current high	ILIH	—	—	10	µA	—	—
Input leakage current low	ILIL	-10	—	—	µA	—	—
Output leakage current high	ILOH	—	—	10	µA	—	—
Output leakage current low	ILOL	-10	—	—	µA	—	—
Pull-up current	IPU	-26	—	-270	µA	VDDQ25_AVB0 = 2.3 V to 2.7 V	Vin = VSS
Pull-down current	IPD	26	—	270	µA	—	Vin =2.3 V to 2.7 V

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Table 3.4.9 DC Characteristics (1.8-V I/O [SDHI (SDR50, SDR104)])

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Input high voltage	VIH	1.27	—	VDDQVA_SD + 0.3	V	VSS = 0 V	—
Input low voltage	VIL	VSS – 0.3	—	0.58	V		—
Output high voltage	VOH	1.4	—	—	V		IOH = -2 mA
Output low voltage	VOL	—	—	0.45	V		IOL = 2 mA
Pin capacitance	CL	—	—	10	pF		—
Input leakage current	ILI	—	—	10	µA	VSS = 0 V Without pull-up or pull-down resistor	—
Output leakage current	ILO	—	—	10	µA		Hi-Z output

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Table 3.4.10 DC Characteristics (1.8-V I/O [MMC])

RZ/G2H
RZ/G2M V1.3 RZ/G2M V3.0
RZ/G2N RZ/G2E

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Input high voltage	VIH	VDDQVA_SDn - 0.45	—	VDDQVA_SDn + 0.3	V	VDDQVA_SDn (n = 0 to 3) = 1.7 to 1.9 V VSS = 0 V	—
Input low voltage	VIL	VSS – 0.3	—	0.58	V		—
Output high voltage	VOH	1.4	—	—	V		IOH = -2 mA
Output low voltage	VOL	—	—	0.45	V		IOL = 2 mA
Pin capacitance	CL	—	—	10	pF		—
Pull-up current	IPU	-20	—	-65	µA		Vin = VSS
Pull-down current	IPD	20	—	65	µA		Vin = 1.7 to 1.9V
Input leakage current	ILI	—	—	10	µA	VSS = 0 V Without pull-up or pull-down resistor	—
Output leakage current	ILO	—	—	10	µA		Hi-Z output

RZ/G2H
RZ/G2M V1.3 RZ/G2M V3.0
RZ/G2N RZ/G2E

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Input high voltage	VIH	VDDQ_SDn - 0.45	—	VDDQ_SDn + 0.3	V	VDDQ_SDn (n = 0, 1, 3) = 1.7 to 1.9 V VSS = 0 V	—
Input low voltage	VIL	VSS – 0.3	—	0.58	V		—
Output high voltage	VOH	1.4	—	—	V		IOH = -2 mA
Output low voltage	VOL	—	—	0.45	V		IOL = 2 mA
Pin capacitance	CL	—	—	10	pF		—
Pull-up current	IPU	-19	—	-195	µA		Vin = VSS
Pull-down current	IPD	19	—	195	µA		Vin = 1.7 to 1.9V
Input leakage current	ILI	—	—	1	µA	VSS = 0 V Without pull-up or pull-down resistor	—
Output leakage current	ILO	—	—	1	µA		Hi-Z output

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Table 3.4.11 DC Characteristics (1.8-V I/O)

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Schmitt input high voltage	VT+	—	—	VDDQ18 × 0.7	V	VDDQ18 = 1.7 to 1.9 V	PRESET#, BSMODE, NMI pins
Schmitt input low voltage	VT-	VDDQ18 × 0.3	—	—	V		
Input high voltage	VIH	VDDQ18 × 0.8	—	VDDQ18 + 0.3	V	—	EXTAL, USB_EXTAL pins
Input low voltage	VIL	-0.3	—	VDDQ18 × 0.2	V		
Input high voltage (1.8-V LVCMOS)	VIH	0.65 × VDDQ18	—	VDDQ18 + 0.3	V	VDDQ18 = 1.7 to 1.9 V	Other pins
Input low voltage (1.8-V LVCMOS)	VIL	-0.3	—	0.35 × VDDQ18	V		
Output high voltage	VOH	0.7 × VDDQ18	—	—	V	VDDQ18 = 1.7 to 1.9 V	IOH = - 4 mA
Output low voltage	VOL	—	—	0.4	V		IOL = 4 mA
Pin capacitance	CL	—	—	10	pF	—	—
Input leakage current	ILI	—	—	10	µA	VDDQ18 = 1.7 to 1.9 V	All input pins
Output leakage current	ILO	—	—	10	µA	Without pull-up or pull-down resistor	Hi-Z output
Pull-up current	IPU	20	—	65	µA	VDDQ18 = 1.7 to 1.9 V	Vin = VSS
Pull-down current	IPD	20	—	65	µA	—	Vin = 1.7 to 1.9 V

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Table 3.4.12 DC Characteristics (1.8-V I/O)

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N **RZ/G2E**

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Schmitt input high voltage	VT+	VDDQ18 × 0.4	—	VDDQ18 × 0.7	V	VDDQ18 = 1.7 to 1.9 V	PRESET#, BSMODE, NMI pins ΔV = |Vout-Vin| ≤ 0.1 [V], Vout: IO voltage of external devices Vin: VDDQ18
Schmitt input low voltage	VT-	VDDQ18 × 0.3	—	VDDQ18 × 0.6	V		
Hysteresis voltage	ΔVT	VDDQ18 × 0.1	—	VDDQ18 × 0.4	V		
Input high voltage	VIH	VDDQ18 × 0.8	—	VDDQ18 + 0.3	V	VDDQ18 = 1.7 to 1.9 V	EXTAL pin
Input low voltage	VIL	-0.3	—	VDDQ18 × 0.2	V		
Input high voltage (1.8-V LVCMOS)	VIH	0.65 × VDDQ18	—	VDDQ18 + 0.3	V	VDDQ18 = 1.7 to 1.9 V	Other pins
Input low voltage (1.8-V LVCMOS)	VIL	-0.3	—	0.35 × VDDQ18	V		
Output high voltage	VOH	0.7 × VDDQ18	—	VDDQ18 + 0.3	V	VDDQ18 = 1.7 to 1.9 V	IOH = -4 mA
Output low voltage	VOL	-0.3	—	0.4	V		IOL = 4 mA
Pin capacitance	CL	—	—	10	pF	—	—
Input leakage current	ILI	—	—	1	μA	VDDQ18 = 1.7 to 1.9 V	All input pins
Output leakage current	ILO	—	—	1	μA	Without pull-up or pull-down resistor	Hi-Z output
Pull-up current	IPU	-19	—	-195	μA	VDDQ_DU = VDDQ_VIN01 = 1.7 to 1.9 V	Vin = VSS
Pull-down current	IPD	19	—	195	μA	—	Vin = 1.7 to 1.9 V
Pull-up current	IPU	-5	—	-39	μA	VDDQ18 = 1.7 to 1.9 V	All pins Vin = VSS
Pull-down current	IPD	5	—	39	μA	—	Other than PRESET# pin Vin = 1.7 to 1.9 V
PRESET# Pull-down current	IPD PRST	12	—	30	μA	VDDQ18 = 1.7 to 1.9 V	PRESET# pin Vin = 1.7 to 1.9 V
PRESET# Pull-down resistor	RPD PRST	65	—	135	kΩ	—	PRESET# pin

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Table 3.4.13 DC Characteristics (I2C open-drain 1.8-V I/O)

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks	
External pull-up voltage	VPU18	1.7	1.8	1.9	V	—	—	I2Cn_SCL/SDA (I2C open-drain assigned channels) *
	VPU33	3.1	3.3	3.5	V	—	—	
Input high voltage	VIH	VDDQ18 × 0.7	—	VPU18 + 0.3	V	VDDQ18 = 1.7 to 1.9 V	—	
			—	VPU33 + 0.3	V			
Input low voltage	VIL	-0.3	—	VDDQ18 × 0.3	V			HDMI0_SCL/SDA
Output low voltage	VOL	—	—	VDDQ18 × 0.2	V	VDDQ18 = 1.7 to 1.9 V	IOL= 2mA	I2C_PMIC_SCL/SDA (only RZ/G2E)
		—	—	0.4	V		IOL= 3mA	
Output low current	IOL	3	—	—	mA		VOL = 0.4V	

Notes: 1. Refer to section 52.1.2 in the RZ/G Gen2_HW_Users_Manual.
2. When using 1.8V I2C pins as 3.3 V tolerant, all the VPU33 power supply for the I2C of this LSI must keep the same power on/off sequence as the VDDQ33 of this LSI.

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Table 3.4.14 DC Characteristics (I2C 3.3-V I/O)

RZ/G2H
RZ/G2M V1.3 RZ/G2M V3.0
RZ/G2N RZ/G2E

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Input high voltage	VIH	2.0	—	VDDQ33 + 0.3	V	VDDQ33 = 3.1 to 3.5 V	
Input low voltage	VIL	-0.3	—	0.8	V		
Output low voltage	VOL	-0.3	—	0.4	V		IOL = 4 mA
Pin capacitance	CL	—	—	10	pF	—	All pins
Input leakage current	ILI	—	—	1	µA	VDDQ33 = 3.1 to 3.5 V	All input pins
Output leakage current	ILO	—	—	1	µA	Without pull-up or pull-down resistor	Hi-Z output

RZ/G2H
RZ/G2M V1.3 RZ/G2M V3.0
RZ/G2N RZ/G2E

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Input high voltage	VIH	2.0	—	VDDQ33 + 0.3	V	VDDQ33, VDDQ_SD0 = 3.0 to 3.6	
Input low voltage	VIL	-0.3	—	0.8	V		
Output low voltage	VOL	-0.3	—	0.4	V		IOL = 4 mA
Pin capacitance	CL	—	—	10	pF	—	All pins
Input leakage current	ILI	—	—	1	µA	VDDQ33, VDDQ_SD0 = 3.0 to 3.6	All input pins
Output leakage current	ILO	—	—	1	µA	Without pull-up or pull-down resistor	Hi-Z output

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Table 3.4.15 DC Characteristics (1.8-V I/O [CSI2])

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement condition	Remarks
Input signal voltage range	V_{PIN}	-50	—	1350	mV	—	—
Input leakage current	I_{LEAK}	-10	—	10	uA	$V_{GNDSH(min)} \leq V_{PIN} \leq V_{GNDSH(max)} + V_{PIN(absmax)}$ Lane module in LP receive mode	—
Ground shift	V_{GNDSH}	-50	—	50	mV	—	—
transient pin voltage level	$V_{PIN(absmax)}$	-0.15	—	1.45	V	—	—
Differential input high threshold	V_{IDTH}	—	—	70	mV	—	HS Receiver
Differential input low threshold	V_{IDTL}	-70	—	—	mV	—	HS Receiver
Single-ended input high voltage	V_{IHHS}	—	—	460	mV	—	HS Receiver
Single-ended input low voltage	V_{ILHS}	-40	—	—	mV	—	HS Receiver
Input common mode voltage	$V_{CMRX(DC)}$	70	—	330	mV	—	HS Receiver
Differential input impedance	Z_{ID}	80	—	125	Ω	—	HS Receiver
Input low voltage	V_{IL}	—	—	550	mV	—	LP Receiver
Input high voltage	V_{IH}	880	—	—	mV	—	LP Receiver
Input hysteresis	V_{HYST}	25	—	—	mV	—	LP Receiver

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Table 3.4.16 DC Characteristics (1.8-V I/O [LVDS])

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement condition	Remarks
Output differential voltage	|VOD|	250	—	450	mV	Termination load = 100 Ω	TIA/EIA-644
Output offset voltage	VOS	1.125	—	1.375	V	Termination load = 100 Ω	TIA/EIA-644
Change in |VOD| between 0 and 1	ΔVOD	—	—	50	mV	Termination load = 100 Ω	TIA/EIA-644
Change in VOS between 0 and 1	ΔVOS	—	—	50	mV	Termination load = 100 Ω	TIA/EIA-644

Table 3.4.17 DC Characteristics (Operating Conditions for HDMI Interface)

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks, Figures
Termination supply Voltage	AVcc	3.15	3.3	3.45	V	—	Minimum supply rise time for RX termination voltage > 2.5 µs Figure 3.4.1
Termination resistance	R_T	45	50	55	Ω	—	Figure 3.4.1

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Table 3.4.18 DC Characteristics (Source DC characteristics at TP1 for HDMI Interface)

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Figures
Single-ended standby output voltage	V_{OFF}	AVcc-10	—	AVcc+10	mV	—	Figure 3.4.2
Single-ended output swing voltage	V_{SWING}	400	—	600	mV	—	Figure 3.4.2
Single-ended high level output voltage	V_H	AVcc-10	—	AVcc+10	mV	TMDSCLK ≤ 165 MHz	Figure 3.4.2
		AVcc-200	—	AVcc+10	mV	TMDSCLK > 165 MHz	
Single-ended low level output voltage	V_L	AVcc-600	—	AVcc-400	mV	TMDSCLK ≤ 165 MHz	Figure 3.4.2
		AVcc-700	—	AVcc-400	mV	TMDSCLK > 165 MHz	

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Table 3.4.19 DC Characteristics (Hot Plug Detect Signal for HDMI)

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
High voltage level	HPD_{VH}	2.0	—	5.3	V	—	Minimum rise time for HPD voltage > 4 µs
Low voltage level	HPD_{VL}	0	—	0.8	V	—	

Please confirm HPD section of HDMI specification. (Note that many Sink device simply connect the HPD signal to the +5V Power signal through a 1000 Ω resistor.)

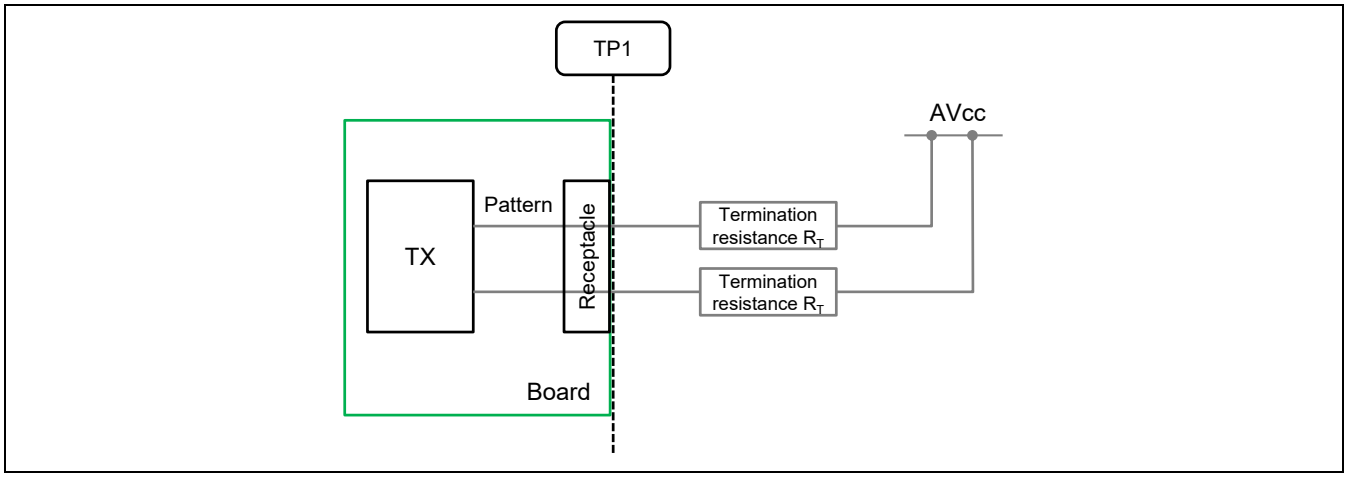


Figure 3.4.1 Balanced Source Test Load for HDMI

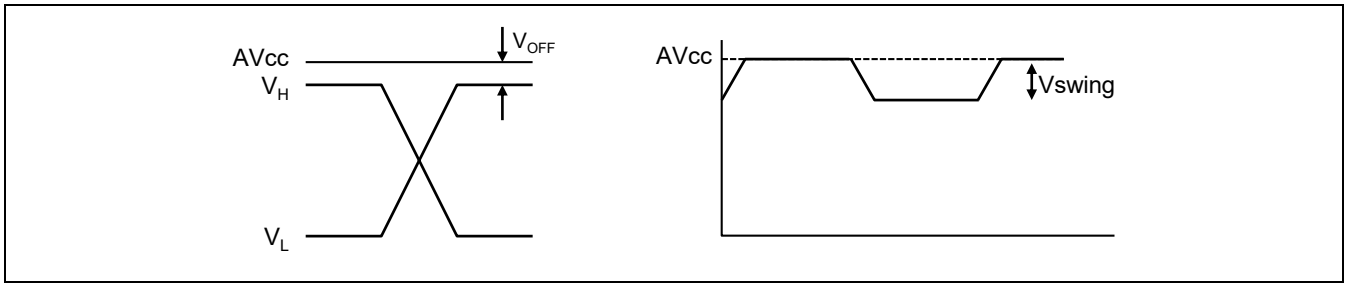


Figure 3.4.2 Single-ended Differential Signal for HDMI

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Table 3.4.20 DC Characteristics (1.35-V I/O [DDR3L])

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N **RZ/G2E**

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Input high voltage (MDQ pin)	VIH	VREF + 0.09	—	—	V	VDDQ_DDR = VDDQ_CK = 1.283 to 1.450 V	MDQ, and MDQS pins
Input low voltage (MDQ pin)	VIL	—	—	VREF - 0.09	V		
Input high voltage	VIH	0.7 × VDDQ_ DDR	—	—	V	VDDQ_DDR = VDDQ_CK = 1.283 to 1.450 V	MBKPRST# pin
Input low voltage	VIL	—	—	0.3 × VDDQ_DDR	V		
Differential input reference voltage	VREF	0.49 × VDDQ_ DDR	0.50 × VDDQ_ DDR	0.51 × VDDQ_DDR	V	VDDQ_DDR = VDDQ_CK = 1.283 to 1.450 V	*1
DC differential input high voltage	VIHD	0.18	—	—	V	MDQS = H, VIN = VDDQ_DDR/2, VDD = 1.0 Vtyp, VDDQ_DDR = VDDQ_CK = 1.283 to 1.450 V	MDQS pins
DC differential input low voltage	VILD	—	—	-0.18	V	MDQS = L, VIN = VDDQ_DDR/2, VDD = 1.0 Vtyp, VDDQ_DDR = VDDQ_CK = 1.283 to 1.450 V	
AC differential input high voltage	VIHD (AC)	0.27	—	—	V	VDD = 1.0 Vtyp, VDDQ_DDR = VDDQ_CK = 1.283 to 1.450 V	MDQS pins
AC differential input low voltage	VILD (AC)	—	—	-0.27	V	VDD = 1.0 Vtyp, VDDQ_DDR = VDDQ_CK = 1.283 to 1.450 V	MDQS pins
Input high voltage	VIH (AC)	VREF + 0.135	—	—	V	—	—
Input low voltage	VIL (AC)	—	—	VREF – 0.135	V	—	—
AC differential input cross point voltage	VIX (AC)	0.5 × VDDQ_ DDR – 0.15	—	0.5 × VDDQ_ DDR, + 0.15	V	VDDQ_DDR = VDDQ_CK = 1.283 to 1.450 V	MDQS pins *2
AC differential output cross point voltage	VOX (AC)	VREF – 0.125	—	VREF + 0.125	V	VDDQ_DDR = VDDQ_CK = 1.450 V	MCK, and MDQS pins (PU, PD not used)

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Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
High Hi-Z leak current	IOZH	—	—	4	µA	VDDQ_DDR = VDDQ_CK = 1.450 V	Other than MZQ and MVREF pins
Low Hi-Z leak current	IOZL	-4	—	—	µA		
High Hi-Z leak current	IOZH	—	—	5	µA		MZQ pin
Low Hi-Z leak current	IOZL	-5	—	—	µA		
High Hi-Z leak current	IOZH	—	—	25	µA	—	MVREF pin
Low Hi-Z leak current	IOZL	-25	—	—	µA	—	
Pin capacitance	CL	—	—	15	pF	—	All pins*3
PLL power supply	*4	1.7	1.8	1.9	V	—	—

Notes: 1. Peak to peak ac noise on VREF may not exceed ± 2 % of VREF.
2. The VIX (AC) indicates the voltage at which differential input signals cross each other. The typical value of VIX (AC) is expected to be 0.5 × VDDQ_DDR.
3. Except power supply pins.
4. VDDQ_MAPLL, VDDQ_MDPLL0, VDDQ_MDPLL1 pins.

Table 3.4.21 DDR3L Interface ODT Characteristics

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N **RZ/G2E**

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Termination voltage	Vtt	VREF – 0.04	VREF	VREF + 0.04	V	VDD = 1.0 Vtyp, VDDQ_DDR = VDDQ_CK = 1.283 to 1.450 V	—
ODT resistance (60 Ω)	RTT60	54.0	—	96.0	Ω		—
ODT resistance (40 Ω)	RTT40	36.0	—	64.0	Ω		—
VM deviation	ΔVM	-7	—	+7	%		*

Note: * VM is a voltage value measured with the ODT turned on without any load applied to this LSI chip. ΔVM is obtained by the following formula:
ΔVM = (2 × VM / VDDQ_DDR -1) × 100

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Table 3.4.22 DC Characteristics (1.1-V I/O [LPDDR4])

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Input high voltage (MDQ pin)	VIH	VREF + 0.09	—	—	V	VDDQVA_DDRn = 1.06 to 1.17 V (n = 0 to 1) VREF= VDDQVA_DDRn*(1/6)	MDQ, and MDQS pins
Input low voltage (MDQ pin)	VIL	—	—	VREF – 0.09	V		
Input high voltage	VIH	0.8 × VDDQVA_DDRn (n = 0 to 1)	—	—	V	VDDQVA_DDRn = 1.06 to 1.17 V (n = 0 to 1)	MBKUP pin
Input low voltage	VIL	—	—	0.2 × VDDQVA_DDRn (n = 0 to 1)	V		
DC differential input high voltage	VIHD	0.09	—	—	V	MDQS = H, VDDQVA_DDRn = 1.06 to 1.17 V (n = 0 to 1)	MDQS pins
DC differential input low voltage	VILD	—	—	-0.09	V	MDQS = L, VDDQVA_DDRn = 1.06 to 1.17 V (n = 0 to 1)	
Output high voltage	VOH	0.99	—	—	V	VDDQVA_DDRn = 1.06 to 1.17 V (n = 0 to 1)	MBKUP pins IOH = 0mA
Output low voltage	VOL	—	—	0.16	V	VDDQVA_DDRn = 1.06 to 1.17 V (n = 0 to 1)	MBKUP pins IOL = 0mA
High Hi-Z leak current	IOZH	—	—	10	µA	VDDQVA_DDRn = 1.06 to 1.17 V (n = 0 to 1)	Other than MZQ
Low Hi-Z leak current	IOZL	-10	—	—	µA		
High Hi-Z leak current	IOZH	—	—	10	µA		MZQ pin
Low Hi-Z leak current	IOZL	-10	—	—	µA		
Pin capacitance	CL	—	—	15	pF	—	All pins*

Note: * Except power supply pins.

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Table 3.4.23 LPDDR4 Interface ODT Characteristics

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
ODT resistance (40 Ω)	RTT40	36	—	44	Ω	VDDQVA_DDRn = 1.06 to 1.17 V (n = 0 to 1)	—

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3.4.1 Overload Condition (Injection Current)

RZ/G2H RZ/G2M V1.3 RZ/G2N RZ/G2M V3.0

The overload condition describes the behavior in case of current injection to the port pins.
Condition: Tj = -40c to Tj Max

Table 3.4.24 Overload Current [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, and RZ/G2N)

Parameter		Symbol	Condition	Ratings*1	Unit
Overload Current *2 Vin > VCC Vin < VSS	Pins supplied by VDDQ33	IINJPM	1 pin	±2	mA
		IINJNM	Sum of all absolute IINJPM + IINJNM of pins supplied as group *3	|50|	mA
	Pins supplied by VDDQ18	IINJPM	1 pin	±2	mA
		IINJNM	Sum of all absolute IINJPM + IINJNM of pins supplied as group *3	|50|	mA
	Pins supplied by VDDQVA_SDn (n = 0,1,2)	IINJPM	1 pin	±2	mA
		IINJNM	Sum of all absolute IINJPM + IINJNM of pins supplied as group *3	|12|	mA
	Pins supplied by VDDQVA_SDn (n = 3)	IINJPM	1 pin	±2	mA
		IINJNM	Sum of all absolute IINJPM + IINJNM of pins supplied as group *3	|22|	mA
	Pins supplied by VDDQ25_ETH	IINJPM	1 pin	±2	mA
		IINJNM	Sum of all absolute IINJPM + IINJNM of pins supplied as group *3	|36|	mA

Notes: 1. The Total current may be limited further by the total power dissipation.
2. Be sure not to exceed the absolute maximum ratings (Max value) of each supply voltage.
3. The total overload current must be within the output current.

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Table 3.4.25 Overload Current [RZ/G2E]

Parameter		Symbol	Condition	Ratings*1	Unit
Overload Current *2 Vin > VCC Vin < VSS	Pins supplied by VDDQ33	IINJPM	1 pin	±2	mA
		IINJNM	Sum of all absolute IINJPM + IINJNM of pins supplied as group *3	|50|	mA
	Pins supplied by VDDQ18	IINJPM	1 pin	±2	mA
		IINJNM	Sum of all absolute IINJPM + IINJNM of pins supplied as group *3	|25.2|	mA
	Pins supplied by VDDQ25_AVB0	IINJPM	1 pin	±2	mA
		IINJNM	Sum of all absolute IINJPM + IINJNM of pins supplied as group *3	|24.4|	mA
	Pins supplied by VDDQ_SDn (n = 0,1)	IINJPM	1 pin	±2	mA
		IINJNM	Sum of all absolute IINJPM + IINJNM of pins supplied as group *3	|5.4|	mA
	Pins supplied by VDDQ_SD3	IINJPM	1 pin	±2	mA
		IINJNM	Sum of all absolute IINJPM + IINJNM of pins supplied as group *3	|22|	mA
	Pins supplied by VDDQ_QSPI	IINJPM	1 pin	±2	mA
		IINJNM	Sum of all absolute IINJPM + IINJNM of pins supplied as group *3	|21.6|	mA

Notes: 1. The Total current may be limited further by the total power dissipation.
2. Be sure not to exceed the absolute maximum ratings (Max value) of each supply voltage.
3. The total overload current must be within the output current.

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3.5 Clock and Reset Timings

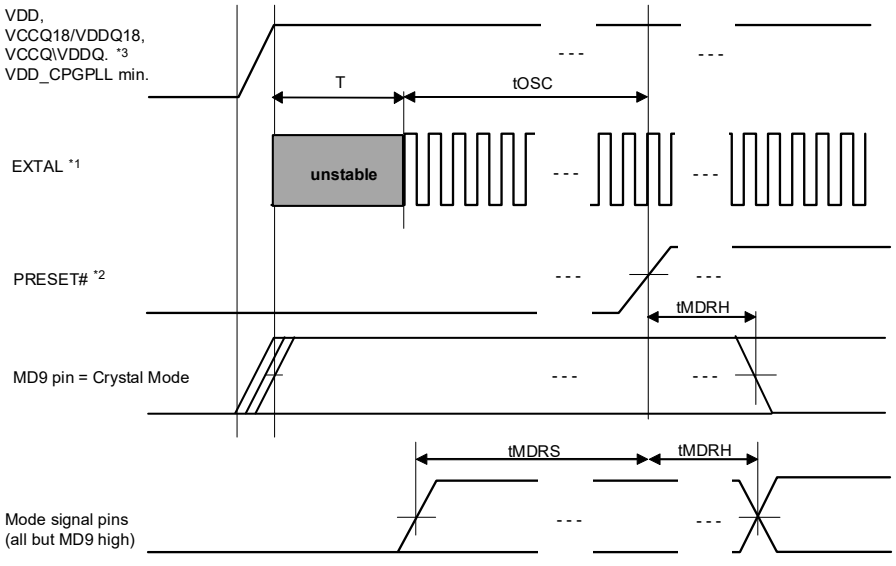
RZ/G2H | RZ/G2M V1.3 | RZ/G2M V3.0 | RZ/G2N | RZ/G2E

Table 3.5.1 Clock and Reset Timing

Conditions: VDDQ33 = 3.3 V ± 0.2 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N] / ± 0.3 V [RZ/G2E],
VDDQ18 = 1.8 V ± 0.1 V, GND = VSS = 0 V,
Tc = -40 to +115 °C [RZ/G2H, RZ/G2M V1.3]
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E]

Pin	Item	Symbol	Min.	Max.	Unit	Figures
PRESET#, EXTAL	Power-on oscillation settling time (Period from power and EXTAL stable clock input to PRESET# rise.)	tOSC	5	—	ms	Figure 3.5.1
		T	0*2	*3	ms	
Mode signal*1	MD reset setup time	tMDRS	5	—	ms	
Mode signal*1	MD reset hold time	tMDRH	3	—	ns	

Notes: 1. MDn (n = 0, 1, 2 ...) and MDT [1:0]. For details of mode signals, refer to section 3, 4, 5 and.6, Mode Pin Settings.
2: Using 0 stabilization time requires an external clock. For mode setting refer to Table 11.3 MD9 Settings in RZ/G 2nd Generation, User's Manual: Hardware.
3: The oscillation stabilization time differs according to matching with the external resonator circuit. It is recommended to determine the oscillation stabilization time by a crystal resonator matching test. For details of the stabilization time "T", please contact the crystal manufacture.



Notes 1: For EXTAL's waveform
Since the unstable oscillation exists when using a crystal resonator, wait for T until clock is stabilized.
T depends on the circuit on the board.
2: For PRESET# input
Note electromagnetic noise because that may cause malfunctions of the LSI.
Note an intermediate voltage level input because that may influence the long-term reliability of the LSI.
3: Voltage rails VDDQ_DU/VDDQ_VIN01 relates to the Mode Pin supply rails
- VDDQ33 for RZ/G2H/G2M/G2N/G2E.

Figure 3.5.1 Reset when Turning on Power Supply (PRESET# vs EXTAL and Mode signal)

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3.6 EXTAL Clock Input/output Timing

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

3.6.1 EXTAL Clock Input Timing

Table 3.6.1 EXTAL Clock Input Timing

Conditions: VDDQ18 = 1.8 V ± 0.1 V, GND = VSS = 0 V, Tc = -40 to +115 °C[RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C[RZ/G2M V3.0, RZ/G2N], Tj = -40 to +115 °C[RZ/G2M V3.0, RZ/G2N]

Item		Symbol	Min.	Typ.	Max.	Unit	Figures
EXTAL clock input frequency	MD[14:13] = LL	fEX	14.40	16.66	16.70	MHz	—
	MD[14:13] = LH		17.30	20.00	20.04	MHz	
	MD[14:13] = HL		21.62	25.00	25.06	MHz	
	MD[14:13] = HH		28.80	33.33	33.40	MHz	
EXTAL clock input cycle time	MD[14:13] = LL	tEXcyc	59.88	60.02	69.44	ns	Figure 3.6.1
	MD[14:13] = LH		49.90	50.00	57.80	ns	
	MD[14:13] = HL		36.90	40.00	46.25	ns	
	MD[14:13] = HH		29.94	30.00	34.72	ns	
EXTAL clock input duty cycle time		tEXduty	0.4	0.5	0.6	tEXcyc	
EXTAL clock input low-level pulse width		tEXL	5	—	—	ns	
EXTAL clock input high-level pulse width		tEXH	5	—	—	ns	
EXTAL clock input rise time		tEXr	—	—	4	ns	
EXTAL clock input fall time		tEXf	—	—	4	ns	

Note: Set the MD9 pin to L (low) during power-on reset when using the EXTAL pin as external clock input and the XTAL pin must be open.

Not to exceed the specification of LPDDR4 operating frequency, input the lower frequency of EXATL or lower the multiplication rate of PLL.

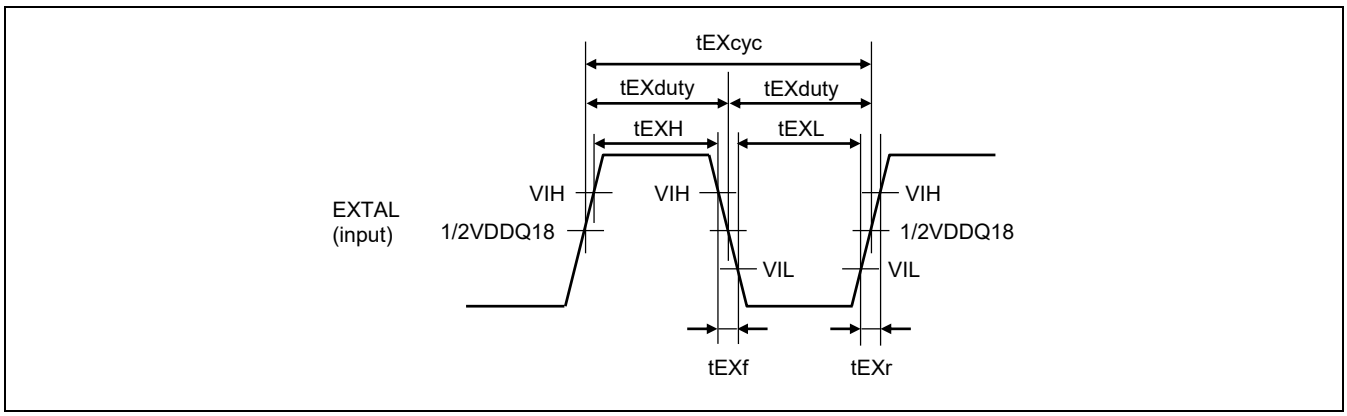


Figure 3.6.1 EXTAL Clock Input Timing

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3.6.2 CLKOUT Clock Output Timing

Table 3.6.2 CLKOUT Clock Output Timing

Conditions: VDDQ18 = 1.8 V ± 0.1 V, GND = VSS = 0 V, Tc = -40 to +115 °C[RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C[RZ/G2M V3.0, RZ/G2N], Tj = -40 to +115 °C[RZ/G2M V3.0, RZ/G2N]

Item		Symbol	Min.	Typ.	Max.	Unit	Figures
CLKOUT clock output frequency	MD18 = L	fCKO	57.52	66.66	66.80	MHz	—
	MD18 = H		38.35	44.44	44.53	MHz	
CLKOUT clock output cycle time	MD18 = L	tCKOcyc	14.97	15.00	17.38	ns	Figure 3.6.2
	MD18 = H		22.45	22.50	26.07	ns	
CLKOUT clock output duty cycle time		tCKOduty	0.4	0.5	0.6	tCKOcyc	
CLKOUT clock output low pulse width		tCKOL	4	—	—	ns	
CLKOUT clock output high pulse width		tCKOH	4	—	—	ns	
CLKOUT clock output rise time		tCKOr	—	—	4	ns	
CLKOUT clock output fall time		tCKOf	—	—	4	ns	

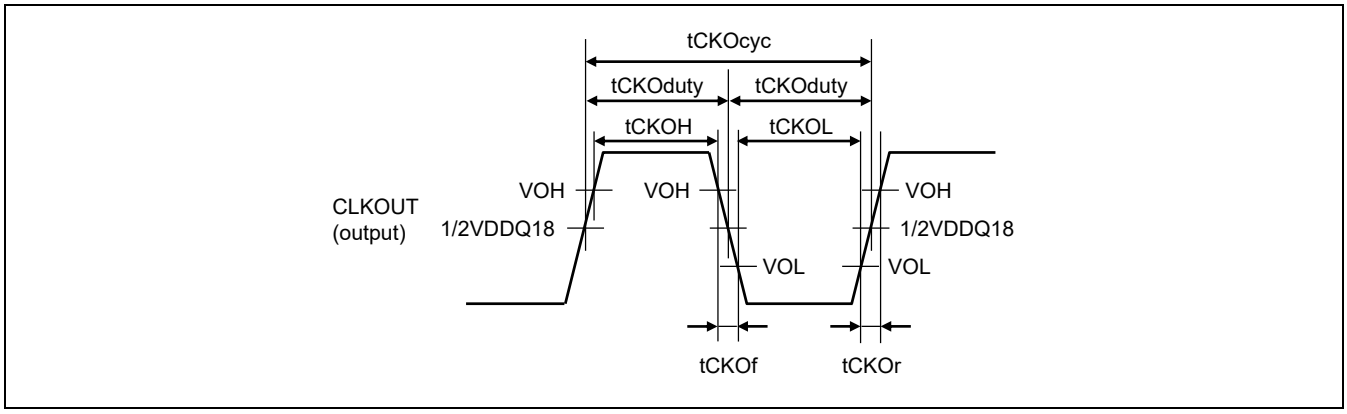


Figure 3.6.2 CLKOUT Clock Output Timing

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3.6.3 EXTAL Crystal resonator Input characteristics [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]

Table 3.6.3 EXTAL Crystal resonator Input characteristic [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]

Conditions: VDDQ18 = 1.8 V ± 0.1 V, GND = VSS = 0 V,
Tc = -40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N]
MD9 pin to High

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Input Frequency Range	MD[14:13] = LL	fEXC	—	16.66	—	MHz	Frequency deviation: ±200 ppm or less
	MD[14:13] = LH		—	20.00	—		
	MD[14:13] = HL		—	25.00	—		
	MD]14:13] = HH		—	33.33	—		
Crystal oscillator stabilization time		T	—	—	5 *	ms	Refer Symbol T in Figure 3.5.1.

Note: * The oscillation stabilization time differs according to the matching with the external resonator circuit. For proper operation of some external modules/devices/interfaces, a tighter frequency deviation might be needed. Input a fitting frequency deviation according to all external modules/devices/interfaces which are used.

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3.7 EXTAL Clock Input/output Timing

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

3.7.1 EXTAL Clock Input Timing

Table 3.7.1 EXTAL Clock Input Timing

Conditions: VDDQ18 = 1.8 V ± 0.1 V, GND = VSS = 0 V, Ta = -40 to +85 °C, Tj = -40 to +115 °C

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks	Figures
EXTAL clock input frequency	fEX	—	48	—	MHz	Frequency deviation: ±100 ppm or less	—
EXTAL clock input cycle time	tEXcyc	—	20.83	—	ns		Figure 3.7.1
EXTAL clock input duty cycle time	tEXduty	0.4	0.5	0.6	tEXcyc	—	
EXTAL clock input low-level pulse width	tEXL	5	—	—	ns	—	
EXTAL clock input high-level pulse width	tEXH	5	—	—	ns	—	
EXTAL clock input rise time	tEXr	—	—	4	ns	—	
EXTAL clock input fall time	tEXf	—	—	4	ns	—	

Note: Set the MD9 pin to L (low) during power-on reset when using the EXTAL pin as external clock input and the XTAL pin must be open.

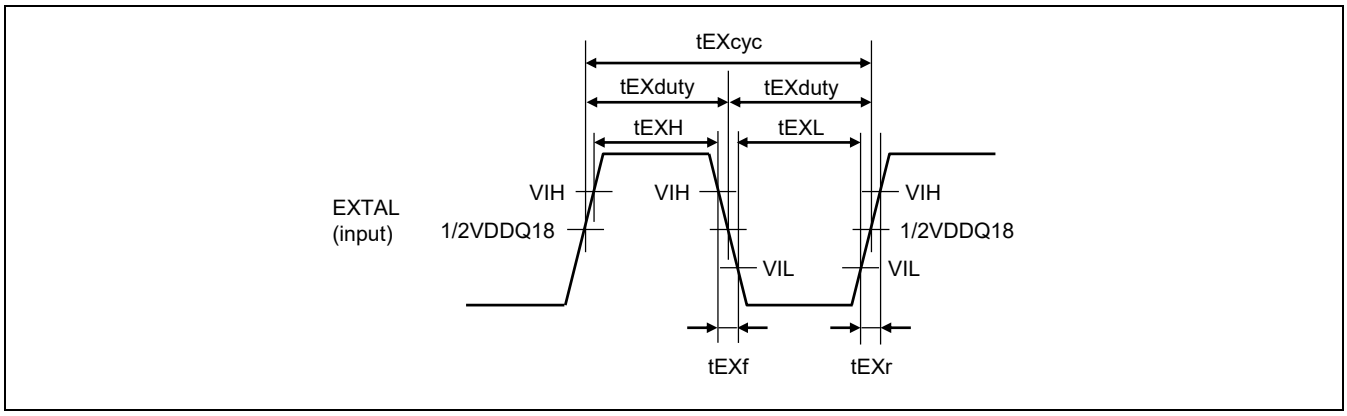


Figure 3.7.1 EXTAL Clock Input Timing

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3.7.2 EXTAL Crystal resonator Input characteristics [RZ/G2E]

Table 3.7.2 EXTAL Crystal resonator Input characteristic [RZ/G2E]

Conditions: VDDQ18 = 1.8 V ± 0.1 V, GND = VSS = 0 V,
Ta = -40 to +85 °C, Tj = -40 to +115 °C,
MD9 pin to High

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Input Frequency Range (with USB)	fEXC	—	48.00	—	MHz	Frequency deviation: ±100 ppm or less
Input Frequency Range (without USB)		—	48.00	—		Frequency deviation: ±200 ppm or less
Crystal oscillator stabilization time	T	—	—	5 *	ms	Refer Symbol T in Figure 3.5.1.

Note: * The oscillation stabilization time differs according to the matching with the external resonator circuit. For proper operation of some external modules/devices/interfaces, a tighter frequency deviation might be needed. Input a fitting frequency deviation according to all external modules/devices/interfaces which are used.

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3.8 PLL Characteristics

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N **RZ/G2E**

Table 3.8.1 PLL1 SSCG Characteristics

Conditions: VDDQ18 = 1.8 V ± 0.1 V, GND = VSS = 0 V, Ta = -40 to +85 °C, Tj = -40 to +115 °C

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
PLL1 modulation frequency	—	+4.02	+4.03	+4.04	kHz	Figure 3.8.1
PLL1 frequency dithering range (down-spread)	—	-3.0	—	+0.0	%	

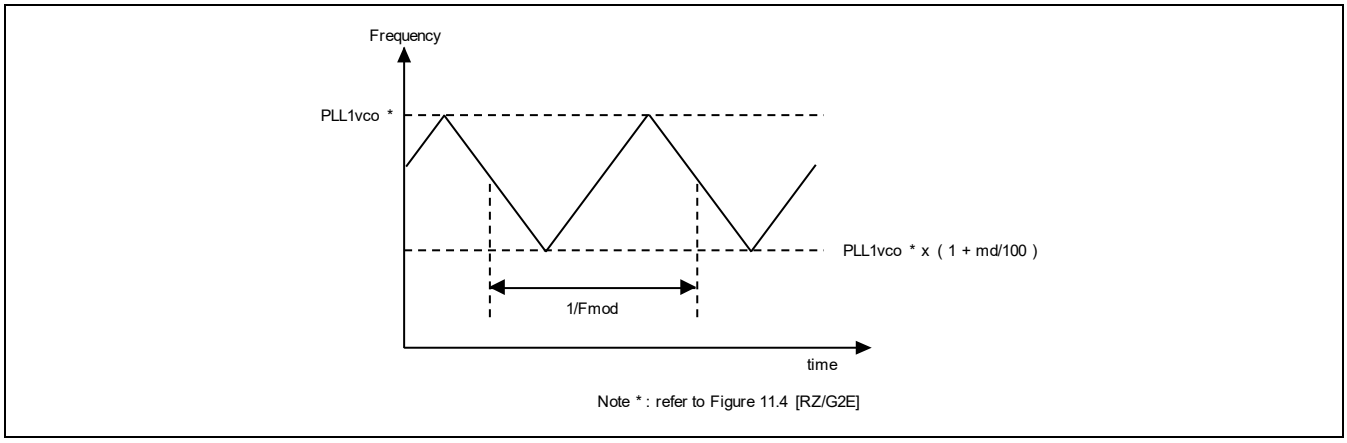


Figure 3.8.1 PLL1 SSCG Time trend of output clock

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3.9 EXTALR Input Timing

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Table 3.9.1 EXTALR Characteristics for RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0 and RZ/G2N

Conditions: VDDQ18 = 1.8 V ± 0.1 V, GND = VSS = 0 V,
Tc = -40 to +115 °C [RZ/G2H, RZ/G2M V1.3]
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N], Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N]

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Input Frequency Range	—	32.5	32.768	33	kHz	—
Input Frequency Tolerance	—	-200	—	+200	ppm	—

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3.10 LBSC

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

3.10.1 Normal Read/Write, Burst ROM Read

Table 3.10.1 Normal Read/Write Access Timing [RZ/G2H/RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N, RZ/G2E]

Conditions: VDDQ33 = 3.3 ± 0.2 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N] / ± 0.3 V [RZ/G2E],
GND = VSSQ = 0 V, Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
CL = 40 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
Address output delay time	tDA	0.0	—	6.0	ns	Figure 3.10.1
CS# output delay time	tDCS	0.0	—	6.0	ns	
BS# output delay time	tDBS	0.0	—	6.0	ns	
RD# output delay time	tDRD	0.0	—	6.0	ns	
RD/WR# output delay time	tDRW	0.0	—	6.0	ns	
Read data setup time	tSD	11.0	—	—	ns	
Read data hold time	tHD	0.0	—	—	ns	
WE# output delay time	tDWE	0.0	—	6.0	ns	
Write data output delay time	tDD	0.0	—	6.0	ns	
External wait signal setup time	tSEW	11.0	—	—	ns	
External wait signal hold time	tHEW	0.0	—	—	ns	

Table 3.3.10.2Burst ROM Read Access Timing

Conditions: VDDQ33 = 3.3 ± 0.2 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N] / ± 0.3 V [RZ/G2E],
GND = VSSQ = 0 V, Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +105 °C/ -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E] ,
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E], CL = 40 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
Address output delay time	tDABST	0.0	—	6.0	ns	Figure 3.10.2
CS# output delay time	tDCSBST	0.0	—	6.0	ns	
RD# output delay time	tDRDBST	0.0	—	6.0	ns	
Read data setup time	tSDBST	11.0	—	—	ns	
Read data hold time	tHDBST	0.0	—	—	ns	

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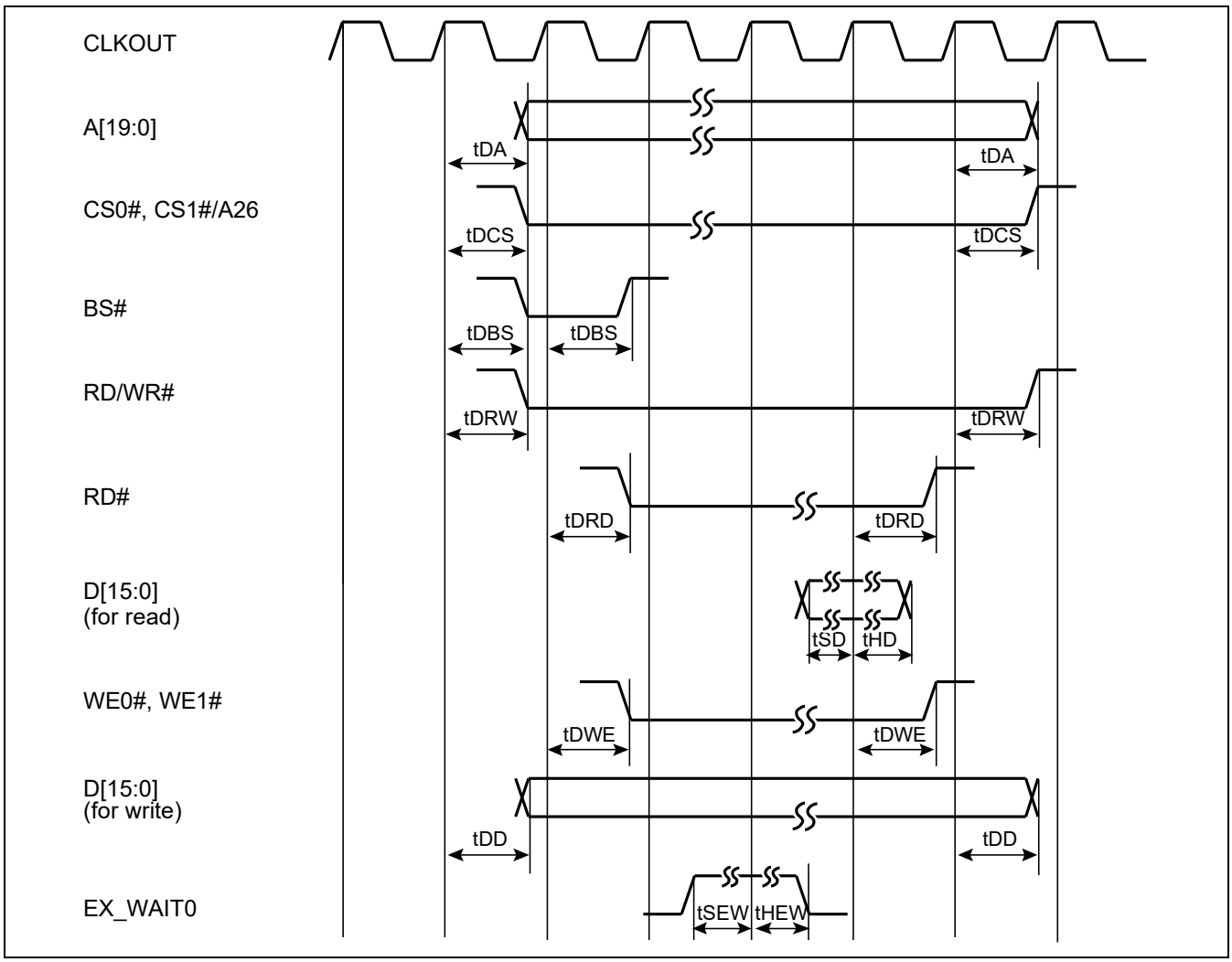


Figure 3.10.1 Normal Read/Write Access Timing

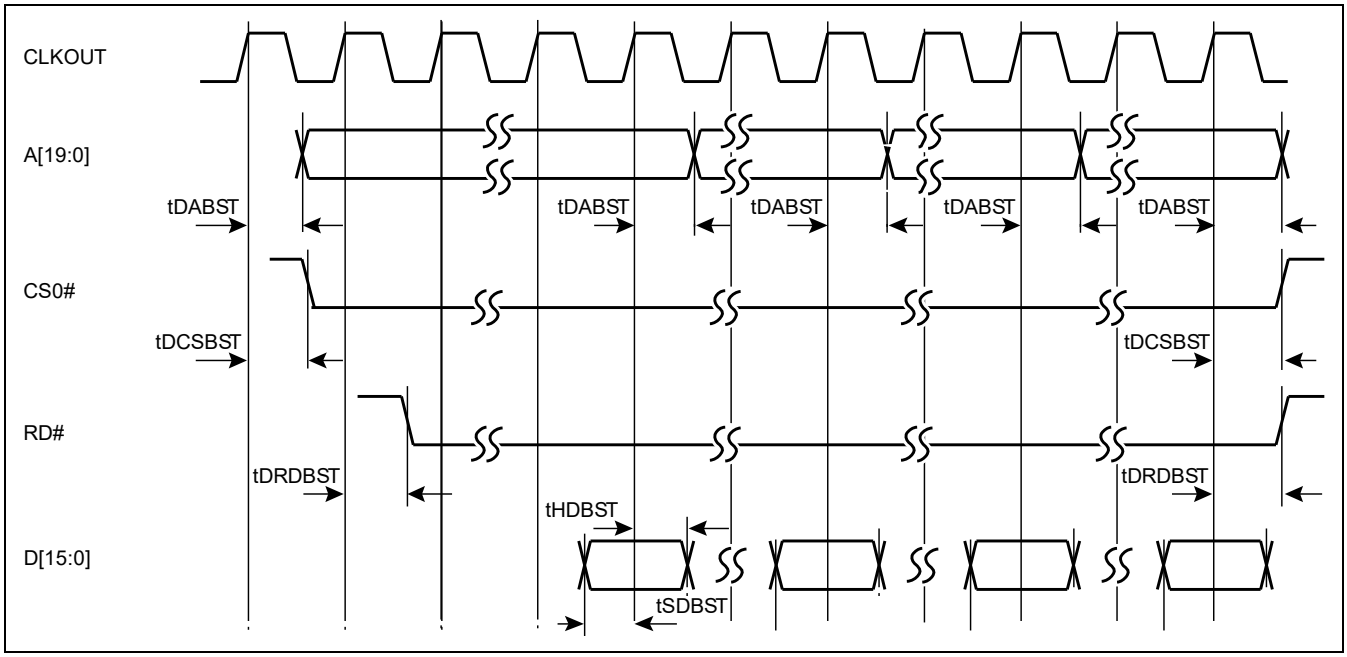


Figure 3.10.2 Burst ROM Read Access Timing

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3.11 CSI2

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Table 3.11.1 AC Characteristics (1.8-V I/O [CSI2])

Conditions: VDDQ18_CSIn = 1.8 V ± 0.1 V, VDD09_CSIn = 0.82 V +0.06 V/ -0.07 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
VDDQ18_CSI0 = 1.8 V ± 0.1 V [RZ/G2E]
GND = VSS = 0 V,
Tc = -40 to + 115°C [RZ/G2H, RZ/G2M V1.3]
Ta = -40 to + 85°C [RZ/G2M V3.0, RZ/G2N, RZ/G2E]
Tj = -40 to 115°C [RZ/G2M V3.0, RZ/G2N, RZ/G2E]

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement condition	Remarks, Figures
Common mode interference beyond 450 MHz	$\Delta V_{CMRX(HF)}$	—	—	100	mVpp	—	HS Receiver
Common mode interference between 50 MHz and 450 MHz	$\Delta V_{CMRX(LF)}$	-50	—	50	mVpp	—	HS Receiver
Data to Clock Receiver Setup time	$t_{SETUP(RX)}$	0.20	—	—	UI	—	HS Receiver Figure 3.11.1
Data to Clock Receiver Hold time	$t_{HOLD(RX)}$	0.20	—	—	UI	—	

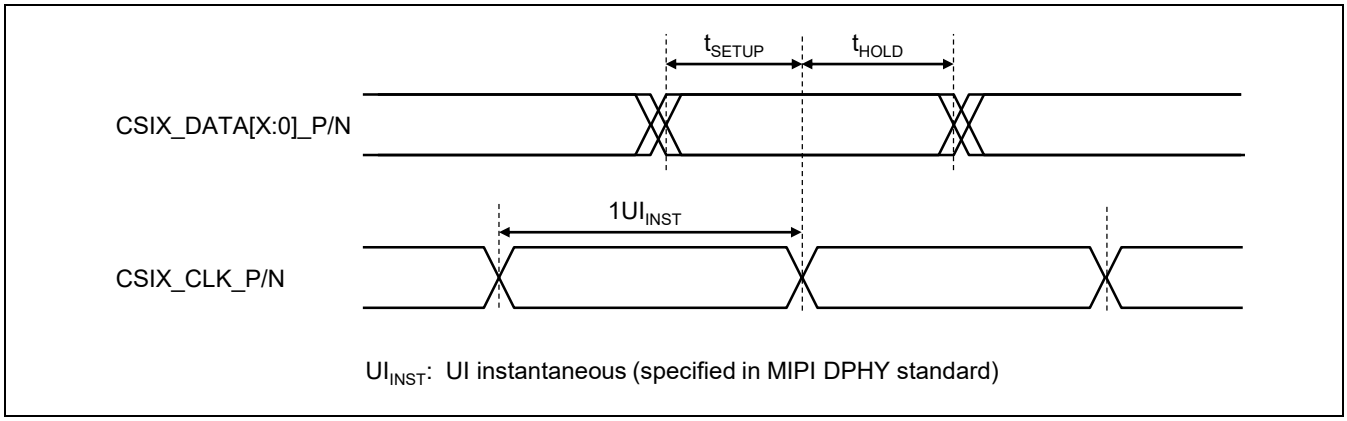


Figure 3.11.1 Data Receive timing

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3.12 Video Input Module (VIN)

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Table 3.12.1 VIN Signal Timing

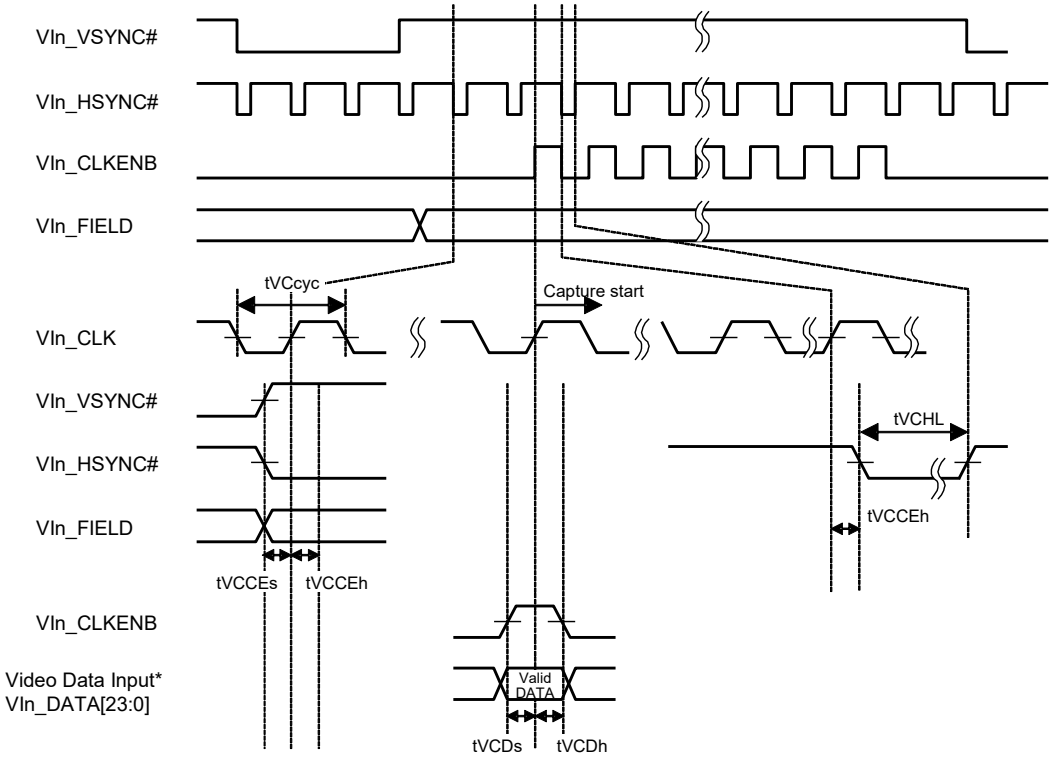
Conditions: VDDQ33 = 3.3 V ± 0.2 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
VDDQ33 = 3.3V ± 0.3 V [RZ/G2E], GND = VSS = 0 V, Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E]

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
VI_CLK cycle time	tVCcyc	10	37	—	ns	Figure 3.12.1
Data setup time	tVCDs	3.5	—	—	ns	
Data hold time	tVCDh	1.5	—	—	ns	
Sync signal setup time	tVCCEs	3.5	—	—	ns	
Sync signal hold time	tVCCEh	1.5	—	—	ns	
VI_HSYNC# hold cycle	tVCMcyc	8	—	—	tVCcyc	
VI_HSYNC# Low period	tVCHL	300	—	—	ns	
VI_VSYNC# Low period	tVCVL	3	—	—	Line	Figure 3.12.2
VI_CLK clock duty	tVCdtyH/L	45	50	55	%	Figure 3.12.3

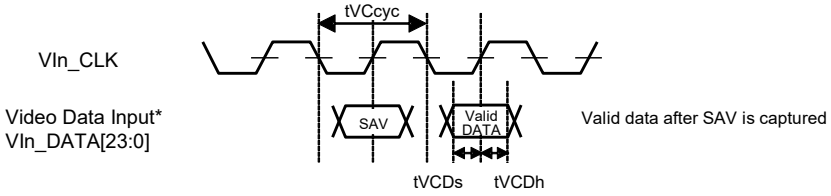
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Capture start timing and electrical characteristics for ITU-R BT.601/BT1358

Vin: VI[5:4] (RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2E)

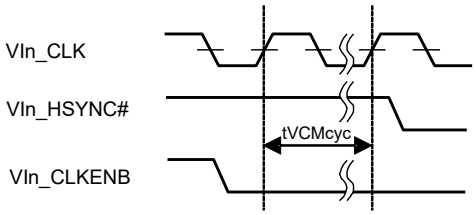


Capture start timing and electrical characteristics for ITU-R BT.656

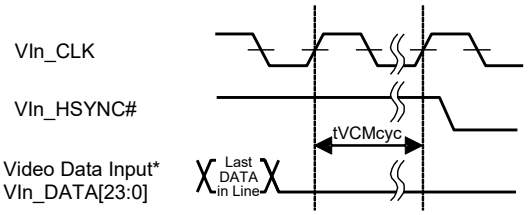


VI_HSYNC# hold cycle timing for ITU-R BT.601/BT1358

In case that Vin_CLKENB is input (VnDMR2.CHS=0):



In case that Vin_CLKENB is not input (VnDMR2.CHS=1):



Note: * For details of available video data input signal, refer to section 30, Video Input Module (VIN).

Figure 3.12.1 Capture start timing and electrical characteristics [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2E]

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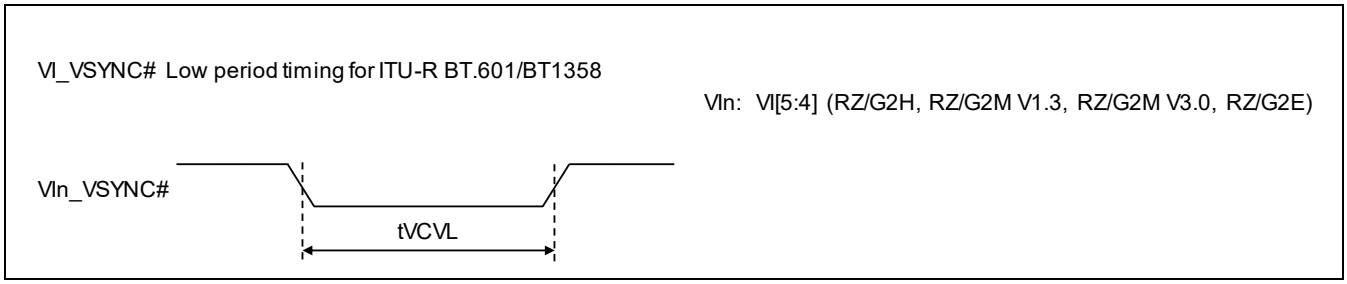


Figure 3.12.2 VI_VSYNC# [RZ/G2H, RZ/G2M V1.3,RZ/G2M V3.0, RZ/G2E]

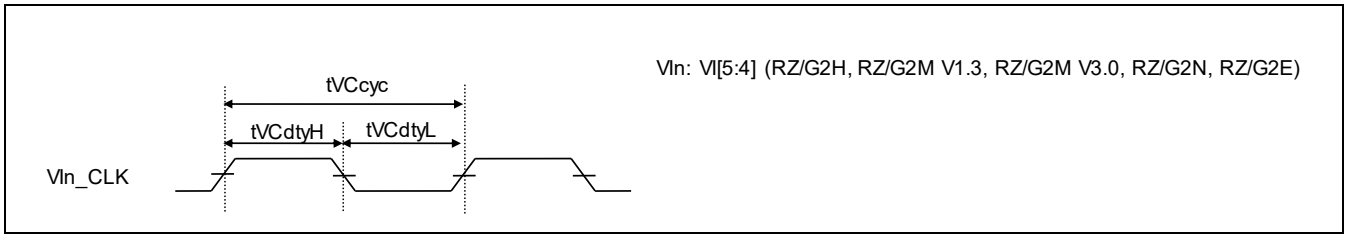


Figure 3.12.3 VI_CLK Clock Duty [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N, RZ/G2E]

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3.13 Display Unit (DU)

RZ/G2H | RZ/G2M V1.3 | RZ/G2M V3.0 | RZ/G2N | RZ/G2E

This electrical characteristic apply to only DU3 output [RZ/G2H, RZ/G2N].
This electrical characteristic apply to only DU2 output [RZ/G2M V1.3, RZ/G2M V3.0].

Table 3.13.1 DOTCLKIN Timing

Conditions: VDDQ18 = 1.8 V ± 0.1 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0 (DU_DOTCLKIN0), RZ/G2N] /
VDDQ33 = 3.3V ± 0.3V [RZ/G2E], GND = VSS = 0 V,
Tc= −40 to +115 °C [RZ/G2H, RZ/G2M V1.3], Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E]

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
DOTCLKIN cycle time	tDICYC	6.7	—	200	ns	Figure 3.13.1
DOTCLKIN High level time	tDCKIH	3	—	—	ns	
DOTCLKIN Low level time	tDCKIL	3	—	—	ns	

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Table 3.13.2 Display Signal Timing

Conditions: VDDQ33 = 3.3 V ± 0.2 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N] / ± 0.3 V[RZ/G2E],
GND = VSS = 0 V,
Tc = -40 to +115 °C, [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E], CL = 20 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
Display input control signal*1 setup time	tDS	5	—	—	ns	Figure 3.13.2 (relative to DOTCLKIN) [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
Display input control signal*1 hold time	tDH	3	—	—	ns	
DOTCLKOUT output cycle time	tDCYC	20	—	200	ns	Figure 3.13.3 [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
		13.3	—	200	ns	Figure 3.13.3 [RZ/G2E]
DOTCLKOUT output high level width	tDCKH	5	—	—	ns	Figure 3.13.3
Display output control signal*1 output delay time (Relative to DOTCLKOUT rising edge*3)	tDD	2	—	8.5	ns	Figure 3.13.3 (relative to DOTCLKOUT) [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
		2	—	11	ns	Figure 3.13.3 (relative to DOTCLKOUT) [RZ/G2E]
Display output control signal*1 output delay time (Relative to DOTCLKOUT falling edge*4)	tDDf	1.5	—	9.0	ns	Figure 3.13.4 [RZ/G2N]
Display digital data*1 output delay time (Relative to DOTCLKOUT rising edge*3)	tDD	2	—	8.5	ns	Figure 3.13.3 (relative to DOTCLKOUT) [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
		2	—	11	ns	Figure 3.13.3 (relative to DOTCLKOUT) [RZ/G2E]
Display digital data*1 output delay time (Relative to DOTCLKOUT falling edge*4)	tDDf	1.5	—	9.0	ns	Figure 3.13.4 [RZ/G2N]

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Item	Symbol	Min.	Typ.	Max.	Unit	Figures
EXHSYNC# input low level width	tEXHLW	4tDCYC	—	—	ns	Figure 3.13.5 [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
EXHSYNC# input high level width	tEXHHW	4tDCYC	—	—	Ns	
EXVSYNC# input low level width	tEXVLW	3HC	—	—	tDCYC	
ODDF# setup time 1*2	tOD1	(ys+yw) × HC	—	—	tDCYC	
ODDF# setup time 2*2	tOD2	1HC	—	—	tDCYC	

Notes: 1. For correspondence between these signals and pin names, refer to Table 3.13.4.
2. ys, yw and HC in Min value of ODDF# setup time 1 and ODDF# setup time 2 (tOD1 and tOD2).
ys: From rise of VSYNC to display start position in the vertical direction of the display screen (unit: raster line)
yw: Vertical display period of display screen (unit: raster line)
HC: Horizontal scan period (unit: dot clock)
3. Set bit 25 in ESCRn to B'0(Initial value). (n = 3[RZ/G2H, RZ/G2N], n = 2[RZ/G2M V1.3, RZ/G2M V3.0], n = 0 and 1[RZ/G2E])
4. Set bit 25 in ESCRn to B'1. (n = 3 [RZ/G2N])

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Table 3.13.3 DOTCLKOUT output cycle time [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

Conditions: VDDQ33 = 3.3 V ± 0.2 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N],
GND = VSS = 0 V, Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N

Load conditions: Characteristic impedance (50 - 60 Ω) + 10pF + Damping resistors (36 Ω)

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
DOTCLKOUT output cycle time*	tDCYC	10	—	200	ns	Figure 3.13.3

Note: * Other items are the same as in Table 3.13.2.

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Table 3.13.4 Correspondence between Signals in Notes and Pin Names

Signal in Note	Pin Name
Display input control signals	DU_EXVSYNC/DU_VSYNC [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
	DU_EXHSYNC/DU_HSYNC [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
	DU_EXODDF/DU_ODDF/DISP/CDE [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0 ,RZ/G2N]
Display output control signals	DU_EXVSYNC/DU_VSYNC [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
	DU_VSYNC [RZ/G2E]
	DU_EXHSYNC/DU_HSYNC [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
	DU_HSYNC [RZ/G2E]
	DU_EXODDF/DU_ODDF/DISP/CDE [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
	DU_DISP_CDE [RZ/G2E]
	DU_DISP
	DU_CDE
Display digital data	DU_DR7
	DU_DR6
	DU_DR5
	DU_DR4
	DU_DR3
	DU_DR2
	DU_DR1
	DU_DR0
	DU_DG7
	DU_DG6
	DU_DG5
	DU_DG4
	DU_DG3
	DU_DG2
	DU_DG1
	DU_DG0
	DU_DB7
	DU_DB6
	DU_DB5
	DU_DB4
	DU_DB3
	DU_DB2
	DU_DB1
	DU_DB0

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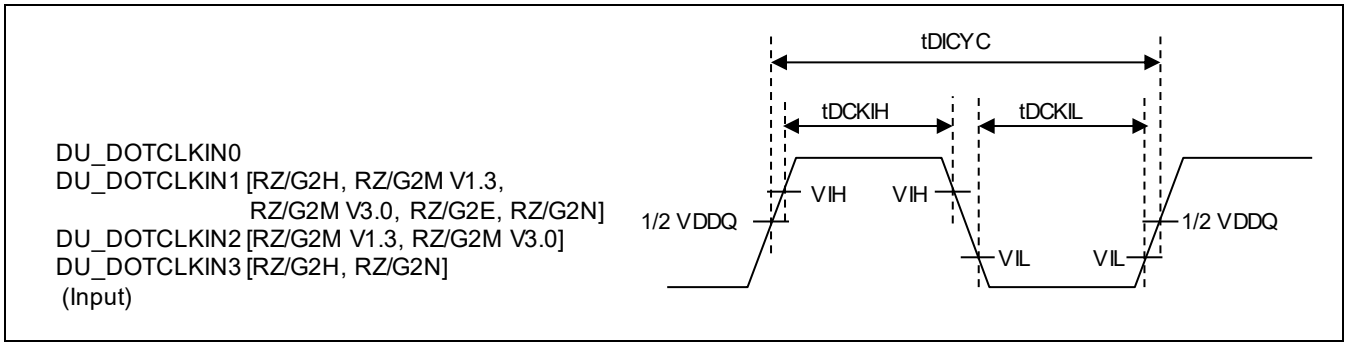
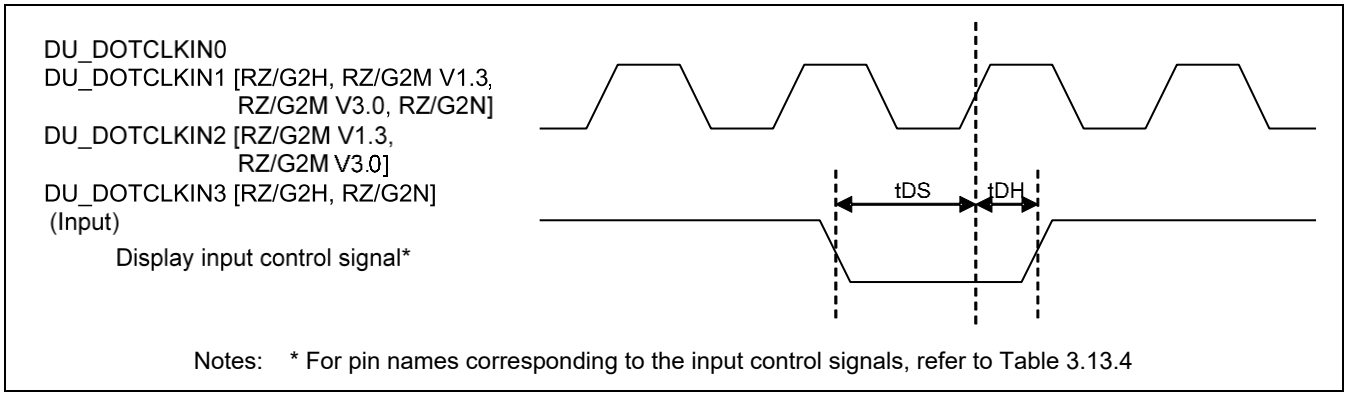
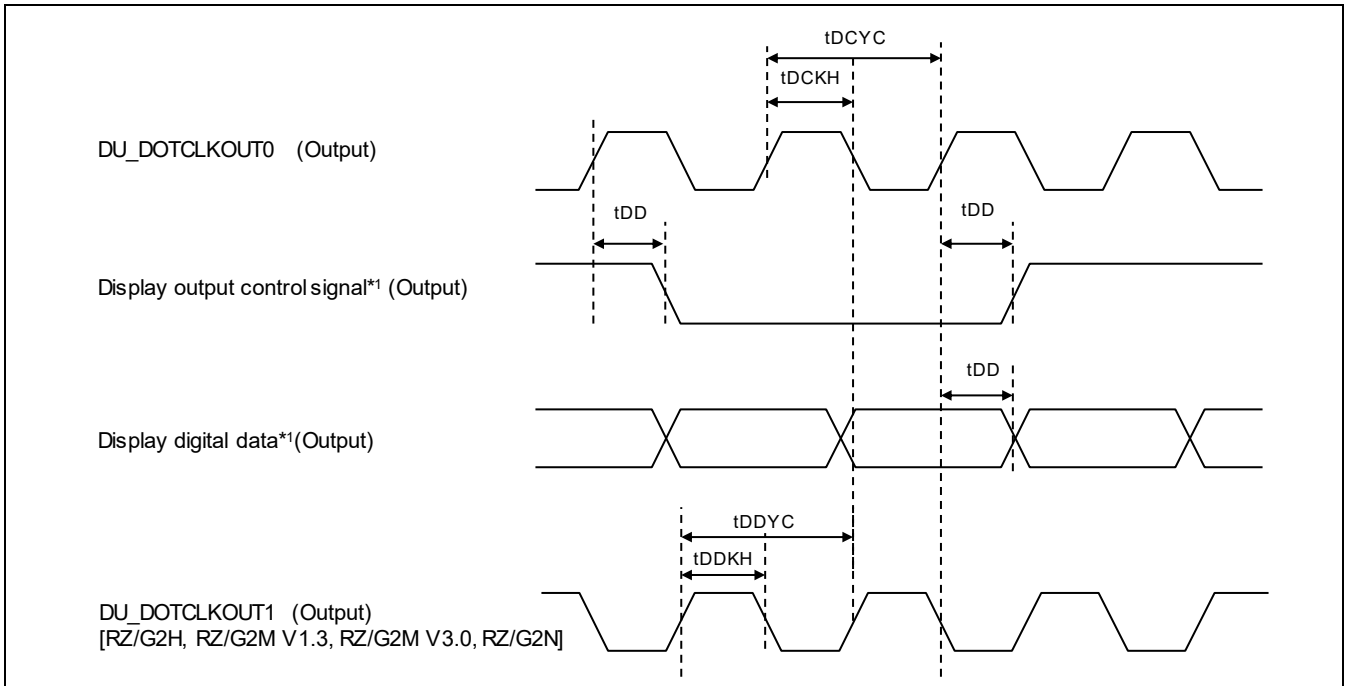


Figure 3.13.1 DOTCLKIN Clock Input Timing



Notes: * For pin names corresponding to the input control signals, refer to Table 3.13.4

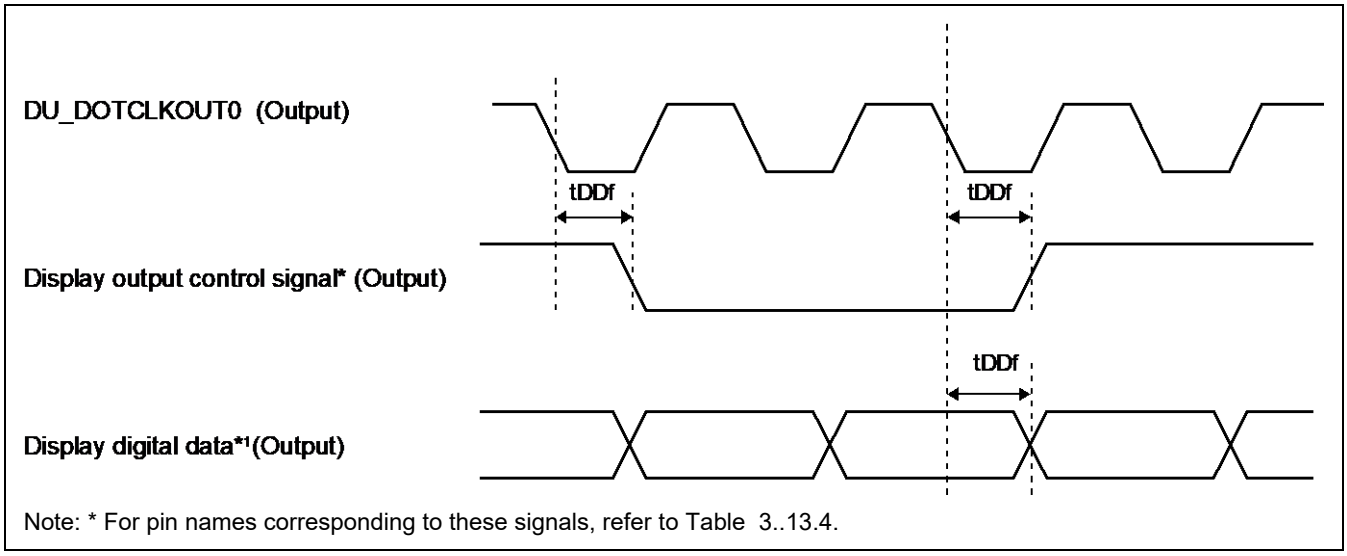
Figure 3.13.2 Display Signal Timing (Relative to DOTCLKIN)
[RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]



Notes: 1. For pin names corresponding to these signals, refer to Table 3.13.4.

Figure 3.13.3 Display Signal Timing (Relative to DOTCLKOUT)

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Note: * For pin names corresponding to these signals, refer to Table 3..13.4.

Figure 3.13.4 Display Signal Timing (Relative to DOTCLKOUT falling edge) [RZ/G2N]

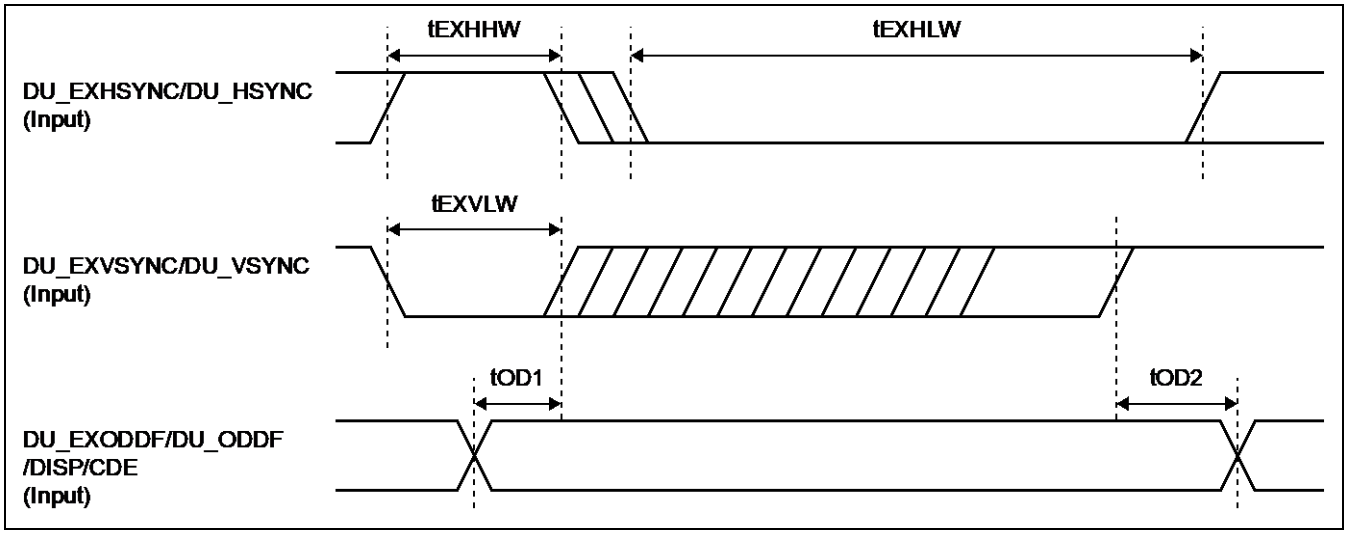


Figure 3.13.5 TV Sync Mode Display Signal Timing [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

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3.14 LVDS-IF

RZ/G2H | RZ/G2M V1.3 | RZ/G2M V3.0 | RZ/G2N | RZ/G2E

Table 3.14.1 AC Characteristics (1.8-V I/O [LVDS]) [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N (in Single-link), RZ/G2E (in Single-link)]

Conditions: VDDQ18_LVDS = VDD18_LVDSPLL1 = 1.8V ± 0.1V,
VDDQ09_LVDS = VDD09_LVDSPLL2 = 0.82V + 0.06V/-0.07V,
GND = VSS = 0V [RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2H, RZ/G2N],
VDDQ18_LVDS = VDD18_LVDSnPLL (n = 0, 1) = 1.8V ± 0.1V,
GND = VSS = VSS_LVDSnPLL (n = 0, 1) = 0V [RZ/G2E]
Tc = -40 to +115°C [RZ/G2M V1.3, RZ/G2H],
Ta = -40 to +85°C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115°C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
CL = 3pF

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement condition	Figures
Input Clock Frequency of LVDS	F_{CPHIN}	31.0 [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]	—	150.0	MHz	—	Figure 3.14.1
Output Clock Frequency of LVDS	$F_{CLKP/CLKN}$	31.0 [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]	—	150.0	MHz	—	Figure 3.14.2
		5.0 [RZ/G2E]					
Output Clock of LVDS	T_{CP}	6.67	—	32.2 [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]	ns	—	
				200.0 [RZ/G2E]			
Output Data Rate of LVDS	$F_{DAP/DAN}$	217.0 [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]	—	1050.0	Mbps	—	
		35.0 [RZ/G2E]					
LVDS Output Pulse Position 0	T_{PPOS0}	-0.150	0	0.150	ns	—	
LVDS Output Pulse Position 1	T_{PPOS1}	(T_{CP}/7) -0.150	T_{CP}/7	(T_{CP}/7) +0.150	ns	—	
LVDS Output Pulse Position 2	T_{PPOS2}	2(T_{CP}/7) -0.150	2T_{CP}/7	2(T_{CP}/7) +0.150	ns	—	
LVDS Output Pulse Position 3	T_{PPOS3}	3(T_{CP}/7) -0.150	3T_{CP}/7	3(T_{CP}/7) +0.150	ns	—	
LVDS Output Pulse Position 4	T_{PPOS4}	4(T_{CP}/7) -0.150	4T_{CP}/7	4(T_{CP}/7) +0.150	ns	—	

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Item	Symbol	Min.	Typ.	Max.	Unit	Measurement condition	Figures
LVDS Output Pulse Position 5	T_{PPOS5}	5(T_{CP}/7) -0.150	5T_{CP}/7	5(T_{CP}/7) +0.150	ns	—	Figure 3.14.2
LVDS Output Pulse Position 6	T_{PPOS6}	6(T_{CP}/7) -0.150	6T_{CP}/7	6(T_{CP}/7) +0.150	ns	—	

Table 3.14.2 AC Characteristics in Dual-link (1.8-V I/O [LVDS]) [RZ/G2E]

Conditions: VDDQ18_LVDS = VDD18_LVDSnPLL (n = 0, 1) = 1.8V ± 0.1V [RZ/G2E],
GND = VSS = VSS_LVDSnPLL (n = 0, 1) = 0V [RZ/G2E],
Ta = -40 to +85°C [RZ/G2E],
Tj = -40 to +115°C [RZ/G2E]
CL = 3pF

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement condition	Figures
Input Clock Frequency of LVDS	F_{CPHIN}	12.0	—	150.0	MHz	—	Figure 3.14.1
Output Clock Frequency of LVDS	$F_{CLKP/CLKN}$	5.0	—	75.0	MHz	—	Figure 3.14.2, Figure 3.14.3
Output Clock of LVDS	T_{CP}	13.3	—	200.0	ns	—	
Output Data Rate of LVDS	$F_{DAP/DAN}$	35	—	525.0	Mbps	—	
LVDS Output Pulse Position 0	T_{PPOS0}	-0.200	0	0.200	ns	—	
LVDS Output Pulse Position 1	T_{PPOS1}	(T_{CP}/7)-0.200	T_{CP}/7	(T_{CP}/7) +0.200	ns	—	
LVDS Output Pulse Position 2	T_{PPOS2}	2(T_{CP}/7)-0.200	2T_{CP}/7	2(T_{CP}/7)+0.200	ns	—	
LVDS Output Pulse Position 3	T_{PPOS3}	3(T_{CP}/7)-0.200	3T_{CP}/7	3(T_{CP}/7)+0.200	ns	—	
LVDS Output Pulse Position 4	T_{PPOS4}	4(T_{CP}/7)-0.200	4T_{CP}/7	4(T_{CP}/7)+0.200	ns	—	
LVDS Output Pulse Position 5	T_{PPOS5}	5(T_{CP}/7)-0.200	5T_{CP}/7	5(T_{CP}/7)+0.200	ns	—	
LVDS Output Pulse Position 6	T_{PPOS6}	6(T_{CP}/7)-0.200	6T_{CP}/7	6(T_{CP}/7)+0.200	ns	—	

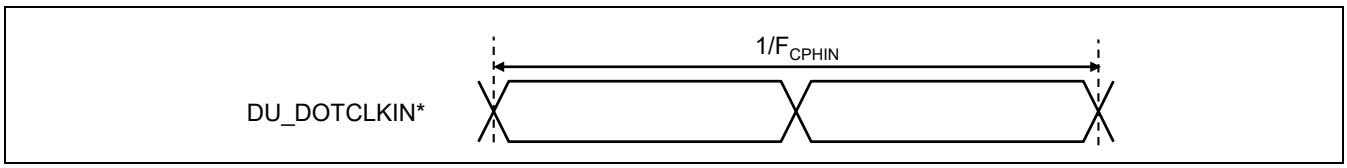


Figure 3.14.1 F_{CPHIN}

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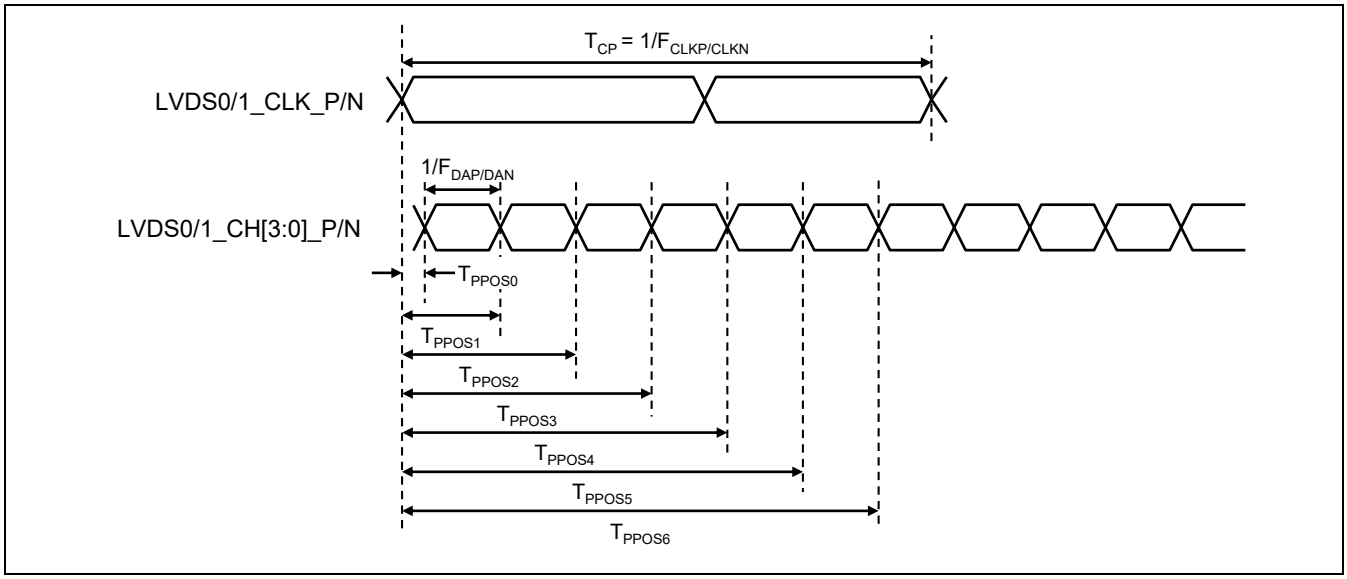


Figure 3.14.2 FCLKP/CLKN, TCP, FDAP/DAN, TPPOS in Single-link

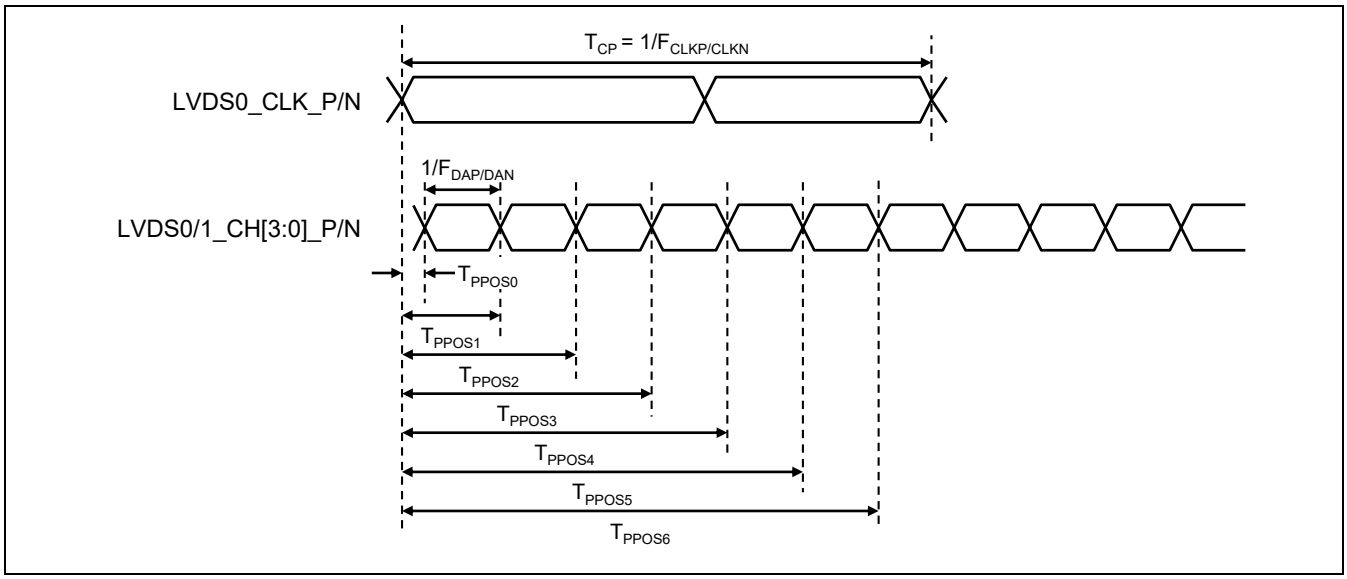


Figure 3.14.3 FCLKP/CLKN, TCP, FDAP/DAN, TPPOS in Dual-link

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3.15 SSI Interface

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Table 3.15.1 SSI Interface Signal Timing

Conditions: VDDQ33 = 3.10 V – 3.50 V, GND = VSS = 0 V, Tc = -40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N], Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N]
CL = 30 pF (other than tRC: Rise-edge clock timing) [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

Conditions: VDDQ33 = 3.00 V – 3.60 V, GND = VSS = 0 V, Ta = -40 to +85 °C, Tj = -40 to +115 °C,
CL = 30 pF (other than tRC: Rise-edge clock timing) [RZ/G2E]

Item	Symbol	Min.	Typ.	Max.	Unit	Note	Figures
Output clock cycle	tO	80	—	15625	ns	—	Figure 3.15.1
Input clock cycle	tI	66	—	15625	ns	—	
Output clock high-cycle	tHC	35	—	—	ns	—	
Output clock low-cycle	tLC	35	—	—	ns	—	
Input clock high-cycle	tHC	28	—	—	ns	—	
Input clock low-cycle	tLC	28	—	—	ns	—	
Rise-edge clock timing	tRC	—	—	20	ns	Output (100pF)	
Output delay	tD	−5	—	19	ns	—	Figure 3.15.2 to Figure 3.15.5
	tD	—	—	19	ns	—	Figure 3.15.6
Setup time	tS	15	—	—	ns	—	Figure 3.15.2 to Figure 3.15.5
Hold time	tH	5	—	—	ns	—	
Audio clock frequency	fAUDIO	3.072	—	25	MHz	—	Figure 3.15.7
Audio clock duty	fAUDIOduty	0.45	—	0.55	fAUDIO	—	

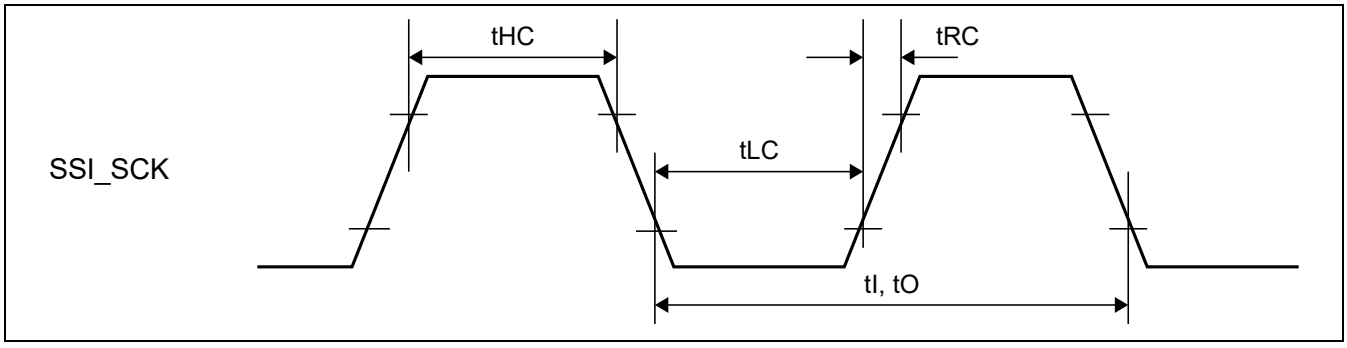


Figure 3.15.1 SCK Clock Input/output Timing

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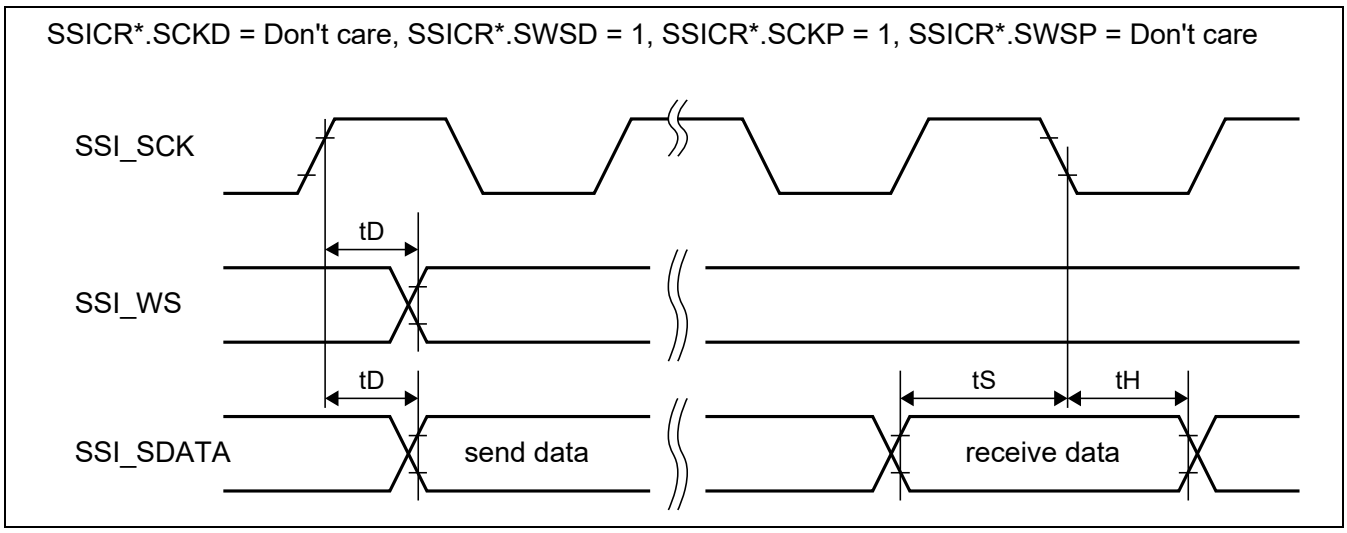


Figure 3.15.2 SSI Timing (1)

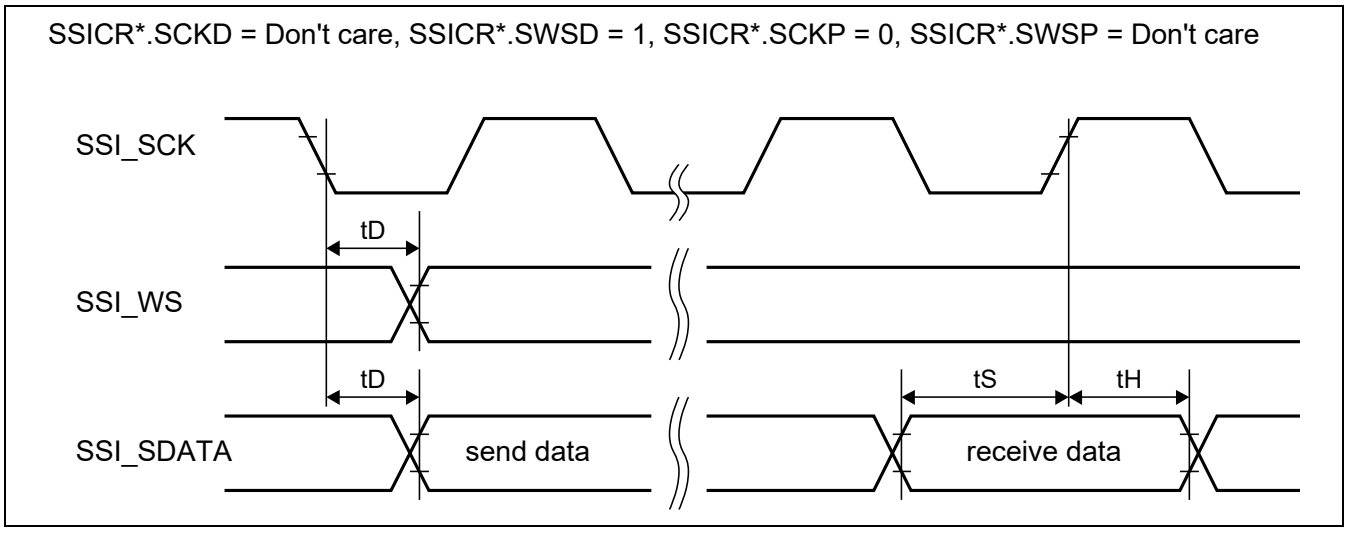


Figure 3.15.3 SSI Timing (2)

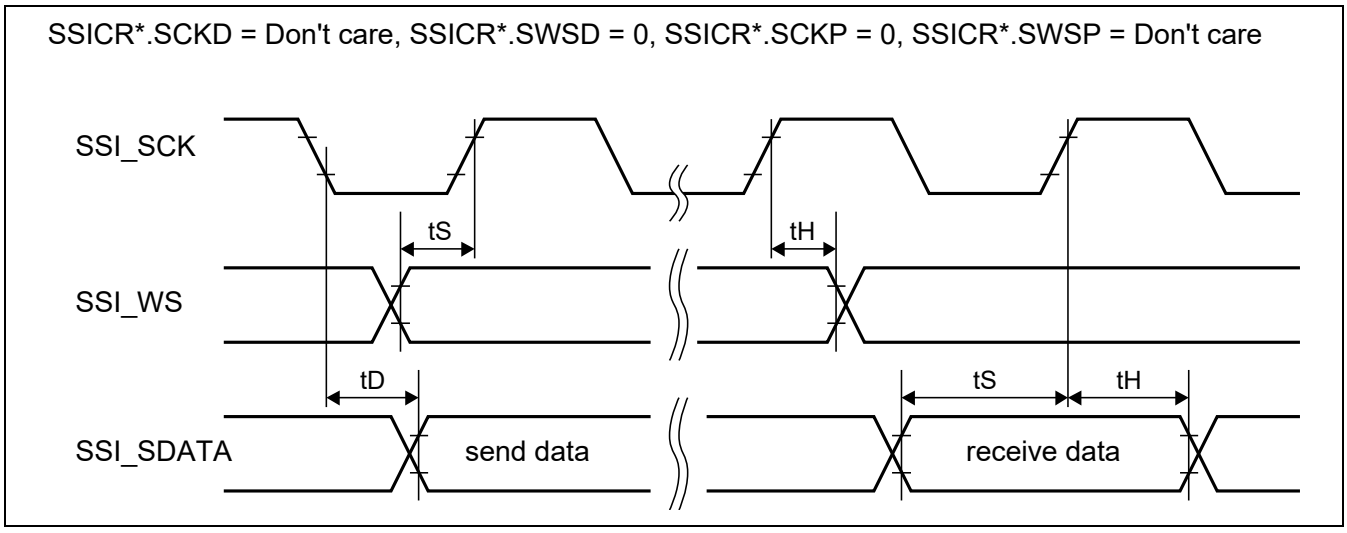


Figure 3.15.4 SSI Timing (3)

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SSICR*.SCKD = Don't care, SSICR*.SWSD = 0, SSICR*.SCKP = 1, SSICR*.SWSP = Don't care

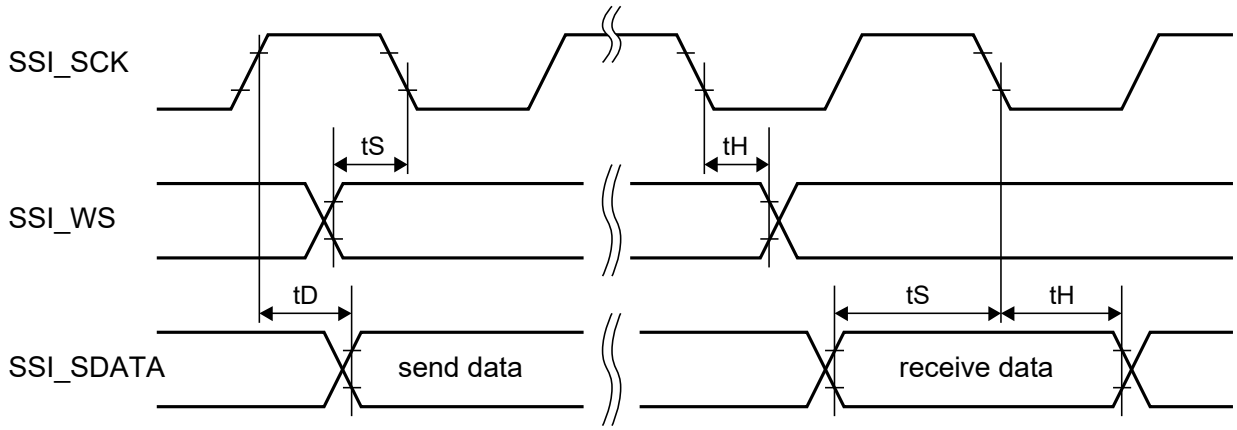


Figure 3.15.5 SSI Timing (4)

The follows are output timings of the MSB bit in the setting of the slave transmission by non-compressio
Send data is no padding bit with a left justify format or a right justify format.
SSICR*.SCKD=0, SSICR*.SWSD=0, SSICR*.DEL=1, SSICR*.TRMD=1
SSICR*.SDTA=0 or SSICR*.SDTA=1 and moreover SSICR*.SWL=SSICR*.DWL

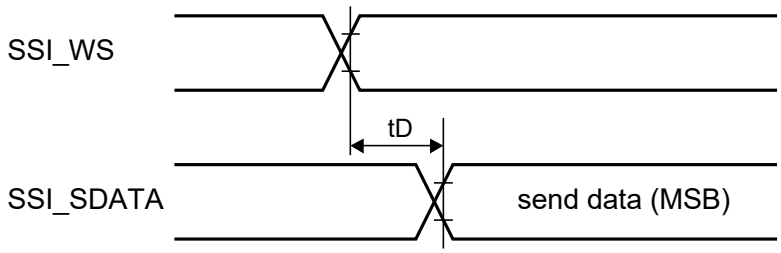


Figure 3.15.6 SSI Timing (5)

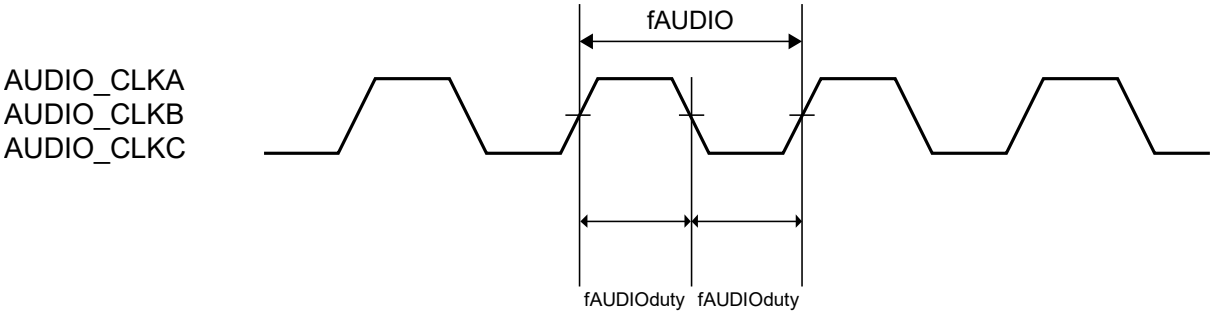


Figure 3.15.7 AUDIO_CLK Input Timing

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3.16 Ethernet AVB-IF Module Signal Timing

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Table 3.16.1 Ethernet Control Timing (RGMII 100Mbps Mode)

Conditions: VDDQ33 = 3.3 ± 0.2 V, VDDQ25_ETH = 2.5 ± 0.1V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N],
VDDQ25_AVB0 = 2.5 ± 0.2V [RZ/G2E],
Tc = -40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E], GND = VSS = 0 V, CL = 30 pF

Recommend: Connection of series 25 Ω as damping resistor to RGMII output buffer. [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
AVB_TXCREFCLK cycle time	—	125 – 50 ppm	—	125 + 50 ppm	MHz	—
AVB_TXC cycle time	Tcyc	36	40	44	ns	
AVB_TXC duty cycle	Duty_T	40	50	60	%	
AVB_TX_CTL to clock output skew	TskewT	-500	0	500	ps	Figure 3.16.1
AVB_TD[3:0] to clock output skew	TskewT	-500	0	500	ps	
AVB_RXC cycle time	Tcyc	36	40	44	ns	—
AVB_RXC duty cycle	Duty_T	40	50	60	%	
AVB_RX_CTL to clock input skew	TskewR	1	1.8	17	ns	Figure 3.16.2
AVB_RD[3:0] to clock input skew	TskewR	1	1.8	17	ns	

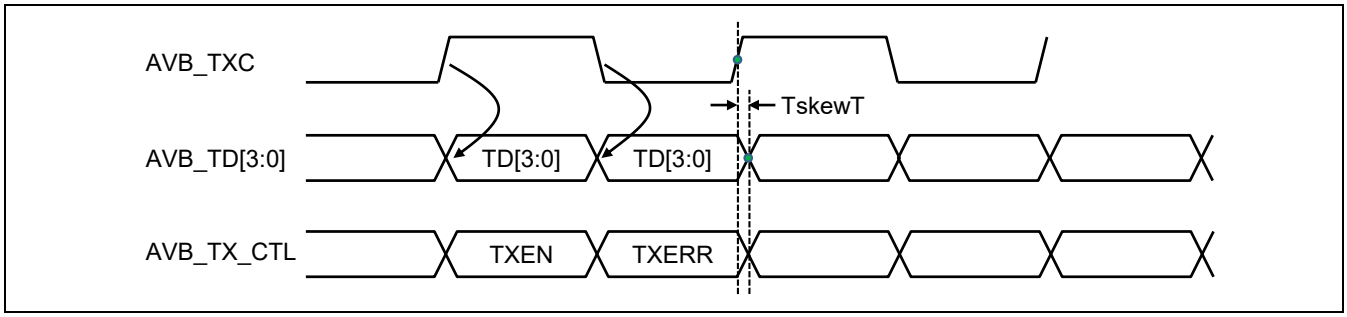


Figure 3.16.1 RGMII 100 Mbps Mode Transmission Timing

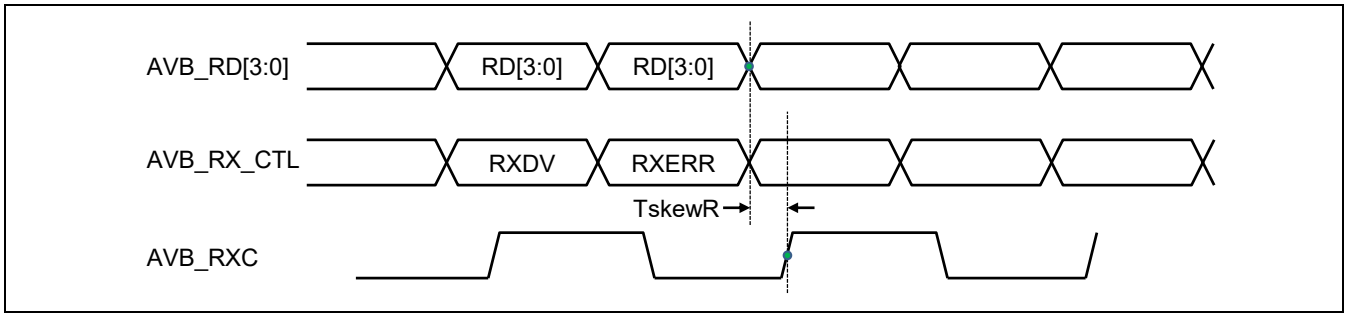


Figure 3.16.2 RGMII 100 Mbps Mode Reception Timing

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Table 3.16.2 Ethernet Control Timing (RGMII 1Gbps Mode)

Conditions: VDDQ33 = 3.3 ± 0.2 V, VDDQ25_ETH = 2.5 ± 0.1V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N],
VDDQ25_AVB0 = 2.5 ± 0.2V [RZ/G2E],
Tc = -40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E], GND = VSS = 0 V, CL = 30 pF

Recommend: Connection of series 25 Ω as damping resistor to RGMII output buffer. [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
AVB_TXCREFCLK cycle time	—	125 – 50 ppm	—	125 + 50 ppm	MHz	—
AVB_TXC cycle time	Tcyc	7.2	8	8.8	ns	
AVB_TXC duty cycle	Duty_G	45	50	55	%	
AVB_TX_CTL to clock output skew	TskewT	-500	0	500	ps	Figure 3.16.3
AVB_TD[3:0] to clock output skew	TskewT	-500	0	500	ps	
AVB_RXC cycle time	Tcyc	7.2	8	8.8	ns	—
AVB_RXC duty cycle	Duty_G	45	50	55	%	
AVB_RX_CTL to clock input skew	TskewR	1	1.8	2.6	ns	Figure 3.16.4
AVB_RD[3:0] to clock input skew	TskewR	1	1.8	2.6	ns	

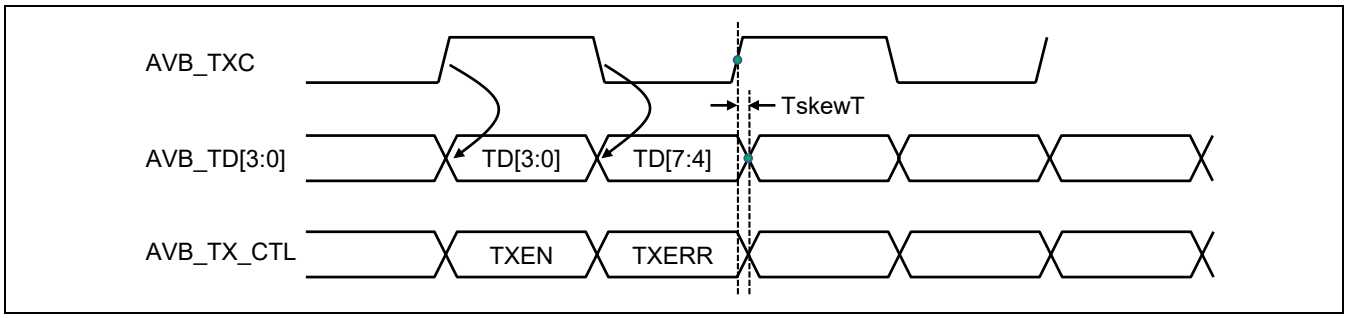


Figure 3.16.3 RGMII 1 Gbps Mode Transmission Timing

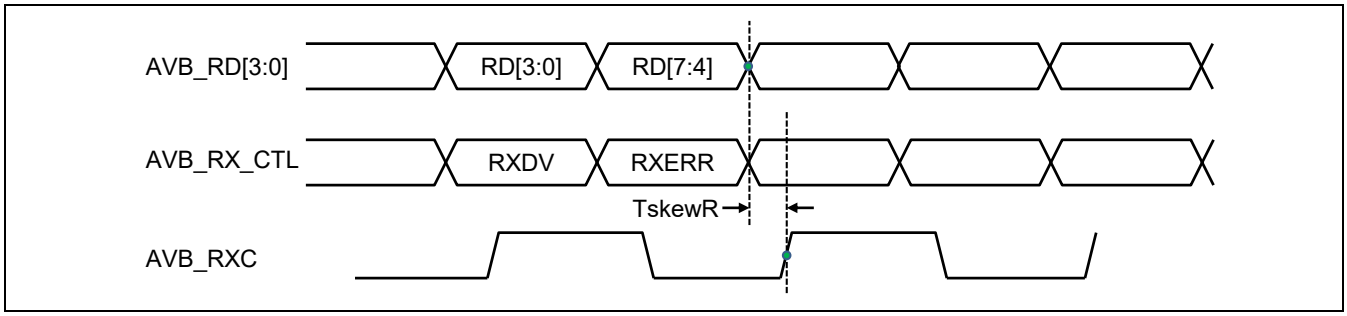


Figure 3.16.4 RGMII 1 Gbps Mode Reception Timing

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Table 3.16.3 Ethernet Control Timing (RGMII Tx clock internal Delay Mode) [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

Conditions: VDDQ33 = 3.3 ± 0.2 V, VDDQ25_ETH = 2.5 ± 0.1V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N],
Tc = -40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N], GND = VSS = 0 V, CL = 30 pF

Recommend: Connection of series 25 Ω as damping resistor to RGMII output buffer. [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
AVB_TXCREFCLK cycle time	—	125 – 50 ppm	—	125 + 50 ppm	MHz	—
AVB_TXC cycle time *1	Tcyc	7.2	8	8.8	ns	
AVB_TXC duty cycle (in 1 Gbps)	Duty_G	45	50	55	%	
AVB_TXC duty cycle (in 100 Mbps)	Duty_T	40	50	60	%	
AVB_TX_CTL setup time	TsetupT	1.2 *2	2.0	—	ns	Figure 3.16.5
		0.95 *3				
AVB_TX_CTL hold time	TholdT	1.2	2.0	—	ns	
AVB_TD[3:0] setup time	TsetupT	1.2 *2	2.0	—	ns	
		0.95 *3				
AVB_TD[3:0] hold time	TholdT	1.2	2.0	—	ns	

Notes: 1. For 100 Mbps, Tcyc will scale to 40 ns ± 4 ns respectively.
2. For [RZ/G2H, RZ/G2M V3.0, RZ/G2N].
3. For [RZ/G2M V1.3].

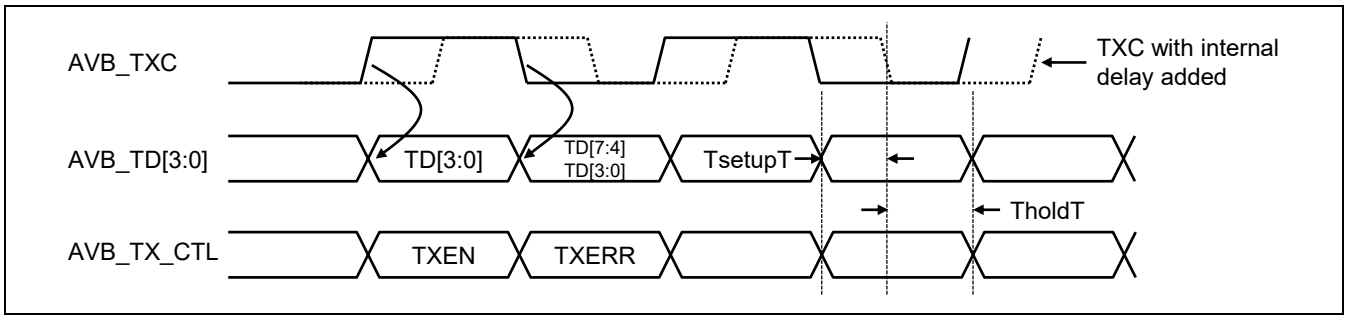


Figure 3.16.5 RGMII Delay Mode Transmission Timing

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Table 3.16.4 Ethernet Control Timing (RGMII Rx clock internal Delay Mode)

Conditions: VDDQ25_ETH = 2.5 ± 0.1 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N],
VDDQ25_AVB0 = 2.5 ± 0.2 V [RZ/G2E],
Tc = -40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E], GND = VSS = 0 V, CL = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
AVB_RXC cycle time *	Tcyc	7.2	8	8.8	ns	—
AVB_RXC duty cycle (in 1 Gbps)	Duty_G	45	50	55	%	
AVB_RXC duty cycle (in 100 Mbps)	Duty_T	40	50	60	%	
AVB_RX_CTL to clock input skew	TskewR	-500	0	500	ps	Figure 3.16. 6
AVB_RD[3:0] to clock input skew	TskewR	-500	0	500	ps	

Note: * For 100 Mbps, Tcyc will scale to 40 ns ± 4 ns respectively.

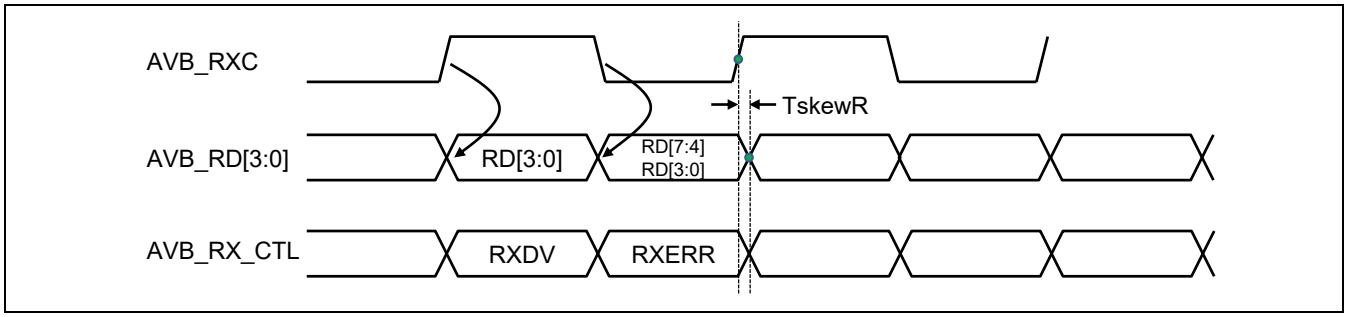


Figure 3.16.6 RGMII Delay Mode Reception Timing

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Table 3.16.5 AVTP pins timing specification [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N, RZ/G2E]

Conditions: VDDQ33 = 3.3 ± 0.2 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N],
VDDQ33 = 3.3 ± 0.3 V [RZ/G2E],
Tc = -40 to+115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E], GND = VSS = 0 V, CL = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
AVB_AVTP_CAPTURE input pulse width	PWidth_capt	3	—	—	Cycle*	Figure 3.16.7
AVB_AVTP_CAPTURE input period	Period_capt	9	—	—	Cycle*	
AVB_AVTP_MATCH output pulse width	PWidth_match	1	—	4	Cycle*	Figure 3.16.8
AVB_AVTP_PPS output pulse width	PWidth_pps	—	32	—	Cycle*	Figure 3.16.9

Note: * 1 cycle = HPϕ cycle.

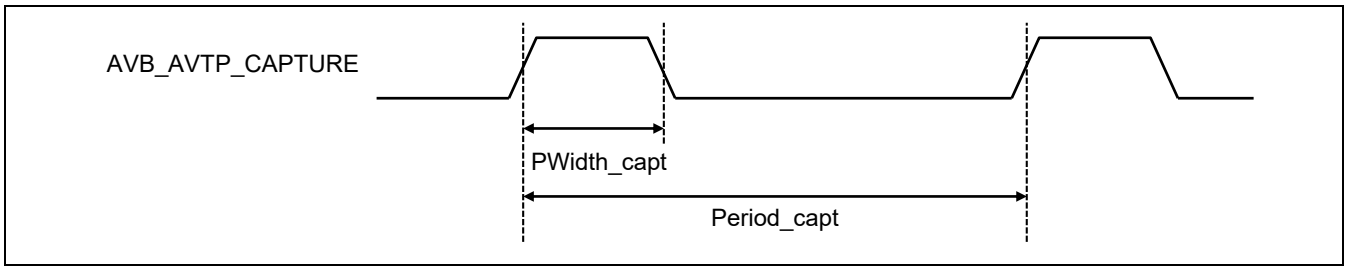


Figure 3.16.7 AVB_AVTP_CAPTURE input Timing

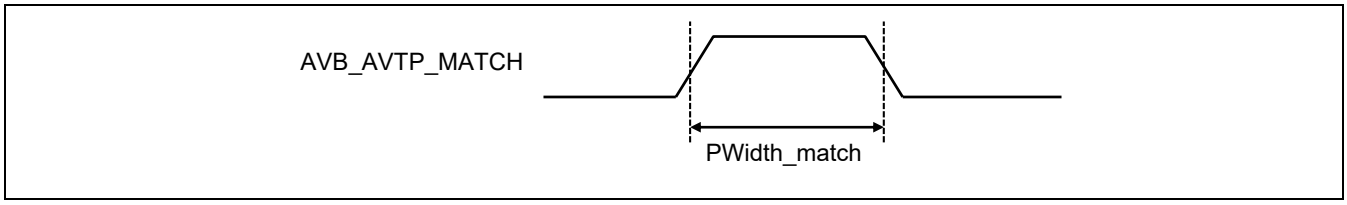


Figure 3.16.8 AVB_AVTP_MATCH output Timing

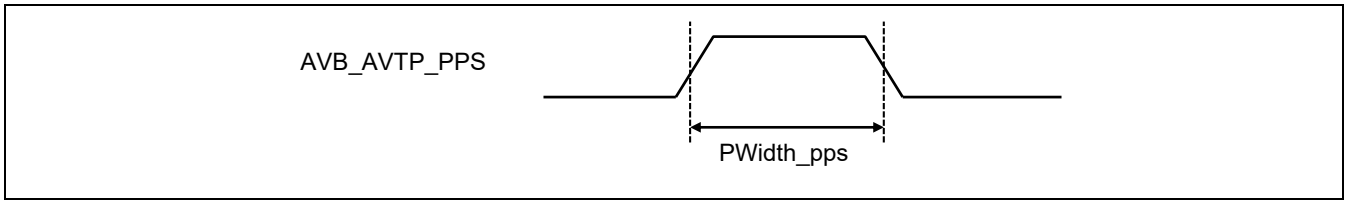


Figure 3.16.9 AVB_AVTP_PPS output Timing

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Table 3.16.6 Sideband pins timing specification

Conditions: VDDQ33 = 3.3 ± 0.2 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N],
VDDQ25_AVB0 = 2.5 ± 0.2 V/3.3 ± 0.3 V [RZ/G2E],
Tc = -40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E], GND = VSS = 0 V, CL = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
AVB_MDIO input pulse width	PWidth_side	2	—	—	Cycle*	Figure 3.16.10
AVB_PHY_INT input pulse width	PWidth_side	2	—	—	Cycle*	
AVB_LINK input pulse width	PWidth_side	2	—	—	Cycle*	

Note: * 1 cycle = HPϕ cycle.

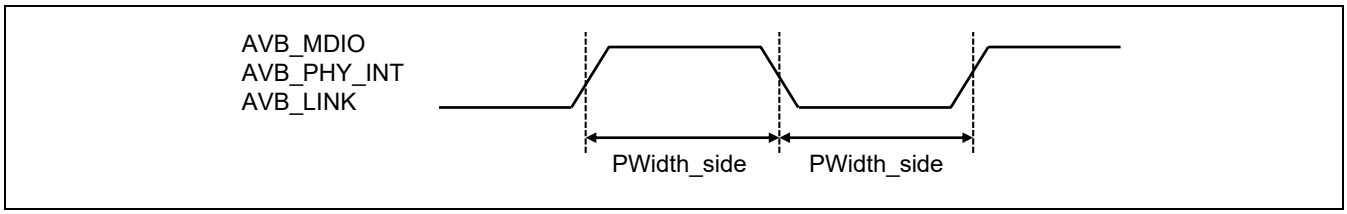


Figure 3.16.10 Sideband signals input Timing

Note: About AVB_MDC, in case of connecting to a device that does not have a built-in pull resistor, should add pull register at external.

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3.17 CAN, CAN-FD

RZ/G2H | RZ/G2M V1.3 | RZ/G2M V3.0 | RZ/G2N | RZ/G2E

Table 3.17.1 CAN Signal Timing

Conditions: VDDQ33 = 3.3 ± 0.2 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N] /± 0.3 V [RZ/G2E],
Tc = -40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
GND = VSS = 0 V, CL = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
Input clock cycle (asynchronous)	tSCYC	20	—	—	ns	Figure 3.17.1
Input clock pulse width	tSCKW	0.4	—	0.6	tSCYC	
Input clock rise time	tSCKr	—	—	0.2	tCYC	
Input clock fall time	tSCKf	—	—	0.2	tCYC	

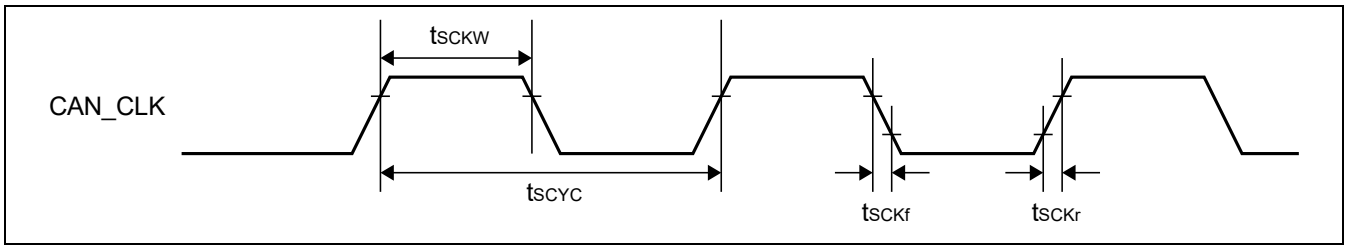


Figure 3.17.1 Input Clock Timing

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3.18 PCIE Controller

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

The description in this section is compliant with the following PCIe standard: 'PCI Express® Base Specification Revision 2.1, March 4, 2009'.

Table 3.18.1 PCIE Controller Characteristics [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N, RZ/G2E]

Conditions: VDDQ18_PCIE0 = 1.8 ± 0.1 V, VDDD_PCIE0 = 1.03 ± 0.05 V [RZ/G2E], VDD33_PCIEn (n = 0, 1) = 3.3 ± 0.2 V, VDD09_PCIEn (n = 0, 1) = 0.82 – 0.07 V / + 0.06 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N], GND = 0 V,
Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3], Ta = −40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = −40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E]

Test Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Differential Input Peak to Peak Voltage (2.5 GT/s)	VRX-DIFFp-p	0.175	—	1.200	V	*1
Differential Input Peak to Peak Voltage (5 GT/s)	VRX-DIFFp-p	0.120	—	1.200	V	*1
Differential Peak to Peak Output Voltage (2.5 & 5 GT/s)	VTX-DIFFp-p	0.800	—	1.2	V	*2
Absolute Delta of DC Common Mode Voltage between D+ and D- (2.5 & 5 GT/s)	VTX-CM-DC-LINE-DELTA	0	—	25	mV	*2
Unit Interval (2.5 GT/s)	UI	399.88	—	400.12	ps	*3
Unit Interval (5 GT/s)	UI	199.94	—	200.06	ps	*3
DC Differential TX Impedance (2.5 GT/s)	ZTX-DIFF-DC	80	—	120	Ω	—
DC Differential TX Impedance (5 GT/s)	ZTX-DIFF-DC	—	—	120	Ω	—
DC Differential Input Impedance (2.5 GT/s)	ZRX-DIFF-DC	80	—	120	Ω	—
DC Input Impedance (2.5 & 5 GT/s)	ZRX-DC	40	—	60	Ω	—

Notes: 1. RXP, RXN: DC test
2. TXP, TXN: DC test
3. Need Reference Clock (Low Voltage Swing, Differential Clocks). The nominal single-ended swing for each clock is 0 to 0.7 V and a nominal frequency of 100 MHz ± 100 PPM.

Table 3.18.2 PCIE Controller External Clock Accuracy

Conditions: VDD09_PCIE = 0.82 V – 0.07 V / + 0.06 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N],
VDDQ18_PCIE = 1.8 ± 0.1 V, VDDD_PCIE = 1.03 ± 0.05 V [RZ/G2E], GND = 0 V,
Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = −40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = −40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E]

Test Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
External clock accuracy (PCIE0_CLK_P, PCIE0_CLK_M)	—	—	100.000	—	MHz	Frequency accuracy: ±100 ppm or less

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3.19 SCIF

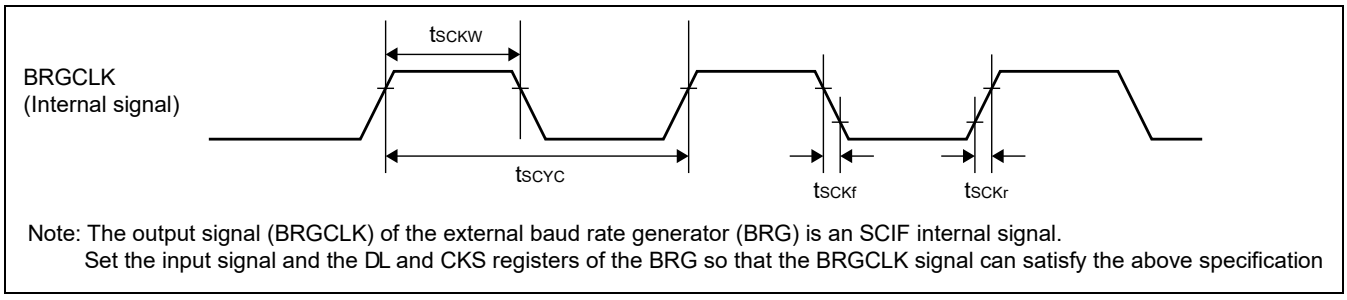
RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Table 3.19.1 SCIF Signal Timing

Conditions: VDDQ33 = VDDQVA_SDn = 3.3 ± 0.2 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N],
VDDQ33 = 3.3 ± 0.3 V [RZ/G2E],
GND = VSS = 0 V, Tc = -40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = −40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E], CL = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
Input clock cycle (asynchronous)	tSCYC	4	—	—	tCYC	Figure 3.19.1
Input clock cycle (synchronous)	tSCYC	8	—	—	tCYC	
Input clock pulse width	tSCKW	0.4	—	0.6	tSCYC	
Input clock rise time	tSCKr	—	—	0.8	tCYC	
Input clock fall time	tSCKf	—	—	0.8	tCYC	
Transmit data delay time	tTXD	—	—	4	tCYC	Figure 3.19.2
Receive data setup time (synchronous)	tRXS	5	—	—	tCYC	
Receive data hold time (synchronous)	tRXH	2	—	—	tCYC	

Note: RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N: tCYC is for one cycle of the S3D4ϕ clock.
RZ/G2E: tCYC is for one cycle of the S3D4Cϕ clock.



Note: The output signal (BRGCLK) of the external baud rate generator (BRG) is an SCIF internal signal.
Set the input signal and the DL and CKS registers of the BRG so that the BRGCLK signal can satisfy the above specification

Figure 3.19.1 Input Clock Timing

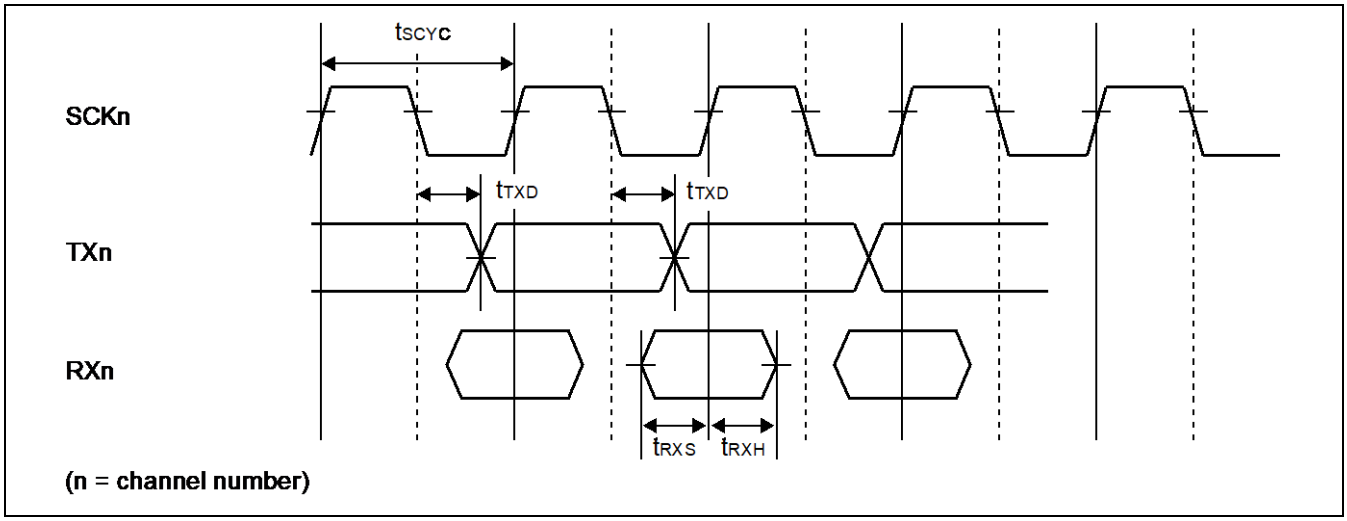


Figure 3.19.2 Input/output Timing in Synchronous Mode

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3.20 HSCIF

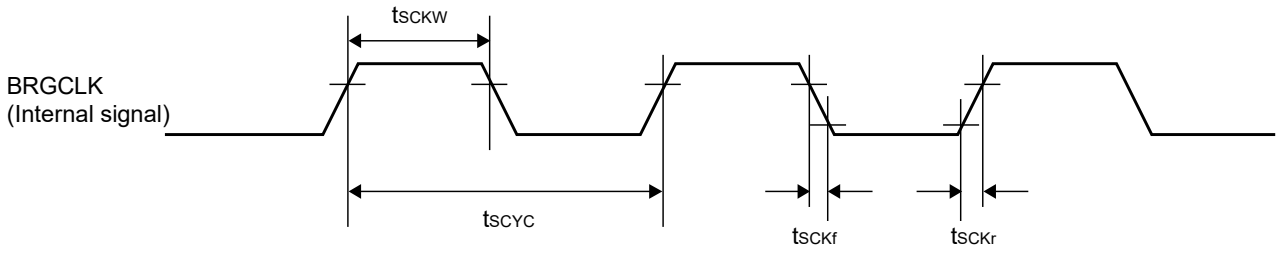
RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Table 3.20.1 HSCIF Signal Timing

Conditions: VDDQ33 = 3.3 ± 0.2 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N],
VDDQ33 = 3.3 ± 0.3 V [RZ/G2E],
GND = VSS = 0 V, Tc = -40 to +115 °C [RZ/G2H, RZ/G2M V1.3], Ta = −40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E], Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E], CL = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
Input clock cycle (asynchronous)	tSCYC	4	—	—	tCYC	Figure 3.20.1
Input clock pulse width	tSCKW	0.4	—	0.6	tSCYC	
Input clock rise time	tSCKr	—	—	0.8	tCYC	
Input clock fall time	tSCKf	—	—	0.8	tCYC	

Note: RZ/G2H, RZ/G2M V1.3,RZ/G2M V3.0, RZ/G2N: tCYC is for one cycle of the S3D1ϕ clock.
RZ/G2E: tCYC is for one cycle of the S3D1Cϕ clock.



Note: The output signal (BRGCLK) of the external baud rate generator (BRG) is an HSCIF internal signal.
Set the input signal and the DL and CKS registers of the BRG so that the BRGCLK signal can satisfy the above specification.

Figure 3.20.1 Input Clock Timing

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3.21 I2C

RZ/G2H | RZ/G2M V1.3 | RZ/G2M V3.0 | RZ/G2N | RZ/G2E

Table 3.21.1 I2C Signal Timing

Conditions: VDDQ33 = 3.3 ± 0.2 V, VDDQ18 = 1.8 V ± 0.1 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N],
VDDQ33 = 3.3 ± 0.3 V, VDDQ18 = 1.8 V ± 0.1 V, VDDQ_SDn = 3.3 ± 0.3 V / 1.8 V ± 0.1 V [RZ/G2E],
GND = VSS = 0 V,
Tc = -40 to +115 °C [RZ/G2H, RZ/G2M V1.3], Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E], CL = 400 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
I2C_SCL frequency	tICYC	—	—	400	kHz	Figure 3.21.1
I2C_SCL low level time	tLOW	1/(2 * tICYC) - 100	—	—	ns	
I2C_SCL high level time	tHIGH	600	—	—	ns	
I2C_SCL/I2C_SDA falling time	tICF	—	—	250	ns	
I2C_SDA bus free time	tICBF	1300	—	—	ns	
I2C_SCL start condition hold time	tICH	600	—	—	ns	
I2C_SCL repeat-start condition setup time	tICS	600	—	—	ns	
I2C_SDA stop condition setup time	tICST	600	—	—	ns	
I2C_SDA setup time	tDAS	100	—	—	ns	
I2C_SDA hold time	tICDH	0	—	900	ns	

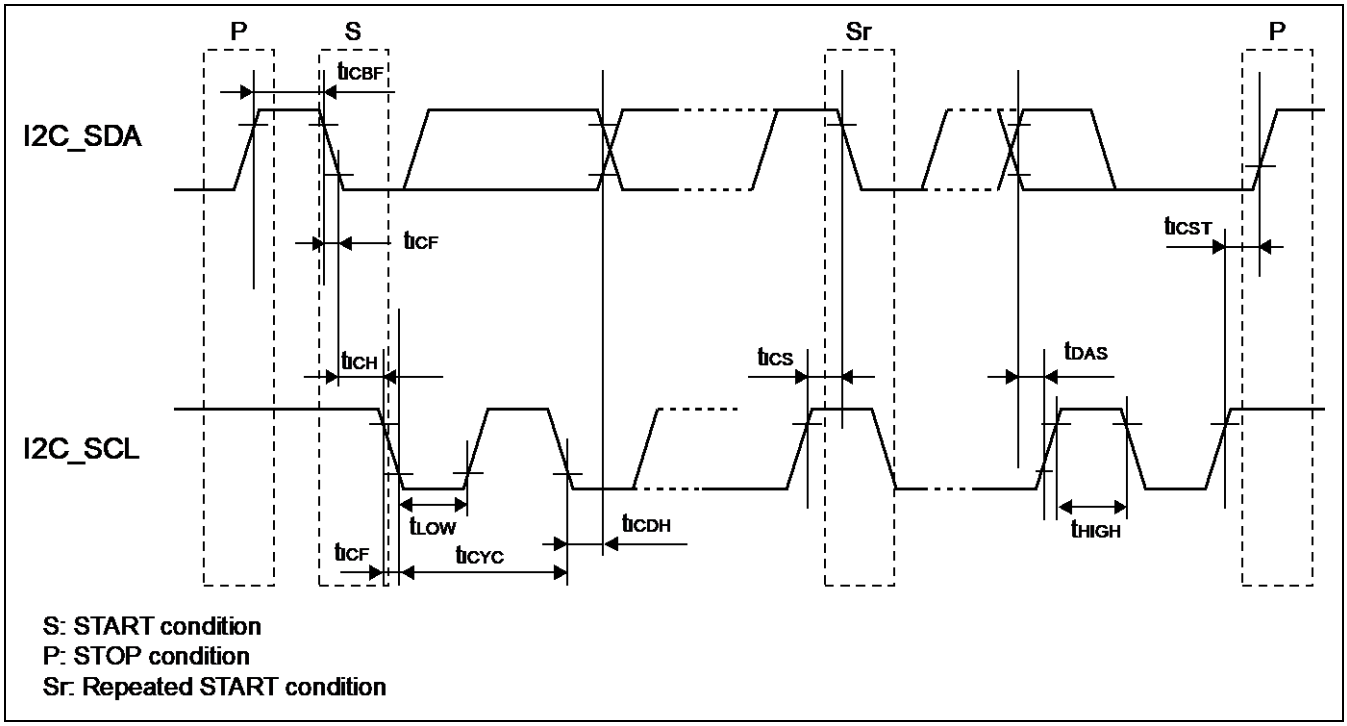


Figure 3.21.1 I2C Signal Timing

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3.22 IIC Bus Interface

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Table 3.22.1 IIC Bus Interface Signal Timing

Condition: VDDQ33 = 3.3 V ± 0.2 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N] / ± 0.3 V [RZ/G2E] or
VDDQ18 = 1.8 V ± 0.1 V, GND = VSS = 0 V,
Tc = -40 to +115 °C [RZ/G2H, RZ/G2M V1.3], Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E], CL = 30 pF

		Standard-Mode		Fast-Mode			
Item	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**	**Figures**
SCLclock frequency	f_{SCL}	0	100	0	400	kHz	Figure 3.22.1
Hold time (after repeat START condition, first clock pulse is generated)	$t_{HD;STA}$	4.0	—	0.6	—	µs	
L period in SCL clock	t_{LOW}	4.7	—	1.3	—	µs	
H period in SCL clock	t_{HIGH}	4.0	—	0.6	—	µs	
Setup time for repeat START condition	$t_{SU;STA}$	4.7	—	0.6	—	µs	
Date hold time	$t_{HD;DAT}$	0	3.45	0	0.9	µs	
Data setup time	$t_{SU;DAT}$	250	—	100	—	ns	
SDA and SCLsignal rise time	t_r	—	1000	—	300	ns	
SDA and SCL signal fall time	t_f	—	300	—	300	ns	
Setup time for STOP condition	$t_{SU;STO}$	4.0	—	0.6	—	µs	
Bus free time between STOP and START conditions	t_{BUF}	4.7	—	1.3	—	µs	
Noise margin at low level of each connected device (including hysteresis)	VnL	0.1 × VDDQ*4	—	0.1 × VDDQ*4	—	V	
Noise margin at high level of each connected device (including hysteresis)	VnH	0.2 × VDDQ*4	—	0.2 × VDDQ*4	—	V	
Spike pulse width suppressed by the input filter	t_{SP}	—	—	0	50	ns	

Notes. 1. All values are referenced at VDDQ*4 × 0.3 and VDDQ*4 × 0.7 levels.
2. To satisfy the I2C-bus specification, pull-up resistors (Rp) with the appropriate resistance must be included depending on the total of bus capacitive load of each line.
Pull-up resistor range should be following, refer Table 3.21.2.
Rp(max) = tr /(0.8473*Cb)
Rp(min) = (VDDQ*4-VOL(max))/IOL
3. The total capacity (Cb) should be less than or equal to 100 pF.
4. VDDQ means VDDQ33 or VDDQ18

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Table 3.22.2 Pull-up Resistor Range of IIC Bus Interface

Symbol	VCCQ Voltage	Standard-Mode		Fast-Mode		Unit	Remarks
		Min.	Max.	Min.	Max.		
Rp (Cb = 100 pF)	Vpullup = 1.8 V	517	11802	517	3540	Ω	—
	Vpullup = 3.3 V	1067	11802	1067	3540	Ω	

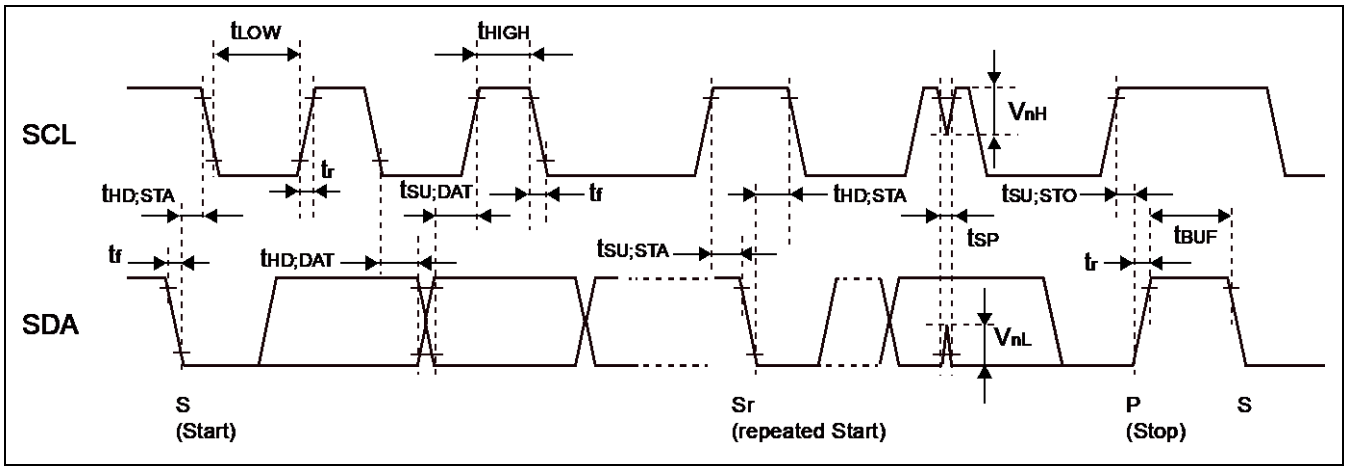


Figure 3.22.1 IIC Bus Interface Signal Timing

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3.23 MSIOF

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Table 3.23.1 MSIOF Module Signal Timing

Conditions: VDDQ33 = 3.3 V ± 0.2 V [RZ/G2H, RZ/G2M V1.3,RZ/G2M V3.0, RZ/G2N],
VDDQ33 = 3.3 V ± 0.3 V [RZ/G2E],
GND = VSS = 0 V, Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E], CL = 30 pF

Item	Symbol	Min.	Max.	Unit	Figures
MSIOF_SCK clock cycle time (when master TX or slave RX)	tMSCYC	4 × tpcyc*	—	ns	Figure 3.23.1, to Figure 3.23.4
MSIOF_SCK clock cycle time (when master RX or slave TX)	tMSCYC	8 × tpcyc*	—	ns	
MSIOF_SCK output clock high-level width	tMSWHO	0.4 × tMSCYC	—	ns	
MSIOF_SCK output clock low-level width	tMSWLO	0.4 × tMSCYC	—	ns	
MSIOF_SCK input high-level width	tMSWHI	0.4 × tMSCYC	—	ns	
MSIOF_SCK input low-level width	tMSWLI	0.4 × tMSCYC	—	ns	
MSIOF_SYNC input setup time in slave mode	tTSFSS	6	—	ns	
MSIOF_SYNC input hold time in slave mode	tTSFSH	2	—	ns	
MSIOF_TXD output delay time1 in slave mode	tTSDD1	1	20	ns	
MSIOF_TXD output delay time2 in slave mode	tTSDD2	1	16	ns	
MSIOF_RXD input setup time in slave mode	tTSRDS	6	—	ns	
MSIOF_RXD input hold time in slave mode	tTSRDH	5	—	ns	
MSIOF_SYNC output delay time in master mode	tTMSFD	-2	8	ns	
MSIOF_TXD output delay time in master mode	tTMDD	-2	8	ns	
MSIOF_RXD input setup time in master mode	tTMRDS	10	—	ns	
MSIOF_RXD input hold time in master mode	tTMRDH	2	—	ns	

Note: * tpcyc is a cycle time of peripheral clock (MSOϕ).

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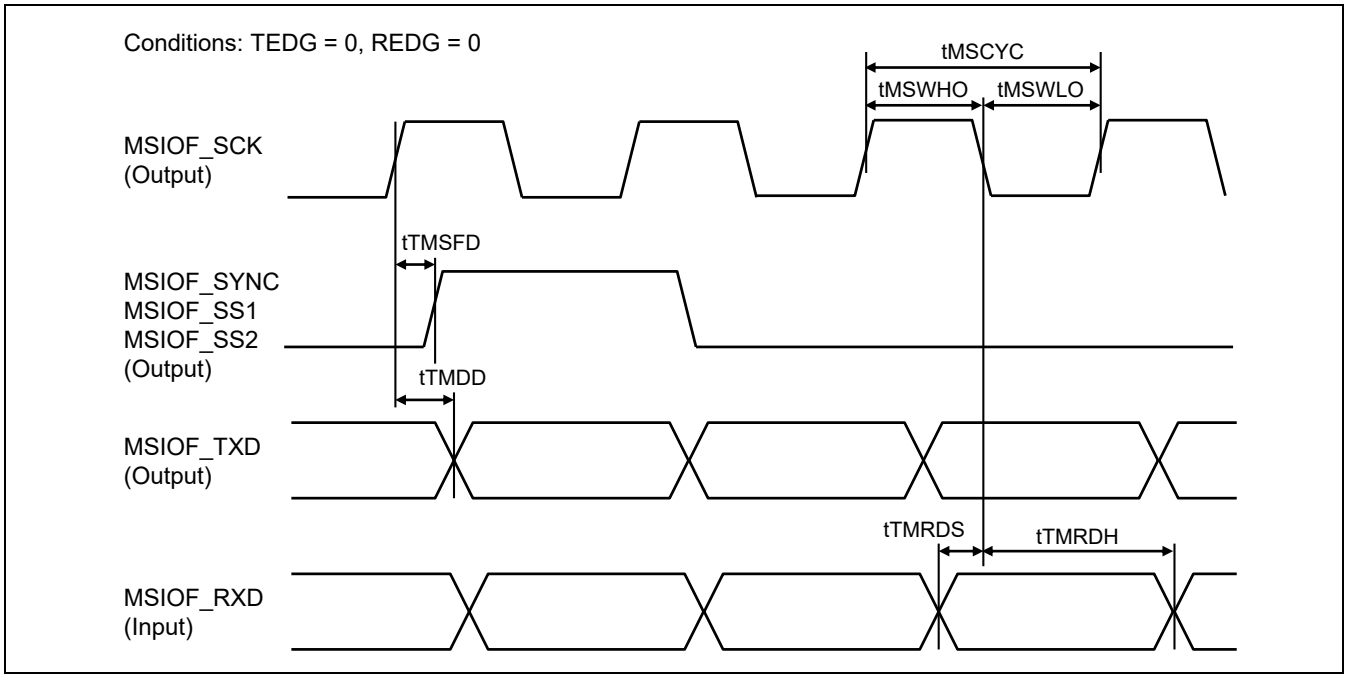


Figure 3.23.1 MSIOF Timing (Master Mode)

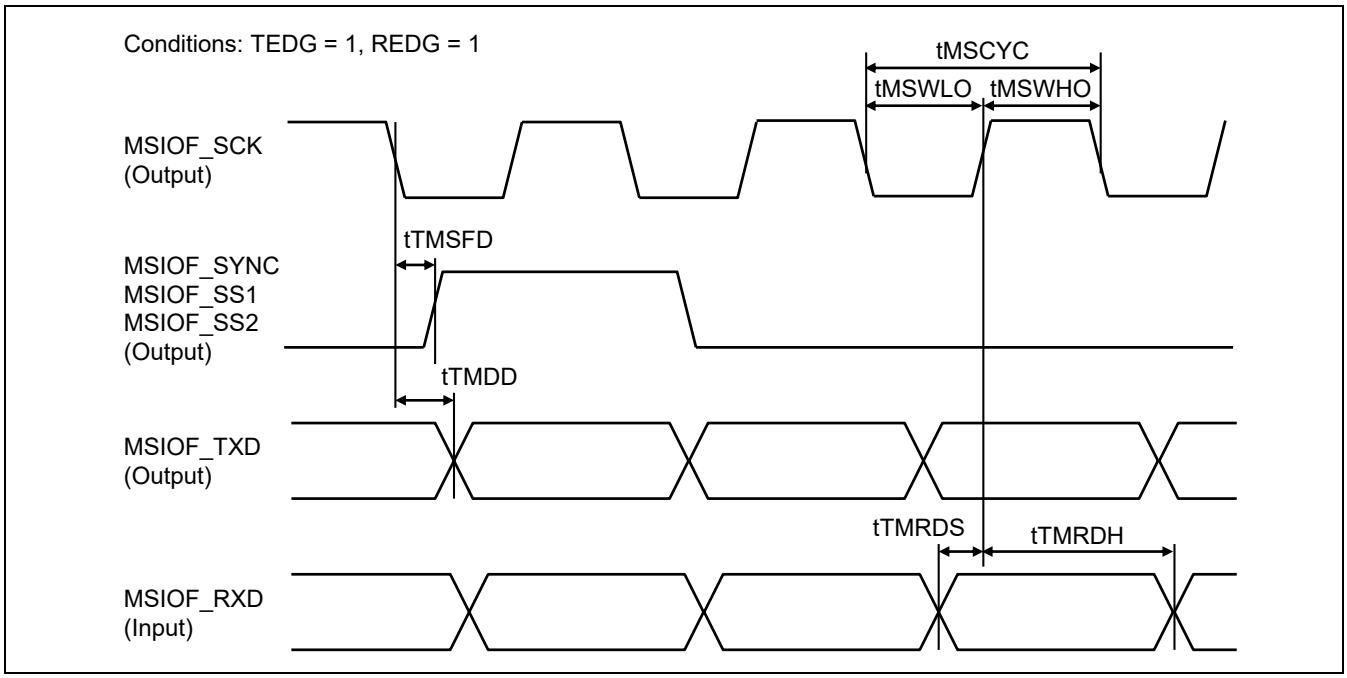


Figure 3.23.2 MSIOF Timing (Master Mode)

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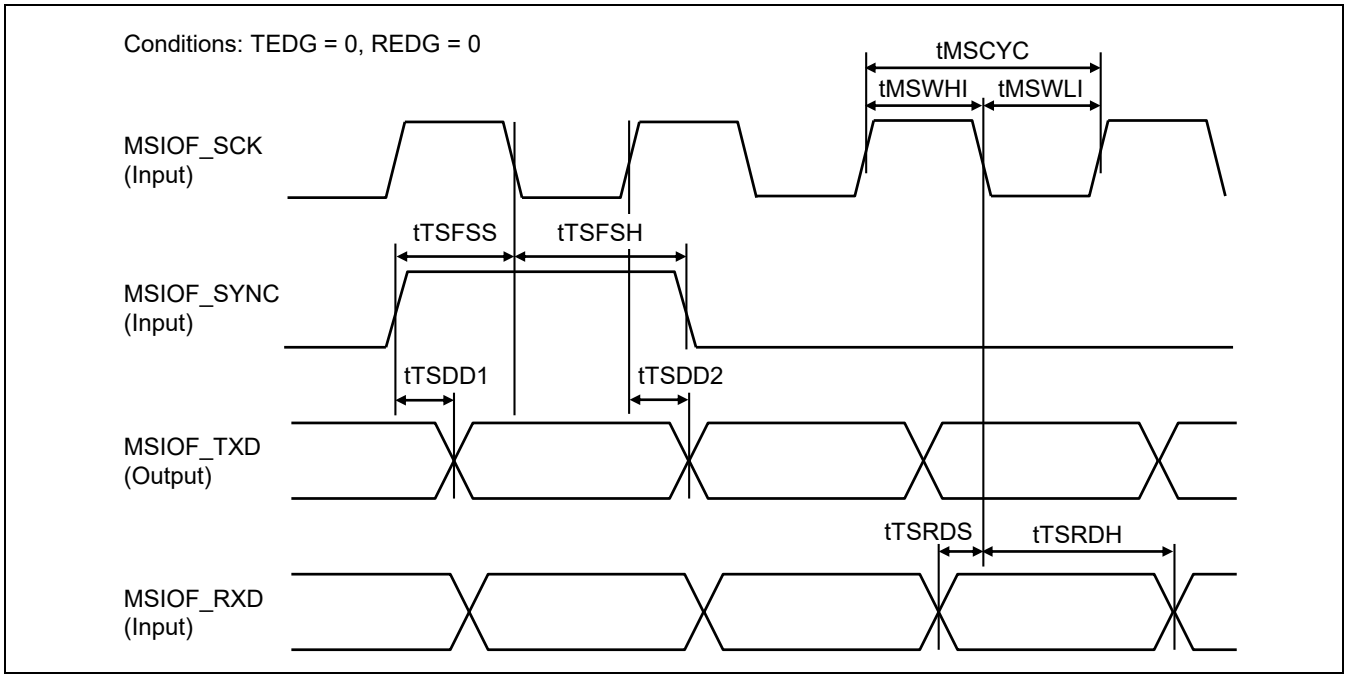


Figure 3.23.3 MSIOF Timing (Slave Mode)

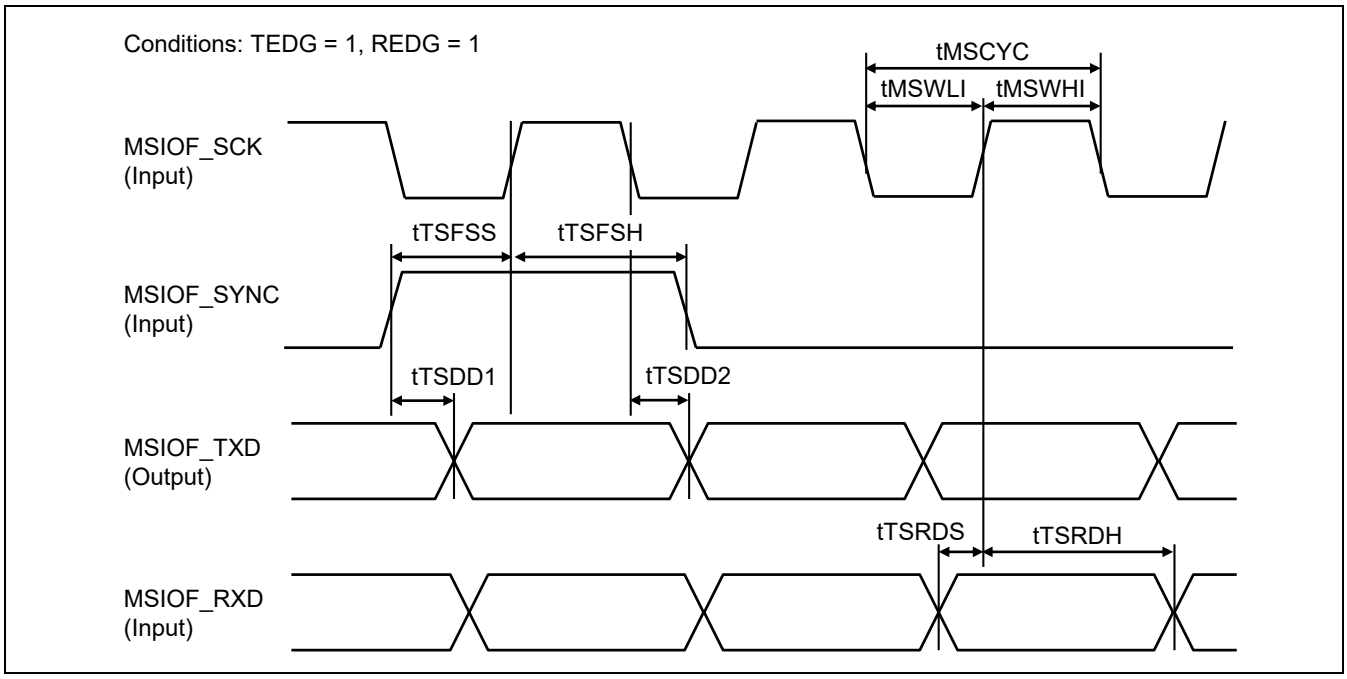


Figure 3.23.4 MSIOF Timing (Slave Mode)

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3.24 RPC Interface

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Table 3.24.1 RPC Timing [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0 and RZ/G2N]

Conditions: VDDQ18 = 1.8V ± 0.1 V, GND = VSS = 0 V,
Tc = −40 to +115 °C [RZ/G2M V1.3], Ta = −40 to + 85 °C [RZ/G2M V3.0, RZ/G2N],
Tj = −40 to + 115 °C [RZ/G2M V3.0, RZ/G2N],
CL = 15 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
SPCLK clock cycle time (HyperFlash)	tSPCYC	6.25	—	—	ns	Figure 3.24.1
SPCLK clock cycle time (QSPI Flash)		12.50	—	—	ns	
SPCLK high pulse width	tSPWH	0.45	—	0.55	tSPCYC	
SPCLK low pulse width	tSPWL	0.45	—	0.55	tSPCYC	
SPCLK rise time	tSPR	—	—	2.0	ns	
SPCLK fall time	tSPF	—	—	2.0	ns	
SPCLK skew	tSPSKEW	—	—	0.04	tSPCYC	
SSL to setup time	tLEAD	1 × tSPCYC – 3	—	8 × tSPCYC + 3	ns	Figure 3.24.2, Figure 3.24.3, Figure 3.24.4
SSL to hold time	tLAG	5.5 × tSPCYC – 3	—	8.5 × tSPCYC + 3	ns	
Data input valid setup time SDR	tVSS	—	—	0.5 × tSPCYC + 3	ns	Figure 3.24.2
Data input valid hold time SDR	tVHS	0	—	—	ns	
Data output setup time	tOS	0.5 × tSPCYC – 2	—	—	ns	
Data output hold time	tOH	0.5 × tSPCYC – 2	—	—	ns	
Data input valid setup time DDR	tVSD	—	—	6.5	ns	Figure 3.24.3
Data input valid hold time DDR	tVHD	0.32 × tSPCYC	—	—	ns	
Data to Data Strobe Skew	tDDSS	-0.65	—	0.65	ns	Figure 3.24.4
SPCLK to Data Strobe Skew	tCDSS	—	—	7.0	ns	
Output Data Setup time in DDR mode	tSDDR	0.25 × tSPCYC – 0.6	—	0.25 × tSPCYC + 0.6	ns	Figure 3.24.3, Figure 3.24.4
Output Data Hold time in DDR mode	tHDDR	0.25 × tSPCYC – 0.6	—	0.25 × tSPCYC + 0.6	ns	
Input Slew rate with Data Strobe usage	tDSISR	0.94	—	—	V/ns	Figure 3.24.5
RPC_RESET assert time	tRPCRA	0	—	—	ns	Figure 3.24.6
RPC_RESET negate time	tRPCRN	10	—	—	ns	Figure 3.24.6

Note: The RZ/G2M V1.3 does not support DDR operation with QSPI (1-/4-bit) and QSPIx2 (8-bit). Therefore, the following DDR related specifications with QSPI and QSPIx2 cannot be applied to the RZ/G2M V1.3.

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Table 3.24.2 RPC Timing [RZ/G2E]

Conditions: VDDQ_QSPI = 1.8V ± 0.1 V, GND = VSS = 0 V,
Ta = −40 to + 85 °C,
Tj = −40 to + 115 °C,
CL = 15 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
SPCLK clock cycle time (HyperFlash)	tSPCYC	6.66	—	—	ns	Figure 3.24.1
SPCLK clock cycle time (QSPI Flash)		12.50	—	—	ns	
SPCLK high pulse width	tSPWH	0.45	—	0.55	tSPCYC	
SPCLK low pulse width	tSPWL	0.45	—	0.55	tSPCYC	
SPCLK rise time	tSPR	—	—	2.0	ns	
SPCLK fall time	tSPF	—	—	2.0	ns	
SPCLK skew	tSPSKEW	—	—	0.04	tSPCYC	
SSL to setup time	tLEAD	1 × tSPCYC – 3	—	8 × tSPCYC + 3	ns	Figure 3.24.2, Figure 3.24.3, Figure 3.24.4
SSL to hold time	tLAG	5.5 × tSPCYC – 3	—	8.5 × tSPCYC + 3	ns	
Data input valid setup time SDR	tVSS	—	—	0.5 × tSPCYC + 3	ns	Figure 3.24.2
Data input valid hold time SDR	tVHS	0	—	—	ns	
Data output setup time	tOS	0.5 × tSPCYC – 2	—	—	ns	
Data output hold time	tOH	0.5 × tSPCYC – 2	—	—	ns	
Data input valid setup time DDR	tVSD	—	—	6.5	ns	Figure 3.24.3
Data input valid hold time DDR	tVHD	0.32 × tSPCYC	—	—	ns	
Data to Data Strobe Skew	tDDSS	-0.65	—	0.65	ns	Figure 3.24.4
SPCLK to Data Strobe Skew	tCDSS	—	—	7.0	ns	
Output Data Setup time in DDR mode	tSDDR	0.25 × tSPCYC – 0.6	—	0.25 × tSPCYC + 0.6	ns	Figure 3.24.3, Figure 3.24.4
Output Data Hold time in DDR mode	tHDDR	0.25 × tSPCYC – 0.6	—	0.25 × tSPCYC + 0.6	ns	
Input Slew rate with Data Strobe usage	tDSISR	0.94	—	—	V/ns	Figure 3.24.5
RPC_RESET assert time	tRPCRA	0	—	—	ns	Figure 3.24.6
RPC_RESET negate time	tRPCRN	10	—	—	ns	Figure 3.24.6

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Table 3.24.3 RPC Timing [RZ/G2E]

Conditions: VDDQ_QSPI = 3.3 V ± 0.3 V, GND = VSS = 0 V, Ta = -40 to +85 °C, Tj = -40 to + 115 °C,
CL = 15 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
SPCLK clock cycle time (HyperFlash)	tSPCYC	10.00	—	—	ns	Figure 3.24.1
SPCLK clock cycle time (QSPI Flash)		12.50	—	—	ns	
SPCLK high pulse width	tSPWH	0.45	—	0.55	tSPCYC	
SPCLK low pulse width	tSPWL	0.45	—	0.55	tSPCYC	
SPCLK rise time	tSPR	—	—	2.0	ns	
SPCLK fall time	tSPF	—	—	2.0	ns	
SPCLK skew	tSPSKEW	—	—	0.04	tSPCYC	
SSL to setup time	tLEAD	1 × tSPCYC – 3	—	8 × tSPCYC + 3	ns	Figure 3.24.2, Figure 3.24.3, Figure 3.24.4
SSL to hold time	tLAG	5.5 × tSPCYC – 3	—	8.5 × tSPCYC + 3	ns	
Data input valid setup time SDR	tVSS	—	—	0.5 × tSPCYC + 3	ns	Figure 3.24.2
Data input valid hold time SDR	tVHS	0	—	—	ns	
Data output setup time	tOS	0.5 × tSPCYC – 2	—	—	ns	
Data output hold time	tOH	0.5 × tSPCYC – 2	—	—	ns	
Data input valid setup time DDR	tVSD	—	—	6.5	ns	Figure 3.24.3
Data input valid hold time DDR	tVHD	0.32 × tSPCYC	—	—	ns	
Data to Data Strobe Skew	tDDSS	-0.65	—	0.65	ns	Figure 3.24.4
SPCLK to Data Strobe Skew	tCDSS	—	—	7.0	ns	
Output Data Setup time in DDR mode	tSDDR	0.25 × tSPCYC – 0.6	—	0.25 × tSPCYC + 0.6	ns	Figure 3.24.3, Figure 3.24.4
Output Data Hold time in DDR mode	tHDDR	0.25 × tSPCYC – 0.6	—	0.25 × tSPCYC + 0.6	ns	
Input Slew rate with Data Strobe usage	tDSISR	0.94	—	—	V/ns	Figure 3.24.5
RPC_RESET assert time	tRPCRA	0	—	—	ns	Figure 3.24.6
RPC_RESET negate time	tRPCRN	10	—	—	ns	Figure 3.24.6

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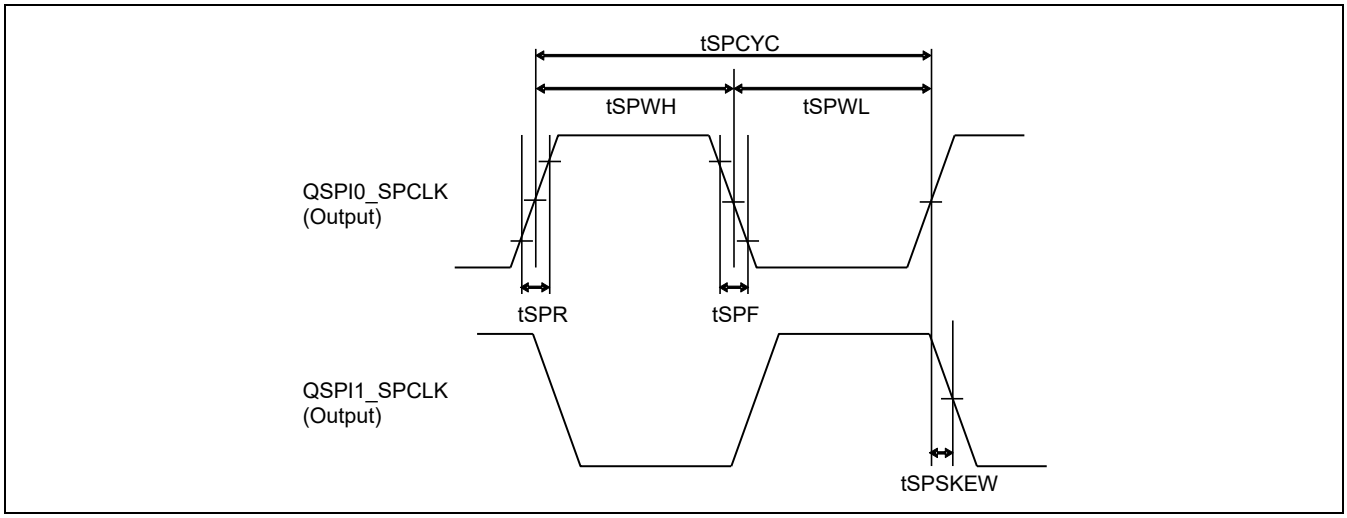
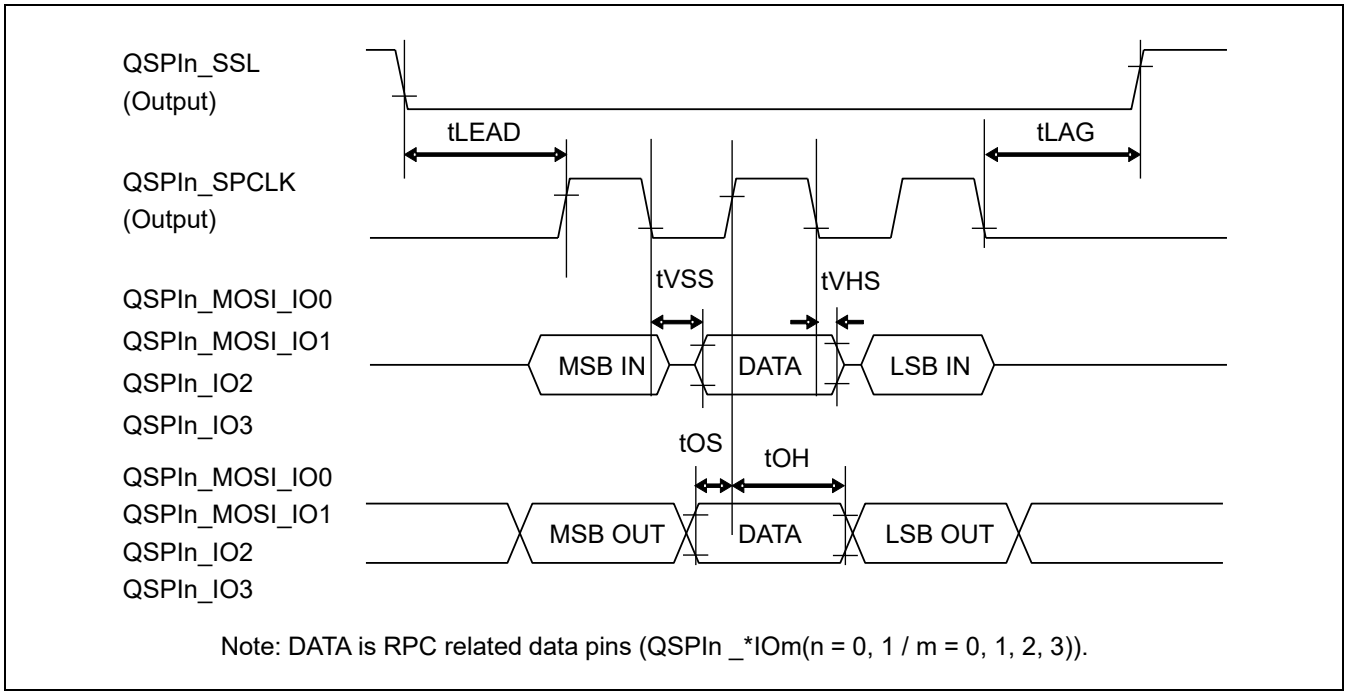


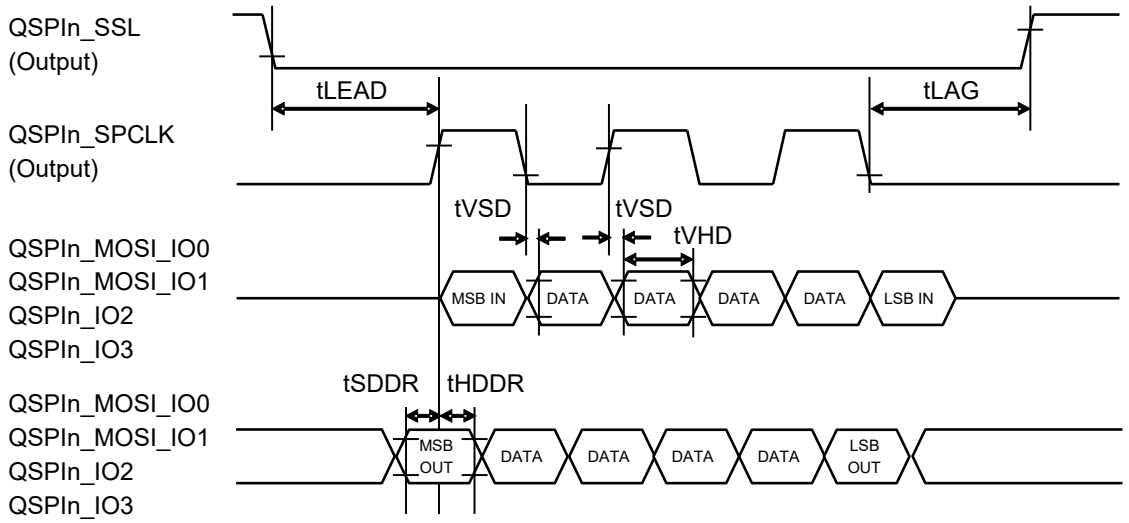
Figure 3.24.1 RPC Clock Timing



Note: DATA is RPC related data pins (QSPIn _*IOm(n = 0, 1 / m = 0, 1, 2, 3)).

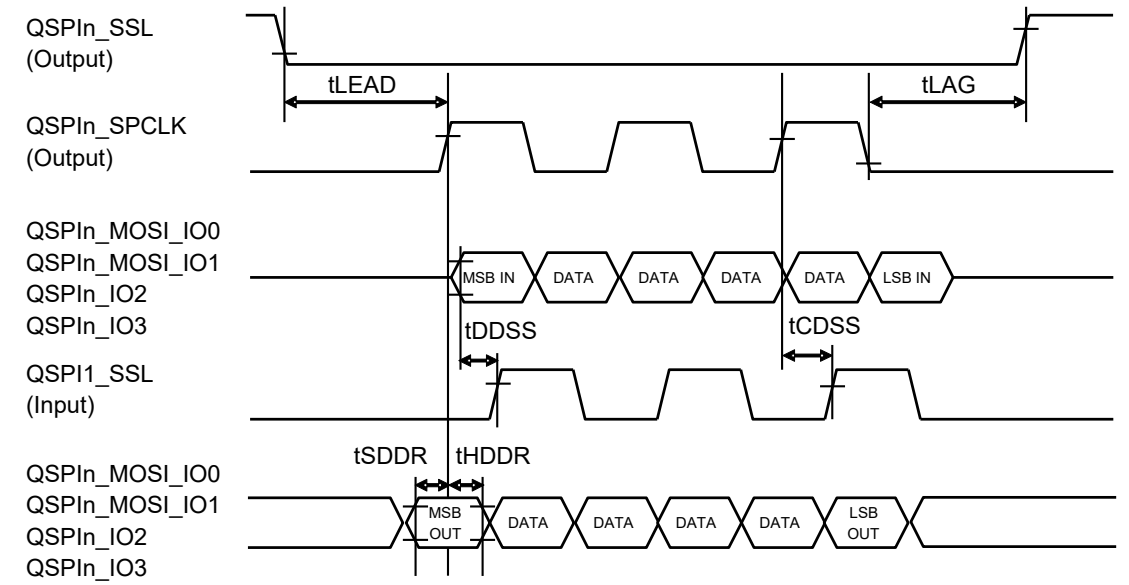
Figure 3.24.2 RPC SDR Operation Timing (QSPI Flash)

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Note: DATA is RPC related data pins (QSPIn_*IOm(n = 0, 1 / m = 0, 1, 2, 3)).

Figure 3.24.3 RPC DDR Operation Timing (QSPI Flash)



Note: DATA is RPC related data pins (QSPIn_*IOm(n = 0, 1 / m = 0, 1, 2, 3)).

Figure 3.24.4 RPC DDR Operation Timing (HyperFlash)

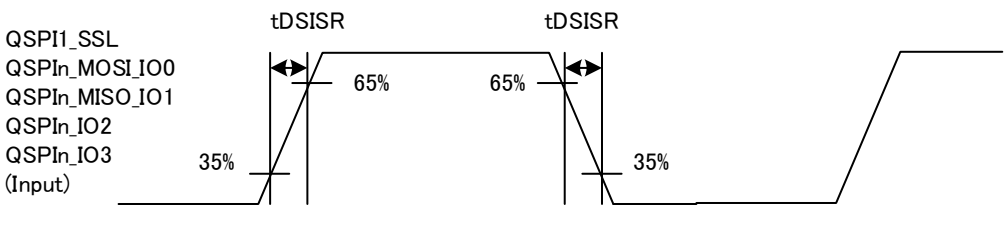


Figure 3.24.5 RPC DDR Operation Timig (Input Slew rate)

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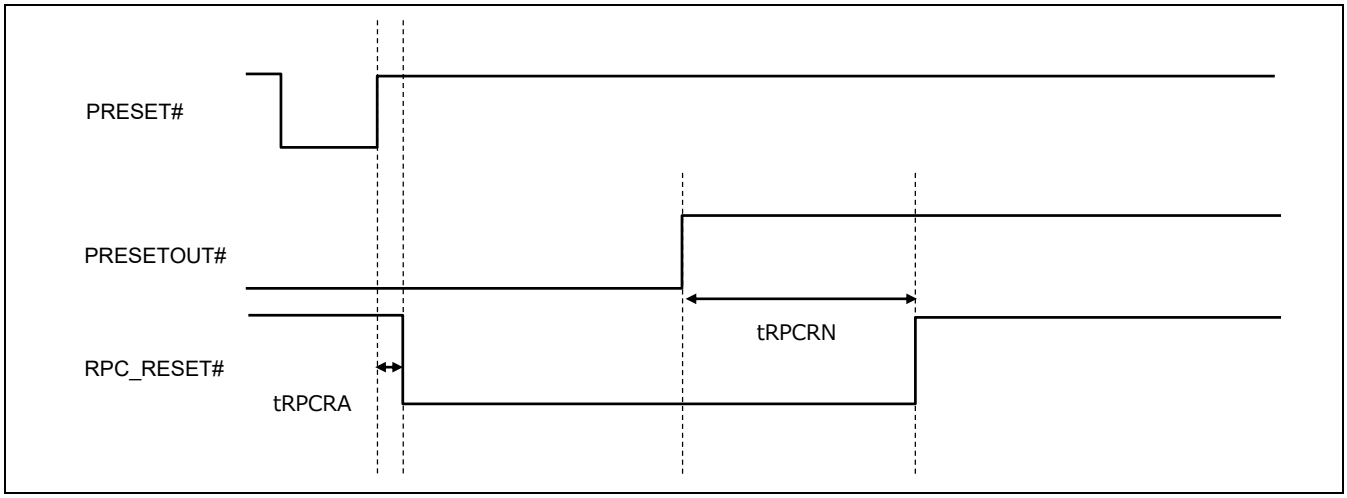


Figure 3.24.6 RPC_RESET# Operation Timing

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3.25 SD Host Interface (SDHI)

RZ/G2H | RZ/G2M V1.3 | RZ/G2M V3.0 | RZ/G2N | RZ/G2E

3.25.1 SDHI (3.3V) Electrical Characteristics

Table 3.25.1 SDHI Signal Timing (Default mode)

Conditions: VDDQVA_SDn (n = 0 to 3) = 3.3 V ± 0.2 V, GND = VSS = 0 V,
Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3], Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N],
VDDQ_SDn (n = 0, 1, 3) = 3.3V ± 0.3 V, GND = VSS = 0 V,
Ta = −40 to + 85 °C [RZ/G2E], Tj = −40 to + 115 °C [RZ/G2E],
CL = 40 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
SDCLK clock cycle time	tSDCYC	40.0	—	—	ns	Figure 3.25.1
SDCMD output data delay time	tSDCMD	—	—	10.0	ns	
	tSDCMDOH	6.0	—	—	ns	
SDDAT output data delay time	tSDDAD	—	—	10.0	ns	
	tSDDADOH	6.0	—	—	ns	
SDCMD input data setup time	tSDCMS	3.0	—	—	ns	
SDCMD input data hold time	tSDCMH	2.0	—	—	ns	
SDDAT input data setup time	tSDDAS	3.0	—	—	ns	
SDDAT input data hold time	tSDDAH	2.0	—	—	ns	

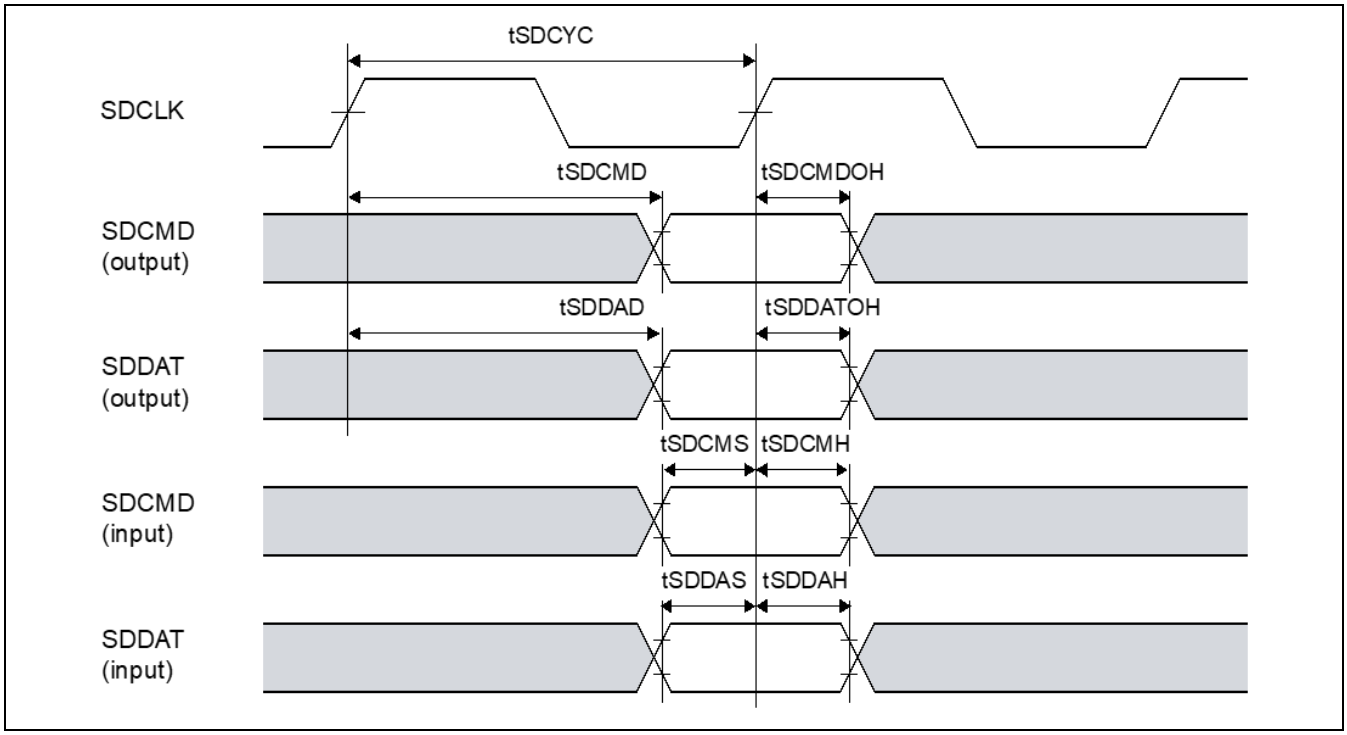


Figure 3.25.1 SDHI Signal Timing (Default mode)

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Table 3.25.2 SDHI Signal Timing (High Speed mode)

Conditions: VDDQVA_SDn (n = 0 to 3) = 3.3 V ± 0.2 V, GND = VSS = 0 V,
Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N], Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N],
VDDQ_SDn (n = 0, 1, 3) = 3.3V ± 0.3 V, GND = VSS = 0 V,
Ta = -40 to +85 °C [RZ/G2E], Tj = -40 to +115 °C [RZ/G2E],
CL = 40 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
SDCLK clock cycle time	t_{SDCYC}	20.0	—	—	ns	Figure 3.25.2
SDCMD output data delay time	t_{SDCMD}	3.0	—	0.5 × t_{SDCYC} + 3.0	ns	
SDCMD output data hold time	$t_{SDCMDOH}$	3.0	—	—	ns	
SDDAT output data delay time	t_{SDDAD}	3.0	—	0.5 × t_{SDCYC} + 3.0	ns	
SDDAT output data hold time	$t_{SDDATOH}$	3.0	—	—	ns	
SDCMD input data setup time	t_{SDCMS}	3.0	—	—	ns	
SDCMD input data hold time	t_{SDCMH}	2.0	—	—	ns	
SDDAT input data setup time	t_{SDDAS}	3.0	—	—	ns	
SDDAT input data hold time	t_{SDDAH}	2.0	—	—	ns	

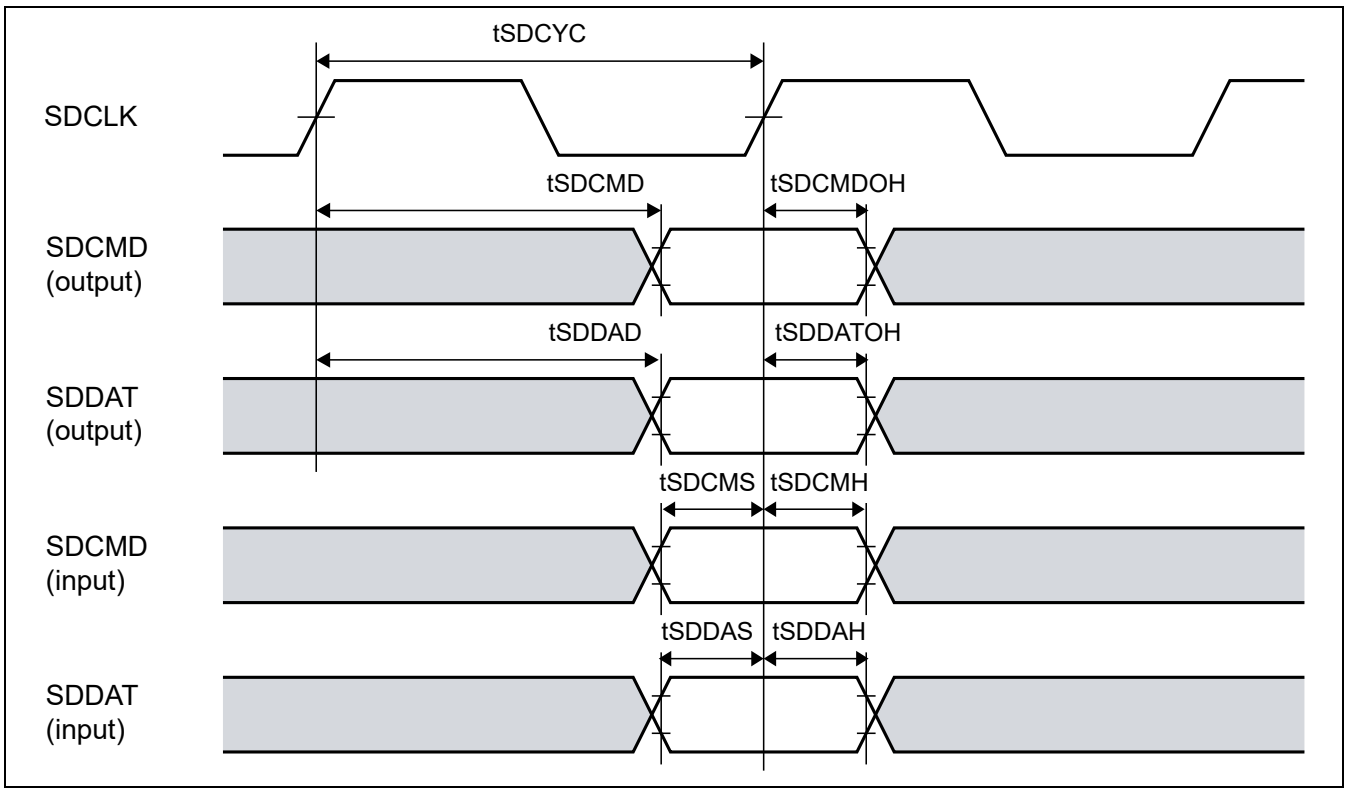


Figure 3.25.2 SDHI Signal Timing (High Speed mode)

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3.25.2 SDHI (1.8V) Electrical Characteristics

Table 3.25.3 SDHI Signal Timing (SDR50 mode)

Conditions: VDDQVA_SDn (n = 0 to 3) = 1.8 V ± 0.1 V, GND = VSS = 0 V,
Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N], Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N],
VDDQ_SDn (n = 0, 1, 3) = 1.8V ± 0.1 V, GND = VSS = 0 V,
Ta = -40 to +85 °C [RZ/G2E], Tj = -40 to +115 °C [RZ/G2E],
CL = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
SDCLK clock cycle time	t_{SDCYC}	10.0	—	—	ns	Figure 3.25.3
SDCMD output data delay time	t_{SDCMD}	1.3	—	t_{SDCYC} – 4	ns	
SDDAT output data delay time	t_{SDDAD}	1.3	—	t_{SDCYC} – 4	ns	
SDCMD input data setup time	t_{SDCMS}	2.0	—	—	ns	
SDCMD input data hold time	t_{SDCMH}	1.5	—	—	ns	
SDDAT input data setup time	t_{SDDAS}	2.0	—	—	ns	
SDDAT input data hold time	t_{SDDAH}	1.5	—	—	ns	

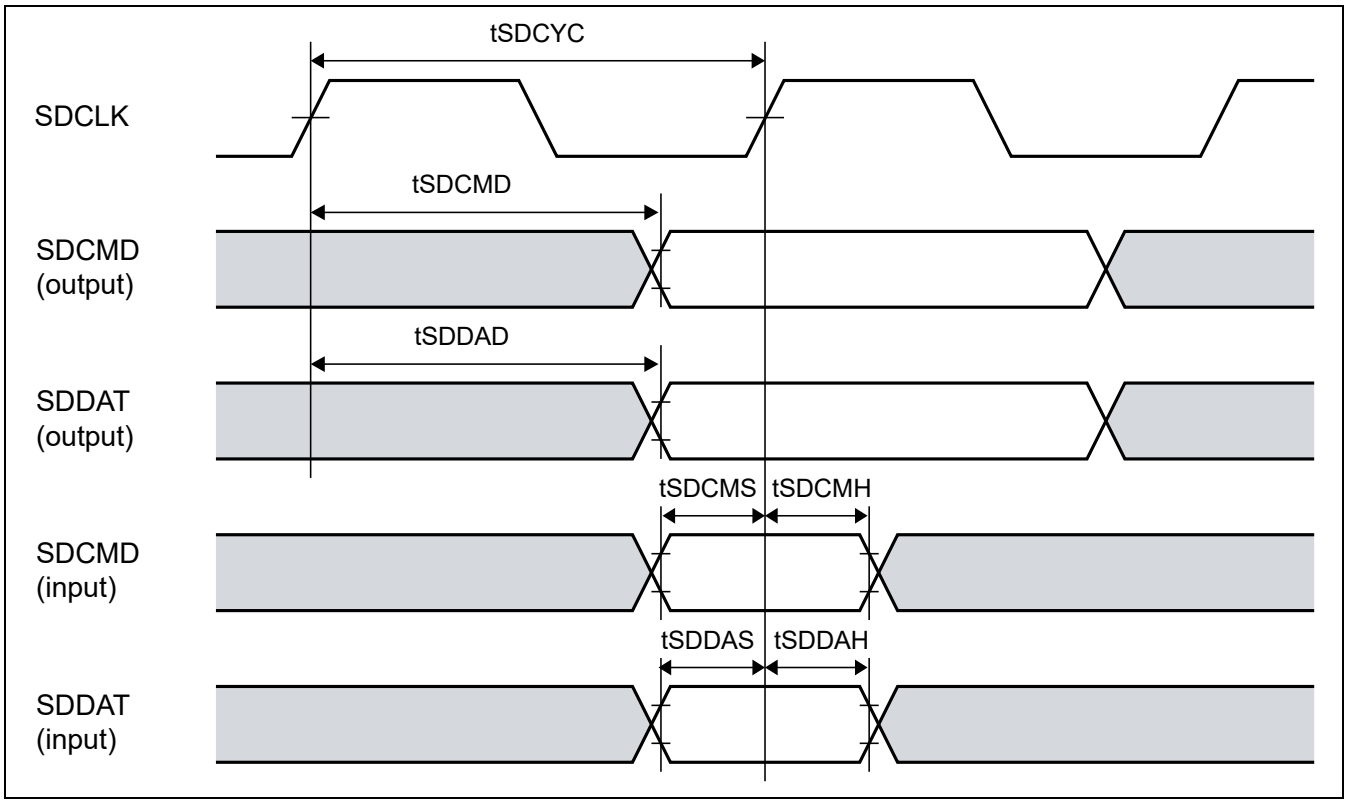


Figure 3.25.3 SDHI Signal Timing (SDR50 mode)

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Table 3.25.4 SDHI Signal Timing (SDR104 mode)

Conditions: VDDQVA_SDn (n = 0 to 3) = 1.8 V ± 0.1 V, GND = VSS = 0 V,
Tc = −20 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -20 to +85 °C [RZ/G2M V3.0, RZ/G2N], Tj = -20 to +115 °C [RZ/G2M V3.0, RZ/G2N]
VDDQ_SDn (n = 0, 1, 3) = 1.8V ± 0.1 V, GND = VSS = 0 V,
Ta = -40 to +85 °C [RZ/G2E], Tj = -40 to +115 °C [RZ/G2E], CL = 10 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
SDCLK clock cycle time	tSDCYC	5.0	—	—	ns	Figure 3.25.4
SDCMD output data delay time	tSDCMD	1.30	—	3.50	ns	
SDDAT output data delay time	tSDDAD	1.30	—	3.50	ns	
SDCMD input data width (for tuning)	tSDICW	2.57	3.07	—	ns	
(after tuning)		2.57	—	—	ns	
SDDAT input data width (for tuning)	tSDIDW	2.57	3.07	—	ns	
(after tuning)		2.57	—	—	ns	

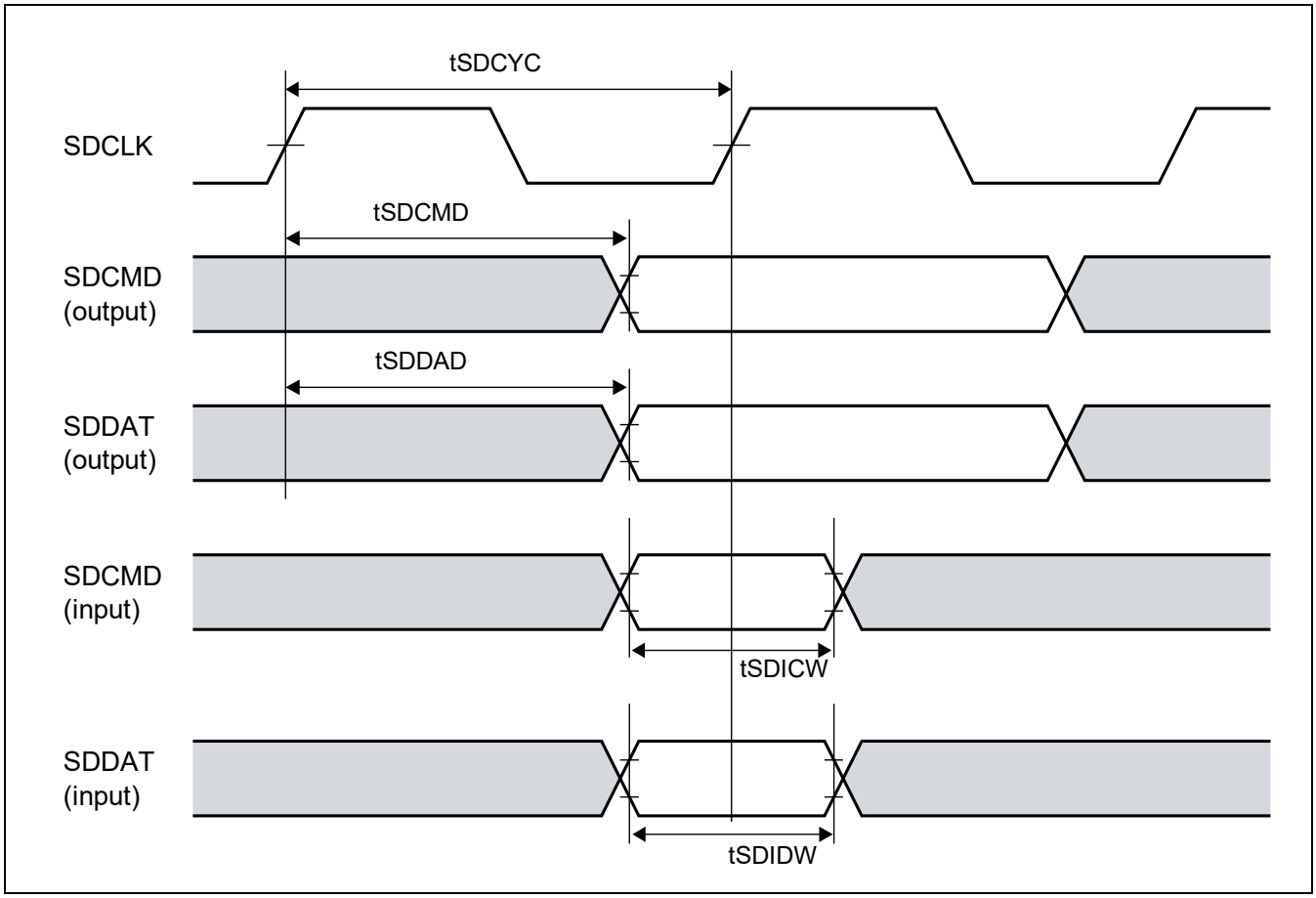


Figure 3.25.4 SDHI Signal Timing (SDR104 mode)

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3.26 MMC Interface

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

3.26.1 MMC (3.3V) Electrical Characteristics [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N and RZ/G2E]

Table 3.26.1 MMC Signal Timing (High Speed mode)

Conditions: VDDQVA_SDn (n = 2, 3) = 3.3 V ± 0.2 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N],
VDDQ_SD3 = 3.3 V ± 0.3 V [RZ/G2E], GND = VSS = 0 V,
Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3], Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E], CL = 40 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
MMCCLK clock cycle time	tMMCCYC	20.0	—	—	ns	Figure 3.26.1
MMCCMD output data delay time	tMMCCMD	3.0	—	0.5 ×tMMCCYC + 3.0	ns	
MMCCMD output data hold time	tMMCCMDOH	3.0	—	—	ns	
MMCDAT output data delay time	tMMCDAD	3.0	—	0.5 ×tMMCCYC + 3.0	ns	
MMCDAT output data hold time	tMMCDATOH	3.0	—	—	ns	
MMCCMD input data setup time	tMMCCMS	3.0	—	—	ns	
MMCCMD input data hold time	tMMCCMH	2.0	—	—	ns	
MMCDAT input data setup time	tMMCDAS	3.0	—	—	ns	
MMCDAT input data hold time	tMMCDAH	2.0	—	—	ns	

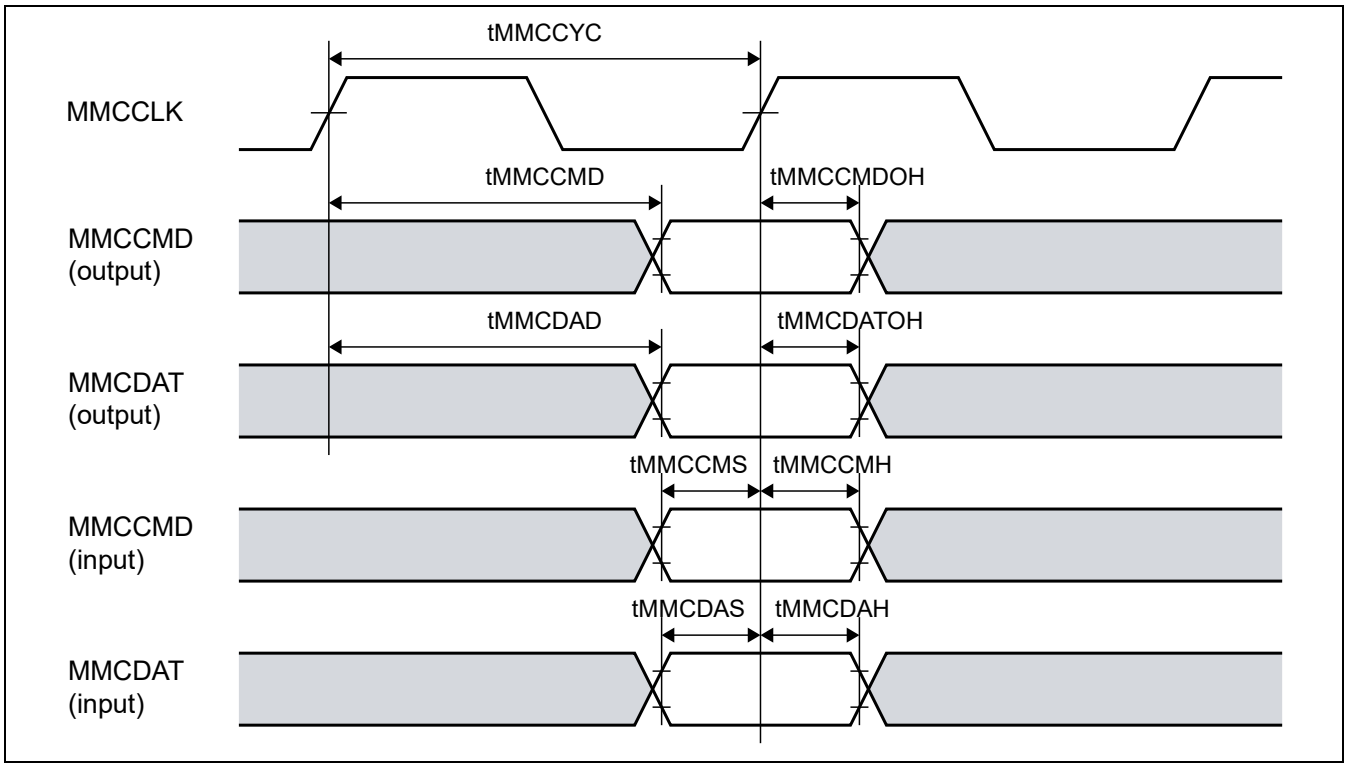


Figure 3.26.1 MMC Signal Timing (High Speed mode)

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3.26.2 MMC (1.8V) Electrical Characteristics [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N and RZ/G2E]

Table 3.26.2 MMC Signal Timing (High Speed mode)

Conditions: VDDQVA_SDn (n = 2, 3) = 1.8 V ± 0.1 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N],
VDDQ_SD3 = 1.8 V ± 0.1 V [RZ/G2E], GND = VSS = 0 V,
Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
CL = 30 pF [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N and RZ/G2E],
GND = VSS = 0 V

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
MMCCLK clock cycle time	t_{MMCCYC}	20.0	—	—	ns	Figure 3.26.2
MMCCMD output data delay time	t_{MMCCMD}	3.0	—	0.5 × t_{MMCCYC} + 3.0	ns	
MMCCMD output data hold time	$t_{MMCCMDOH}$	3.0	—	—	ns	
MMCDAT output data delay time	t_{MMCDAD}	3.0	—	0.5 × t_{MMCCYC} + 3.0	ns	
MMCDAT output data hold time	$t_{MMCDATOH}$	3.0	—	—	ns	
MMCCMD input data setup time	t_{MMCCMS}	3.0	—	—	ns	
MMCCMD input data hold time	t_{MMCCMH}	2.0	—	—	ns	
MMCDAT input data setup time	t_{MMCDAS}	3.0	—	—	ns	
MMCDAT input data hold time	t_{MMCDAH}	2.0	—	—	ns	

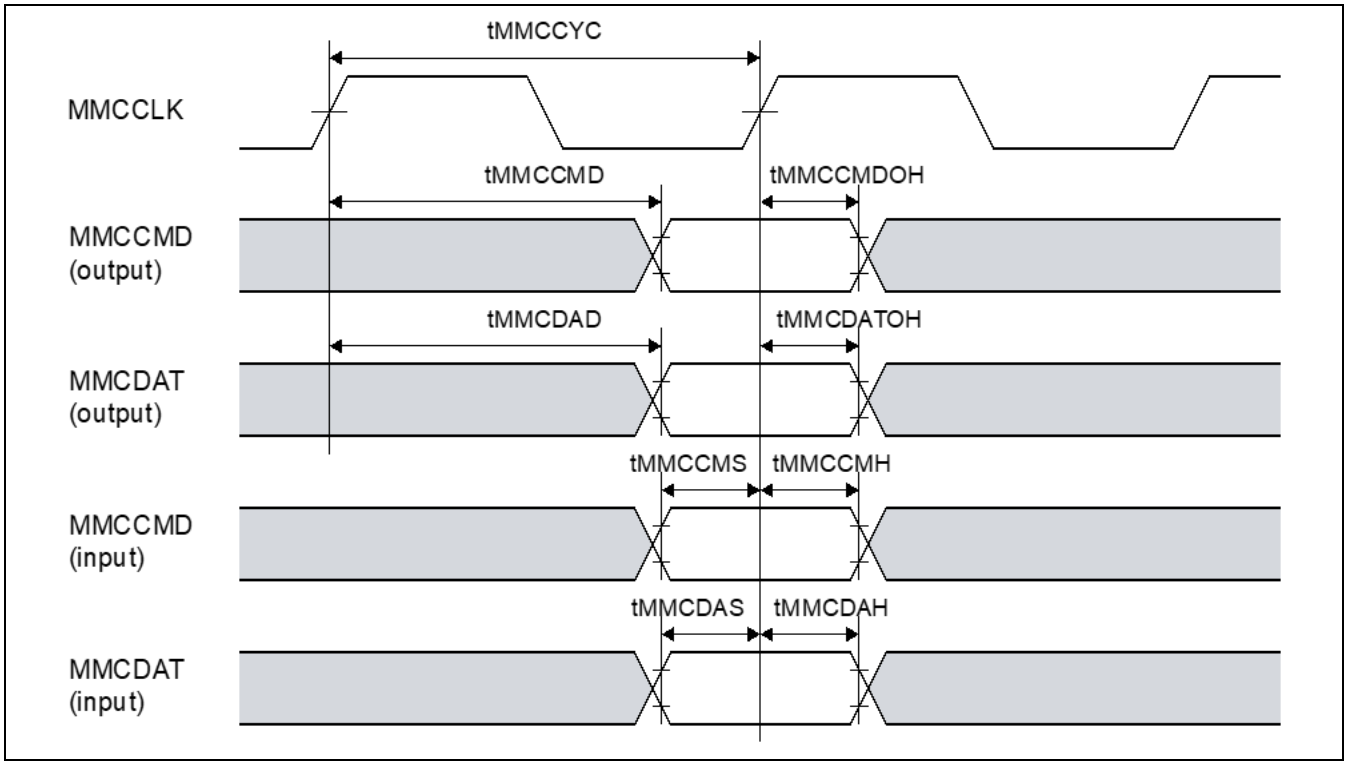


Figure 3.26.2 MMC Signal Timing

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Table 3.26.3 MMC Signal Timing (HS200 mode) [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N and RZ/G2E]

Conditions: VDDQVA_SDn (n = 2, 3) = 1.8 V ± 0.1 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N],
VDDQ_SD3 = 1.8 V ± 0.1 V [RZ/G2E], GND = VSS = 0 V,
Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
CL = 10 pF [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N and RZ/G2E],
GND = VSS = 0 V

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
MMCCLK clock cycle time	tMMCCYC	5.0	—	—	ns	Figure 3.26.3
MMCCMD output data delay time	tMMCCMD	1.30	—	3.40	ns	
MMCDAT output data delay time	tMMCDAD	1.30	—	3.40	ns	
MMCCMD input data width (for tuning)	tMMCICW	2.57	3.07	—	ns	
(after tuning)		2.57	—	—		
MMCDAT input data width (for tuning)	tMMCIDW	2.57	3.07	—	ns	
(after tuning)		2.57	—	—		

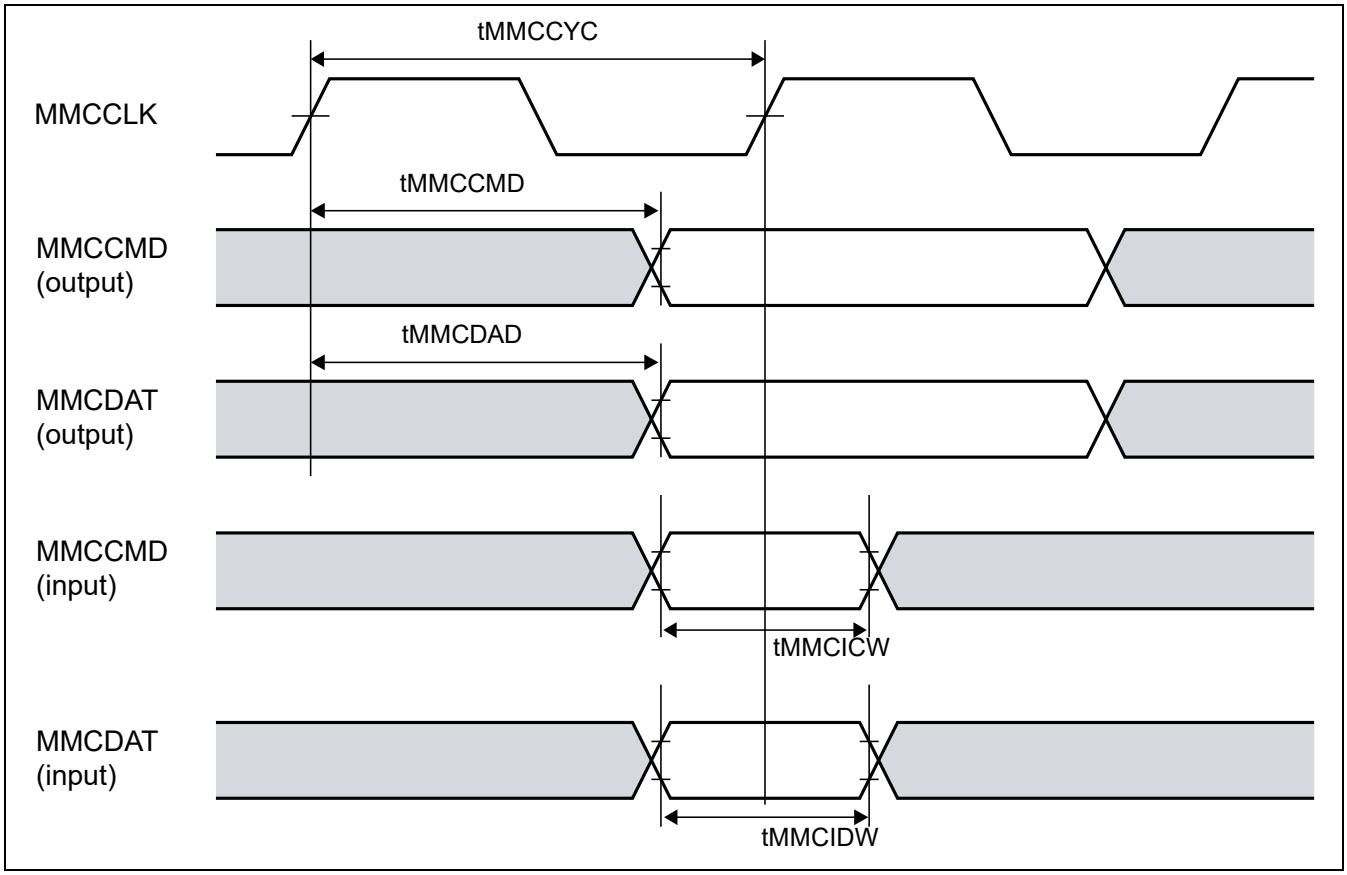


Figure 3.26.3 MMC Signal Timing (HS200 mode)

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Table 3.26.4 MMC Signal Timing (HS400 mode) [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N and RZ/G2E]

Conditions: VDDQVA_SDn (n = 2, 3) = 1.8 V ± 0.1 V[RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N],
VDDQ_SD3 = 1.8 V ± 0.1 V [RZ/G2E], GND = VSS = 0 V,
Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E], CL = 10 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks	Figures
MMCCLK clock cycle time	tMMCCYC	5.0	—	—	ns		Figure 3.26.4
MMCDS data strobe cycle time	tMMCDCYC	5.0	—	—	ns		
MMCDS minimum pulse with	tDSW	2.0	—	—	ns		
Input Slew rate with MMCDS/MMCDAT	tDSISR	1.125	—	—	V/ns		Figure 3.26.5
MMCDAT input data setup time	tMMCDIDS	—	—	0.6	ns	eMMC0-1 [RZ/G2H, RZ/G2M V3.0, RZ/G2N, RZ/G2E] eMMC0 [RZ/G2M V1.3]	Figure 3.26.4
				0.5	ns	eMMC1 [RZ/G2M V1.3]	
MMCDAT input data hold time	tMMCDIDH	0.5 × tMMCCYC – 1.0	—	—	ns		
MMCDAT output data setup time	tMMCDWDS	0.6	—	—	ns		
MMCDAT output data hold time	tMMCDWDH	0.6	—	—	ns		

The MMCCMD input timing for HS400 mode is the same as CMD timing for HS200 mode.

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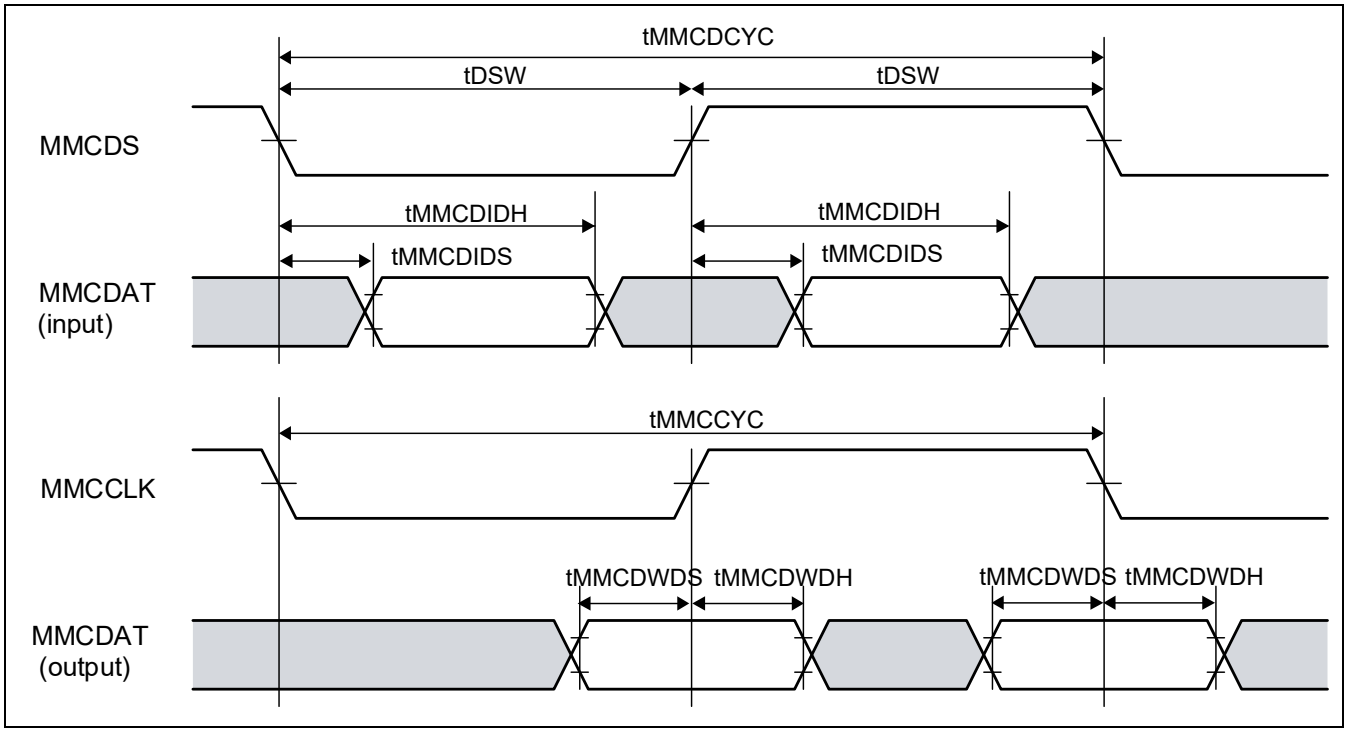


Figure 3.26.4 MMC Signal Timing (HS400 mode)

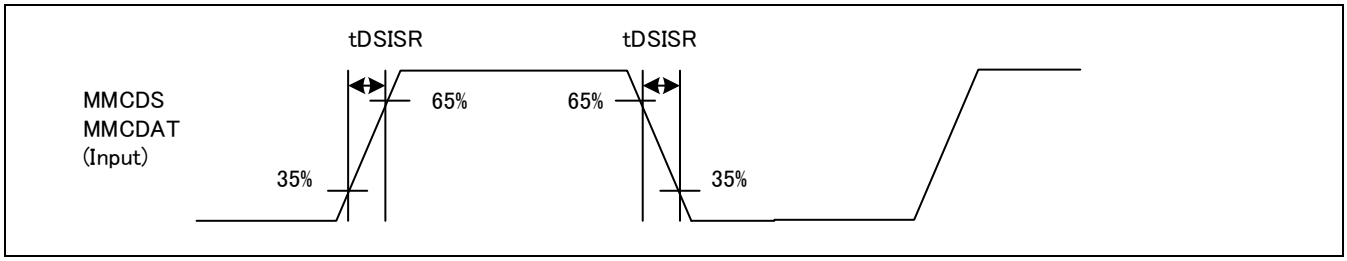


Figure 3.26.5 MMC Operation Timing (HS400 mode) (Input Slew rate)

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3.27 Serial ATA (Gen3)

RZ/G2H
RZ/G2M V1.3 RZ/G2M V3.0
RZ/G2N RZ/G2E

The description in this section is compliant with the following Serial ATA standard: 'Serial ATA International Organization: Serial ATA Revision 3.2, August 7, 2013'.

Table 3.27.1 Serial ATA (Gen3) Interface Characteristics [RZ/G2H, RZ/G2N]

Conditions: VDD33_SATA = VDD33_PCIE = 3.3 ± 0.3 V, VDD09_SATA = VDD09_PCIE = 0.82 -0.07 V / + 0.06 V, GND = 0 V, Tc = -40 to +115 °C [RZ/G2H], Ta = -40 to +85 °C [RZ/G2N], Tj = -40 to +115 °C [RZ/G2N]

Test Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
RX Differential Input Voltage (Gen1i)	Vdiff RX	325	—	600	mVppd	*1
RX Differential Input Voltage (Gen2i)	Vdiff RX	275	—	750	mVppd	*1
RX Differential Input Voltage (Gen3i)	Vdiff RX	200	—	900	mVppd	*1
TX Differential Output Voltage (Gen1i)	Vdiff TX	400	—	600	mVppd	*2
TX Differential Output Voltage (Gen2i)	Vdiff TX	400	—	700	mVppd	*2
TX Differential Output Voltage (Gen3i)	Vdiff TX	240	—	1000	mVppd	*2
DC Coupled Common Mode Voltage (Gen1i)	Vcm dc	200	—	450	mV	*2
Unit Interval (Gen1i)	TUI	666.4333	666.6667	670.2333	ps	*3
Unit Interval (Gen2i)	TUI	333.2167	333.3333	335.1167	ps	*3
Unit Interval (Gen3i)	TUI	166.6083	166.6667	167.5583	ps	*3
COMRESET Transmit Gap Length (Gen1i and Gen2i and Gen3i)	TScomreset	—	480	—	UIOOB	*4
COMWAKE Transmit Gap Length (Gen1i and Gen2i and Gen3i)	TScomwake	—	160	—	UIOOB	*4
TX Differential Impedance (Gen1i)	ZdiffTX	85	—	115	Ω	*2
TX Single-Ended Impedance (Gen1i)	Zs-eTX	40	—	—	Ω	*2
RX Differential Impedance (Gen1i)	ZdiffRX	85	—	115	Ω	*1
RX Single-Ended Impedance (Gen1i)	Zs-eRX	40	—	—	Ω	*1

Notes: 1. RXP, RXN: DC test
2. TXP, TXN: DC test
3. Need Reference Clock (Low Voltage Swing, Differential Clocks). The nominal single-ended swing for each clock is 0 to 0.7 V and a nominal frequency of 100 MHz ± 100 PPM.
4 TXP, TXN: UIOOB (UI During OOB Signaling) = 646.67 to 686.67 ps, Not tested.

Table 3.27.2 Serial ATA (Gen3) External Clock Accuracy

Conditions: VDD09_PCIE = 0.82 V – 0.07 V / + 0.06 V, GND = 0 V, Tc = −40 to +115 °C [RZ/G2H], Ta = -40 to +85 °C [RZ/G2N], Tj = -40 to +115 °C [RZ/G2N]

Test Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
External clock accuracy (PCIE1_CLK_P, PCIE1_CLK_M)	—	—	100.000	—	MHz	Frequency accuracy: ±100 ppm or less

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3.28 USB Signal Timing

RZ/G2H | RZ/G2M V1.3 | RZ/G2M V3.0 | RZ/G2N | RZ/G2E

The descriptions in this section are compliant with the following USB 2.0 standards: "Universal Serial Bus Specification Revision 2.0" and "On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification".

Table 3.28.1 USB High-speed Signal Timing

Conditions: VDDQ33 = VDDQ33_USB2* = 3.3 ± 0.2 V, VDDQ18 = 1.8 ± 0.1 V, VDD09_USB2* = 0.82 – 0.07 V / + 0.06 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N], VDDQ33 = VDDQ33_USB2* = 3.3 ± 0.3 V, VDDQ18 = VDDQ18_USB20 = 1.8 ± 0.1 V [RZ/G2E], VSS = 0 V,
Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E]

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
High-speed data rate	THSDRAT	479.76	480	480.24	Mb/s	—

Table 3.28.2 USB Low-/full-speed Signal Timing

Conditions: VDDQ33 = VDDQ33_USB2* = 3.3 ± 0.2 V, VDDQ18 = 1.8 ± 0.1 V, VDD09_USB2* = 0.82 - 0.07 V / + 0.06 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N],
VDDQ33 = VDDQ33_USB2* = 3.3 ± 0.3 V, VDDQ18 = VDDQ18_USB20 = 1.8 ± 0.1 V [RZ/G2E],
VSS = 0 V,
Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E], CL = 50 pF

Item		Symbol	Min.	Typ.	Max.	Unit	Figures
Low-speed*	Rise time	tR	75	—	300	ns	Figure 3.28.1
	Fall time	tF	75	—	300	ns	
	Differential Rise and Fall Time Matching (tR/tF)	tRFM1	80	—	125	%	
Full-speed	Rise time	tR	4	—	20	ns	
	Fall time	tF	4	—	20	ns	
	Differential Rise and Fall Time Matching (tR/tF)	tRFM	90	—	111.11	%	

Note: * The USB 2.0 Function module does not support Low-speed.

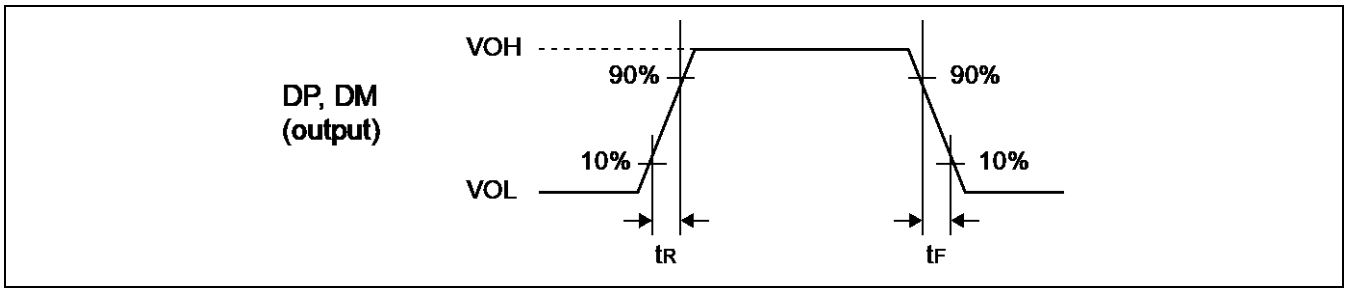


Figure 3.28.1 USB Low-/full-speed Signal Timing

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Table 3.28.3 USB 2.0 External Clock Accuracy

Conditions: VDDQ18 = 1.8 V ± 0.1V,
VSS = 0 V,
Tc = −40 to +115°C [RZ/G2H, RZ/G2M V1.3], Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E]

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
External clock accuracy (USB_XTAL, USB_EXTAL)	—	—	50.000	—	MHz	Frequency deviation: ±100 ppm or less

Note: USB2.0 External Clock is not supported RZ/G2E.

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3.29 USB 3.0 (Super-Speed)

RZ/G2H | RZ/G2M V1.3 | RZ/G2M V3.0 | RZ/G2N | RZ/G2E

The description in this section is compliant with the following USB 3.0 standard: 'Universal Serial Bus 3.0 Specification Revision 1.0, Jun 6, 2011'.

Table 3.29.1 USB 3.0 (Super-Speed 5 GT/s) Interface Characteristics

Conditions: VDDQ33_USB3* = 3.3 ± 0.2 V, VDD09_USB3* = 0.82 V – 0.07 V / + 0.06 V, VSS = 0 V,
[RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N],
Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3], Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N]
VDDQ18_USB30 = 1.8 ± 0.1 V, VDDD_USB30 = 1.03 ± 0.05 V
Ta = −40 to +85 °C , Tj = −40 to + 115 °C [RZ/G2E]

Test Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Differential Rx peak to peak voltage	$V_{RX-DIFFp-p}$	0.030	—	—	V	*1
Differential p-p Tx voltage swing	$V_{TX-DIFFp-p}$	0.8	—	1.2	V	*2
Absolute DC Common Mode Voltage between U1 and U0	$V_{TX-CM-DC-ACTIVEIDLE-DELTA}$	—	—	200	mV	*2
Unit Interval	UI	199.94	—	200.06	ps	*3
DC Differential TX Impedance	$R_{TX-DIFF-DC}$	72	—	120	Ω	—
DC Differential Input Impedance	$R_{RX-DIFF-DC}$	72	—	120	Ω	—
DC Input Impedance {DC common mode impedance}	ZRX-DC {R_{TX-DC}, R_{RX-DC}}	36 {18}	— {—}	60 {30}	Ω {Ω}	—

Notes: 1. RXP, RXN: DC test
2. TXP, TXN: DC test
3. Need Reference Clock (Low Voltage Swing, Differential Clocks). The nominal single-ended swing for each clock is 0 to 0.7 V and a nominal frequency of 100 MHz ±100 PPM.

Table 3.29.2 USB 3.0 (Super-Speed 5 GT/s) External Clock Accuracy

Conditions: VDD09_USB30 = 0.82 V – 0.07 V / + 0.06 V,
VDDQ18_USB30 = 1.8 V ± 0.1 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
VDDQ18_USB30 = 1.8 V ± 0.1 V, VDDD_USB30 = 1.03 ± 0.05 V [RZ/G2E], VSS = 0 V,
Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E]

Test Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
External clock accuracy (USB_XTAL, USB_EXTAL) *	—	—	50.000	—	MHz	Frequency accuracy: ±100 ppm or less
External clock accuracy (USB_3S0_CLK_P,USB_3S0_CLK_M)	—	—	100.000	—	MHz	

Notes: For details about selecting clock sources, refer to Figure 63.1 in User's Manual (Page. 63-1)
* Except for RZ/G2E

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3.30 TMU

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Table 3.30.1 TMU Signal Timing

Conditions: VDDQ33 = 3.3 V ± 0.2 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]/± 0.3 V [RZ/G2E],
GND = VSS = 0 V,
Tc = -40 to +115 °C [RZ/G2H, RZ/G2M V1.3], Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E]

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
TCLK clock cycle	tTCLKCY	4	—	16.37	tCYC	Figure 3.30.1
Input clock pulse width	tTCLKW	0.4	—	0.6	tTCLKCY	

Note: RZ/G2H, RZ/G2M V1.3,RZ/G2M V3.0, RZ/G2N, RZ/G2E: tCYC is for one cycle of the S3D2ϕ clock.

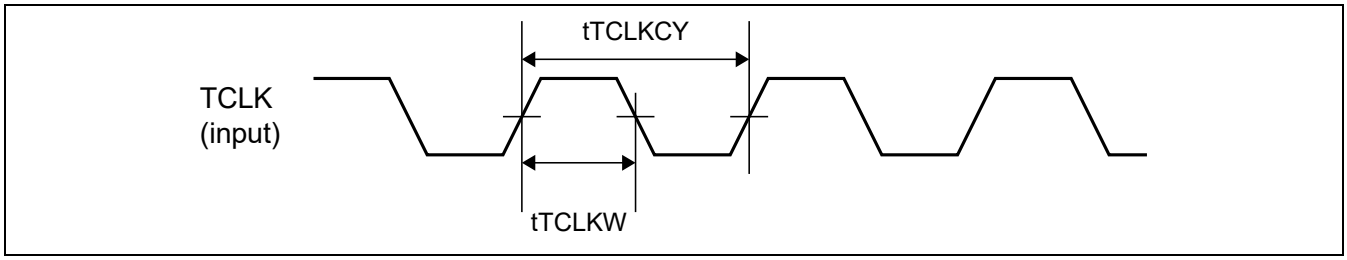


Figure 3.30.1 TMU Signal Timing

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3.31 R-NANDC

RZ/G2H
RZ/G2M V1.3 RZ/G2M V3.0
RZ/G2N RZ/G2E

Table 3.31.1 R-NANDC Timing [RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

Conditions: VDDQ33 = VDDQVA_SDn = 3.3 ± 0.2 V, GND = VSS = 0 V, Tc = -40 to +115 °C[RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N], Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N], CL = 50 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
Output signal delay	tOD	0	—	3.7	ns	Figure 3.31.1
rise-fall delay delta of each output signals	tRFD	0	—	2.7	ns	—
Read data setup time from NFRE# rise	tSD	10	—	—	ns	Figure 3.31.1
Read data hold time from NFRE# rise	tHD	0	—	—	ns	
Read data setup time from NFRE# rise (fast mode)	tSD	10-tpcyc *1	—	—	ns	
Read data hold time from NFRE# rise (fast mode)	tHD	tpcyc *1	—	—	ns	
NFWE# rise to NFRB# fall	tWB	(N+1) × tpcyc – 8 *1 *2	—	—	ns	
Ready to RE# low	tRR	(M+1) × tpcyc + 0 *1 *3	—	—	ns	

Notes: 1. tpcyc is a cycle time of S3D1ϕ
2. N is value of TIME_SEQ_1.TWB bit
3. M is value of TIME_SEQ_1.TRR bit

Table 3.31.2 R-NANDC Timing [RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

Conditions: VDDQ18 = 1.8 ± 0.1 V, GND = VSS = 0 V, Tc = -40 to +115 °C [RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N], CL = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
Output signal delay	tOD	0	—	3	ns	Figure 3.31.1
rise-fall delay delta of each output signals	tRFD	0	—	1.9	ns	—
Read data setup time from NFRE# rise	tSD	8.5	—	—	ns	Figure 3.31.1
Read data hold time from NFRE# rise	tHD	0	—	—	ns	
Read data setup time from NFRE# rise (fast mode)	tSD	8.5 – tpcyc *1	—	—	ns	
Read data hold time from NFRE# rise (fast mode)	tHD	tpcyc *1	—	—	ns	
NFWE# rise to NFRB# fall	tWB	(N+1) × tpcyc – 8 *1 *2	—	—	ns	
Ready to RE# low	tRR	(M+1) × tpcyc + 0 *1 *3	—	—	ns	

Notes: 1. tpcyc is a cycle time of S3D1ϕ
2. N is value of TIME_SEQ_1.TWB bit
3. M is value of TIME_SEQ_1.TRR bit

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Table 3.31.3 R-NANDC Timing [RZ/G2E]

Conditions: VDDQ33 = VDDQ_MMC = 3.3 ± 0.3 V, GND = VSS = 0 V, Ta = -40 to +85 °C, Tj = -40 to +115 °C, CL = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
Output signal delay	tOD	0	—	2.2	ns	Figure 3.31.1
rise-fall delay delta of each output signals	tRFD	0	—	1	ns	—
Read data setup time from NFRE# rise	tSD	8.75	—	—	ns	Figure 3.31.1
Read data hold time from NFRE# rise	tHD	0	—	—	ns	
Read data setup time from NFRE# rise (fast mode)	tSD	8.75 – tpcyc *1	—	—	ns	
Read data hold time from NFRE# rise (fast mode)	tHD	tpcyc *1	—	—	ns	
NFWE# rise to NFRB# fall	tWB	(N+1) × tpcyc – 8 *1 *2	—	—	ns	
Ready to RE# low	tRR	(M+1) × tpcyc + 0 *1 *3	—	—	ns	

Notes: 1. tpcyc is a cycle time of S3D1Cϕ
2. N is value of TIME_SEQ_1.TWB bit
3. M is value of TIME_SEQ_1.TRR bit

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Table 3.31.4 R-NANDC Timing [RZ/G2E]

Conditions: VDDQ18 = VDDQ_MMC = 1.8 ± 0.1 V, GND = VSS = 0 V, Ta = -40 to +85 °C, Tj = -40 to +115 °C, CL = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
Output signal delay	tOD	0	—	2.2	ns	Figure 3.31.1
rise-fall delay delta of each output signals	tRFD	0	—	1	ns	—
Read data setup time from NFRE# rise	tSD	8.75	—	—	ns	Figure 3.31.1
Read data hold time from NFRE# rise	tHD	0	—	—	ns	
Read data setup time from NFRE# rise (fast mode)	tSD	8.75 – tpcyc *1	—	—	ns	
Read data hold time from NFRE# rise (fast mode)	tHD	tpcyc *1	—	—	ns	
NFWE# rise to NFRB# fall	tWB	(N+1) × tpcyc – 8 *1 *2	—	—	ns	
Ready to RE# low	tRR	(M+1) × tpcyc + 0 *1 *3	—	—	ns	

Notes: 1. tpcyc is a cycle time of S3D1Cϕ
2. N is value of TIME_SEQ_1.TWB bit
3. M is value of TIME_SEQ_1.TRR bit

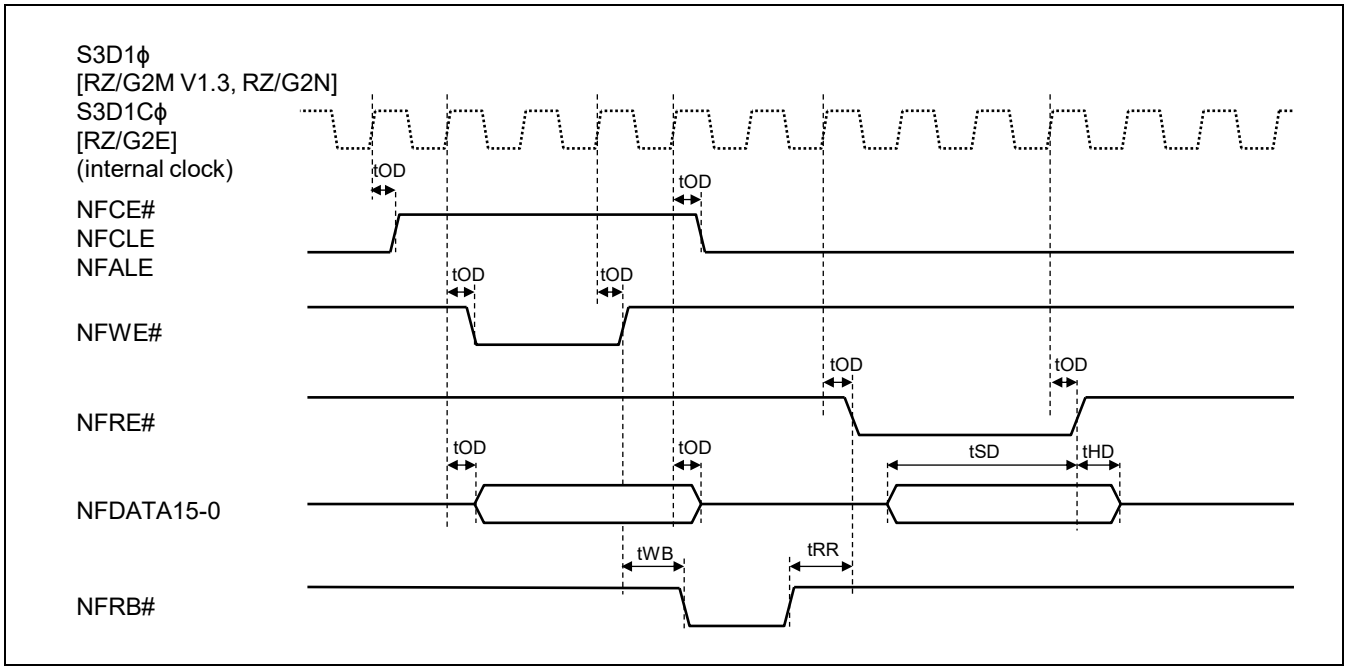


Figure 3.31.1 Input/output Timing in Synchronous Mode

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3.32 DBSC4 Access Timing

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Table 3.32.1 DBSC4 Access Timing (DDR3L) [RZ/G2E]

Conditions for DDR3L: VDDQ_DDR = 1.35 V + 0.100/-0.067 V, GND = VSS = 0 V, Ta = -40 to +85 °C,
Tj = -40 to +115 °C
MDQ, MDQS, MDQS#, and MDM pins = output driver 34Ω setting, other pins = output driver 40Ω setting

Item	Symbol	Min.	Max.	Unit	Figures
MCK average clock period	tCK(avg)	1.074	1.266	ns	Figure 3.32.2
MCK absolute high pulse width	tCH(abs)	0.44	—	tCK(avg)	Figure 3.32.2
MCK absolute low pulse width	tCL(abs)	0.44	—	tCK(avg)	Figure 3.32.2
Command, Address, and Control output setup time to MCK, MCK#	tOS(1T)	310	—	ps	Figure 3.32.3
	tOS(2T)	890	—	ps	
Command, Address, and Control output hold time from MCK, MCK#	tOH(1T)	310	—	ps	Figure 3.32.3
	tOH(2T)	320	—	ps	
Command, Address, and Control pulse width for each output	tOPW(1T)	620	—	ps	Figure 3.32.3
	tOPW(2T)	1210	—	ps	
Write Latency	WL	CWL	—	tCK(avg)	Figure 3.32.4
MDQS, MDQS# rising edge to MCK, MCK# rising edge (write)	tWDQSS	-0.20	0.20	tCK(avg)	Figure 3.32.4
MDQS, MDQS# falling edge setup time to MCK, MCK# rising edge (write)	tWDSS	0.25	—	tCK(avg)	Figure 3.32.4
MDQS, MDQS# falling edge hold time from MCK, MCK# rising edge (write)	tWDSH	0.25	—	tCK(avg)	Figure 3.32.4
MDQS, MDQS# differential high pulse width (write)	tWDQSH	0.45	0.55	tCK(avg)	Figure 3.32.5
MDQS, MDQS# differential low pulse width (write)	tWDQSL	0.45	0.55	tCK(avg)	Figure 3.32.5
MDQS, MDQS# differential WRITE Preamble (write)	tWPRE	0.9	—	tCK(avg)	Figure 3.32.5
MDQS, MDQS# differential WRITE Postamble (write)	tWPST	0.3	—	tCK(avg)	Figure 3.32.5
MDQ and MDM output setup time to MDQS, MDQS# (write)	tWDS	167	—	ps	Figure 3.32.6
MDQ and MDM output hold time from DQS, DQS# (write)	tWDH	167	—	ps	Figure 3.32.6
MDQ and MDM output pulse width for each output (write)	tWDIPW	334	—	ps	Figure 3.32.6
Read latency	RL	CL	—	tCK(avg)	Figure 3.32.7
MDQS, MDQS# rising edge input access time from rising MCK, MCK# (read)	tRDQSCK	-225	1375	ps	Figure 3.32.7
MDQS, MDQS# differential input high pulse width (read)	tRQSH	0.4	—	tCK(avg)	Figure 3.32.8

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Item	Symbol	Min.	Max.	Unit	Figures
MDQS, MDQS# differential input low pulse width (read)	tRQSL	0.4	—	tCK(avg)	Figure 3.32.8
MDQS, MDQS# differential READ Preamble (read)	tRPRE	0.9	—	tCK(avg)	Figure 3.32.8
MDQS, MDQS# differential READ Postamble (read)	tRPST	0.3	—	tCK(avg)	Figure 3.32.8
MDQS, MDQS# to DQ skew, per group, per access (read)	tRDQSQ	—	124	ps	Figure 3.32.9
MDQ input hold time from MDQS, MDQS# (read)	tRQH	0.35	—	tCK(avg)	Figure 3.32.9

Note: The signal timing is based on the following electric potential:
For MCK output, MDQS input/output: Differential input/output cross point voltage
For MDQ input: MVREF
For outputs other than MCK or MDQS: 0.5 × VDDQ_DDR

- Reference Load and VTT Termination of AC Timing

  Reference Load for AC Timing

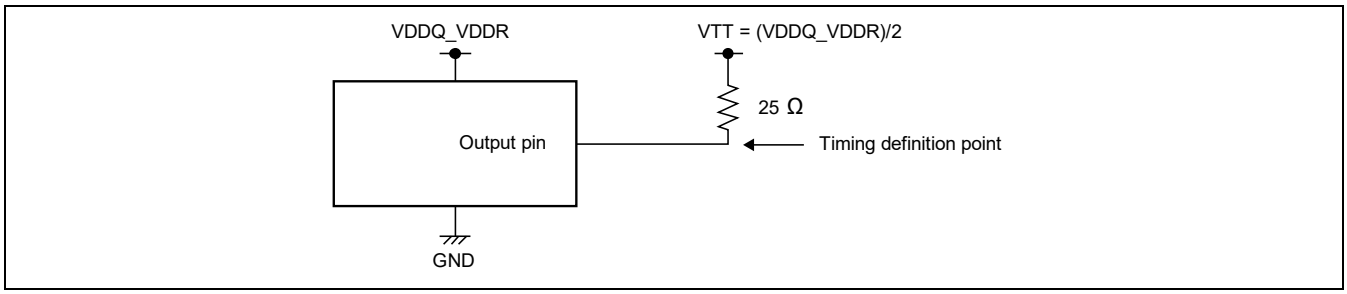


Figure 3.32.1 Reference Load for AC Timing

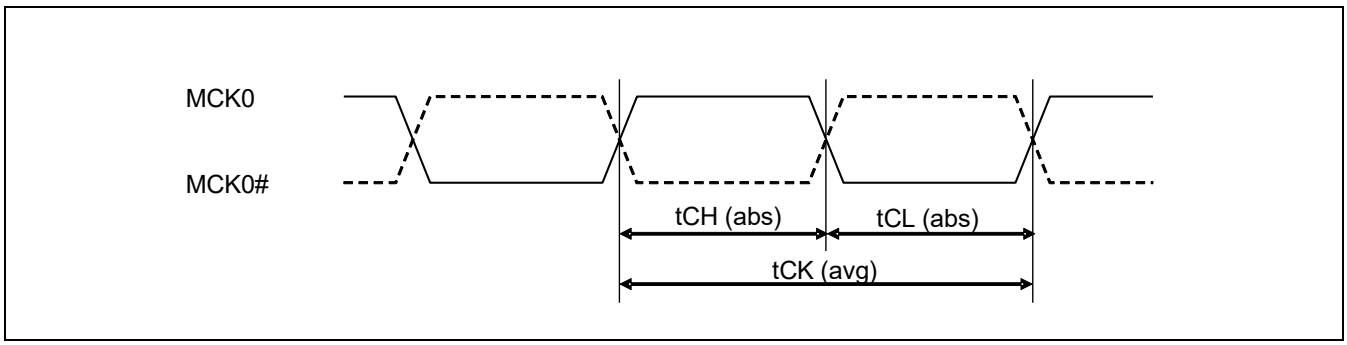


Figure 3.32.2 MCK Clock Output

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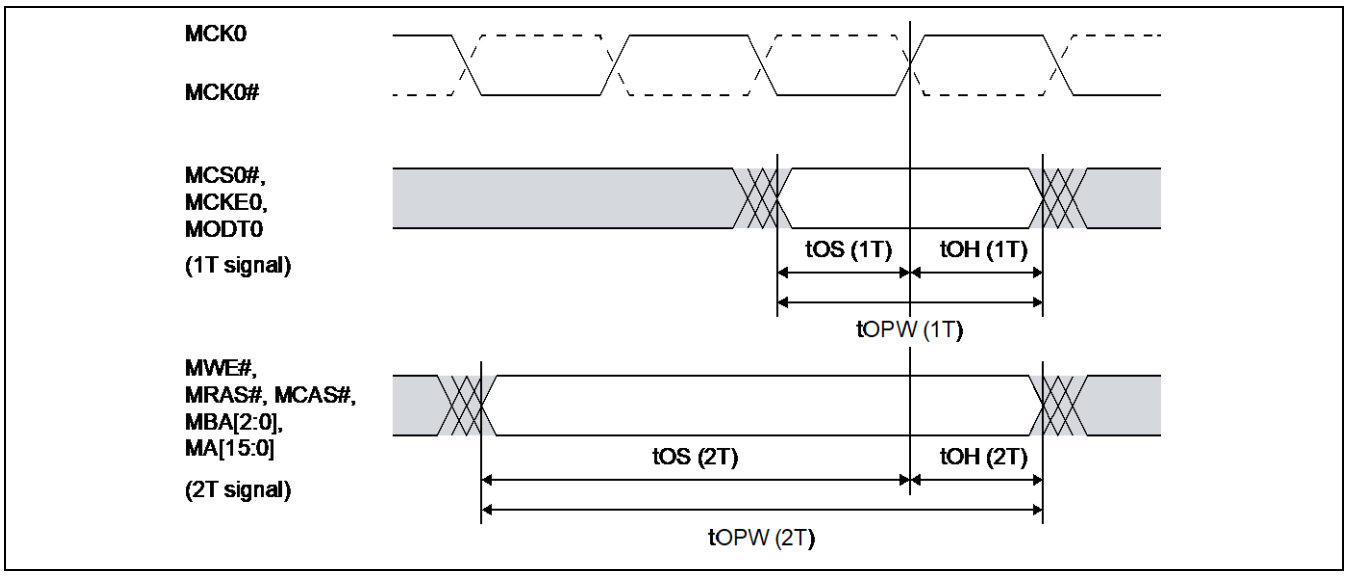


Figure 3.32.3 Command, Address, and Control Output Timing relative to MCK Output

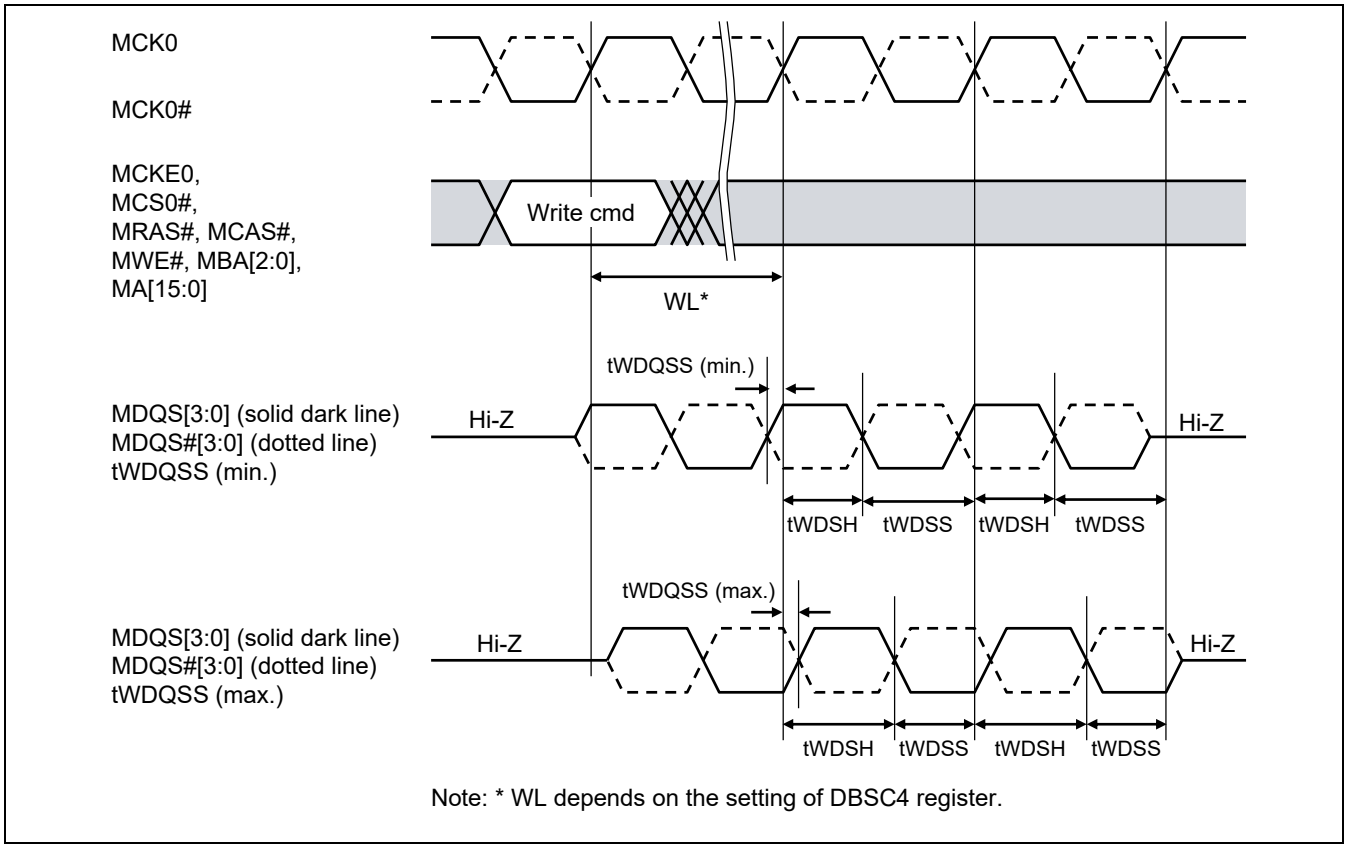


Figure 3.32.4 MDQS Output Timing relative to MCK Output (write)

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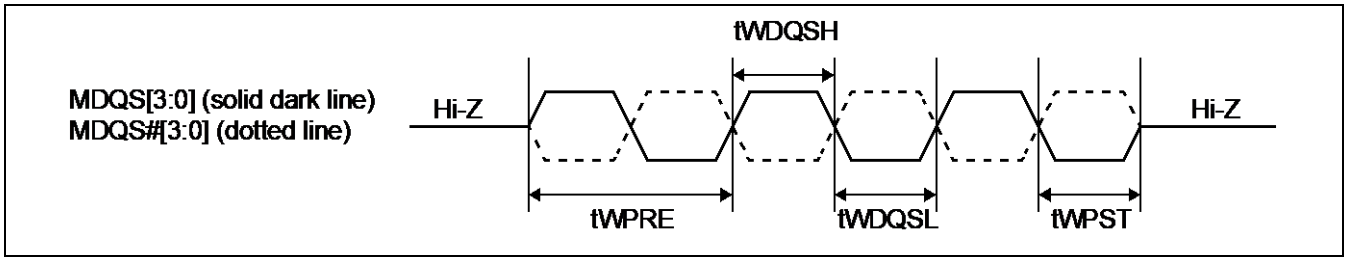


Figure 3.32.5 MDQS Output Timing (write)

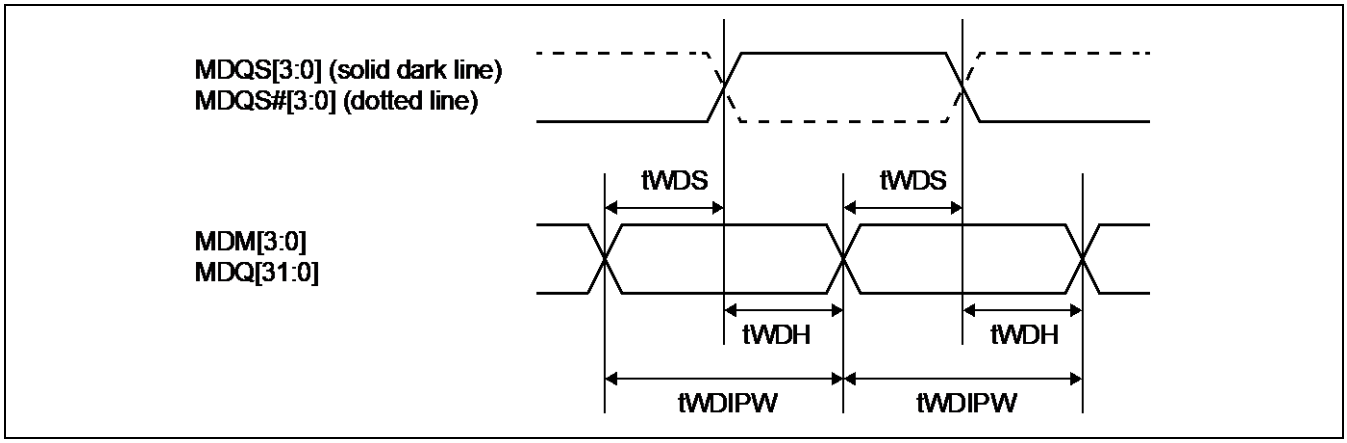


Figure 3.32.6 MDQ/MDM Output Timing relative to MDQ (write)

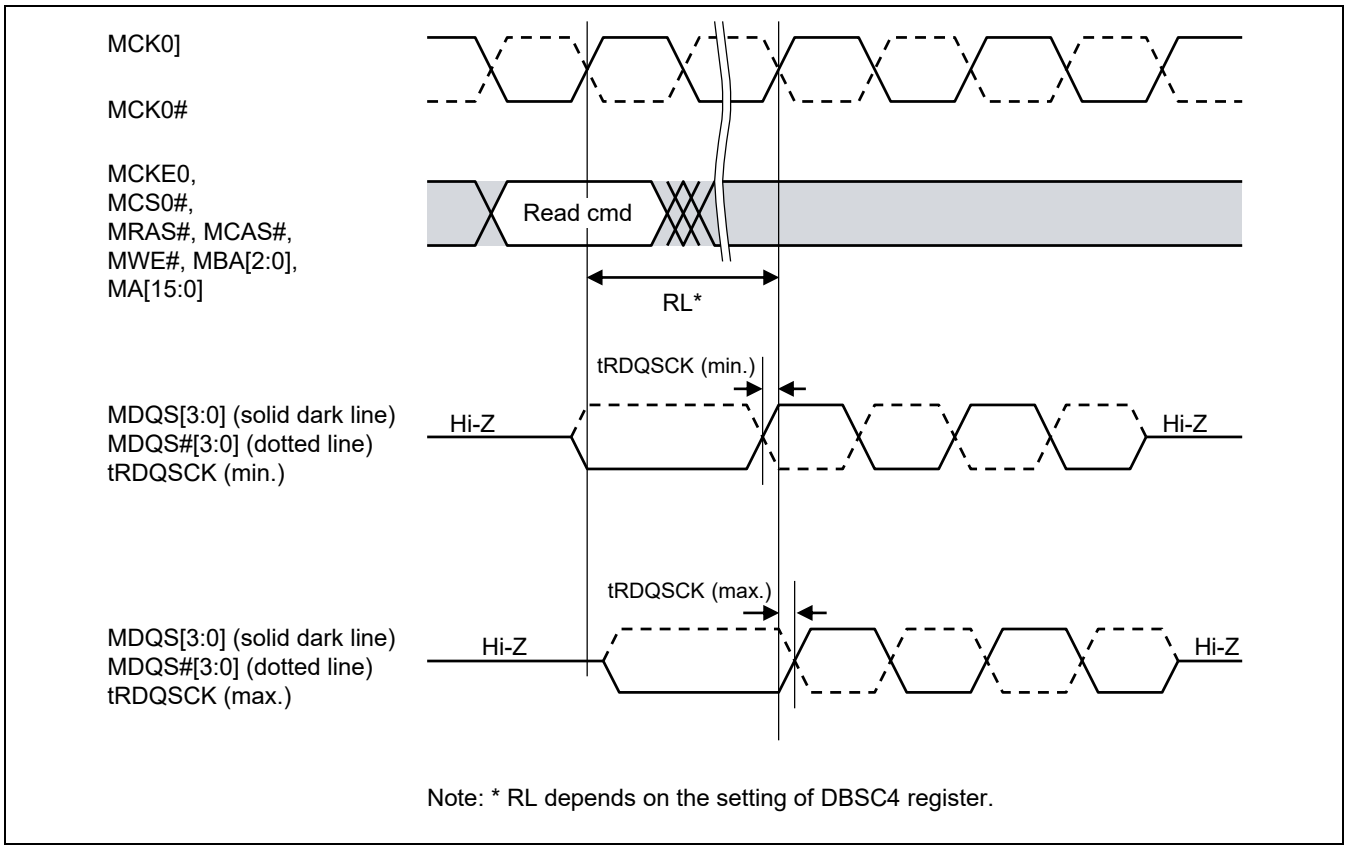


Figure 3.32.7 MDQS Input Timing relative to MCK Output (read)

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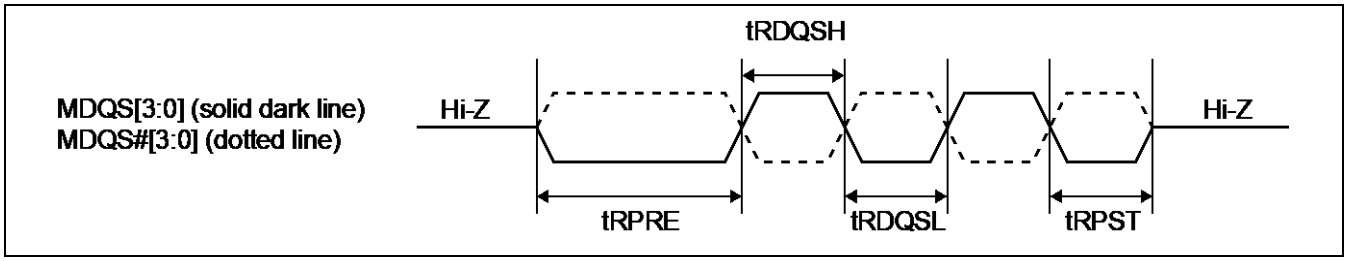


Figure 3.2.32.8 MDQS Input Timing (read)

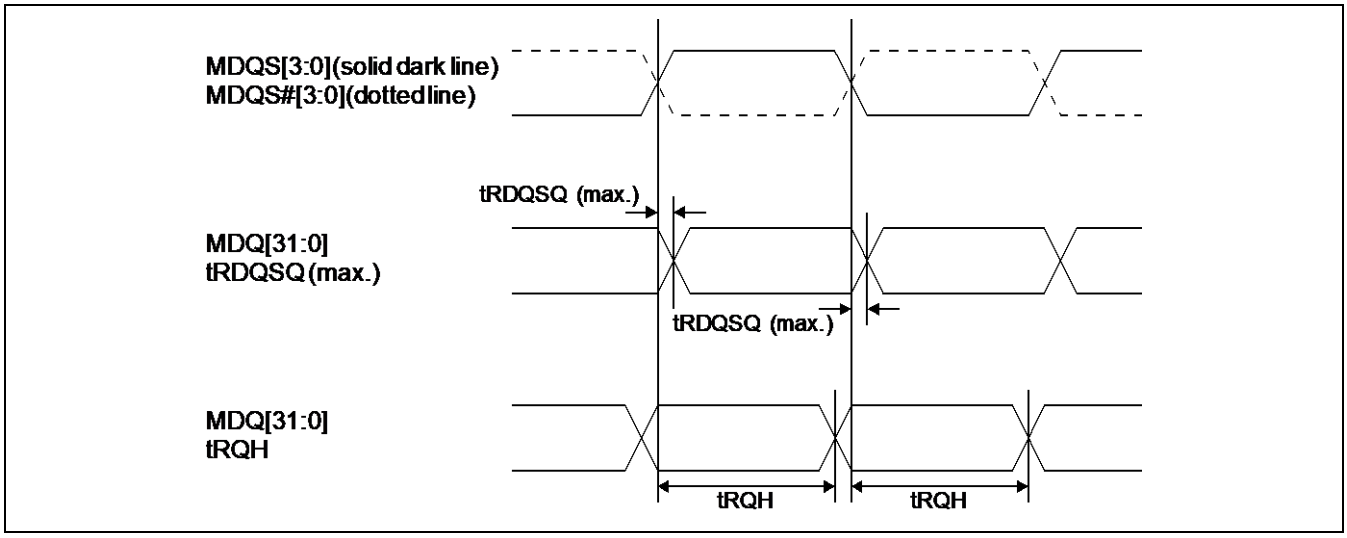


Figure 3.32.9 MDQ Input Timing relative to MDQS (read)

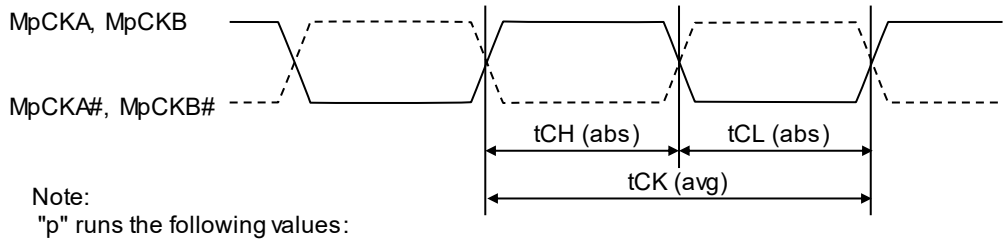
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Table 3.32.2 DBSC4 Access Timing (LPDDR4) [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

Conditions for LPDDR4: VDDQ_DDR = 1.1 V + 0.07/- 0.04V, GND = VSS = 0 V,
Tc = -40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N]

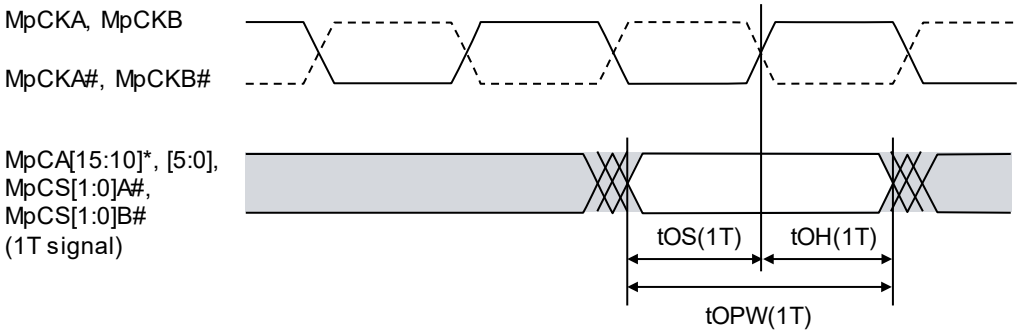
Item	Symbol	Min.	Max.	Unit	Figures
MCK average clock period	tCK(avg)	0.625	2.5	ns	Figure 3.32.10
MCK absolute high pulse width	tCH(abs)	0.44	0.56	tCK(avg)	
MCK absolute low pulse width	tCL(abs)	0.44	0.56	tCK(avg)	
Command, Address, and Control output setup time to MCK, MCK#	tOS(1T)	191	—	ps	Figure 3.32.11
Command, Address, and Control output hold time from MCK, MCK#	tOH(1T)	191	—	ps	
Command, Address, and Control pulse width for each output	tOPW(1T)	425	—	ps	
MDQS, MDQS# rising edge to MCK, MCK# rising edge (write)	tWDQSS	0.77	1.23	tCK(avg)	Figure 3.32.12
MDQS, MDQS# falling edge setup time to MCK, MCK# rising edge (write)	tWDSS	0.22	—	tCK(avg)	
MDQS, MDQS# falling edge hold time from MCK, MCK# rising edge (write)	tWDSH	0.22	—	tCK(avg)	
MDQS, MDQS# differential high pulse width (write)	tWDQSH	0.4	—	tCK(avg)	Figure 3.32.13
MDQS, MDQS# differential low pulse width (write)	tWDQSL	0.4	—	tCK(avg)	
MDQS, MDQS# differential WRITE Preamble (write)	tWPRE	1.8	—	tCK(avg)	
MDQS, MDQS# differential WRITE Postamble (write)	tWPST	0.4	—	tCK(avg)	
MDQ and MDM output setup time to MDQS, MDQS# (write)	tWDS	97	—	ps	Figure 3.32.14
MDQ and MDM output hold time from DQS, DQS# (write)	tWDH	97	—	ps	
MDQ and MDM output pulse width for each output (write)	tWDIPW	194	—	ps	
MDQS, MDQS# rising edge input access time from rising MCK, MCK# (read)	tRDQSCK	1500	4600	ps	Figure 3.32.15
MDQS, MDQS# differential input high pulse width (read)	tRQSH	0.38	—	tCK(avg)	Figure 3.32.16
MDQS, MDQS# differential input low pulse width (read)	tRQSL	0.38	—	tCK(avg)	
MDQS, MDQS# differential READ Preamble (read)	tRPRE	1.8	—	tCK(avg)	
MDQS, MDQS# differential READ Postamble (read)	tRPST	0.4	—	tCK(avg)	
Read Data Eye Mask (read)	TdIVW_total	—	0.25	UI	Figure 3.32.17
	VdIVW_total	140	—	mV	

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Note:
"p" runs the following values:
from 0 to 1 for RZ/G2H, RZ/G2M V1.3 and RZ/G2M V3.0
0 for RZ/G2N

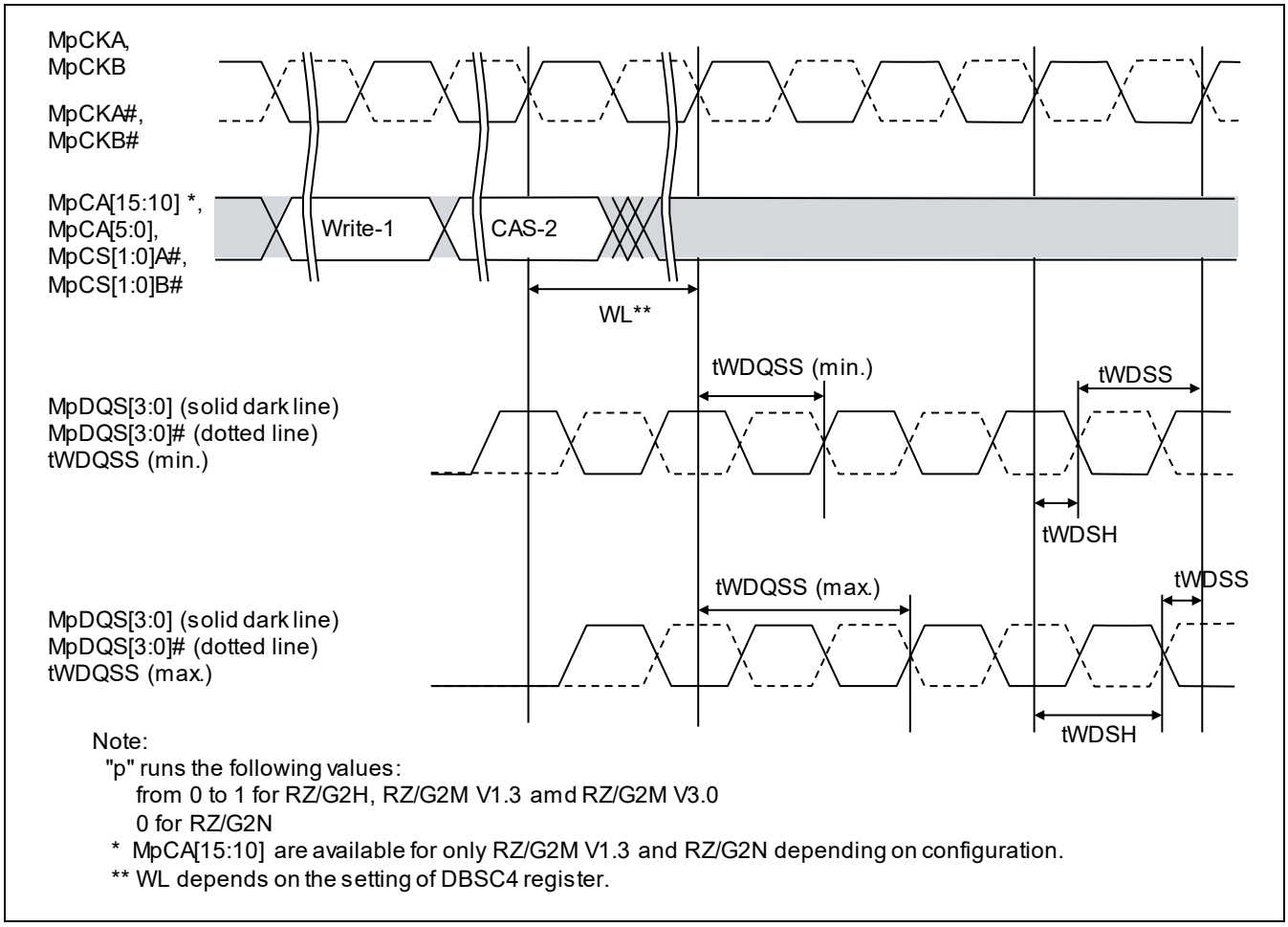
Figure 3.32.10 MCK Clock Output



Note:
"p" runs the following values:
from 0 to 1 for RZ/G2H, RZ/G2M V1.3 and RZ/G2M V3.0
0 for RZ/G2N
* MpCA[15:10] are available for only RZ/G2M V1.3 and RZ/G2N depending on configuration.

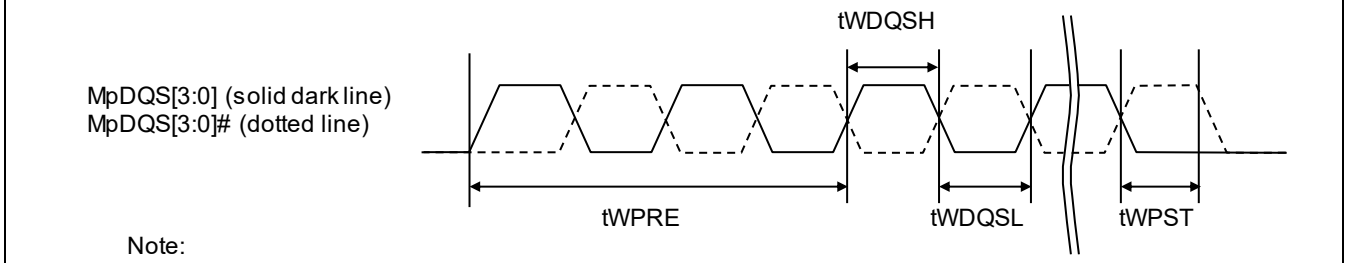
Figure 3.32.11 Command, Address, and Control Output Timing relative to MCK Output

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Note:
"p" runs the following values:
from 0 to 1 for RZ/G2H, RZ/G2M V1.3 amd RZ/G2M V3.0
0 for RZ/G2N
* MpCA[15:10] are available for only RZ/G2M V1.3 and RZ/G2N depending on configuration.
** WL depends on the setting of DBSC4 register.

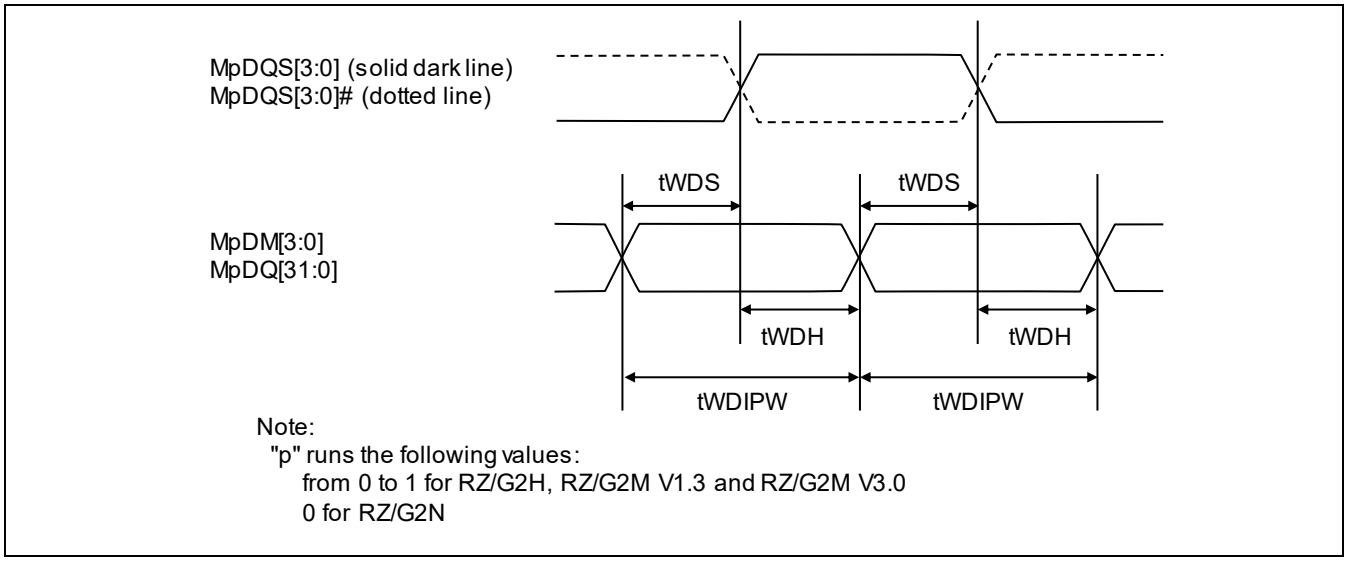
Figure 3.32.12 MDQS Output Timing relative to MCK Output (write)



Note:
"p" runs the following values:
from 0 to 1 for RZ/G2H, RZ/G2M V1.3 and RZ/G2M V3.0
0 for RZ/G2N

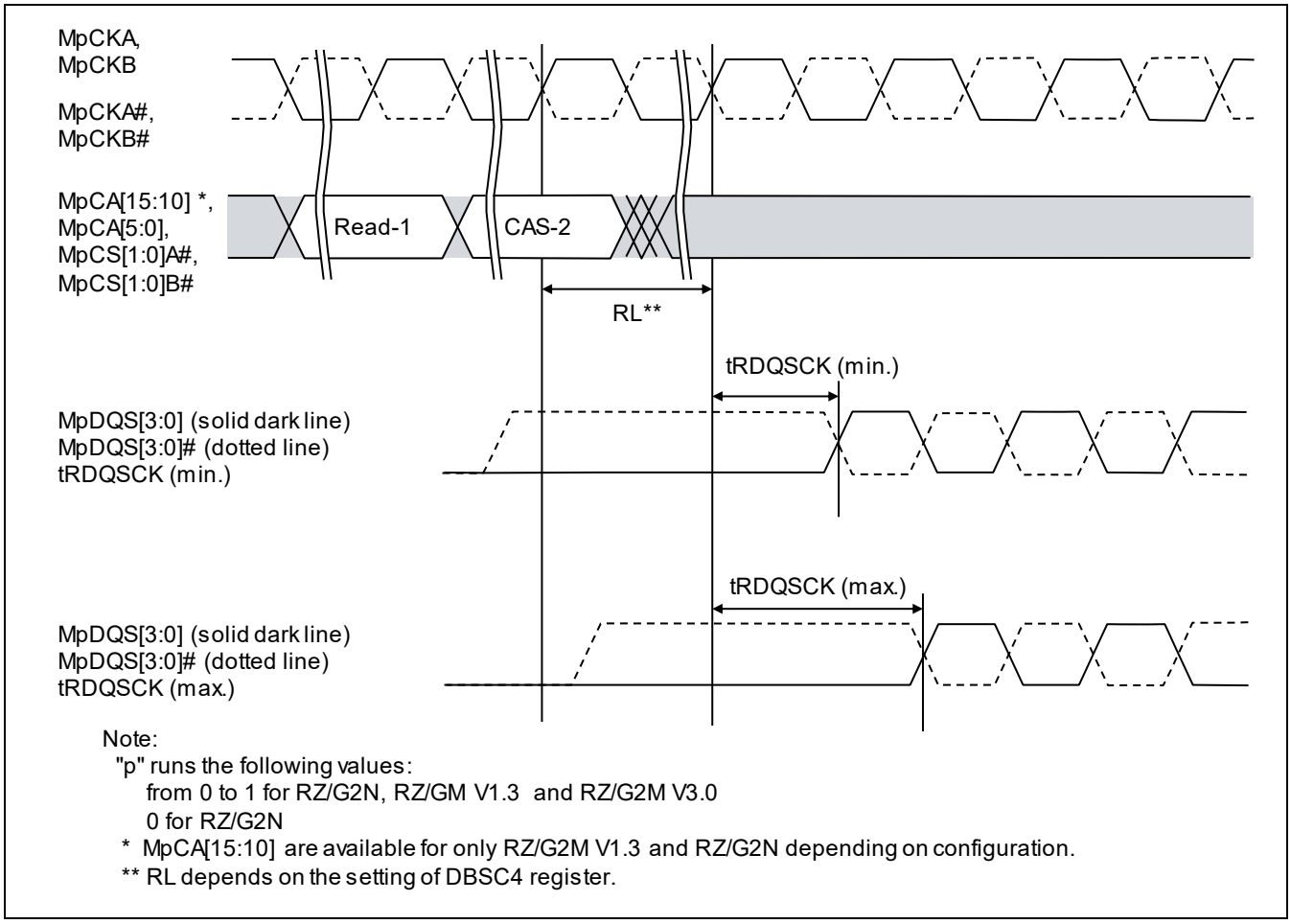
Figure 3.32.13 MDQS Output Timing (write)

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Note:
"p" runs the following values:
from 0 to 1 for RZ/G2H, RZ/G2M V1.3 and RZ/G2M V3.0
0 for RZ/G2N

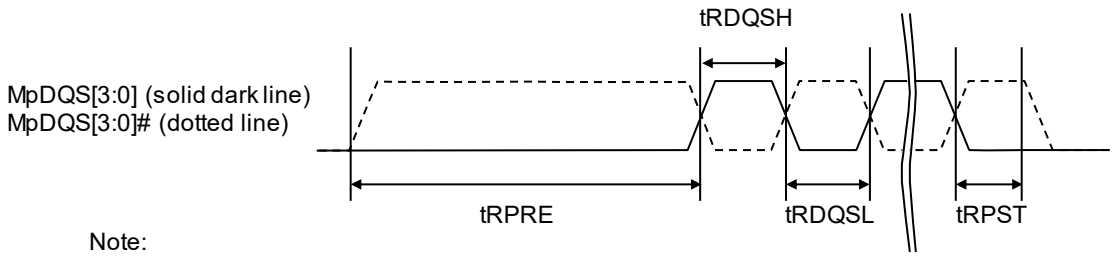
Figure 3.32.14 MDQ/MDM Output Timing relative to MDQ (write)



Note:
"p" runs the following values:
from 0 to 1 for RZ/G2N, RZ/GM V1.3 and RZ/G2M V3.0
0 for RZ/G2N
* MpCA[15:10] are available for only RZ/G2M V1.3 and RZ/G2N depending on configuration.
** RL depends on the setting of DBSC4 register.

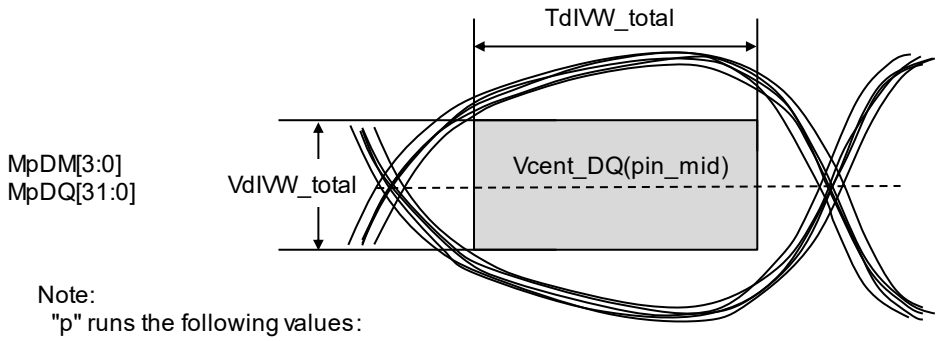
Figure 3.32.15 MDQS Input Timing relative to MCK Output (read)

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Note:
"p" runs the following values:
from 0 to 1 for RZ/G2H , RZ/G2M V1.3 and RZ/G2M V3.0
0 for RZ/G2N

Figure 3.32.16 MDQS Input Timing (read)



Note:
"p" runs the following values:
from 0 to 1 for RZ/G2H, RZ/G2M V1.3 and RZ/G2M V3.0
0 for RZ/G2N

Figure 3.32.17 Read Data Eye Mask (read)

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3.33 Debug and Trace

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

3.33.1 JTAG IF

Table 3.33.1 JTAG IF Signal Timing

Conditions: VDDQ18 = 1.8 V ± 0.1 V, GND = VSS = 0 V, Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E], CL = 30 pF

[RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N, and RZ/G2E]

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
TCK Input clock cycle	tTCKcyc	50*	—	—	ns	Figure 3.33.1
TCK Input clock pulse width (high level)	tTCKH	20	—	—	ns	
TCK Input clock pulse width (low level)	tTCKL	20	—	—	ns	
TDI/TMS setup time	tTDIS	15	—	—	ns	Figure 3.33.2
TDI/TMS hold time	tTDIH	15	—	—	ns	
TDO output delay time	tTDO	0	—	14	ns	

[RZ/G2H]

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
TCK Input clock cycle	tTCKcyc	70*	—	—	ns	Figure 3.33.1
TCK Input clock pulse width (high level)	tTCKH	30	—	—	ns	
TCK Input clock pulse width (low level)	tTCKL	30	—	—	ns	
TDI/TMS setup time	tTDIS	25	—	—	ns	Figure 3.33.2
TDI/TMS hold time	tTDIH	25	—	—	ns	
TDO output delay time	tTDO	0	—	24	ns	

Note: * The cycle is 500 ns (2 MHz) during boundary scan operation.

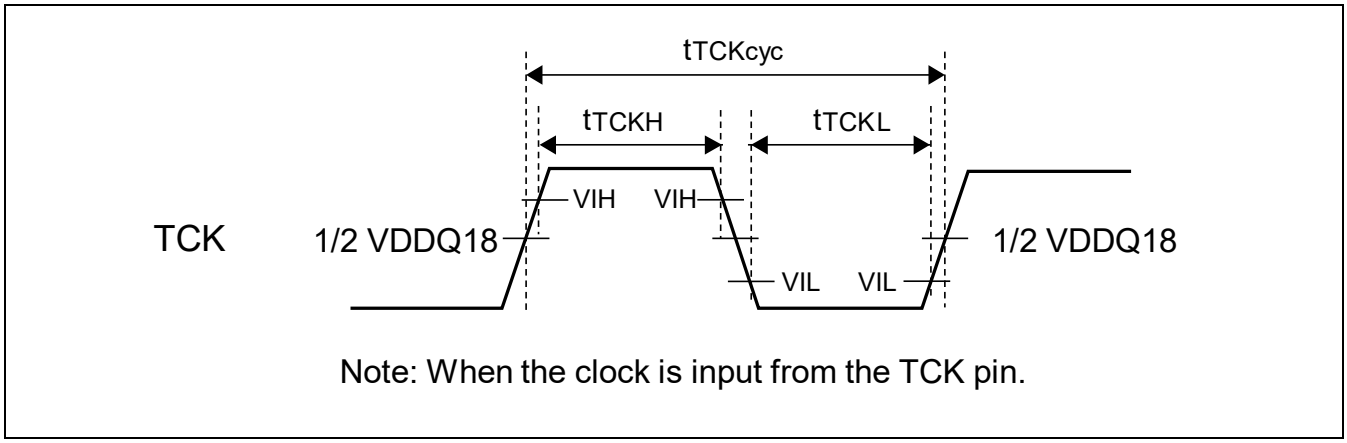


Figure 3.33.1 TCK Input Timing

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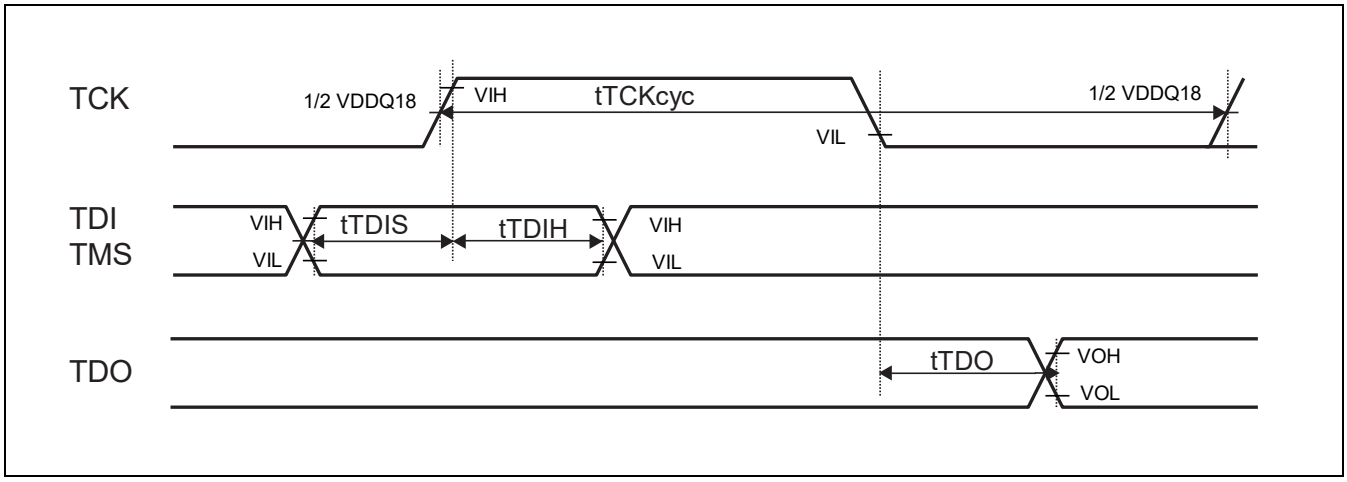


Figure 3.33.2 Data Transfer Timing

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3.34 GPIO

RZ/G2H
RZ/G2M V1.3 RZ/G2M V3.0
RZ/G2N RZ/G2E

Table 3.34.1 GPIO Module Signal Timing

Conditions: VDDQ33 = 3.3 V ± 0.2 V, VDDQVA_SDn = 3.3 V ± 0.2 V / 1.8 V ± 0.1 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
VDDQ33 = 3.3 V ± 0.3 V, VDD_QSPI = VDDQ_SDn = 3.3 V ± 0.3 V / 1.8 V ± 0.1 V, VDDQ25_AVB0 = 3.3 V ± 0.3 V / 2.5 V ± 0.2 V [RZ/G2E]
Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E]

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
GPIO input active width	tIOAW	2	—	—	tGPCYC	Figure 3.34.1

Note: tGPCYC: One cycle of the S3D4ϕ clock for RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N, and RZ/G2E.

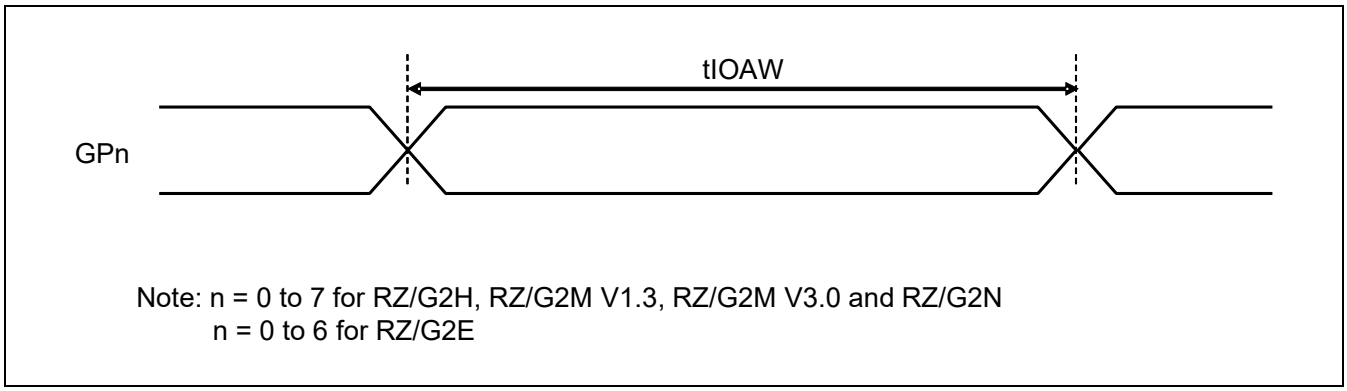


Figure 3.34.1 GPIO signal Timing

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3.35 Internal PLL Characteristics (reference only)

RZ/G2H | RZ/G2M V1.3 | RZ/G2M V3.0 | RZ/G2N | RZ/G2E

Table 3.35.1 Internal PLL Characteristics (reference only)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
PLL long term jitter	—	-500	—	+500	ps	Term = 1μs

Note: RZ/G2H, RZ/G2M V1.3,RZ/G2M V3.0, RZ/G2N : PLL1, RZ/G2E:PLL0

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3.36 HDMI-IF

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Table 3.36.1 AC Characteristics (Source AC characteristics at TP1 for HDMI Interface)

Conditions: VDDQ18_HDMIn (n=0,1) = 1.8 V ± 0.1V,
VDDQ09_HDMIn (n=0,1) = 0.82 V + 0.06 V / - 0.07V, GND = VSS = 0V,
Tc = -40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N]

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks, Figures
Rise time	T_R	75	—	—	ps	20%-80%	Figure 3.36.1
Fall time	T_F	75	—	—	ps	20%-80%	Figure 3.36.1
Intra-pair skew	Tra	—	—	0.15	Tbit	—	*1 Figure 3.36.2
Inter-pair skew	Ter	—	—	0.20	Tcharacter	—	*2 Figure 3.36.3
Eye Diagram Mask	—	—	—	—	—	Eye Diagram Mask	Figure 3.36.4
TMDSCLK frequency	$F_{TMDSCLK}$	25	—	297	MHz	—	
TMDSCLK period	$P_{TMDSCLK}$	3.367	—	40	ns	—	Figure 3.36.5
TMDSCLK Duty cycle	T_{CDC}	40	50	60	%	$t_{CDC} = t_{CPH}/P_{TMDSCLK}$	Figure 3.36.5
TMDSCLK Differential Jitter	—	—	—	0.25	Tbit	—	*1

Notes: 1. Tbit Time duration of a single bit carried across the TMDS data channels.
2. Tcharacter Time duration of a single TMDS character carried across the TMDS data channels. This is equal to 10*Tbit.

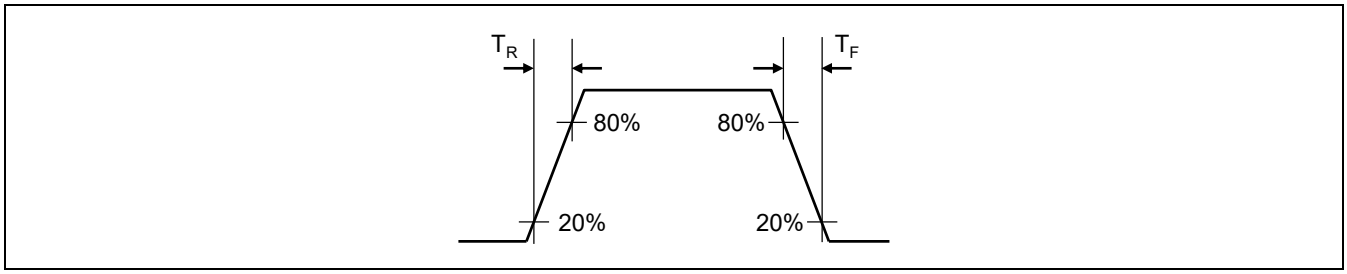


Figure 3.36.1 TMDS Output Signals Rise and Fall Time Definition for HDMI

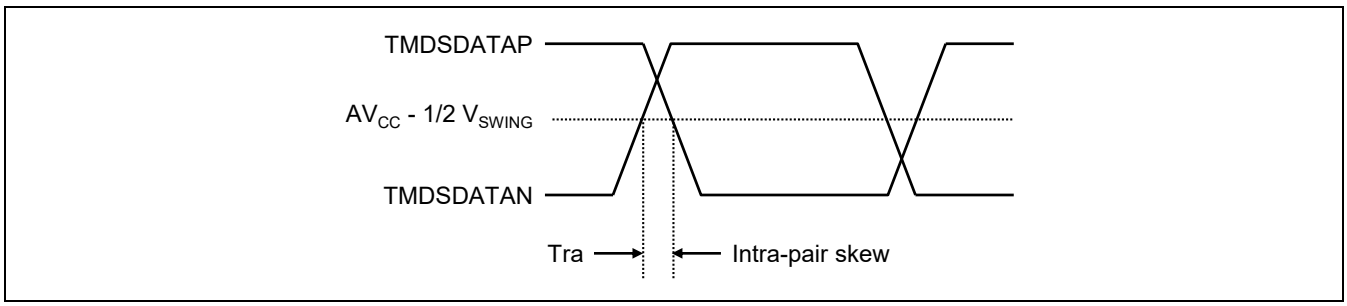


Figure 3.36.2 Intra-Pair Skew Definition for HDMI

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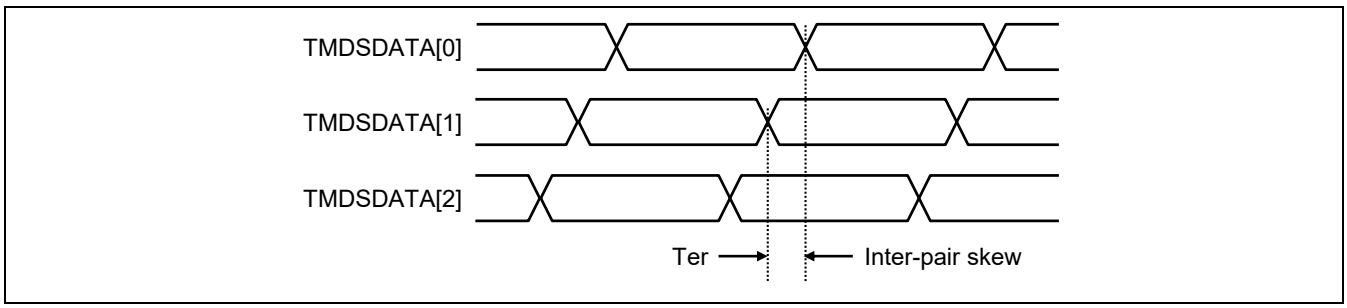


Figure 3.36.3 Inter-Pair Skew Definition for HDMI

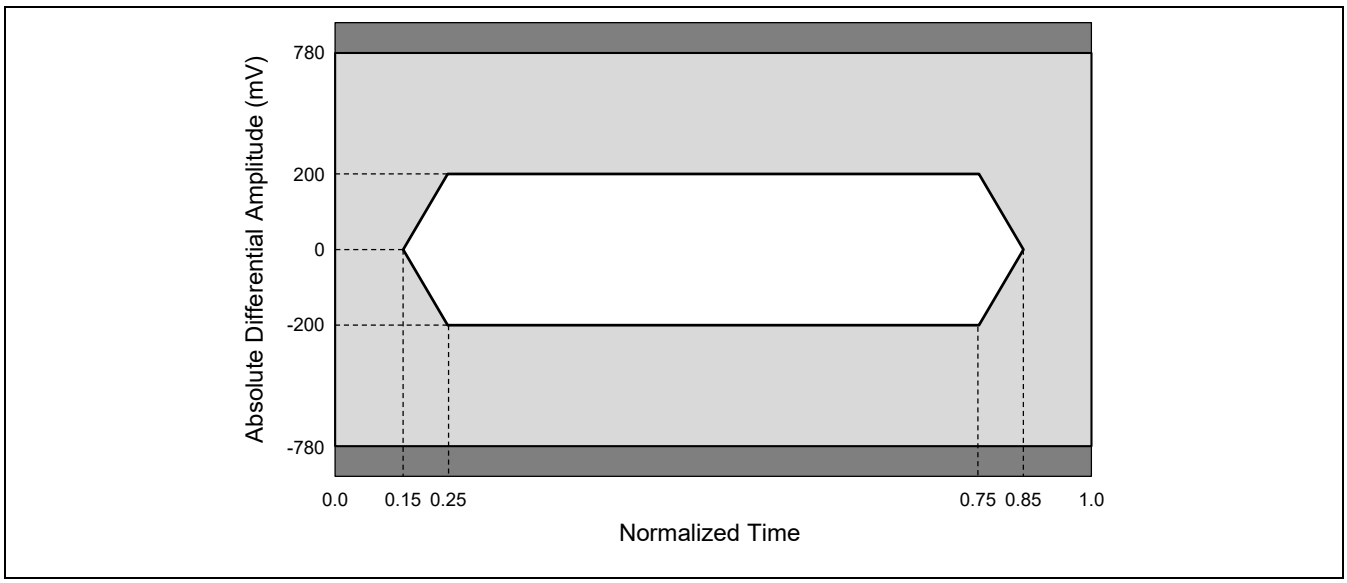


Figure 3.36.4 Eye Diagram Mask Definition at TP1 for HDMI

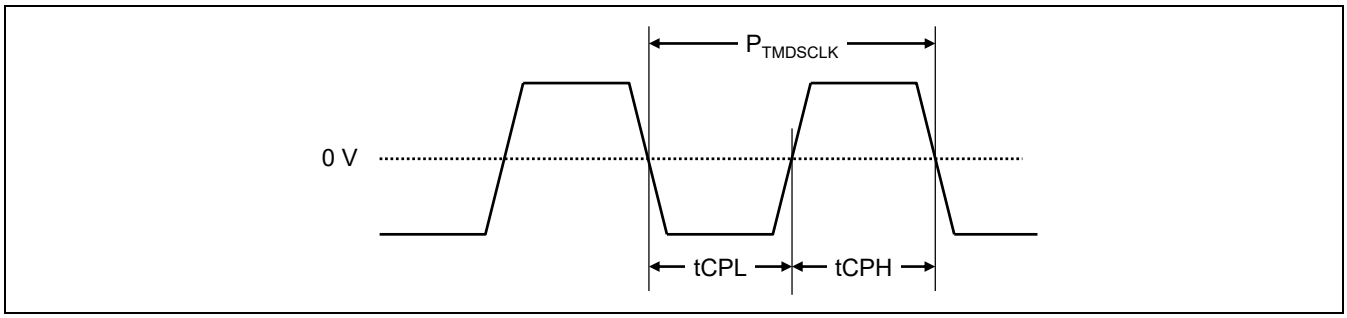


Figure 3.36.5 TMDS Clock Signal Definition for HDMI

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Table 3.36.2 HDMI Dot Clock Input (DU_DOTCLKIN1/2) Characteristics

Conditions: VDDQ18 = 1.8 V ± 0.1 V, GND = VSS = 0 V,
Tc = -40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N]

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Frequency range	fo	25	—	40	MHz	—	—
Frequency tolerance	f_tol	-100	—	100	ppm	—	—
Deterministic jitter	Dj	—	—	0	ps	—	—
RMS jitter	RMSj	—	—	600	fs	100 kHz~5 MHz	—

Table 3.36.3 AC Characteristics (DDC Signal for HDMI)

Conditions: VDDQ18 = 1.8 V ± 0.1 V,
GND = VSS = 0 V,
Tc = -40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N]

Item	Symbol	Conditons	Min	Typ	Max	Unit
HDSCL Clock Frequency	f_{HDSCL}	Standard mode	—	—	100	kHz
Bus Free Time (stop and start)	t_{HDSDA_BFtime}		4.7	—	—	µs
HDSCL Hold Time (on start)	$t_{HDSCL_HOLD_ST}$		4.0	—	—	µs
HDSCL Low Width	t_{L_HDSCL}		4.7	—	—	µs
HDSCL High Width	t_{H_HDSCL}		4.0	—	—	µs
HDSCL Setup Time (on start)	$t_{HDSCL_SETUP_ST}$		4.7	—	—	µs
HDSDA Hold Time	t_{HDSDA_HOLD}		0	—	3.45	µs
HDSDA Setup Time	t_{HDSDA_SETUP}		250	—	—	ns
HDSCL Setup Time	t_{HDSCL_SETUP}		4.0	—	—	µs

Note: Capacitive load for each bus line (Cb): Max. 400 pF
HDMI0/1_SDA and HDMI0/1_SCL Signals Rising Time (Cb ≤ 300 pF): Max. 1000 ns
HDMI0/1_SDA and HDMI0/1_SCL Signals Falling Time (Cb ≤ 300 pF): Max. 300 ns

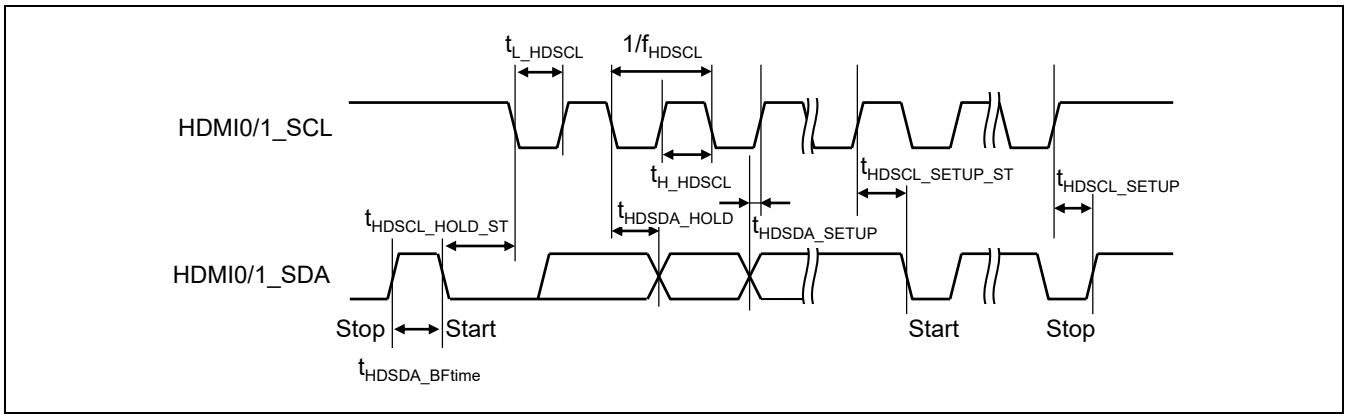


Figure 3.36.6 DDC Signals Definition for HDMI

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3.37 Usage Note

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

Table 3.37.1 shows the usage notes of some I/O pins when using external pull-up resistor.

Table 3.37.1 Usage notes of I/O pins

I/O Pin	Condition	Module name	product	Usage notes	Remarks
3.3V and 1.8 V	Use of external pull-up resister at 1.8 V	SDHI	RZ/G2H, RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N	The following measure 1) or 2) shall be implemented. 1) VDD or VDDQ18 shall be turned on after the corresponding pin voltage, IOV is turned on. The combinations of power-on sequence are as follows; IOV → VDD → VDDQ18 IOV → VDDQ18 → VDD VDD → IOV → VDDQ18 VDDQ18 → IOV → VDD 2) External pullup resistor shall be less than or equal to 2.7 KΩ.	*1
		SDHI	RZ/G2E	The above 2) shall be implemented.	*2
2.5V	Use of external pull-up resister at 2.5 V	Ethernet AVB-IF	RZ/G2H, RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N	External pull-up resister shall be less than or equal to 9.3 KΩ.	—

Notes: 1. Make sure that POCCTRL0 in PFC is changed when the corresponding pin voltage is used at 1.8 V.
2. Make sure that POCCTRL0 to 2 in PFC are changed when the corresponding pin voltage is used at 1.8 V.

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3.38 The accuracy of Thermal Sensor Characteristics

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

The accuracy of the temperature sensors of RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N varies from part number and accuracy of the temperature sensors is as follows.

Table 3.38.1 Part number and accuracy

Products	Part number	Accuracy of the temperature sensors
RZ/G2H	R8A774E0HA01BN#U0 R8A774E0HA01BN#G0 R8A774E1HA01BN#U0 R8A774E1HA01BN#G0	5.1 to 14.9 ℃ *1 @Tjs = 115 ℃ - 8.0 to -1.8 ℃ *1 @Tjs = - 40 ℃
RZ/G2H	other than the above	± 5℃
RZ/G2M V1.3	R8A774A0HA01BG#U2 R8A774A0HA01BG#G2 R8A774A1HA01BG#U2 R8A774A1HA01BG#G2	4.25 to 12.35 ℃ *1 @Tjs = 115 ℃ - 6.7 to - 0.3 ℃ *1 @Tjs = - 40 ℃
RZ/G2M V3.0	R8A774A2HA01BG#U7 R8A774A2HA01BG#G7 R8A774A3HA01BG#U7 R8A774A3HA01BG#G7	
RZ/G2M V1.3	other than the above	± 5℃
RZ/G2M V3.0	other than the above	
RZ/G2N	R8A774B0HA01BG#U0 R8A774B0HA01BG#G0 R8A774B1HA01BG#U0 R8A774B1HA01BG#G0	1.8 to 9.8 ℃ *1 @Tjs = 115 ℃ - 5.6 to - 1.8 ℃ *1 @Tjs = - 40 ℃
RZ/G2N	other than the above	± 5℃

Note: Tjs means output temperature of thermal sensor.

Note.1: Accuracy ranges are reference values. Calculation examples of Tj are shown below (e.g., RZ/G2H).
When Tjs = 115 ℃, the temperature range of Tj is between 100.1 and109.9 ℃.
(Tj = 115 - 14.9 = 100.1 ℃, Tj = 115 - 5.1 = 109.9 ℃)
When Tjs = - 40 ℃, the temperature range of Tj is between - 38.2 and - 32.0 ℃.
(Tj = - 40 + 1.8 = - 38.2 ℃, Tj = - 40 + 8.0 = - 32.0 ℃.)

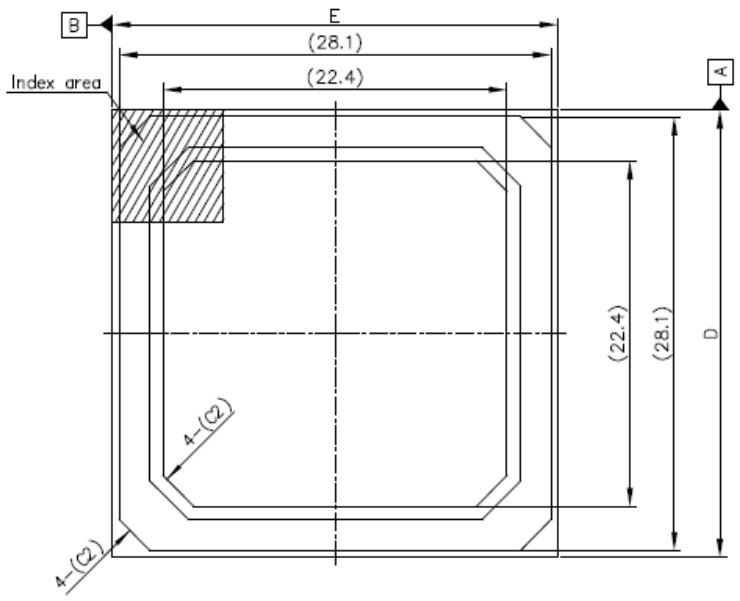
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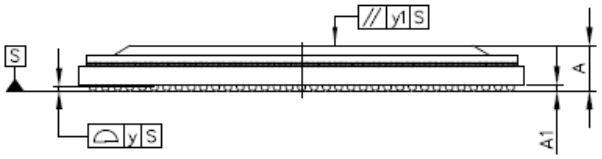
Section 4 Package Dimensions

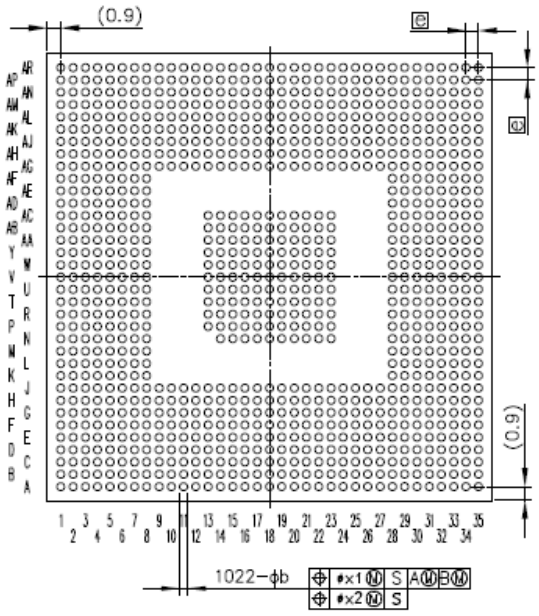
(1) RZG2H Package Outline Drawing

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HFBGA1022-29x29-0.80	PRBG1022GC-A	———	6.8

Unit:mm







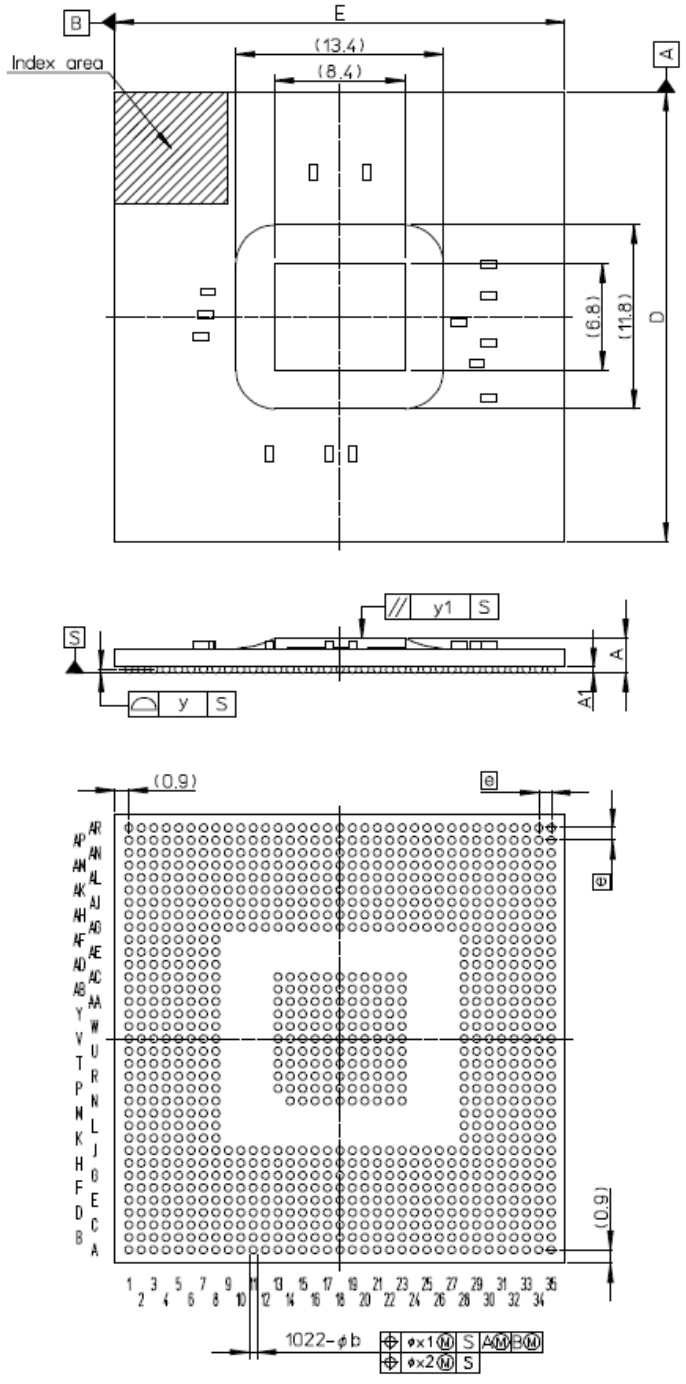
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	28.8	29.0	29.2
E	28.8	29.0	29.2
A	(2.75)	(2.95)	3.15
A1	0.35	0.40	0.45
e	———	0.80	———
b	0.45	0.50	0.55
x1	———	———	0.20
x2	———	———	0.08
y	———	———	0.15
y1	———	———	0.20

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(2) RZG2M Package Outline Drawing

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-FBGA1022-29x29-0.80	PRBG1022GB-A	————	3.2

Unit:mm



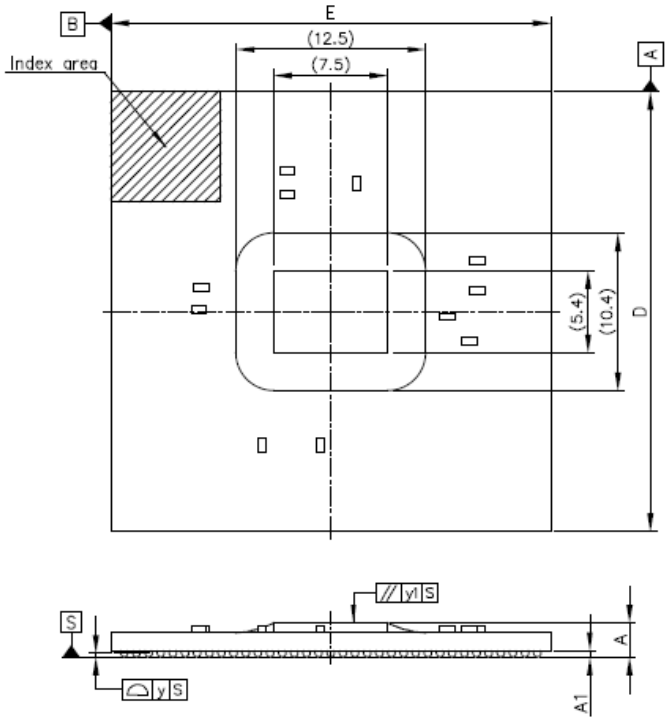
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	28.8	29.0	29.2
E	28.8	29.0	29.2
A	(2.1)	(2.3)	2.5
A1	0.35	0.40	0.45
e	——	0.8	——
b	0.45	0.50	0.55
x1	——	——	0.20
x2	——	——	0.08
y	——	——	0.15
y1	——	——	0.20

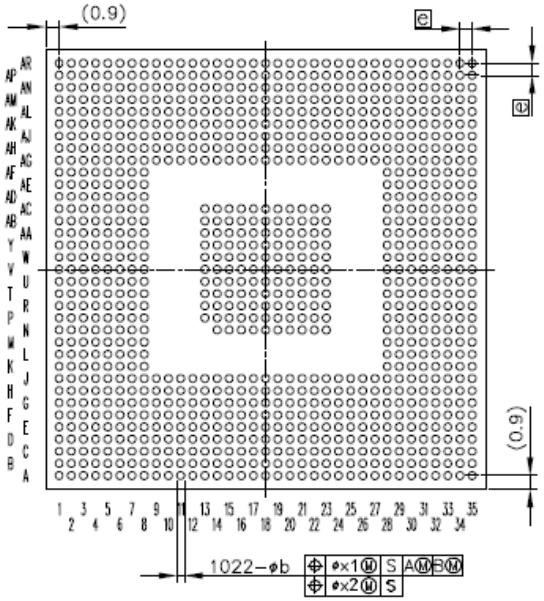
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(3) RZG2N Package Outline Drawing

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-FBGA1022-29x29-0.80	PRBG1022GA-B	————	3.2

Unit:mm





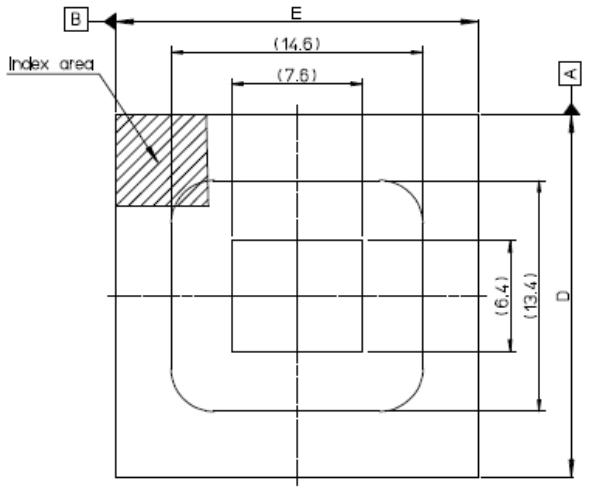
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	28.8	29.0	29.2
E	28.8	29.0	29.2
A	(2.1)	(2.3)	2.5
A1	0.35	0.40	0.45
e	——	0.8	——
b	0.45	0.50	0.55
x1	——	——	0.20
x2	——	——	0.08
y	——	——	0.15
y1	——	——	0.20

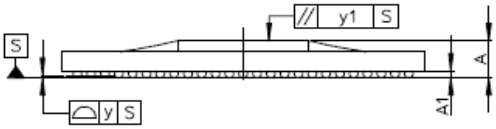
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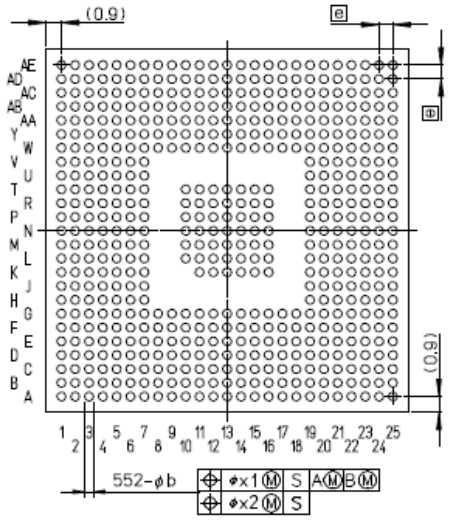
(4) RZG2E Package Outline Drawing

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-FBGA552-21x21-0.80	PRBG0552GA-A	----------	1.6g

Unit:mm







Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	20.85	21.00	21.15
E	20.85	21.00	21.15
A	(2.05)	(2.25)	2.45
A1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x1	—	—	0.20
x2	—	—	0.08
y	—	—	0.15
y1	—	—	0.20

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REVISION HISTORY	RZ/G Series, 2nd Generation Datasheet

Rev.	Data	Description	
		Page	Summary
1.00	Dec 25, 2024	—	First edition issued
1.01	Jun 30, 2025	—	Page number and total page number corrected.
		77	3.5 Clock Reset Timing, Figure 3.5.1 Notes 3. Supplemental information for power type and applicable prdocucts.

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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TOYOSU FORESIA, 3-2-24 Toyosu,
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