

MC74VHC1G66

SPST Normally Open (NO) Analog Switch

The MC74VHC1G66 is a single pole single throw (SPST) analog switch. It achieves high speed propagation delays and low ON resistances while maintaining low power dissipation. This bilateral switch controls analog and digital voltages that may vary across the full power-supply range (from V_{CC} to GND).

The MC74VHC1G66 is compatible in function to a single gate of the High Speed CMOS MC74VHC4066 and the metal-gate CMOS MC14066. The device has been designed so that the ON resistances (R_{ON}) are much lower and more linear over input voltage than R_{ON} of the metal-gate CMOS or High Speed CMOS analog switches.

The ON/OFF control inputs are compatible with standard CMOS outputs. The ON/OFF control input structure provides protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. This input structure helps prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

Features

- High Speed: $t_{PD} = 20$ ns (Typ) at $V_{CC} = 5.0$ V
- Low Power Dissipation: $I_{CC} = 1.0$ μ A (Max) at $T_A = 25^\circ$ C
- Diode Protection Provided on Inputs and Outputs
- Improved Linearity and Lower ON Resistance over Input Voltage
- Chip Complexity: 11 FETs or 3 Equivalent Gates
- ON/OFF Control Input has OVT
- Chip Complexity: FETs = 11
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



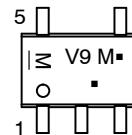
ON Semiconductor®

www.onsemi.com

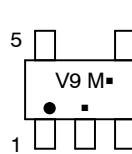
MARKING DIAGRAMS



SC-88A
DF SUFFIX
CASE 419A



TSOP-5
DT SUFFIX
CASE 483



V9 = Device Code
M = Date Code*
■ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

PIN ASSIGNMENT

1	IN/OUT X_A
2	OUT/IN Y_A
3	GND
4	ON/OFF CONTROL
5	V_{CC}

FUNCTION TABLE

On/Off Control Input	State of Analog Switch
L	Off
H	On

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

MC74VHC1G66

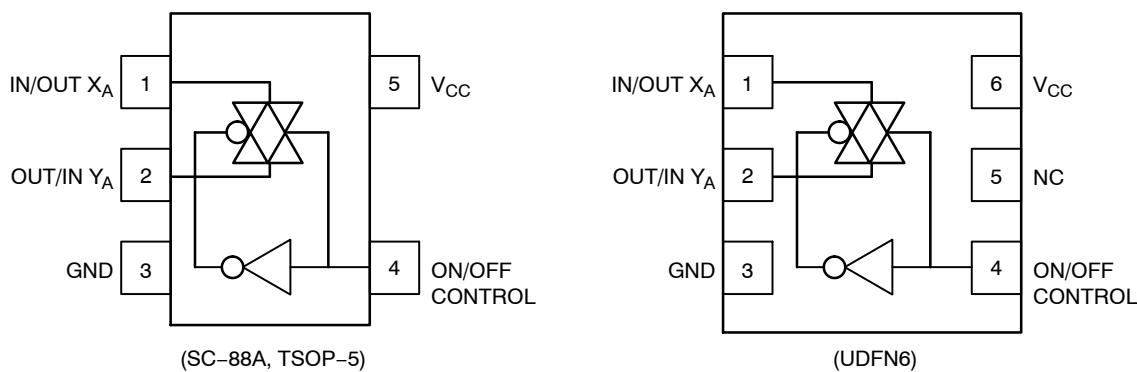


Figure 1. Pinout Diagrams

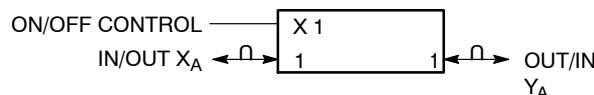


Figure 2. Logic Symbol

MAXIMUM RATINGS

Symbol	Characteristics	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +7.0	V
V_{IN}	Digital Input Voltage	-0.5 to +7.0	V
V_{IS}	Analog Output Voltage	-0.5 to V_{CC} +0.5	V
I_{IK}	Digital Input Diode Current	-20	mA
I_{CC}	DC Supply Current, V_{CC} and GND	+25	mA
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction Temperature Under Bias	+150	°C
θ_{JA}	Thermal Resistance SC70-5 (Note 1) SOT23-5	350 230	°C/W
P_D	Power Dissipation in Still Air at 85°C SC70-5 SOT23-5	150 200	mW
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	>2000 >200 N/A	V
$I_{LATCHUP}$	Latchup Performance Above V_{CC} and Below GND at 125°C (Note 5)	±500	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit	
V_{CC}	DC Supply Voltage	2.0	5.5	V	
V_{IN}	DC Input Voltage	GND	5.5	V	
V_{IS}	DC Output Voltage	GND	V_{CC}	V	
T_A	Operating Temperature Range	-55	+125	°C	
t_r, t_f	Input Rise and Fall Time ON/OFF Control Input	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	0 0	100 20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Device Junction Temperature versus
Time to 0.1% Bond Failures

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

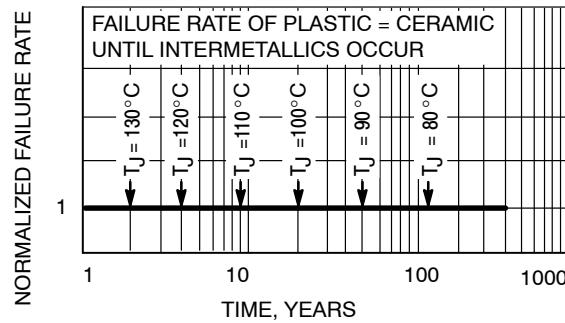


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	$T_A = 25^\circ\text{C}$		$T_A \leq 85^\circ\text{C}$		$-55 \leq T_A \leq 125^\circ\text{C}$		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	Minimum High-Level Input Voltage ON/OFF Control Input	R_{ON} = Per Spec	2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V_{IL}	Maximum Low-Level Input Voltage ON/OFF Control Input	R_{ON} = Per Spec	2.0 3.0 4.5 5.5		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
I_{IN}	Maximum Input Leakage Current ON/OFF Control Input	$V_{IN} = V_{CC}$ or GND	0 to 5.5		± 0.1		± 1.0		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $V_{IO} = 0 \text{ V}$	5.5		1.0		20		40	μA
R_{ON}	Maximum "ON" Resistance	$V_{IN} = V_{IH}$ $V_{IS} = V_{CC}$ or GND $ I_{IS} \leq 5 \text{ mA}$ (Figure 4)	3.0 4.5 5.5		60 45 40		70 50 45		100 60 55	Ω
I_{OFF}	Maximum Off-Channel Leakage Current	$V_{IN} = V_{IL}$ $V_{IS} = V_{CC}$ or GND Switch Off (Figure 5)	5.5		0.1		0.5		1.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

MC74VHC1G66

AC ELECTRICAL CHARACTERISTICS $C_{load} = 50 \text{ pF}$, Input $t_r/t_f = 3.0 \text{ ns}$

Symbol	Parameter	Test Conditions	V_{CC} (V)	$T_A = 25^\circ\text{C}$			$T_A \leq 85^\circ\text{C}$		$-55 \leq T_A \leq 125^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input X to Y	$Y_A = \text{Open}$ (Figure 14)	2.0 3.0 4.5 5.5	1 0.6 0.6 0.6	5 2 1 1		6 3 1 1		7 4 2 1	ns	
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, ON/OFF Control to Analog Output	$R_L = 1000 \Omega$ (Figure 15)	2.0 3.0 4.5 5.5	32 28 24 20	40 35 30 25		45 40 35 30		50 45 40 35	ns	
t_{PZL}, t_{PZH}	Maximum Propagation Delay, ON/OFF Control to Analog Output	$R_L = 1000 \Omega$ (Figure 15)	2.0 3.0 4.5 5.5	32 28 24 20	40 35 30 25		45 40 35 30		50 45 40 35	ns	
C_{IN}	Maximum Input Capacitance	ON/OFF Control Input	0.0		3	10		10		10	pF
		Control Input = GND Analog I/O Feedthrough	5.0		4 4	10 10		10 10		10 10	

C_{PD}	Power Dissipation Capacitance (Note 6)	Typical @ $25^\circ\text{C}, V_{CC} = 5.0 \text{ V}$						pF
		18						

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Test Conditions	V_{CC}	Limit 25°C	Unit
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 10)	$f_{in} = 1 \text{ MHz Sine Wave}$ Adjust f_{in} voltage to obtain 0 dBm at V_{OS} Increase f_{in} = frequency until dB meter reads -3 dB $R_L = 50 \Omega$	3.0 4.5 5.5	150 175 180	MHz
ISO_{off}	Off-Channel Feedthrough Isolation (Figure 11)	$f_{in} = \text{Sine Wave}$ Adjust f_{in} voltage to obtain 0 dBm at V_{IS} $f_{in} = 10 \text{ kHz}, R_L = 600 \Omega$	3.0 4.5 5.5	-80 -80 -80	dB
NOISE _{feed}	Feedthrough Noise Control to Switch (Figure 12)	$V_{in} \leq 1 \text{ MHz Square Wave } (t_r = t_f = 2 \text{ ns})$ $R_L = 600 \Omega$	3.0 4.5 5.5	45 60 130	mV _{PP}
THD	Total Harmonic Distortion (Figure 13)	$f_{in} = 1 \text{ kHz}, R_L = 10 \text{ k}\Omega$ THD = THD _{Measured} - THD _{Source} $V_{IS} = 3.0 \text{ V}_{PP}$ sine wave $V_{IS} = 5.0 \text{ V}_{PP}$ sine wave	3.3 5.5	0.30 0.15	%

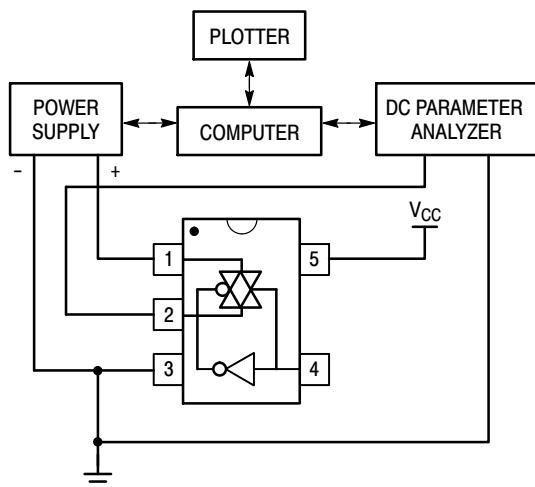


Figure 4. On Resistance Test Set-Up

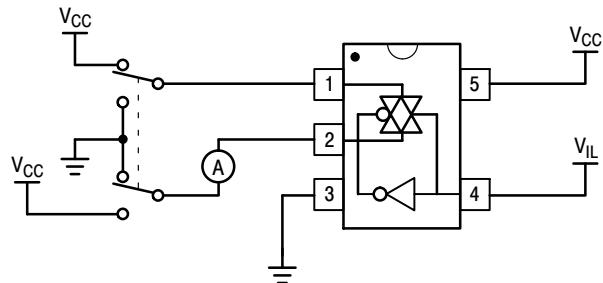


Figure 5. Maximum Off-Channel Leakage Current Test Set-Up

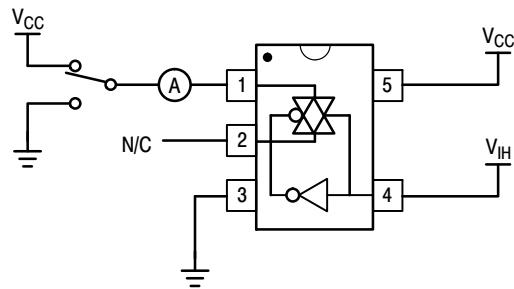


Figure 6. Maximum On-Channel Leakage Current Test Set-Up

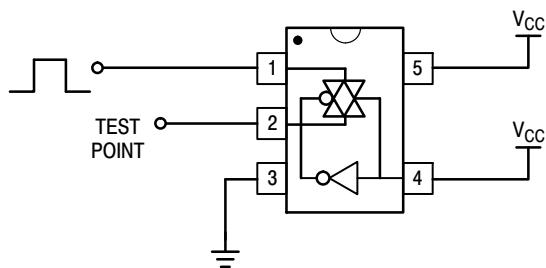


Figure 7. Propagation Delay Test Set-Up

Switch to Position 2 when testing t_{PLZ} and t_{PZL}
Switch to Position 1 when testing t_{PHZ} and t_{PZH}

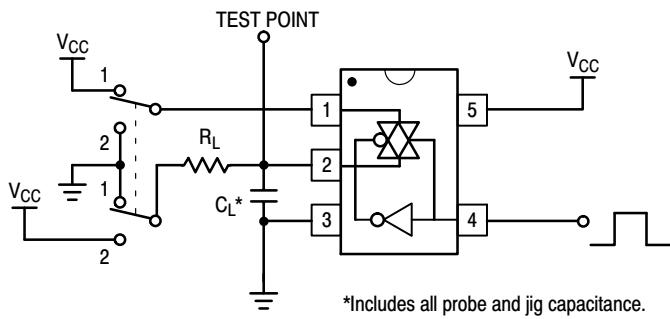


Figure 8. Propagation Delay Output Enable/Disable Test Set-Up

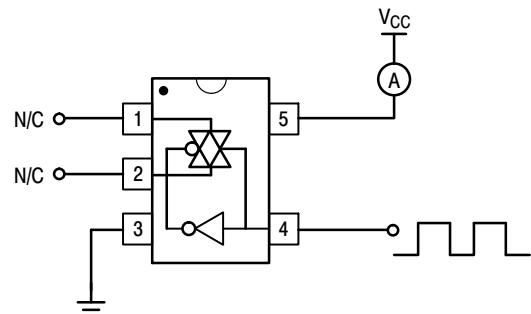


Figure 9. Power Dissipation Capacitance Test Set-Up

MC74VHC1G66

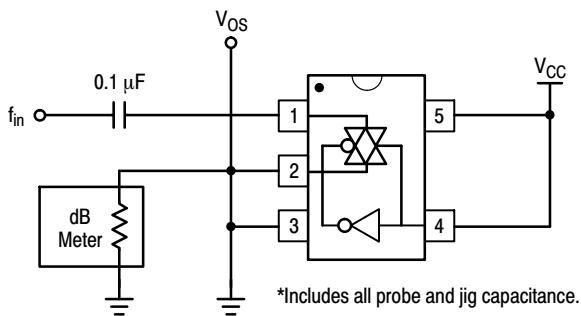


Figure 10. Maximum On-Channel Bandwidth Test Set-Up

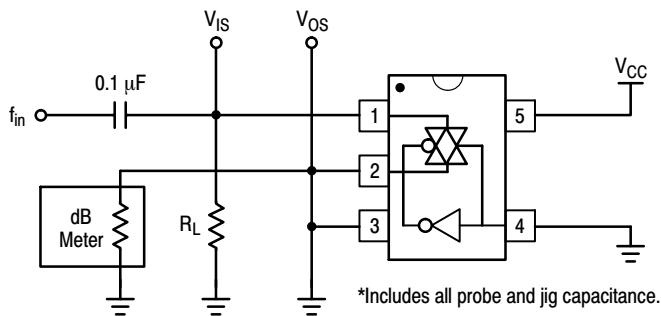


Figure 11. Off-Channel Feedthrough Isolation Test Set-Up

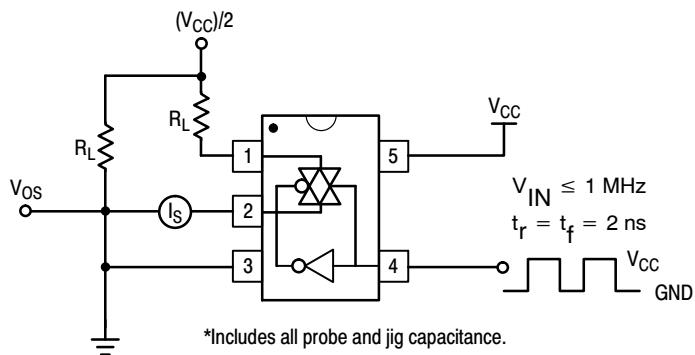


Figure 12. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set-Up

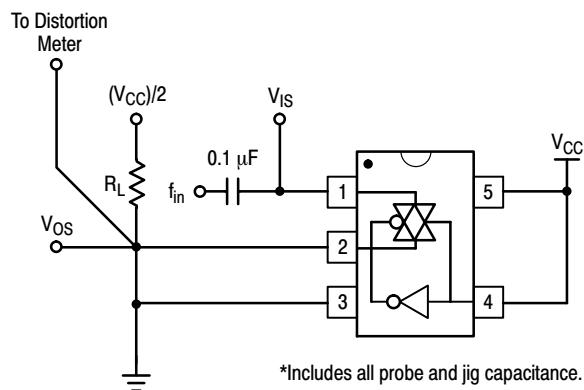


Figure 13. Total Harmonic Distortion Test Set-Up

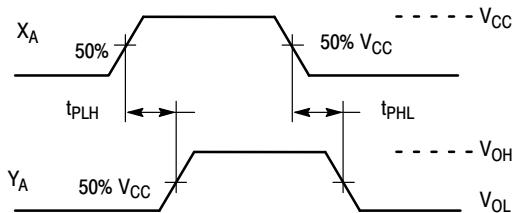


Figure 14. Propagation Delay, Analog In to Analog Out Waveforms

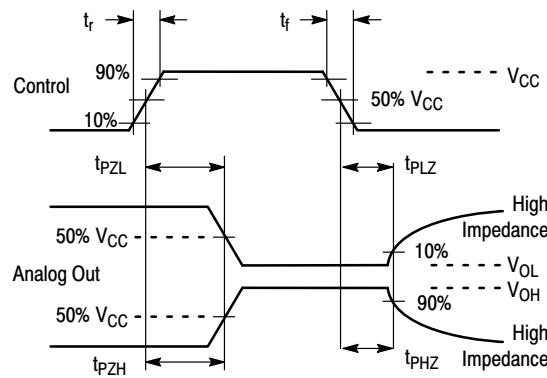


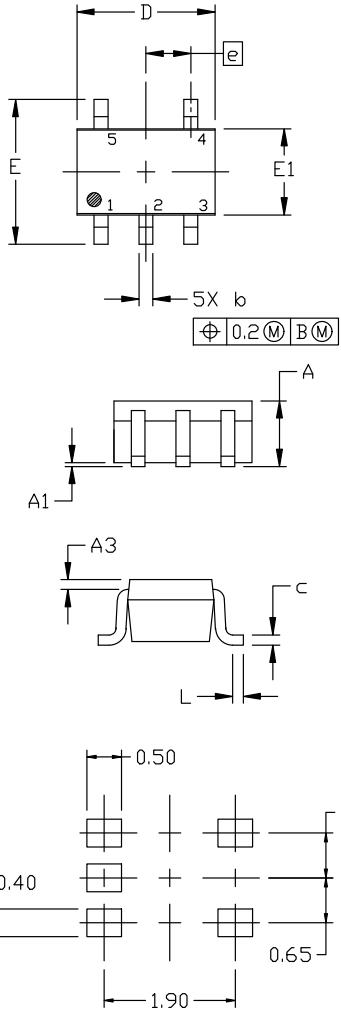
Figure 15. Propagation Delay, ON/OFF Control

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74VHC1G66DFT1G		
NLVH1G66DFT1G*	SC-88A (Pb-Free)	3000 / Tape & Reel
MC74VHC1G66DFT2G		
NLVH1G66DFT2G*		
MC74VHC1G66DTT1G	TSOP-5 (Pb-Free)	3000 / Tape & Reel
NLVH1G66DTT1G*		

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.



**RECOMMENDED
MOUNTING FOOTPRINT**

- * For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLE 1:
PIN 1. BASE
2. Emitter
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 6:
PIN 1. Emitter 2
2. BASE 2
3. Emitter 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 2:
PIN 1. ANODE
2. Emitter
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 7:
PIN 1. BASE
2. Emitter
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. Emitter

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

SC-88A (SC-70-5/SOT-353)
CASE 419A-02
ISSUE M

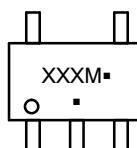
DATE 11 APR 2023

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3 0.20 REF			
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30

**GENERIC MARKING
DIAGRAM***



*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code

M = Date Code

■ = Pb-Free Package

(Note: Microdot may be in either location)

DOCUMENT NUMBER:	98ASB42984B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SC-88A (SC-70-5/SOT-353)	PAGE 1 OF 1

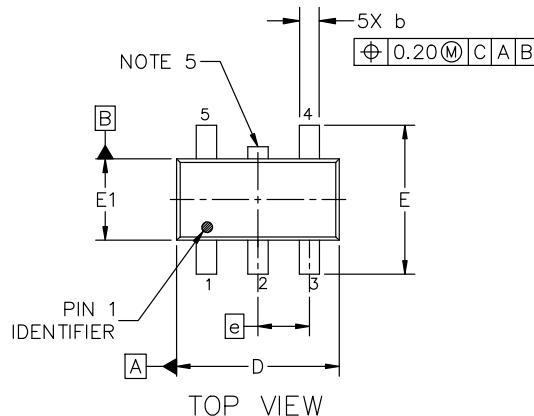
onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.



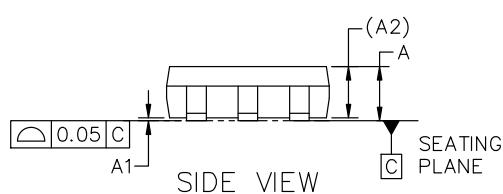
TSOP-5 3.00x1.50x0.95, 0.95P

CASE 483
ISSUE P

DATE 01 APR 2024



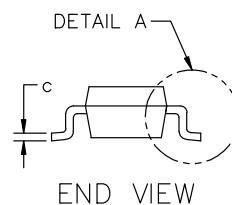
TOP VIEW



SIDE VIEW

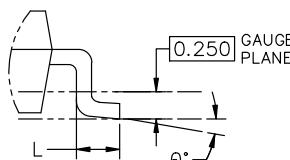
NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.



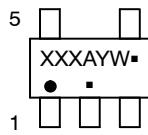
END VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2 0.950 REF.			
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e	0.950 BSC		
L	0.200	0.400	0.600
θ	0°	5°	10°



DETAIL "A"
SCALE 2:1

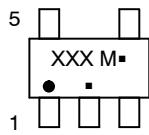
**GENERIC
MARKING DIAGRAM***



Analog

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
■ = Pb-Free Package

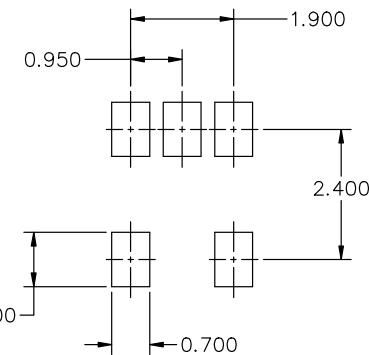
(Note: Microdot may be in either location)



Discrete/Logic

XXX = Specific Device Code
M = Date Code
■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DOCUMENT NUMBER:	98ARB18753C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TSOP-5 3.00x1.50x0.95, 0.95P	PAGE 1 OF 1

onsemi and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, **ONSEMI**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales

