

# Self-Protected Low Side Driver with Temperature and Current Limit

## NCV8405A, NCV8405B

NCV8405A/B is a three terminal protected Low-Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain-to-Gate clamping for overvoltage protection. This device is suitable for harsh automotive environments.

### Features

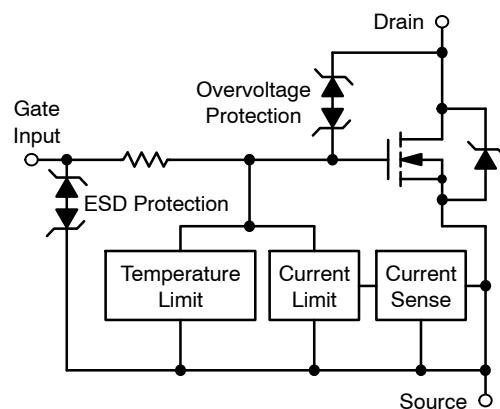
- Short-Circuit Protection
- Thermal Shutdown with Automatic Restart
- Overvoltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

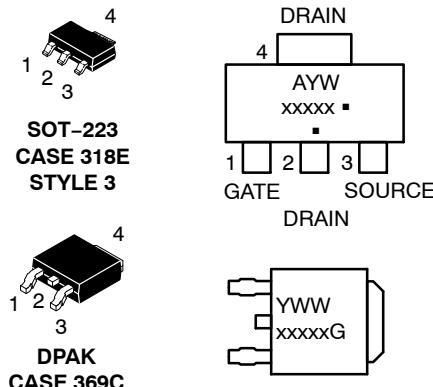
- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

V <sub>(BR)DSS</sub> (Clamped)	R <sub>DS(ON)</sub> TYP	I <sub>D</sub> MAX
42 V	90 mΩ @ 10 V	6.0 A*

\*Max current limit value is dependent on input condition.



### MARKING DIAGRAM



A = Assembly Location

Y = Year

W, WW = Work Week

xxxxx = 8405A or 8405B

G or ▀ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

# NCV8405A, NCV8405B

**MAXIMUM RATINGS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage Internally Clamped	$V_{DSS}$	42	V
Drain-to-Gate Voltage Internally Clamped ( $R_G = 1.0 \text{ M}\Omega$ )	$V_{DGR}$	42	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 14$	V
Continuous Drain Current	$I_D$	Internally Limited	
Power Dissipation – SOT-223 Version @ $T_A = 25^\circ\text{C}$ (Note 1) @ $T_A = 25^\circ\text{C}$ (Note 2) @ $T_S = 25^\circ\text{C}$	$P_D$	1.0 1.7 11.4	W
Power Dissipation – DPAK Version @ $T_A = 25^\circ\text{C}$ (Note 1) @ $T_A = 25^\circ\text{C}$ (Note 2) @ $T_S = 25^\circ\text{C}$		2.0 2.5 40	
Thermal Resistance – SOT-223 Version Junction-to-Ambient Steady State (Note 1) Junction-to-Ambient Steady State (Note 2) Junction-to-Soldering Point Steady State	$R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JS}$	130 72 11	$^\circ\text{C}/\text{W}$
Thermal Resistance – DPAK Version Junction-to-Ambient Steady State (Note 1) Junction-to-Ambient Steady State (Note 2) Junction-to-Soldering Point Steady State	$R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JS}$	60 50 3.0	
Single Pulse Drain-to-Source Avalanche Energy ( $V_{DD} = 40 \text{ V}$ , $V_G = 5.0 \text{ V}$ , $I_{PK} = 2.8 \text{ A}$ , $L = 80 \text{ mH}$ , $R_{G(ext)} = 25 \Omega$ , $T_J = 25^\circ\text{C}$ )	$E_{AS}$	275	mJ
Load Dump Voltage $V_{LD} = V_A + V_S$ ( $V_{GS} = 0$ and $10 \text{ V}$ , $R_I = 2.0 \Omega$ , $R_L = 6.0 \Omega$ , $t_d = 400 \text{ ms}$ )	$V_{LD}$	53	V
Operating Junction Temperature	$T_J$	-40 to 150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to 150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted onto min pad FR4 PCB, (2 oz. Cu, 0.06" thick).
2. Surface-mounted onto 2" sq. FR4 board (1" sq., 1 oz. Cu, 0.06" thick).

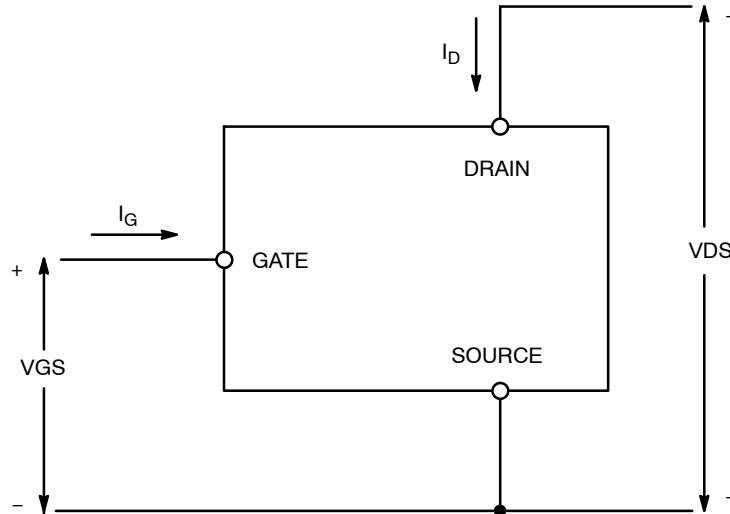


Figure 1. Voltage and Current Convention

# NCV8405A, NCV8405B

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage (Note 3)	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 10 mA, T <sub>J</sub> = 25°C	V <sub>(BR)DSS</sub>	42	46	51	V
	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 10 mA, T <sub>J</sub> = 150°C (Note 5)		42	45	51	
Zero Gate Voltage Drain Current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 32 V, T <sub>J</sub> = 25°C	I <sub>DSS</sub>		0.5	2.0	μA
	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 32 V, T <sub>J</sub> = 150°C (Note 5)			2.0	10	
Gate Input Current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 5.0 V	I <sub>GSSF</sub>		50	100	μA

## ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 150 μA	V <sub>GS(th)</sub>	1.0	1.6	2.0	V
Gate Threshold Temperature Coefficient		V <sub>GS(th)/T<sub>J</sub></sub>		4.0		-mV/°C
Static Drain-to-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.4 A, T <sub>J</sub> = 25°C	R <sub>DS(on)</sub>		90	100	mΩ
	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.4 A, T <sub>J</sub> = 150°C (Note 5)			165	190	
	V <sub>GS</sub> = 5.0 V, I <sub>D</sub> = 1.4 A, T <sub>J</sub> = 25°C			105	120	
	V <sub>GS</sub> = 5.0 V, I <sub>D</sub> = 1.4 A, T <sub>J</sub> = 150°C (Note 5)			185	210	
	V <sub>GS</sub> = 5.0 V, I <sub>D</sub> = 0.5 A, T <sub>J</sub> = 25°C			105	120	
	V <sub>GS</sub> = 5.0 V, I <sub>D</sub> = 0.5 A, T <sub>J</sub> = 150°C (Note 5)			185	210	
Source-Drain Forward On Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 7.0 A	V <sub>SD</sub>		1.05		V

## SWITCHING CHARACTERISTICS (Note 5)

Turn-ON Time (10% V <sub>IN</sub> to 90% I <sub>D</sub> )	V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 12 V I <sub>D</sub> = 2.5 A, R <sub>L</sub> = 4.7 Ω	t <sub>ON</sub>		20		μs
Turn-OFF Time (90% V <sub>IN</sub> to 10% I <sub>D</sub> )		t <sub>OFF</sub>		110		
Slew-Rate ON (70% V <sub>DS</sub> to 50% V <sub>DS</sub> )	V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 12 V, R <sub>L</sub> = 4.7 Ω	-dV <sub>DS</sub> /dt <sub>ON</sub>		1.0		V/μs
Slew-Rate OFF (50% V <sub>DS</sub> to 70% V <sub>DS</sub> )		dV <sub>DS</sub> /dt <sub>OFF</sub>		0.4		

## SELF PROTECTION CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted) (Note 4)

Current Limit	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 5.0 V, T <sub>J</sub> = 25°C (Note 6)	I <sub>LIM</sub>	6.0	9.0	11	A		
	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 5.0 V, T <sub>J</sub> = 150°C (Notes 5, 6)		3.0	5.0	8.0			
	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 10 V, T <sub>J</sub> = 25°C (Note 6)		7.0	10.5	13			
	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 10 V, T <sub>J</sub> = 150°C (Notes 5, 6)		4.0	7.5	10			
Temperature Limit (Turn-off)	V <sub>GS</sub> = 5.0 V (Notes 5, 6)		T <sub>LIM(off)</sub>	150	180	200	°C	
Thermal Hysteresis	V <sub>GS</sub> = 5.0 V		ΔT <sub>LIM(on)</sub>		15			
Temperature Limit (Turn-off)	V <sub>GS</sub> = 10 V (Notes 5, 6)		T <sub>LIM(off)</sub>	150	165	185		
Thermal Hysteresis	V <sub>GS</sub> = 10 V		ΔT <sub>LIM(on)</sub>		15			

## GATE INPUT CHARACTERISTICS (Note 5)

Device ON Gate Input Current	V <sub>GS</sub> = 5 V I <sub>D</sub> = 1.0 A	I <sub>GON</sub>		50		μA
	V <sub>GS</sub> = 10 V I <sub>D</sub> = 1.0 A			400		
Current Limit Gate Input Current	V <sub>GS</sub> = 5 V, V <sub>DS</sub> = 10 V	I <sub>GCL</sub>		0.05		mA
	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 10 V			0.4		

# NCV8405A, NCV8405B

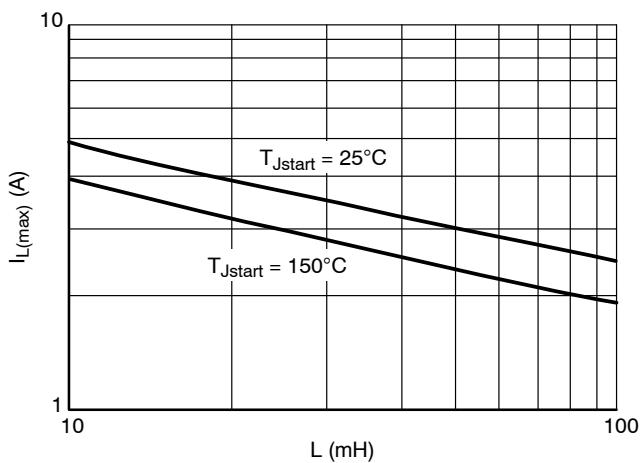
## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
<b>GATE INPUT CHARACTERISTICS</b> (Note 5)						
Thermal Limit Fault Gate Input Current	$V_{GS} = 5\text{ V}$ , $V_{DS} = 10\text{ V}$	$I_{GTL}$		0.22		mA
	$V_{GS} = 10\text{ V}$ , $V_{DS} = 10\text{ V}$			1.0		
<b>ESD ELECTRICAL CHARACTERISTICS</b> ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (Note 5)						
Electro-Static Discharge Capability	Human Body Model (HBM)	ESD	4000			V
	Machine Model (MM)		400			

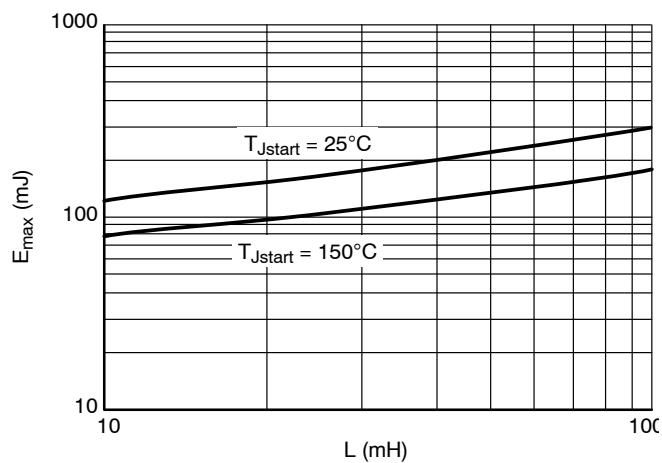
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width  $\leq 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
4. Fault conditions are viewed as beyond the normal operating range of the part.
5. Not subject to production testing.
6. Refer to Application Note AND8202/D for dependence of protection features on gate voltage.

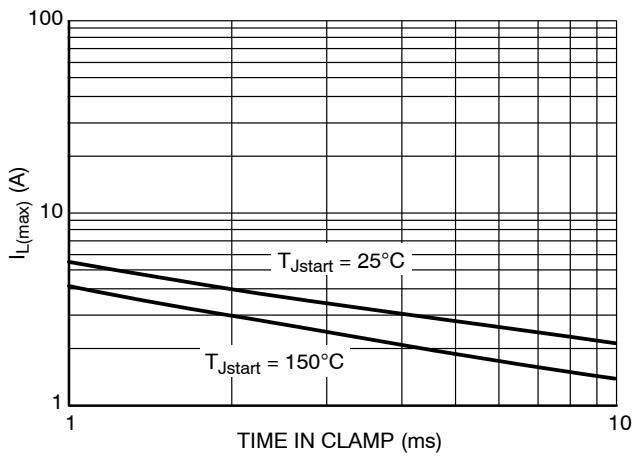
## TYPICAL PERFORMANCE CURVES



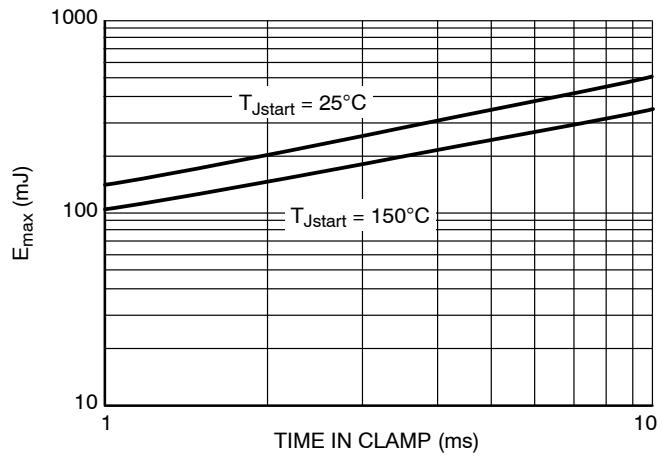
**Figure 2. Single Pulse Maximum Switch-off Current vs. Load Inductance**



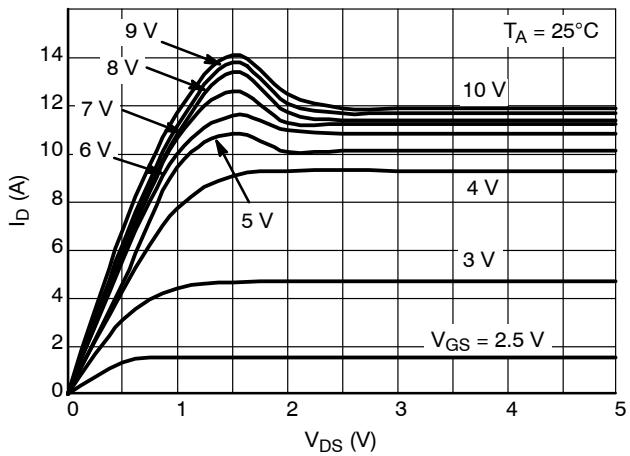
**Figure 3. Single Pulse Maximum Switching Energy vs. Load Inductance**



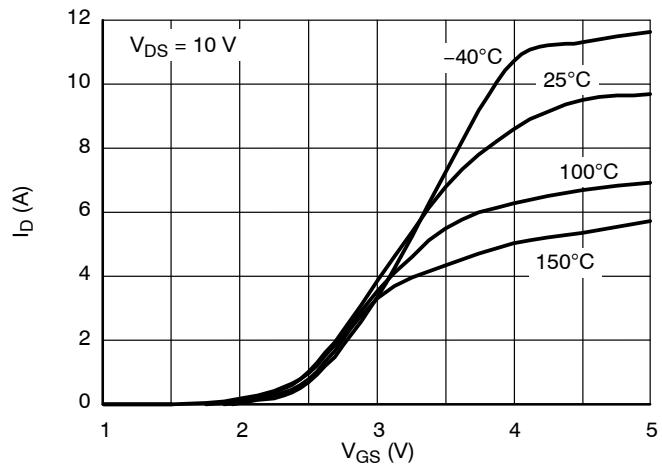
**Figure 4. Single Pulse Maximum Inductive Switch-off Current vs. Time in Clamp**



**Figure 5. Single Pulse Maximum Inductive Switching Energy vs. Time in Clamp**



**Figure 6. Output Characteristics**



**Figure 7. Transfer Characteristics**

## TYPICAL PERFORMANCE CURVES

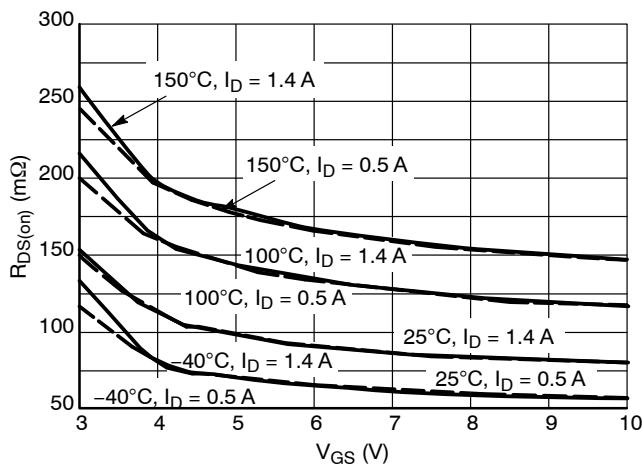


Figure 8.  $R_{DS(on)}$  vs. Gate-Source Voltage

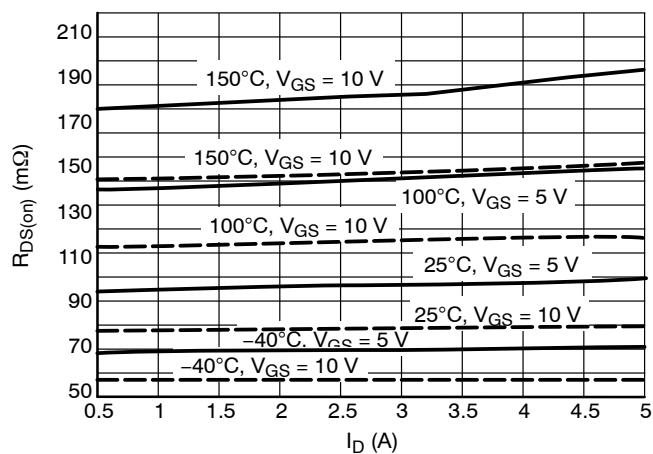


Figure 9.  $R_{DS(on)}$  vs. Drain Current

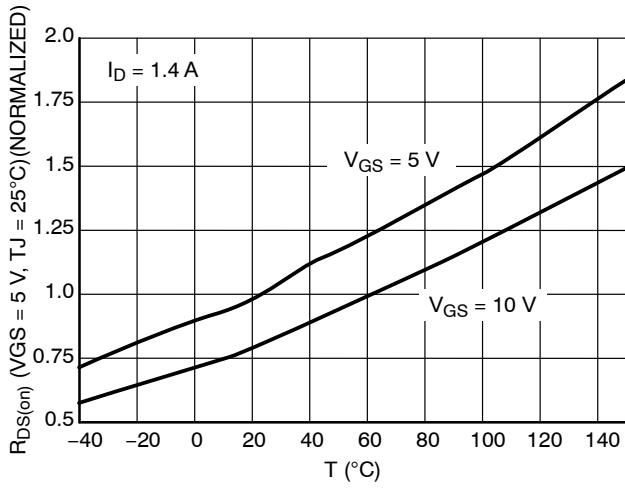


Figure 10. Normalized  $R_{DS(on)}$  vs. Temperature

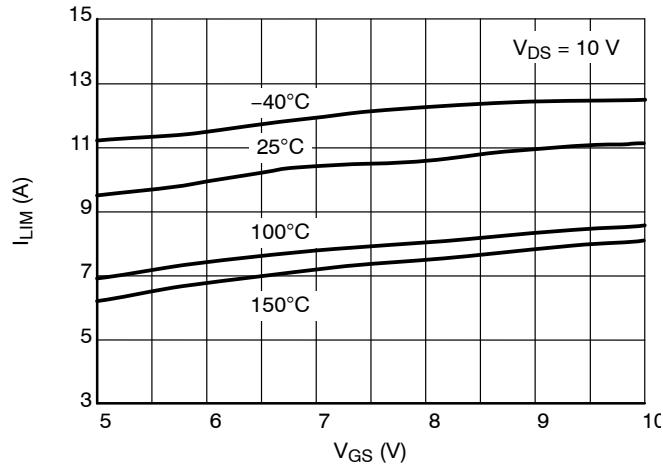


Figure 11. Current Limit vs. Gate-Source Voltage

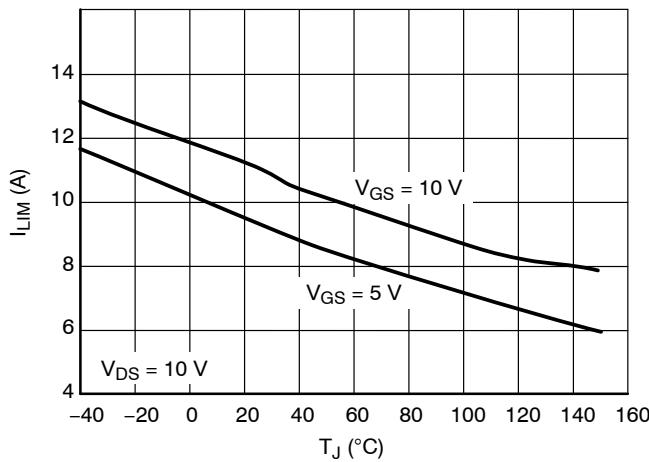


Figure 12. Current Limit vs. Junction Temperature

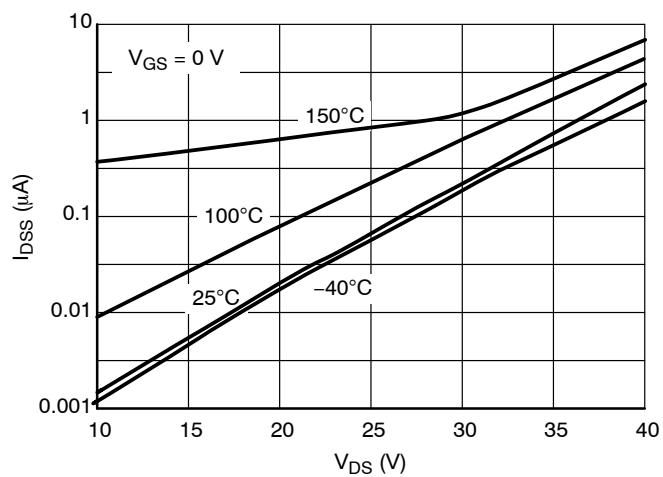


Figure 13. Drain-to-Source Leakage Current

## TYPICAL PERFORMANCE CURVES

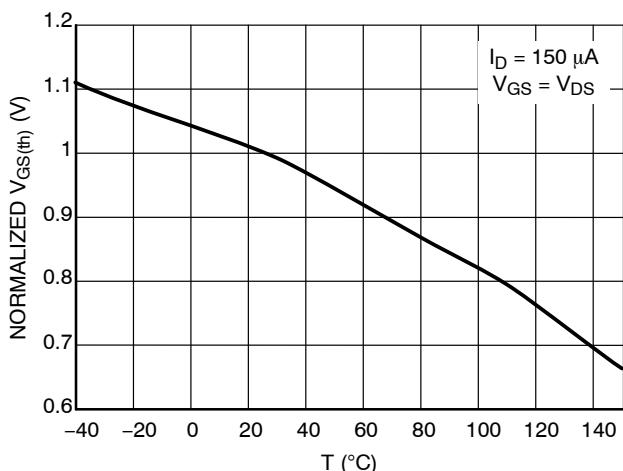


Figure 14. Normalized Threshold Voltage vs. Temperature

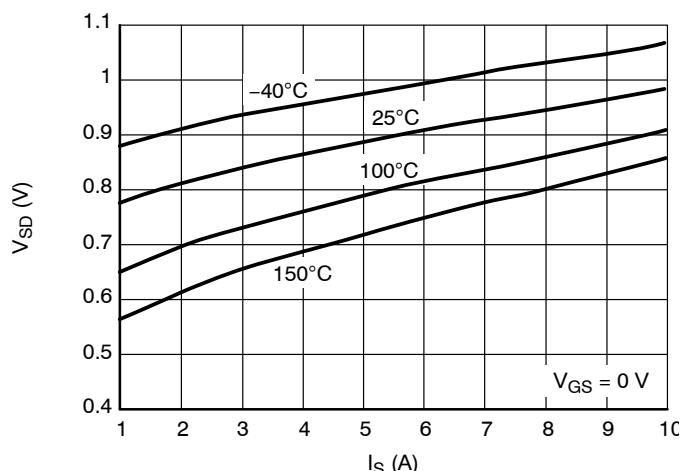


Figure 15. Body-Diode Forward Characteristics

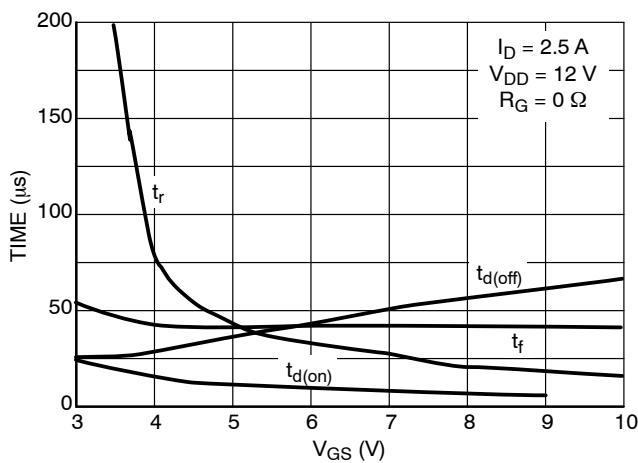


Figure 16. Resistive Load Switching Time vs. Gate-Source Voltage

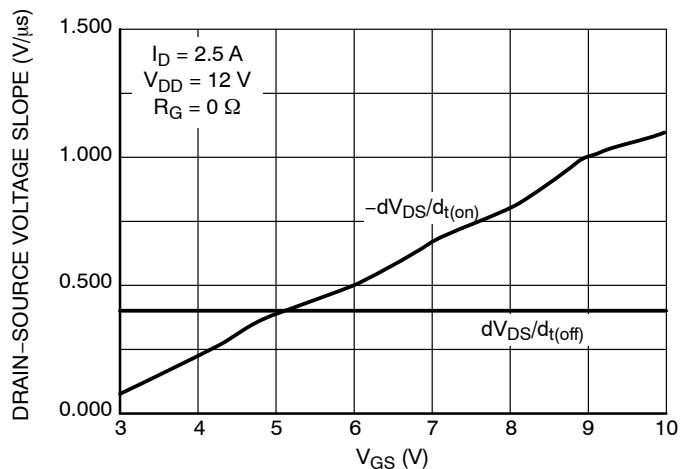


Figure 17. Resistive Load Switching Drain-Source Voltage Slope vs. Gate-Source Voltage

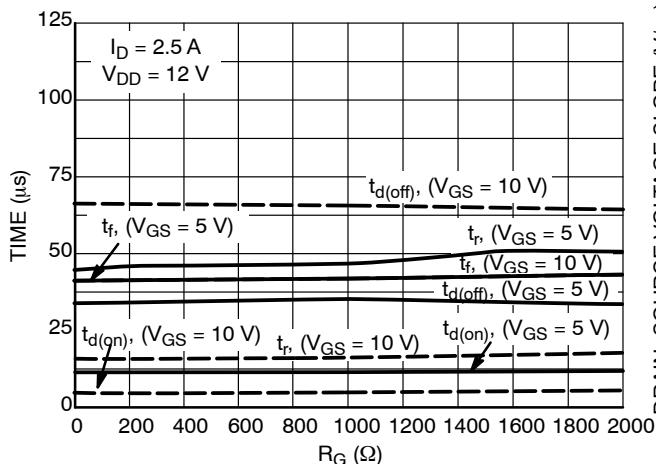


Figure 18. Resistive Load Switching Time vs. Gate Resistance

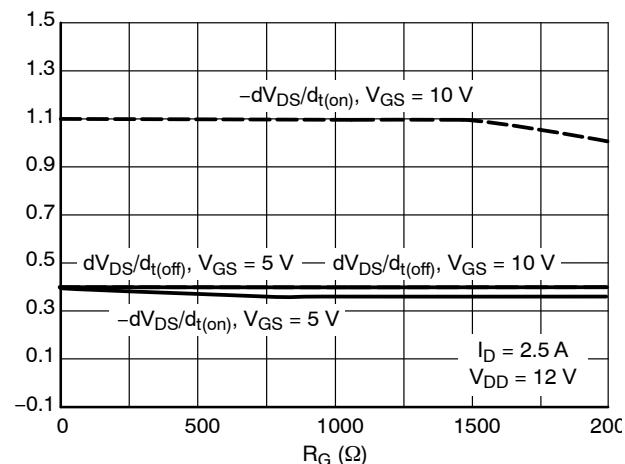


Figure 19. Drain-Source Voltage Slope during Turn On and Turn Off vs. Gate Resistance

# NCV8405A, NCV8405B

## TYPICAL PERFORMANCE CURVES

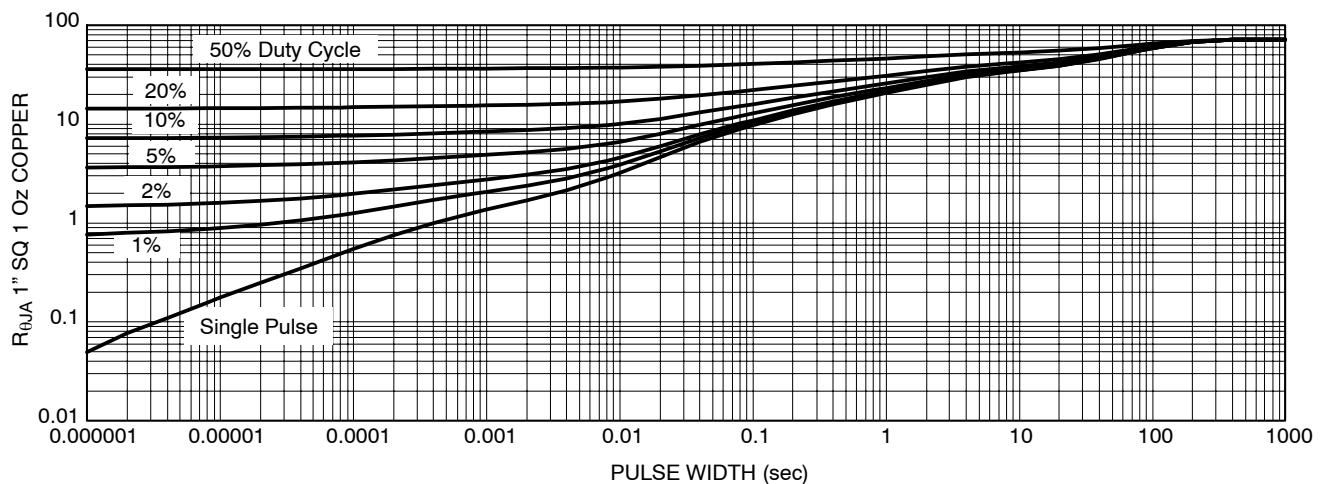


Figure 20. Transient Thermal Resistance

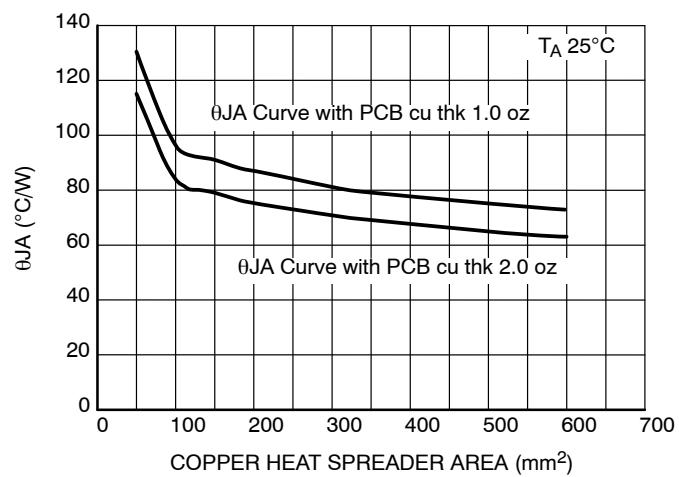
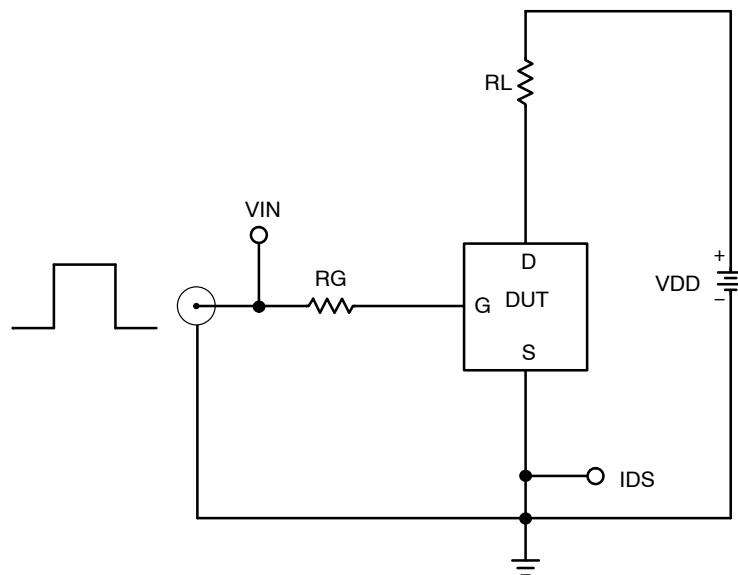
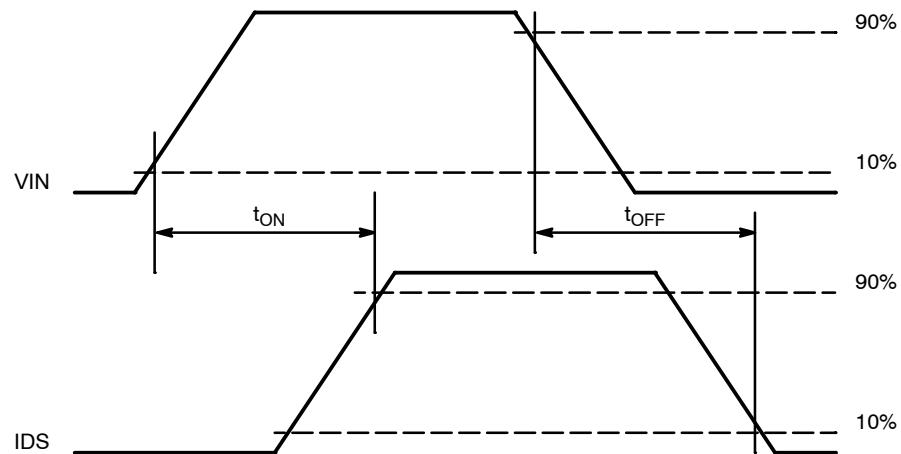


Figure 21.  $\theta_{JA}$  vs. Copper

**TEST CIRCUITS AND WAVEFORMS**



**Figure 22. Resistive Load Switching Test Circuit**



**Figure 23. Resistive Load Switching Waveforms**

TEST CIRCUITS AND WAVEFORMS

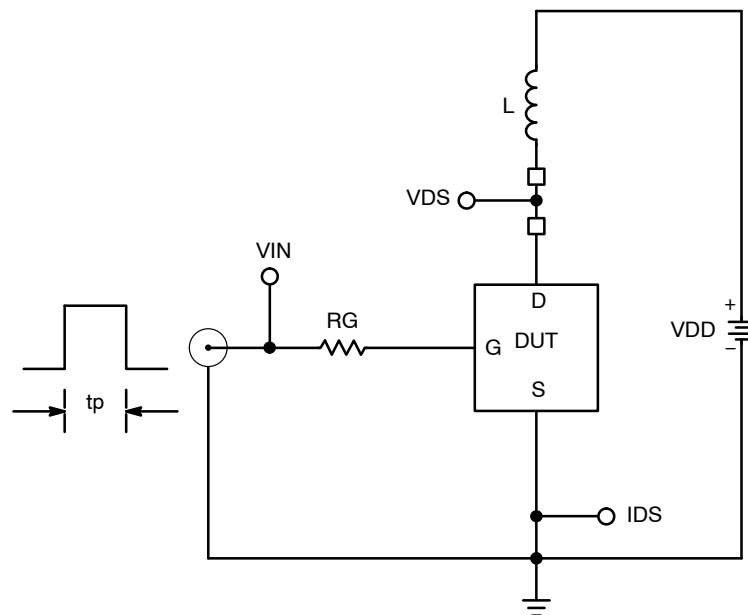


Figure 24. Inductive Load Switching Test Circuit

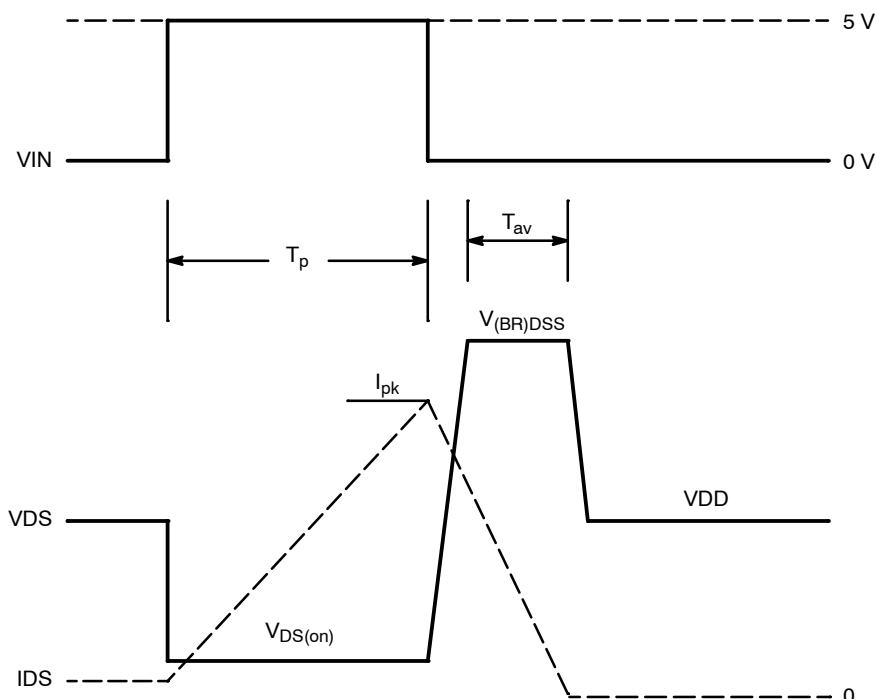


Figure 25. Inductive Load Switching Waveforms

## NCV8405A, NCV8405B

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NCV8405ASTT1G	SOT-223 (Pb-Free)	1000 / Tape & Reel
NCV8405ASTT3G	SOT-223 (Pb-Free)	4000 / Tape & Reel
NCV8405ADTRKG	DPAK (Pb-Free)	2500 / Tape & Reel
NCV8405BDTRKG	DPAK (Pb-Free)	2500 / Tape & Reel

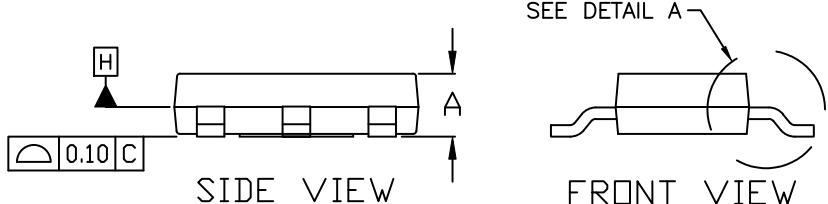
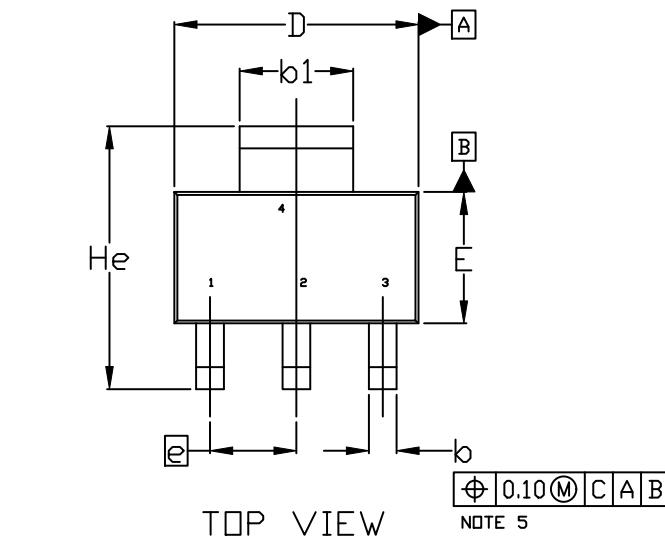
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



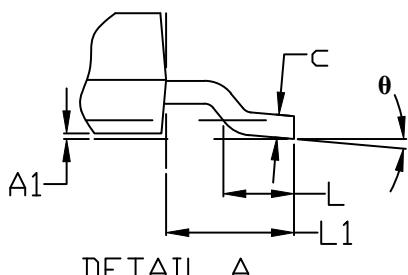
SCALE 1:1

**SOT-223 (TO-261)**  
CASE 318E-04  
ISSUE R

DATE 02 OCT 2018



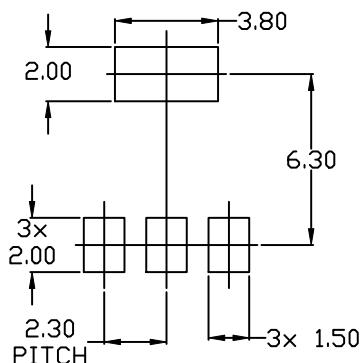
FRONT VIEW



## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
$\theta$	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

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DESCRIPTION:	SOT-223 (TO-261)	PAGE 1 OF 2

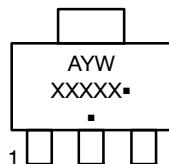
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**SOT-223 (TO-261)**  
**CASE 318E-04**  
**ISSUE R**

DATE 02 OCT 2018

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. Emitter 4. COLLECTOR	STYLE 2: PIN 1. ANODE 2. CATHODE 3. NC 4. CATHODE	STYLE 3: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 4: PIN 1. SOURCE 2. DRAIN 3. GATE 4. DRAIN	STYLE 5: PIN 1. DRAIN 2. GATE 3. SOURCE 4. GATE
STYLE 6: PIN 1. RETURN 2. INPUT 3. OUTPUT 4. INPUT	STYLE 7: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2 4. CATHODE	STYLE 8: CANCELLED	STYLE 9: PIN 1. INPUT 2. GROUND 3. LOGIC 4. GROUND	STYLE 10: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE
STYLE 11: PIN 1. MT 1 2. MT 2 3. GATE 4. MT 2	STYLE 12: PIN 1. INPUT 2. OUTPUT 3. NC 4. OUTPUT	STYLE 13: PIN 1. GATE 2. COLLECTOR 3. Emitter 4. COLLECTOR		

**GENERIC  
MARKING DIAGRAM\***



A = Assembly Location

Y = Year

W = Work Week

XXXXX = Specific Device Code

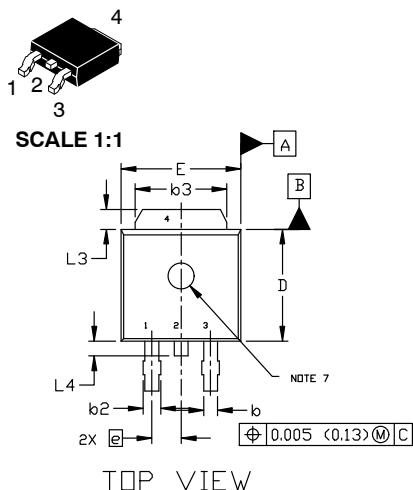
■ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	SOT-223 (TO-261)	PAGE 2 OF 2

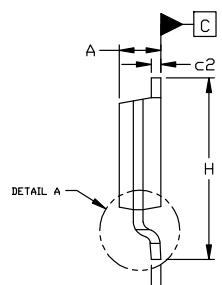
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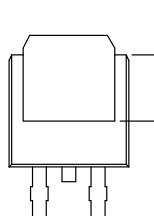
TOP VIEW

**DPAK (SINGLE GAUGE)**  
CASE 369C  
ISSUE G

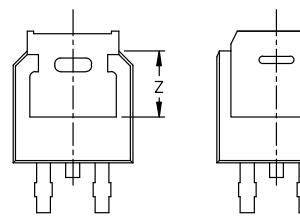
DATE 31 MAY 2023



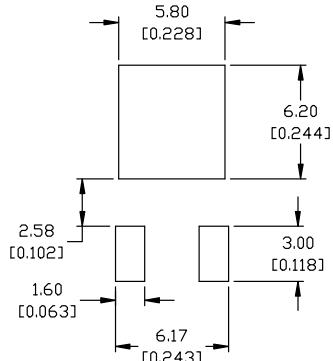
SIDE VIEW



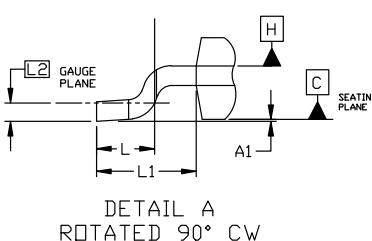
BOTTOM VIEW



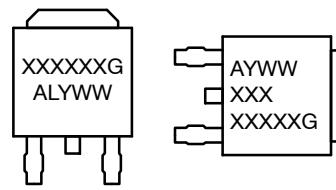
BOTTOM VIEW



ALTERNATE CONSTRUCTIONS

DETAIL A  
ROTATED 90° CW

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC	0.229 BSC		
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF	0.290 REF		
L2	0.020 BSC	0.51 BSC		
L3	0.035	0.050	0.89	1.27
L4	----	0.040	----	1.01
Z	0.155	----	3.93	----

**GENERIC  
MARKING DIAGRAM\***


XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

## RECOMMENDED MOUNTING FOOTPRINT\*

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

STYLE 1:  
PIN 1. BASE  
2. COLLECTOR  
3. Emitter  
4. COLLECTOR

STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

STYLE 3:  
PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. CATHODE

STYLE 4:  
PIN 1. CATHODE  
2. ANODE  
3. GATE  
4. ANODE

STYLE 5:  
PIN 1. GATE  
2. ANODE  
3. CATHODE  
4. ANODE

STYLE 6:  
PIN 1. MT1  
2. MT2  
3. GATE  
4. MT2

STYLE 7:  
PIN 1. GATE  
2. COLLECTOR  
3. Emitter  
4. COLLECTOR

STYLE 8:  
PIN 1. N/C  
2. CATHODE  
3. ANODE  
4. CATHODE

STYLE 9:  
PIN 1. ANODE  
2. CATHODE  
3. RESISTOR ADJUST  
4. CATHODE

STYLE 10:  
PIN 1. CATHODE  
2. ANODE  
3. CATHODE  
4. ANODE

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DESCRIPTION:	DPAK (SINGLE GAUGE)	PAGE 1 OF 1

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