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AK5734

4-Channel Differential Audio ADC with Diagnostics

1. General Description

The AK5734 is a 4-channel audio ADC with an integrated SAR ADC, enabling robust error detection. The error detection function monitors the connection status of the line and microphone inputs. The AK5734 includes mic PGAs (pre-gain amplifiers) and programmable microphone bias. These functions make it ideal for microphone array applications such as automotive ANC (Active Noise Cancelation). The digital audio interface supports I^2S, multi-slot TDM, and left-justified formats, making it easy to connect to your DSP of choice.

2. Features

1. Audio ADC
- **4-Channel Audio ADC**
- **Full-differential Input and Single-ended Input**
- **PGA for Microphone: 0dB or 6dB - 20dB (1dB step)**
- **Input Voltage: 2.0 Vrms**
- **ADC Performance:**
  - **S/(N+D): typ 92B**
  - **DR, S/N: typ 100dB**
- **5 Types of LPF**
  - **Voice Filter**
  - **Sharp Roll Off Filter**
  - **Slow Roll Off Filter**
  - **Short Delay Sharp Roll Off Filter (GD=4.9/fs)**
  - **Short Delay Slow Roll Off Filter (GD=4.3/fs)**
- **Digital Volume: MUTE, -115dB - +52dB (1dB step)**
- **Digital HPF for DC-offset cancellation: fc=2Hz**

2. Sampling Rate: 8kHz - 192kHz

3. Master Clock: 128fs, 192fs, 256fs, 384fs, 512fs, 1024fs, 2048fs

4. Master/Slave Mode

5. Audio Interface Format: MSB First, 2's complement
- **16/24bit I^2S**
- **16/24bit Left justified**
- **16/24bit TDM interface up to 16ch cascaded connection**

6. SAR ADC
- **1ch SAR ADC for Error Detection**

7. Error Detect Function
- **Open**
- **Short across Inputs**
- **Short to Ground**
- **Short to MIC Bias Voltage**
- **Short to Battery**
- **MIC Bias Over Current/Voltage**
- **Charge Pump Under Voltage**
- **Over Temperature**

8. Programmable MIC Bias Voltage: 5V - 9V (0.5V step)

9. µP I/F: I^2C-Bus (Ver 1.0, 400kHz mode) or SPI

10. Power Supply:
- **AVDD= 3.0 - 3.6V (typ. 3.3V)**
- **DVDD = 3.0 - 3.6V (typ. 3.3V) or 1.7- 1.98V (typ. 1.8V)**
- **CPVDD = 3.0 - 3.6V (typ. 3.3V)**

11. Operating Temperature Range: Ta = –40 - 105°C

12. Package: 48-pin QFN (7x7mm, 0.5mm pitch)

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3. Table of Contents

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4. Block Diagram

■ Block Diagram

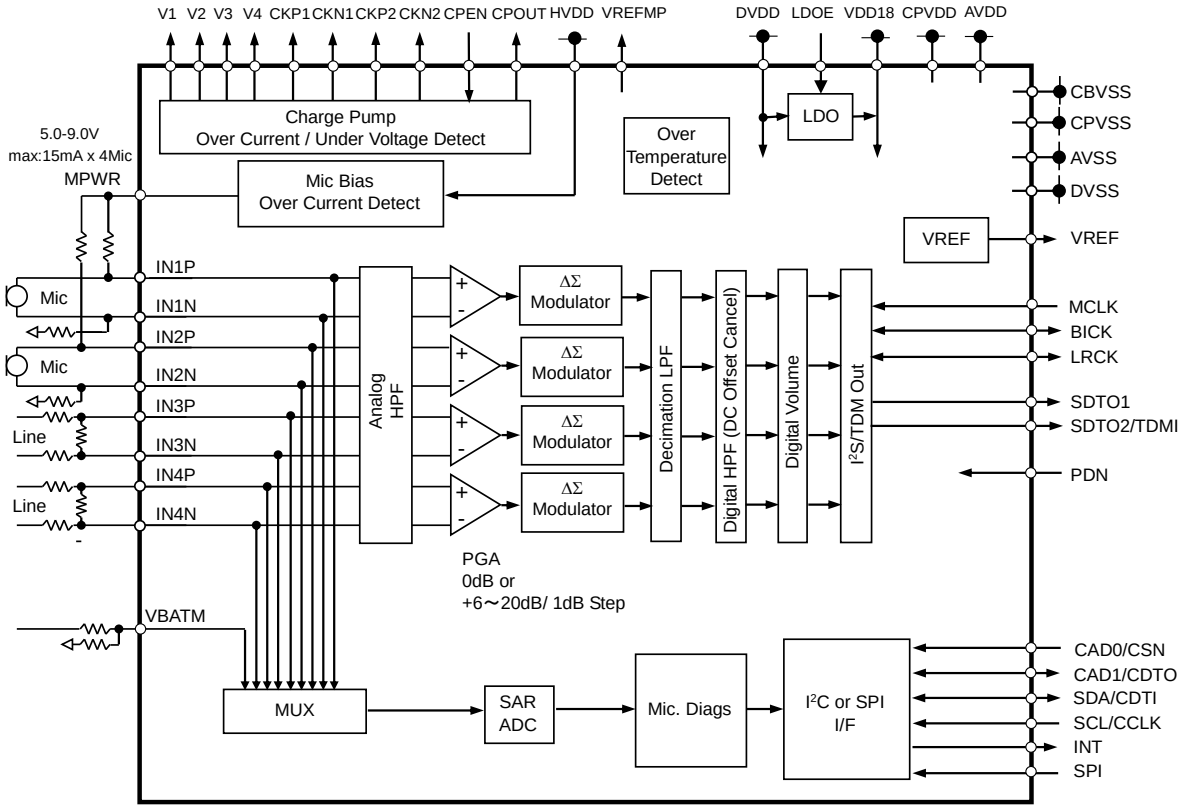

Figure 1. AK5734 Block Diagram

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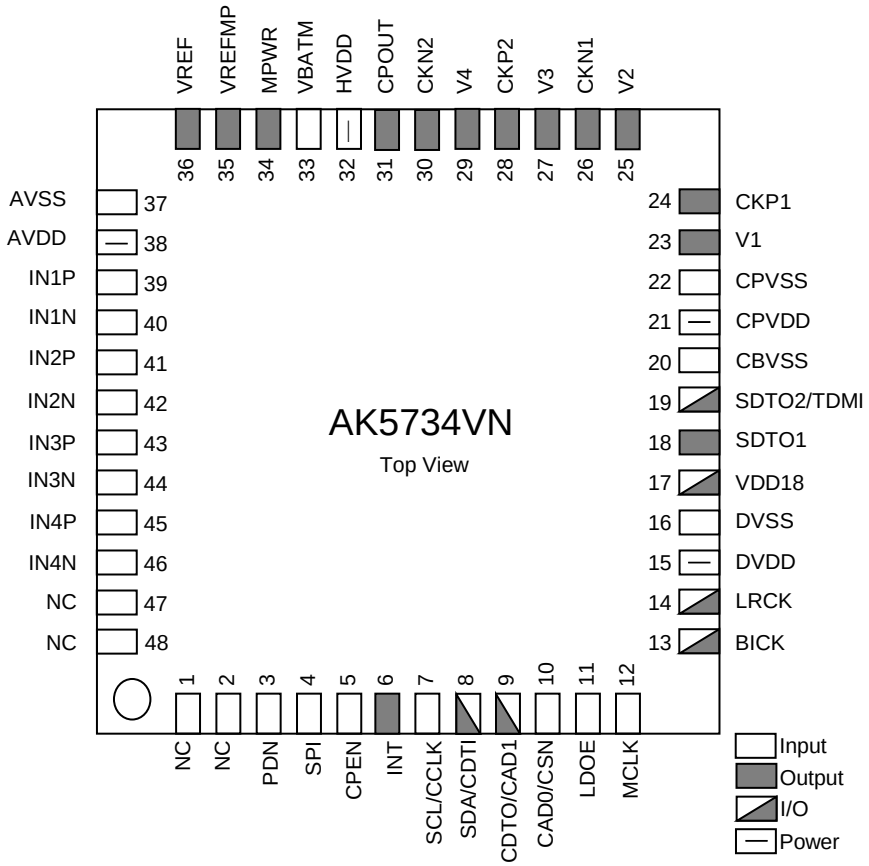
5. Pin Configurations and Functions

■ Pin Configurations



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■ Pin Functions

No.	Pin Name	I/O	Function	State at Power Down
1	NC	-	This pin should be connected to AVSS or DVDD	-
2	NC	-	This pin should be connected to AVSS or DVDD	-
3	PDN	I	Power-Down Mode Pin The AK5734 is in power-down mode and it is held at reset when the PDN pin = “L”. Bringing the PDN pin high brings the device out of reset. The AK5736 operates normally when the PDN pin =”H”.	Hi-z
4	SPI	I	Control Mode Select Pin “L”: I^{2}C Bus control mode, “H”: 4-wire serial control mode	Hi-z
5	CPEN	I	Internal Charge Pump Enable/Disable Pin. “L”: Enable, Voltage that is boosted by internal charge pump is supplied from the CPOUT pin to the HVDD pin. Connect CPOUT pin to the HVDD pin externally. “H”: Disable, Internal charge pump is powered down. An external voltage should be supplied to the HVDD pin. In this case, connect AVDD to the CPVDD pin externally.	Hi-z
6	INT	O	Interrupt Signal Output Pin (Active “L”) Connect this pin to DVDD via an external 10kΩ resistor.	Hi-z
7	SCL	I	(SPI pin = “L”) Control Data Clock Pin in I^{2}C Bus control mode	Hi-z
	CCLK		(SPI pin = “H”) Control Data Clock Pin in 4-wire serial control mode	
8	SDA	I/O	(SPI pin = “L”) Control Data Input / Output Pin in I^{2}C Bus control mode	Hi-z
	CDTI	I	(SPI pin = “H”) Control Data Input Pin in 4-wire serial control mode	
9	CAD1	I	(SPI pin = “L”) Chip Address 1 Pin in I^{2}C Bus control mode	Hi-z
	CDTO	O	(SPI pin = “H”) Control Data Output Pin in 4-wire serial control mode	
10	CAD0	I	(SPI pin = “L”) Chip Address 0 Pin in I^{2}C Bus control mode	Hi-z
	CSN		(SPI pin = “H”) Chip Select Pin in serial control mode in 4-wire serial control mode	
11	LDOE	I	LDO Enable Pin “L”: LDO Disable, “H”: LDO Enable	Hi-z
12	MCLK	I	Master Clock Input Pin	Hi-z
13	BICK	I/O	Audio Serial Data Clock Pin	Pulled-down by 100kΩ
14	LRCK	I/O	Channel Clock Pin	Pulled-down by 100kΩ
15	DVDD	-	Digital Power Supply Pin, 3.0 - 3.6V or 1.7 - 1.98V Connect this pin to DVSS via a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic capacitor.	-
16	DVSS	-	Digital Ground Pin 0V	-
17	VDD18	-	Digital Core Power Supply Pin, 1.7 - 1.98V (LDOE pin= “L”)	-
		O	LDO Stabilization Capacitor Connect Pin. (LDOE pin= “H”) Connect a 4.7μF -40% - +20% ceramic capacitor to this pin.	Pulled-down by 500Ω

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No.	Pin Name	I/O	Function	State at Power Down
18	SDTO1	O	Audio Serial Data Output1 Pin	"L"
19	SDTO2	O	Audio Serial Data Output2 Pin	Pulled-down by 100kΩ
	TDMI	I	TDM Data Input Pin	
20	CBVSS	-	Charge Pump Ground Pin, 0V	-
21	CPVDD	-	Charge Pump Power Supply Pin, 3.0 - 3.6V Connect this pin to CPVSS via a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic capacitor.	-
22	CPVSS	-	Charge Pump Ground Pin, 0V	-
23	V1	O	Charge Pump Boost Pin Do not connect this pin to an external device to draw current. Connect a 2.2uF-40% - +20% capacitor between the CKP1 pin and this pin.	Pulled-up to CPVDD by 100kΩ
24	CKP1	O	Charge Pump Clock pin	"L"
25	V2	O	Charge Pump Boost Pin Do not connect this pin to an external device to draw current. Connect a 2.2uF-40% - +20% capacitor between the CKN1 pin and this pin.	Pulled-up to CPVDD by 200kΩ
26	CKN1	O	Charge Pump Clock pin	"H" (CPVDD)
27	V3	O	Charge Pump Boost Pin Do not connect this pin to an external device to draw current. Connect a 2.2uF-40% - +20% capacitor between the CKP2 pin and this pin.	Pulled-up to CPVDD by 300kΩ
28	CKP2	O	Charge Pump Clock pin	"L"
29	V4	O	Charge Pump Boost Pin Do not connect this pin to an external device to draw current. Connect a 2.2uF-40% - +20% capacitor between the CKN2 pin and this pin.	Pulled-up to CPVDD by 400kΩ
30	CKN2	O	Charge Pump Clock pin	"H" (CPVDD)
31	CPOUT	O	Charge Pump Output Pin Connect HVDD to this pin externally when using the internal charge pump (CPEN pin = "L"). This pin should also be connected to AVSS via a 10uF ceramic capacitor. This pin should be open when not using the internal charge pump (CPEN pin = "H").	Pulled-up to CPVDD by 500kΩ
32	HVDD	I	High voltage power input pin Connect this pin to a load dump protected 12V - 16V. When CPEN pin="H", HVDD voltage, not a charge pump, makes the analog voltage like a MIC bias voltage and Pre Gain Amp etc.	-
33	VBATM	I	Battery Power Monitor Pin	Pulled-down by 1MΩ

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No.	Pin Name	I/O	Function	State at Power Down
34	MPWR	O	MIC Bias Voltage Output Pin Normally, connect this pin to AVSS via a 1ohm resistor and a 10μF ceramic capacitor. * The maximum bias is 9V. The capacitance of the connecting external capacitor must be a minimum of 3.5μF and maximum of 10μF+20%, including variation tolerance, including temperature change and bias voltage difference. The external capacitor must be mounted as close as possible to the MPWR pin. A variation of a 1ohm external resistor must be within ±10% including allowable value and temperature drift. At startup, a maximum of 500mA current may flow. Note to the allowable power of the resistor and the capacity of the HVDD power supply.	Pulled-down by 4.5kΩ
35	VREFMP	O	Voltage Reference Pin for MPWR. Connect this pin to AVSS via a 2.2μF capacitor.	Pulled-down by 188kΩ
36	VREF	O	Voltage Reference Decoupling Pin Connect this pin to AVSS via a 1.0μF capacitor.	Pulled-down by 500Ω
37	AVSS	-	Analog Ground pin 0V	-
38	AVDD	-	Analog Power Supply Pin, 3.0 - 3.6V Normally, connect this pin to AVSS via a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic capacitor.	-
39	IN1P	I	Ch1 Positive Input Pin	Pulled-down by 1.4MΩ
40	IN1N	I	Ch1 Negative Input Pin	Pulled-down by 1.4MΩ
41	IN2P	I	Ch2 Positive Input Pin	Pulled-down by 1.4MΩ
42	IN2N	I	Ch2 Negative Input Pin	Pulled-down by 1.4MΩ
43	IN3P	I	Ch3 Positive Input Pin	Pulled-down by 1.4MΩ
44	IN3N	I	Ch3 Negative Input Pin	Pulled-down by 1.4MΩ
45	IN4P	I	Ch4 Positive Input Pin	Pulled-down by 1.4MΩ
46	IN4N	I	Ch4 Negative Input Pin	Pulled-down by 1.4MΩ
47	NC	-	This pin should be connected to AVSS or DVDD	-
48	NC	-	This pin should be connected to AVSS or DVDD	-
-	EP	-	Exposed Pad Connect the pad to AVSS.	-

Note 1. All digital input pins should not be left floating.

■ Handling of Unused Pins

The unused I/O pins should be connected appropriately.

Classification	Pin Name	Setting
Analog	IN1-4P, IN1-4N	Open
	V1, V2, V3, V4, CPOUT, CKP1, CKN1, CKP2, CKN2	Open
	MPWR, VBATM	Open
Digital	SDTO1-2, INT, CDTO	Open

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Note that output pins with no corresponding input data will still receive (and therefore output) non-zero noise data from their respective ADC. Therefore, unused data output pins should be muted via the digital volume feature.

Note that TDM slot layout is fixed – slots with no corresponding input data will contain zeroes if muted, ADC noise data if not muted.

When not using the internal charge pump and the MPWR pin, power up the AK5734 after setting PDMPN bit (address 5EH) = "0" and RSTN bit = "1". In I^2C bus mode, AK5734's roll over address is 4BH, therefore set the address to 5EH directly.

6. Absolute Maximum Ratings

(AVSS = DVSS = CPVSS = CBVSS = 0V;

Parameter		Symbol	Min.	Max.	Unit
Power Supplies:	Analog (AVDD pin)	AVDD	−0.3	5.5	V
	Digital Interface (DVDD pin)	DVDD	−0.3	5.5	V
	Digital Core (VDD18 pin) (Note 3)	VDD18	−0.3	1.98	V
	Charge Pump (CPVDD pin)	CPVDD	−0.3	5.5	V
	High Voltage (HVDD pin)	HVDD	−0.3	18	V
Input Current (Any Pin Except Supplies)		IIN	-	±10	mA
IN1-4P, IN1-4N Input Voltage (Note 4)					
No protection resistor		VINA	−0.3	10.1	V
With protection resistor (use MPWR pin)		VINR	−0.3	18	V
With protective resistor (not use MPWR pin)		VINR	−0.3	48	V
VBATM	(ATTVB bit = "0")	VINBAT	−0.3	18	V
	(ATTVB bit = "1")		−0.3	10.1	
Digital Input Voltage		VIND	−0.3	DVDD+0.3	V
Ambient Temperature (Power applied)		Ta	−40	105	°C
Storage Temperature		Tstg	−65	150	°C

Note 2)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies:	Analog (AVDD pin)	AVDD	−0.3	5.5	V
	Digital Interface (DVDD pin)	DVDD	−0.3	5.5	V
	Digital Core (VDD18 pin) (Note 3)	VDD18	−0.3	1.98	V
	Charge Pump (CPVDD pin)	CPVDD	−0.3	5.5	V
	High Voltage (HVDD pin)	HVDD	−0.3	18	V
Input Current (Any Pin Except Supplies)		IIN	-	±10	mA
IN1-4P, IN1-4N Input Voltage (Note 4)					
No protection resistor		VINA	−0.3	10.1	V
With protection resistor (use MPWR pin)		VINR	−0.3	18	V
With protective resistor (not use MPWR pin)		VINR	−0.3	48	V
VBATM	(ATTVB bit = "0")	VINBAT	−0.3	18	V
	(ATTVB bit = "1")		−0.3	10.1	
Digital Input Voltage		VIND	−0.3	DVDD+0.3	V
Ambient Temperature (Power applied)		Ta	−40	105	°C
Storage Temperature		Tstg	−65	150	°C

Note 2: All voltages are with respect to ground. AVSS, DVSS and CPVSS must be connected to the same analog ground plane.

Note 3: When an external power supply is connected to the VDD18 and the 1.8V LDO is Off, (LDOE pin="L").

Note 4: The maximum voltage depends on the presence or absence of protection resistors. If a short between the battery and analog input is expected, insert a protection resistor. VINA is the voltage at IN1-4P and IN1-4N pins, and VINR is the voltage at the signal source side of the protection resistor. Refer to Recommended External Circuits.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

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7. Recommended Operating Conditions

(AVSS = DVSS = CPVSS = CBVSS = 0V;

Parameter		Symbol	Min.	Max.	Unit
Power Supplies:	Analog (AVDD pin)	AVDD	−0.3	5.5	V
	Digital Interface (DVDD pin)	DVDD	−0.3	5.5	V
	Digital Core (VDD18 pin) (Note 3)	VDD18	−0.3	1.98	V
	Charge Pump (CPVDD pin)	CPVDD	−0.3	5.5	V
	High Voltage (HVDD pin)	HVDD	−0.3	18	V
Input Current (Any Pin Except Supplies)		IIN	-	±10	mA
IN1-4P, IN1-4N Input Voltage (Note 4)					
No protection resistor		VINA	−0.3	10.1	V
With protection resistor (use MPWR pin)		VINR	−0.3	18	V
With protective resistor (not use MPWR pin)		VINR	−0.3	48	V
VBATM	(ATTVB bit = “0”)	VINBAT	−0.3	18	V
	(ATTVB bit = “1”)		−0.3	10.1	
Digital Input Voltage		VIND	−0.3	DVDD+0.3	V
Ambient Temperature (Power applied)		Ta	−40	105	°C
Storage Temperature		Tstg	−65	150	°C

Note 2)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies	Analog (AVDD pin)	AVDD	3.0	3.3	3.6	V
	(LDOE pin= “L”) (Note 5)					
	Digital Interface (DVDD pin) (Note 6)	DVDD	1.7	1.8	1.98	V
	Digital Core (VDD18 pin)	VDD18	1.7	1.8	1.98	V
	(LDOE pin= “H”) (Note 7)					
	Digital Interface (DVDD pin)	DVDD	3.0	3.3	3.6	V
	Charge Pump (CPVDD pin) (Note 8)	CPVDD	3.0	3.3	3.6	V
	Analog (HVDD pin) (Note 9)	HVDD	12	14.5	16	V

Note 2: All voltages are with respect to ground. AVSS, DVSS and CPVSS must be connected to the same analog ground plane.

Note 5: DVDD must be powered up before or at the same time as VDD18 when the LDOE pin=“L”. The power up sequence between AVDD and DVDD, AVDD and VDD18 are not critical.

Note 6: DVDD should be in the range of VDD18 ±0.1V when the LDOE pin= “L”.

Note 7: The internal LDO outputs 1.8V when the LDOE pin=“H”. The power up sequence between DVDD and AVDD is not critical.

Note 8: Connect the CPVDD pin to AVDD when the CPEN pin=“H”. If the CPEN pin is “L”, the voltage difference between CPVDD and AVDD should be less than 0.1V. There is no restriction on the voltage difference during the rise and fall of CPVDD and AVDD.

Note 9: When the internal charge pump is not used and an external power supply is supplied to the HVDD pin, the AK5734 should be reset by setting RSTN bit=“0” or PDN pin=“L” if the HVDD voltage drops to a value lower than recommended operating conditions or has an instantaneous interruption. This is recommended in order to avoid clicking noises.

Note 10: Exposed Pad on the back surface of the package must be connected to ground. At least 24 thermal vias should be added when solid ground is applied on one layer, and 8 or more thermal vias are recommended when solid ground is applied on two layers.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

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8. Analog Characteristics

(Ta = 25°C; AVDD = DVDD = CPVDD = 3.3V; AVSS = DVSS = CPVSS = CBVSS = 0V; MCLK = 512fs, fs = 48kHz, BICK = 64fs; Signal Frequency = 1kHz; 24bit Data; Measurement frequency = 20Hz - 20kHz; HVDD = CPOUT (CPEN pin = "L") / HVDD = 14.5V (CPEN pin = "H"); IN*P DC level = 6.0V / IN*N DC level = 3.0V (Differential, *:1-4), IN*P DC level = 4.5V / IN*N DC level = 0V (Single-ended *:1-4); unless otherwise specified)

Parameter				Min.	Typ.	Max.	Unit
ADC Analog Characteristics :							
Resolution				-	-	24	Bit
Input Voltage		PGA 0dB	Differential (Note 11)	1.9	2.0	2.1	Vrms
			Single-ended	0.95	1.0	1.05	Vrms
		PGA 20dB	Differential (Note 11)	0.18	0.2	0.22	Vrms
			Single-ended	0.091	0.1	0.109	Vrms
PGA(Pre Gain Amp) Gain step Error				-0.3	0	0.3	dB
Input Impedance				0.8	1.48	2	MΩ
S/(N+D)	fs=48kHz	0dB	–0.5dBFS, Differential	86	92	-	dB
			–0.5dBFS, Single-ended	86	92	-	
		20dB	–0.5dBFS, Differential	81	87	-	
			–0.5dBFS, Single-ended	78	84	-	
	fs=96kHz, 192kHz (Note 12)	0dB	–0.5dBFS, Differential	85	91	-	dB
			–0.5dBFS, Single-ended	84	90	-	
		20dB	–0.5dBFS, Differential	79	85	-	
			–0.5dBFS, Single-ended	75	81	-	
S/N	fs=48kHz	0dB	A-weighted, Differential	95	100	-	dB
			A-weighted, Single-ended	94	99	-	
		20dB	A-weighted, Differential	90	96	-	
			A-weighted, Single-ended	85	91	-	
	fs=96kHz, 192kHz (Note 12)	0dB	Flat, Differential	90	95	-	dB
			Flat, Single-ended	89	94	-	
		20dB	Flat, Differential	81	87	-	
			Flat, Single-ended	75	81	-	
Dynamic Range		0dB	–60dBFS, A-weighted Differential	95	100	-	dB
			–60dBFS, A-weighted Single-ended	94	99	-	
		20dB	–60dBFS, A-weighted Differential	90	96	-	
			–60dBFS, A-weighted Single-ended	85	91	-	
Interchannel Isolation		0dB		90	100	-	dB
		20dB		70	80	-	
Interchannel Gain Mismatch		0dB		-	0	0.2	dB
		20dB		-	0	0.3	
Peak Input Voltage (Note 13)				0	-	9.5	V

Note 11: The voltage difference between IN*P and IN*N pins (*=1-4). Input voltage is not proprtional to AVDD.

Note 12: Measurement conditions: frequency = 20Hz - 20kHz and MCLK = 256fs (fs = 96kHz) or 128fs (fs = 192kHz).

Note 13: Input voltage range of IN*P and IN*N pins that satisfies the above analog characteristics.

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(Ta = 25°C; AVDD = DVDD = CPVDD = 3.3V; AVSS = DVSS = CPVSS = CBVSS = 0V; MCLK = 512fs, fs = 48kHz, BICK = 64fs; Signal Frequency = 1kHz; 24bit Data; Measurement frequency = 20Hz - 20kHz;, HVDD = CPOUT(CPEN pin = "L") / HVDD = 14.5V (CPEN pin = "H"); IN*P DC level = 6.0V / IN*N DC level = 3.0V (Differential mode *=1-4), IN*P DC level = 4.5V / IN*N DC level = 0V (Single-ended mode *=1-4), unless otherwise specified)

Parameter			Min.	Typ.	Max.	Unit
CMRR (Note 14)	0dB	Differential (1kHz, 20kHz)	70	85	-	dB
	20dB	Differential (1kHz, 20kHz)	70	85	-	
PSRR (Note 15)	0dB	Differential / Single-ended	-	80	-	dB
	20dB	Differential / Single-ended	-	100	-	
PSMR (Note 16)	0dB	100mVpp, 0.1kHz, 0.5kHz, 15.5kHz Differential / Single-ended	-	–100	-	dB
CMMR (Note 17)	0dB	100mVpp, 0.1kHz, 0.5kHz, 15.5kHz Differential	-	–100	-	
Analog HPF Cutoff Frequency			1.8	4	10	Hz
Peak Input Voltage (Note 18)			0	-	9.5	V

Note 14: Input conditions are 1.0 Vpp, (Gain = 0 dB), or 0.1 Vpp, (Gain = 20 dB), signal to the IN*P pin and the IN*N pin (*=1-4) with the same phase and an input DC level = 4.5 V.

Note 15: PSRR is measured at AVDD and DVDD with 1kHz, 20mVpp input.

Note 16: This value shows the level of the modulation wave, [dBFS], that appears on |1kHz ± superimposed noise frequency of the power supply|, when a sine wave of 0.1 Vpp is superimposed on the AVDD pin and the DVDD pin, inputting a 1 kHz/- 0.5 dB sine wave to the IN*P and the IN*N pins, (*=1-4). The superimposed noise frequency is 0.1kHz, 0.5kHz or 15.5kHz.

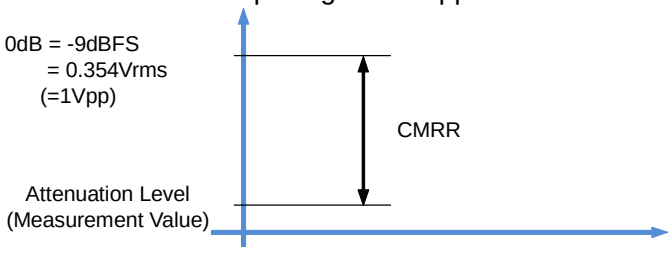
Note 17: This value shows the level of the modulation wave, [dBFS], that appears on |1kHz ± common mode noise frequency|, when a sine wave of 1 kHz / - 0.5 dB is input to the IN*P and the IN*N pins, (*1-4), in the same phase while the input DC level = 4.5 V, inputting a 0.1 Vpp sine wave to the IN*P and the IN*N pins. The common mode noise frequency is 0.1kHz, 0.5kHz or 15.5kHz.

Note 18: The input voltage range of the IN*P and the IN*N pins, (*1-4), that satisfies the above analog characteristics.

Definition of CMRR

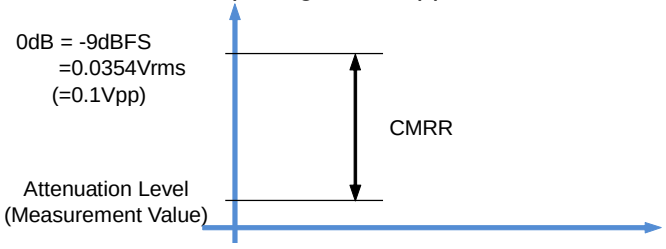
1. When Gain = 0dB

CMRR is measured by applying a 1kHz or 20kHz, 1.0Vpp signal to both the IN*P and the IN*N pins in phase. CMRR represents the ratio of the input signal 1.0Vpp and the attenuation level.



2. When Gain = 20dB

CMRR is measured by applying a 1kHz or 20kHz, 0.1Vpp signal to both the IN*P and the IN*N pins in phase. CMRR represents the ratio of the input signal 0.1Vpp and the attenuation level.



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(Ta = 25°C; AVDD = DVDD = CPVDD = 3.3V; AVSS = DVSS = CPVSS = CBVSS = 0V; MCLK = 512fs, fs = 48kHz, BICK = 64fs; HVDD = CPOUT (CPEN pin = "L"), HVDD = 14.5V(CPEN pin ="H"))

Parameter		Min.	Typ.	Max.	Unit
MIC Bias Voltage:					
Output DC Voltage (Note 19)	MBS3-0 bits= "0000"	4.90	5	5.10	V
	MBS3-0 bits= "0001"	5.39	5.5	5.61	V
	MBS3-0 bits= "0010"	5.88	6	6.12	V
	MBS3-0 bits= "0011"	6.37	6.5	6.63	V
	MBS3-0 bits= "0100"	6.86	7	7.14	V
	MBS3-0 bits= "0101"	7.35	7.5	7.65	V
	MBS3-0 bits= "0110"	7.84	8	8.16	V
	MBS3-0 bits= "0111"	8.33	8.5	8.67	V
	MBS3-0 bits= "1000"	8.78	9	9.22	V
Microphone Current (for 4 channels)		-	-	60	mA
Output Noise Level (A-weighted)		-	-100	-94	dBV

Note 19: When MBS3-0 bits = "0000"/"0001"/"0010"/"0011"/"0100"/"0101"/"0110"/"0111"/"1000", the DC output voltage (typ.) is 1.515/1.667/1.818/1.969/2.121/2.272/2.424/2.575/2.727 × AVDD(V), respectively.
When MBS3-0 bits = "0000"/"0001"/"0010"/"0011"/"0100"/"0101"/"0110"/"0111", the DC output voltage (Min, Max) is ±2.0% of typical DC output voltage.
When MBS3-0 bits = "1000", the DC output voltage, (Min, Max), is ±2.5% of typical DC output voltage.

(Ta = 25°C; AVDD = DVDD = CPVDD = 3.0 - 3.6V; AVSS = DVSS = CPVSS = CBVSS = 0V; MCLK = 512fs, fs = 48kHz, BCLK = 64fs, CPEN pin = "L")

Parameter		min	typ	max	Unit
MIC Bias Voltage:					
Microphone Current (for 4 channels total)	MBS3-0 bits = "0000"	-	-	33	mA
	MBS3-0 bits = "0001"	-	-	36	mA
	MBS3-0 bits = "0010"	-	-	40	mA
	MBS3-0 bits = "0011"	-	-	43	mA
	MBS3-0 bits = "0100"	-	-	46	mA
	MBS3-0 bits = "0101"	-	-	50	mA
	MBS3-0 bits = "0110"	-	-	53	mA
	MBS3-0 bits = "0111"	-	-	52	mA
	MBS3-0 bits = "1000"	-	-	44	mA

Note 20: Voltage difference between CPVDD and AVDD should be less than 0.1V.

(Ta = 25°C; AVDD = DVDD = CPVDD = 3.0 - 3.6V; HVDD = 12.0 - 16.0V; AVSS = DVSS = CPVSS = CBVSS = 0V; MCLK = 512fs, fs = 48kHz, BCLK = 64fs, CPEN in = "H")

Parameter		min	typ	max	Unit
MIC Bias Voltage:					
Microphone Current (for 4 channels total)	MBS3-0 bits = "0000"	-	-	33	mA
	MBS3-0 bits = "0001"	-	-	36	mA
	MBS3-0 bits = "0010"	-	-	40	mA
	MBS3-0 bits = "0011"	-	-	43	mA
	MBS3-0 bits = "0100"	-	-	46	mA
	MBS3-0 bits = "0101"	-	-	50	mA
	MBS3-0 bits = "0110"	-	-	53	mA
	MBS3-0 bits = "0111"	-	-	56	mA
	MBS3-0 bits = "1000"	-	-	60	mA

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(Ta = 25°C; AVDD = DVDD = CPVDD = 3.3V; AVSS = DVSS = CPVSS = CBVSS = 0V; HVDD = CPOUT (CPEN pin = “L”), HVDD = 14.5V (CPEN pin = ”H”))

Parameter		Min.	Typ.	Max.	Unit
SAR ADC Characteristics (DC):					
Resolution		-	-	12	Bit
IN*P&IN*N pin Input Voltage (Note 21)		0	-	10.1	V
VBATM pin Input Voltage (Note 22)	ATTVB bit = “0”	0	14.5	18	V
VBATM pin Input Voltage (Note 22)	ATTVB bit = “1”	0	-	10.1	V
Integral Nonlinearity (INL) (Note 23)		–4	-	+5	LSB
Differential Nonlinearity (DNL) (Note 23)		–4	-	+4	LSB
IN*P&IN*N pin Attenuation error		–1.4	-	1.4	%
VBATM pin Attenuation error	ATTVB bit = “0”	–1.8	-	+1.8	%
	ATTVB bit = “1”	–1.4	-	+1.4	%
MPWR pin Attenuation error		–1.4	-	+1.4	%

Note 21: Input signals of IN*P and IN*N pins are attenuated by 30% via internal resistance and input to the SAR ADC. The SAR ADC operates with an input voltage to IN*P, IN*N pins greater than 330mV. Input signals recognized as full scale are proportional to AVDD, e.g. full-scale input is 10V when AVDD = 3.0V and full-scale input voltage will be 11V when AVDD = 3.3V. Do not input a voltage more than 10.1V, since this exceeds the absolute maximum rating.

Note 22: When ATTVB bit = “0” (default), input signal of the VBATM pin is attenuated by 10% via internal resistance and input to the SARADC.
The attenuation ratio will be 30% when ATTVB bit = “1”.

Note 23: The IN*P, IN*N and VBATM pins should be within the conditions stated below to guarantee specified performance.

- IN*P, IN*N pin ≥ 330mV
- (ATTVB bit = 0): VBATM pin ≥1V,
  (ATTVB bit = 1): VBATM pin ≥330mV

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(Ta=25°C; AVDD = DVDD = CPVDD = 3.3V; AVSS = DVSS = CPVSS = CBVSS = 0V)

Parameter	Min.	Typ.	Max.	Unit
Power Supplies				
Power Supply Current				
Normal operation (PDN pin = "H", LDOE pin = "H" CPEN pin = "L")				
AVDD	-	8	11	mA
DVDD (fs = 48kHz)	-	15	22	mA
DVDD (fs = 96kHz)	-	21	31	mA
DVDD (fs = 192kHz)	-	21	31	mA
CPVDD (MIC bias current = 53mA)	-	350	390	mA
Power down (PDN pin = "L" , LDOE pin = "H") (Note 24)				
AVDD+DVDD+CPVDD		1	100	μA
Power Supply Current				
Normal operation (PDN pin = "H", LDOE pin = "L" CPEN pin = "L")				
AVDD	-	8	11	mA
DVDD+VDD18 (fs = 48kHz)	-	15	22	mA
DVDD+VDD18 (fs = 96kHz)	-	21	31	mA
DVDD+VDD18 (fs = 192kHz)	-	21	31	mA
CPVDD (MIC bias current = 53mA)	-	350	390	mA
Power down (PDN pin = "L" , LDOE pin = "L") (Note 24)				
AVDD+DVDD+CPVDD+VDD18		1	100	μA
Power Supply Current				
Normal operation (PDN pin = "H", LDOE pin = "H" CPEN pin = "H")				
AVDD+CPVDD	-	8	11	mA
DVDD (fs = 48kHz)	-	15	22	mA
DVDD (fs = 96kHz)	-	21	31	mA
DVDD (fs = 192kHz)	-	21	31	mA
HVDD (MIC bias current =60mA)	-	75	80	mA
Power down (PDN pin = "L" , LDOE pin = "H") (Note 24)				
AVDD+DVDD+CPVDD+HVDD		1	300	μA
Power Supply Current				
Normal operation (PDN pin = "H", LDOE pin = "L" CPEN pin = "H")				
AVDD+CPVDD	-	8	11	mA
DVDD+VDD18 (fs = 48kHz)	-	15	22	mA
DVDD+VDD18 (fs = 96kHz)	-	21	31	mA
DVDD+VDD18 (fs = 192kHz)	-	21	31	mA
HVDD (MIC bias current = 60mA)	-	75	80	mA
Power down (PDN pin = "L" , LDOE pin = "L") (Note 24)				
AVDD+DVDD+CPVDD+VDD18+HVDD		1	300	μA

Note 24: All digital input pins are fixed to DVDD or DVSS. The power supply current of DVDD is in TDM mode.

Note 25: Power consumption of DVDD in normal operation is measured with a 1kHz sine wave applied the IN1P, IN3P, IN1N and IN3N pins, and 180° phase-shifted 1 kHz sine wave applied to the IN2P, IN4P, IN2N and IN4N pins.

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9. Filter Characteristics

■ ADC Filter Characteristics (fs = 16kHz) (VOICE bit = “1”)

(Ta = -40 - +105°C; AVDD = 3.0 - 3.6V, DVDD = 1.7 - 1.98V (LDOE pin = “L”), 3.0 - 3.6V (LDOE pin = “H”), VDD18 = 1.7 - 1.98V (LDOE pin = “L”), HVDD = CPOUT(CPEN pin = “L”) / HVDD = 12 - 16V(CPEN pin = ”H”)

Parameter		Symbol	Min.	Typ.	Max.	Unit
VOICE (Figure 2)						
Passband (Note 26)	0dB/0.03dB	PB	0	-	6.3	kHz
	-3.0dB		-	6.9	-	kHz
Stopband (Note 26)		SB	8.0	-	-	kHz
Stopband Attenuation		SA	60	-	-	dB
Group Delay Distortion : 0Hz-8kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 27)		GD	-	18.8	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	1.3	-	Hz

Note 26. The frequency is proportional to the sampling rate (fs). It does not include the characteristics of HPF.

Note 27. The delay time introduced by the digital filters. This is the time from the application of an analog signal to the appearance of the L channel MSB on the SDTO*n* pin.

Note 28. VOICE bit = “1” setting is valid only when fs ≤ 48kHz. If the fs is over 48kHz, VOICE bit = “1” is invalid and the digital filter is set depending on SD bit and SLOW bit settings.

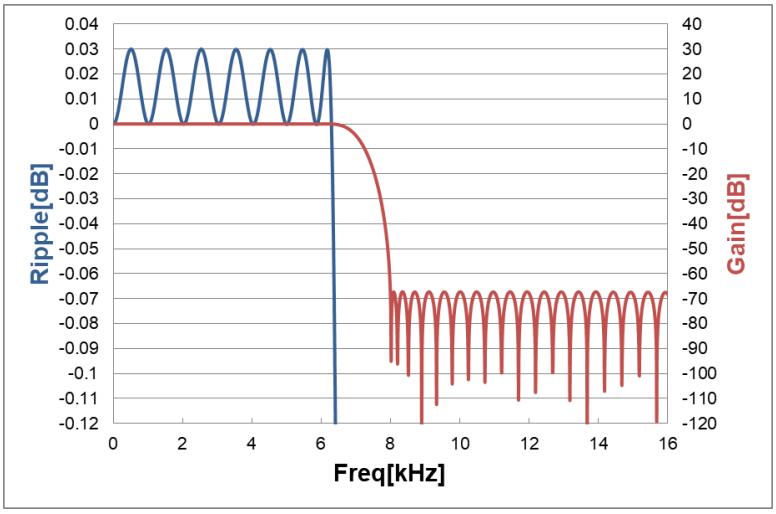

Figure 2. Voice Filter (fs = 16kHz)

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■ ADC Filter Characteristics (fs = 48kHz)

(Ta = -40 - +105°C; AVDD = 3.0 - 3.6V, DVDD = 1.7 - 1.98V (LDOE pin = "L"), 3.0 - 3.6V (LDOE pin = "H"), VDD18 = 1.7 - 1.98V (LDOE pin = "L"), HVDD = CPOUT (CPEN pin = "L") / HVDD = 12 - 16V (CPEN pin = "H"))

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (Decimation LPF): SHARP ROLL-OFF (Figure 3) (SD bit = "0", SLOW bit = "0")						
Passband (Note 29)	+0.001/–0.06dB –6.0dB	PB	0 -	- 24.4	22.0 -	kHz kHz
Stopband (Note 29)		SB	27.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 20.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 30)		GD	-	18.8	-	1/fs
Digital Filter (Decimation LPF): SLOW ROLL-OFF (Figure 4) (SD bit= "0", SLOW bit="1")						
Passband (Note 29)	+0.001/–0.076dB –6.0dB	PB	0 -	- 21.9	12.5 -	kHz kHz
Stopband (Note 29)		SB	36.5	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 20.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 30)		GD	-	6.6	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF FILTER (Figure 5) (SD bit= "1", SLOW bit= "0")						
Passband (Note 29)	+0.001/–0.06dB –6.0dB	PB	0 -	- 24.4	22.0 -	kHz kHz
Stopband (Note 29)		SB	27.9		-	kHz
Stopband Attenuation		SA	85		-	dB
Group Delay Distortion 0 - 20.0kHz		ΔGD	-	-	2.6	1/fs
Group Delay (Note 30)		GD	-	4.9	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SLOW ROLL-OFF (Figure 6) (SD bit="1", SLOW bit="1")						
Passband (Note 29)	+0.001/–0.076dB –6.0dB	PB -	0 -	- 21.9	12.5 -	kHz kHz
Stopband (Note 29)		SB	36.5	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 20.0kHz		ΔGD	-	-	1.2	1/fs
Group Delay (Note 30)		GD	-	4.3	-	1/fs
Digital Filter (HPF):						
Frequency Response (Note 29)	–3.0dB –0.5dB –0.1dB	FR	- - -	2.0 5.0 13.0	- - -	Hz Hz Hz

Note 29: The passband and stopband frequencies scale with fs.
For example, PB (+0.001dB/–0.06dB) =0.46 × fs (SHARP ROLL-OFF).
For example, PB (+0.001dB/–0.076dB) =0.26 × fs (SLOW ROLL-OFF).

Note 30: The delay time introduced by the digital filters. This is the time from the application of an analog signal to the appearance of the L channel MSB on the SDTO*n* pin.

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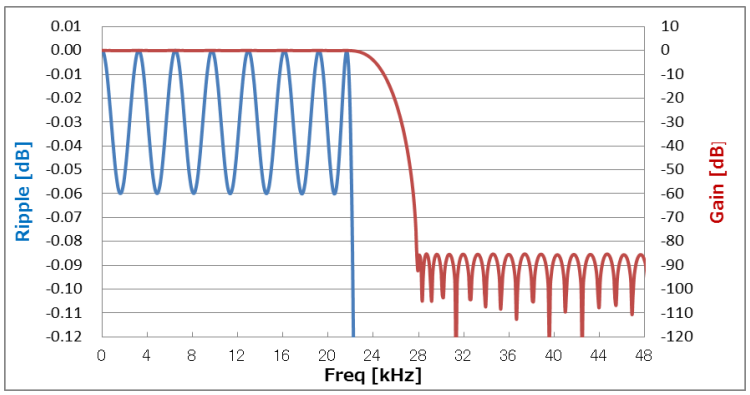

Figure 3. SHARP ROLL-OFF (fs=48kHz)

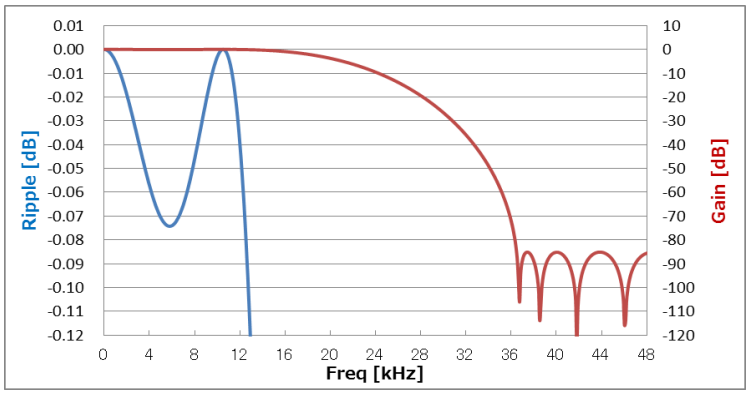

Figure 4. SLOW ROLL-OFF (fs=48kHz)

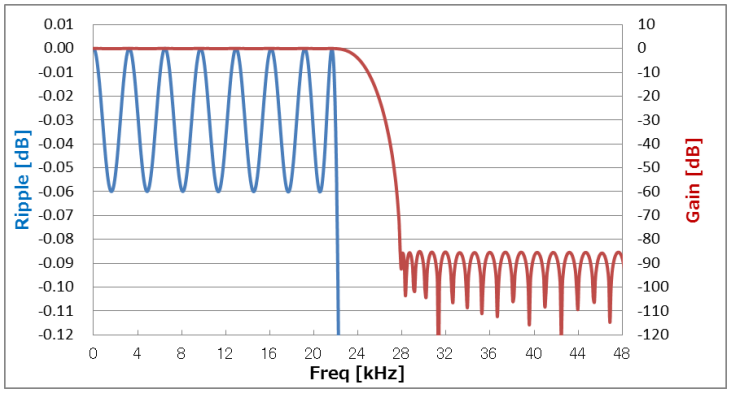

Figure 5. SHORT DELAY SHARP ROLL-OFF (fs=48kHz)

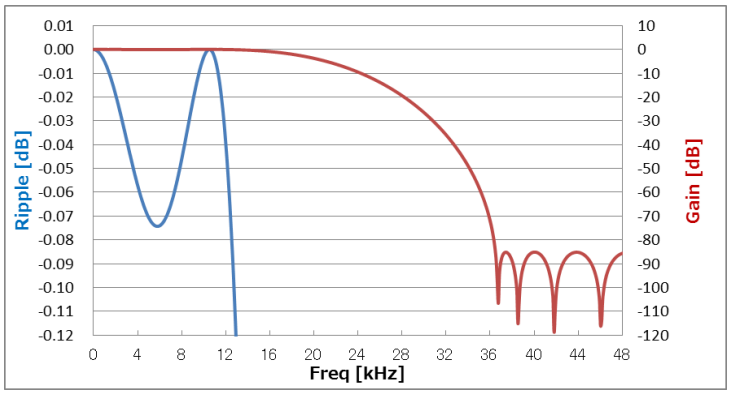

Figure 6. SHORT DELAY SLOW ROLL-OFF (fs=48kHz)

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■ ADC Filter Characteristics (fs = 96kHz)

(Ta = -40 - +105°C; AVDD = 3.0 - 3.6V, DVDD = 1.7 - 1.98V (LDOE pin = “L”), 3.0 - 3.6V (LDOE pin = “H”), VDD18 = 1.7 - 1.98V (LDOE pin = “L”), HVDD = CPOUT (CPEN pin = “L”) / HVDD = 12 - 16V (CPEN pin = ”H”))

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (Decimation LPF): SHARP ROLL-OFF (Figure 7) (SD bit=”0”, SLOW bit=”0”)						
Passband (Note 29)	0.001dB/–0.06dB –6.0dB	PB	0	- 48.8	44.1	kHz kHz
Stopband (Note 29)		SB	55.7	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 30)		GD	-	18.8	-	1/fs
Digital Filter (Decimation LPF): SLOW ROLL-OFF (Figure 8) (SD bit=”0”, SLOW bit=”1”)						
Passband (Note 29)	+0.001dB/–0.076dB –6.0dB	PB	0 -	- 43.8	25	kHz kHz
Stopband (Note 29)		SB	73	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 30)		GD	-	6.6	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF (Figure 9) (SD bit=”1”, SLOW bit=”0”)						
Passband (Note 29)	+0.001dB/–0.06dB –6.0dB	PB	0 -	- 48.8	44.1 -	kHz kHz
Stopband (Note 29)		SB	55.7		-	kHz
Stopband Attenuation		SA	85		-	dB
Group Delay Distortion 0 - 40.0kHz		ΔGD	-	-	2.8	1/fs
Group Delay (Note 30)		GD	-	4.9	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SLOW ROLL-OFF (Figure 10) (SD bit=”1”, SLOW bit=”1”)						
Passband (Note 29)	+0.001dB/–0.076dB –6.0dB	PB	0 -	- 43.8	25 -	kHz kHz
Stopband (Note 29)		SB	73	-	-	kHz
Stopband Attenuation		SA	85		-	dB
Group Delay Distortion 0 - 40.0kHz		ΔGD	-	-	1.2	1/fs
Group Delay (Note 30)		GD	-	4.4	-	1/fs
Digital Filter (HPF):						
Frequency Response (Note 29)	–3.0dB –0.5dB –0.1dB	FR	- - -	2.0 5.0 13.0	- - -	Hz Hz Hz

Note 29: The passband and stopband frequencies scale with fs.
For example, PB (+0.001dB/–0.06dB) =0.46 × fs (SHARP ROLL-OFF).
For example, PB (+0.001dB/–0.076dB) =0.26 × fs (SLOW ROLL-OFF).

Note 30: The delay time introduced by the digital filters. This is the time from the application of an analog signal to the appearance of the L channel MSB on the SDTO*n* pin.

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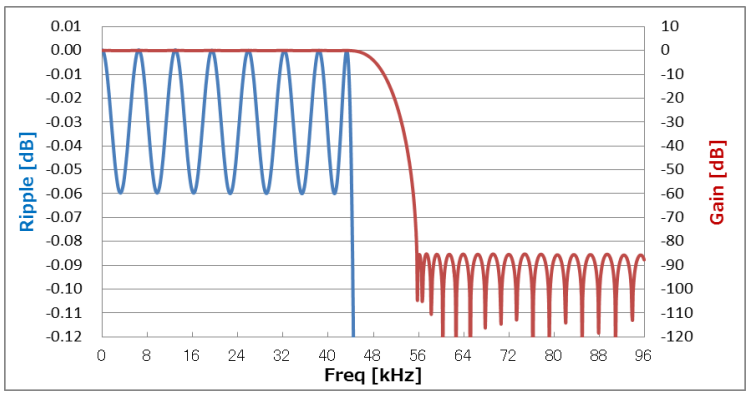

Figure 7. SHARP ROLL-OFF (fs=96kHz)

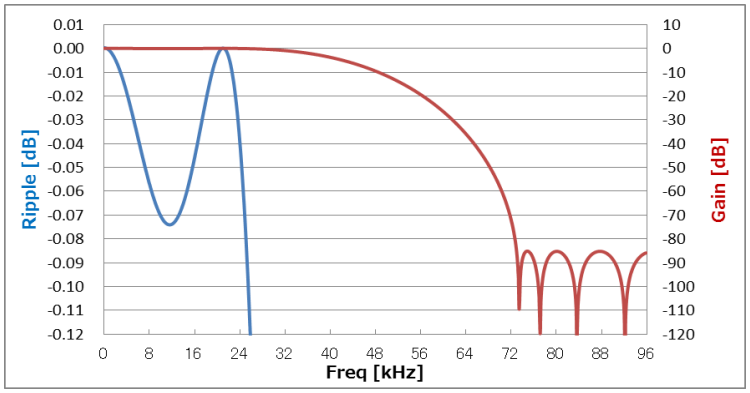

Figure 8. SLOW ROLL-OFF (fs=96kHz)

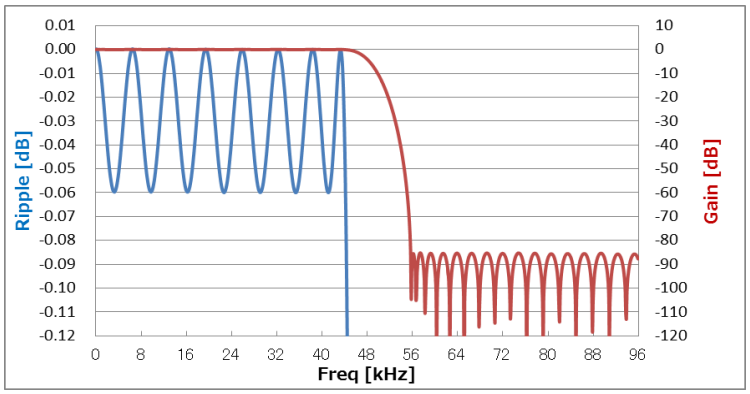

Figure 9. SHORT DELAY SHARP ROLL-OFF (fs=96kHz)

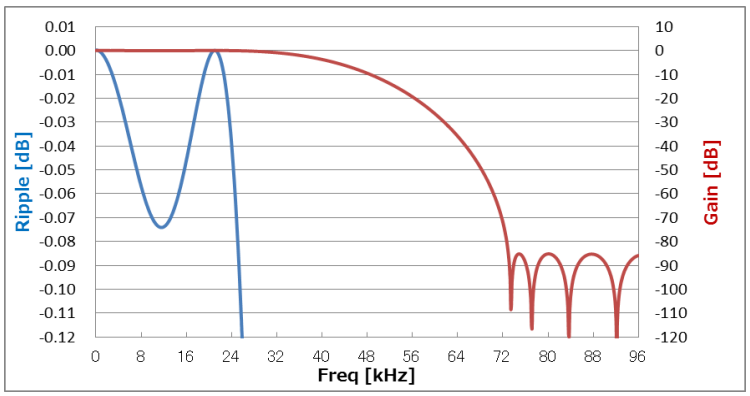

Figure 10. SHORT DELAY SLOW ROLL-OFF (fs=96kHz)

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■ ADC Filter Characteristics (fs = 192kHz)

(Ta = -40 - +105°C; AVDD = 3.0 - 3.6V, DVDD = 1.7 - 1.98V (LDOE pin = "L"), 3.0 - 3.6V (LDOE pin = "H"), VDD18 = 1.7 - 1.98V (LDOE pin = "L"), HVDD = CPOUT (CPEN pin = "L") / HVDD = 12 - 16V (CPEN pin = "H"))

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (Decimation LPF): SHARP ROLL-OFF (Figure 11) (SD bit= "0", SLOW bit= "0")						
Passband (Note 29)	+0.001B/–0.037dB	PB	0	-	83.7	kHz
	–6.0dB			100.2		kHz
Stopband (Note 29)		SB	122.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 30)		GD	-	14.4	-	1/fs
Digital Filter (Decimation LPF): SLOW ROLL-OFF (Figure 12) (SD bit= "0", SLOW bit= "1")						
Passband (Note 29)	0.001dB/–0.1dB	PB	0	-	31.5	kHz
	–6.0dB			75.2		kHz
Stopband (Note 29)		SB	146	-		kHz
Stopband Attenuation		SA	85	-		dB
Group Delay Distortion 0 - 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 30)		GD	-	7.3	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF FILTER (Figure 13) (SD bit= "1", SLOW bit= "0")						
Passband (Note 29)	+0.001B/–0.037dB	PB	0	-	83.7	kHz
	–6.0dB		-	100.2	-	kHz
Stopband (Note 29)		SB	122.9	-	-	kHz
Stopband Attenuation		SA	85		-	dB
Group Delay Distortion 0 - 40.0kHz		ΔGD	-	-	0.3	1/fs
Group Delay (Note 30)		GD	-	6.0	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SLOW ROLL-OFF FILTER (Figure 14) (SD bit "1", SLOW bit= "1")						
Passband (Note 29)	+0.001dB/–0.1dB	PB	0	-	31.5	kHz
	–6.0dB		-	75.2	-	kHz
Stopband (Note 29)		SB	146	-		kHz
Stopband Attenuation		SA	85	-		dB
Group Delay Distortion 0 - 40.0kHz		ΔGD	-	-	0.4	1/fs
Group Delay (Note 30)		GD	-	5.8	-	1/fs
Digital Filter (HPF):						
Frequency Response	–3.0dB	FR	-	2.0	-	Hz
	–0.5dB		-	5.0	-	Hz
(Note 29)	–0.1dB		-	13.0	-	Hz

Note 29: The passband and stopband frequencies scale with fs.
For example, PB (+0.001dB/–0.037dB) =0.436 × fs (SHARP ROLL-OFF).
For example, PB (+0.001dB/–0.1dB) = 0.164 × fs (SLOW ROLL-OFF).

Note 30: The delay time introduced by the digital filters. This is the time from the application of an analog signal to the appearance of the L channel MSB on the SDTO*n* pin.

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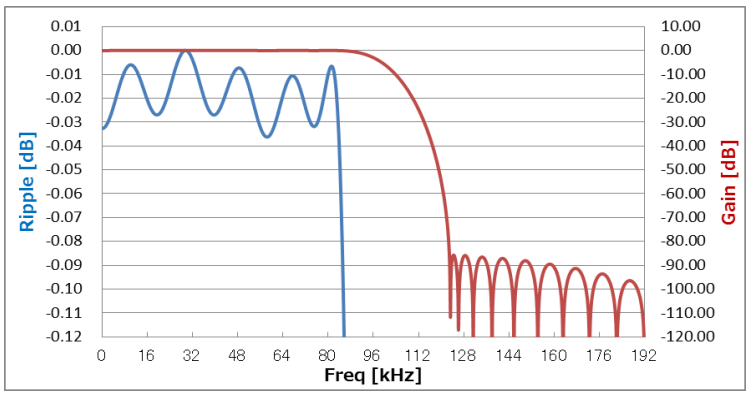

Figure 11. SHARP ROLL-OFF (fs=192kHz)

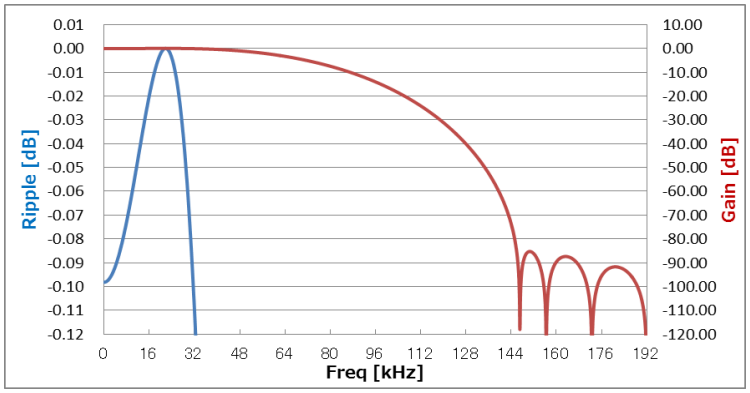

Figure 12. SLOW ROLL-OFF (fs=192kHz)

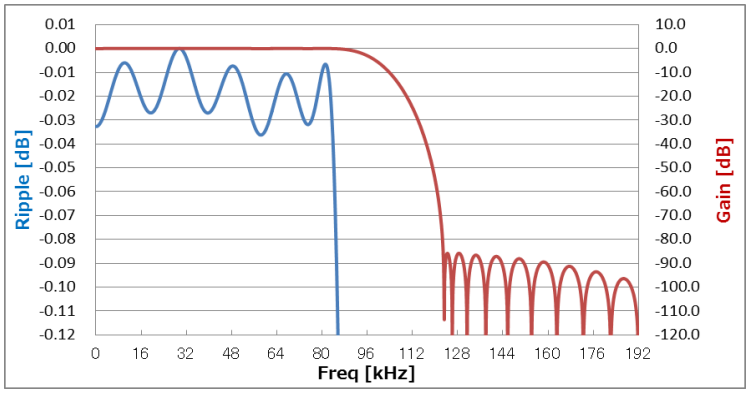

Figure 13. SHORT DELAY SHARP ROLL-OFF (fs=192kHz)

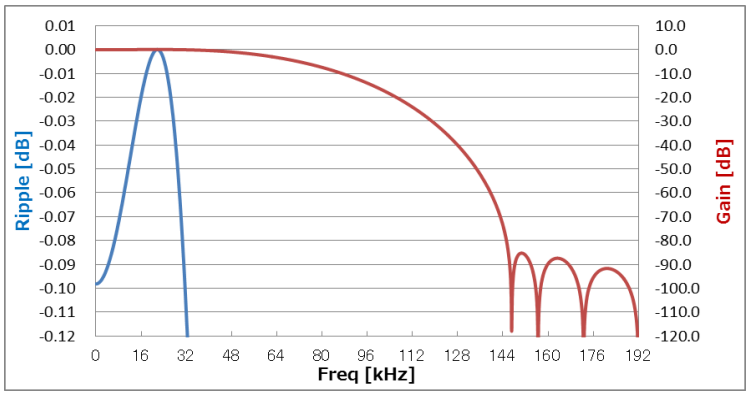

Figure 14. SHORT DELAY SLOW ROLL-OFF (fs=192kHz)

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10. DC Characteristics

(Ta = −40 - 105°C; AVDD = 3.0 - 3.6V, DVDD = 1.7 - 1.98V (LDOE pin = "L"), 3.0 - 3.6V (LDOE pin = "H"), VDD18 = 1.7 - 1.98V (LDOE pin = "L"), CPVDD = 3.0 - 3.6V, HVDD = CPOUT (CPEN pin = "L") / HVDD = 14.5V (CPEN pin = "H"))

Parameter	Symbol	Min.	Typ.	Max.	Unit
DVDD=3.0V - 3.6V (LDOE pin= "H")					
High-Level Input Voltage (Note 31)	VIH	70%DVDD	-		V
Low-Level Input Voltage (Note 31)	VIL		-	30%DVDD	V
High-Level Output Voltage (Note 32) (Iout=−100μA)	VOH	DVDD−0.5	-		V
Low-Level Output Voltage (Note 32) (except SDA, INT pin: Iout= 100μA)	VOL	-		0.5	V
(SDA, INT pin: Iout= 3mA)	VOL	-		0.4	V
DVDD=1.7 - 1.98V (LDOE pin= "L")					
High-Level Input Voltage (Note 31)	VIH	80%DVDD	-		V
Low-Level Input Voltage (Note 31)	VIL	-	-	20%DVDD	V
High-Level Output Voltage (Note 32) (Iout=−100μA)	VOH	DVDD−0.3	-	-	V
Low-Level Output Voltage (Note 32) (except SDA, INT pin: Iout= 100μA)	VOL1		-	0.3	V
(SDA, INT pin: Iout= 3mA)	VOL2		-	20%DVDD	V
Input Leakage Current	Iin	-	-	±10	μA

Note 31: MCLK, PDN, BICK (Slave Mode), LRCK (Slave Mode), SPI, LDOE, CAD0/CSN, SCL/CCLK, CPEN, CAD1 (I^2C mode), TDMI (TDM mode), SDA/CDTI

Note 32: BICK (Master Mode), LRCK (Master Mode), SDTO1, SDTO2 (Stereo mode), INT, SDA/CDTI (I^2C mode), CDTO (4-wire mode)

Note 33: Pull-up resistor of pins mentioned in INT pin and SDA pin should be connected to a voltage less than DVDD+0.3V.

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11. Switching Characteristics

■ System Clocks

□ Slave Mode

(Ta = –40 - +105°C; AVDD = 3.0 - 3.6V, DVDD = 1.7 - 1.98V (LDOE pin = "L"), 3.0 - 3.6V (LDOE pin = "H"), VDD18 = 1.7 - 1.98V (LDOE pin = "L"), CPVDD = 3.0 - 3.6V, HVDD = CPOUT (CPEN pin = "L") / HVDD = 14.5V (CPEN pin = "H"), C_L = 20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK Input Timing					
(Note 34)					
Frequency	fMCLK	4.096	-	36.864	MHz
Pulse Duty Low	tMCLKL	40	-	60	%
Pulse Duty High	tMCLKH	40	-	60	%
LRCK Input Timing					
Stereo Mode					
Frequency					
Normal Speed	fsn				
MCLK 1024fs, 2048fs		8	-	16	kHz
MCLK 256fs, 384fs 521fs		8	-	48	kHz
Double Speed	fsd				
MCLK 256fs		48	-	96	kHz
MCLK 384fs		48	-	96	kHz
Quad Speed	fsq				
MCLK 128fs		96	-	192	kHz
MCLK 192fs		96	-	192	kHz
Duty Cycle	dLRCK	45	-	55	%
TDM128 Mode					
Frequency					
Normal Speed	fsn	8	-	48	kHz
Double Speed	fsd	48	-	96	kHz
Quad Speed	fsd	96	-	192	kHz
Pulse Width Low	tLRCKL	1/(128fsn)	-	-	s
		1/(128fsd)	-	-	s
		1/(128fsq)	-	-	s
Pulse Width High	tLRCKH	1/(128fsn)	-	-	s
		1/(128fsd)	-	-	s
		1/(128fsq)	-	-	s

Note 34. Refer to Table 5, Table 6, Table 7, Table 8 and Table 9 for supported MCLK frequencies in each operation mode.

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LRCK Input Timing (Continued)						
TDM256 Mode						
Frequency						
Normal Speed		fsn	8	-	48	kHz
Double Speed		fsd	48	-	96	kHz
Pulse Width Low		tLRCKL	1/(256fsn)	-	-	s
			1/(256fsd)	-	-	s
Pulse Width High		tLRCKH	1/(256fsn)	-	-	s
			1/(256fsd)	-	-	s
TDM512 Mode						
Frequency						
Normal Speed		fsn	8	-	48	kHz
Pulse Width Low		tLRCKL	1/(512fsn)	-	-	s
Pulse Width High		tLRCKH	1/(512fsn)	-	-	s
BICK Input Timing						
Stereo Mode						
Period		tBICK	-		-	
Normal Speed			1/(64fsn)	-	-	s
Double Speed			1/(64fsd)	-	-	s
Quad Speed			1/(64fsq)	-	-	s
Duty Cycle		dBICK	-	50	-	%
TDM128 Mode						
Period		tBICK				
Normal Speed			-	1/(128fsn)	-	s
Double Speed			-	1/(128fsd)	-	s
Quad Speed			-	1/(128fsq)	-	s
Pulse Width Low		tBICKL				
Normal Speed			66	-	-	ns
Double Speed			33	-	-	ns
Quad Speed			17	-	-	ns
Pulse Width High		tBICKH				
Normal Speed			66	-	-	ns
Double Speed			33	-	-	ns
Quad Speed			17	-	-	ns
TDM256 Mode						
Period		tBICK				
Normal Speed			-	1/(256fsn)	-	s
Double Speed			-	1/(256fsd)	-	s
Pulse Width Low		tBICKL				
Normal Speed			33	-	-	ns
Double Speed			17	-	-	ns
Pulse Width High		tBICKH				
Normal Speed			33	-	-	ns
Double Speed			17	-	-	ns
TDM512 Mode						
Period		tBICK				
Normal Speed			-	1/(512fsn)	-	s
Pulse Width Low		tBICKL				
Normal Speed			17	-	-	ns
Pulse Width High		tBICKH				
Normal Speed			17	-	-	ns

Note 35. BICK rising edge must not occur at the same time as LRCK edge.

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□ Master Mode

(Ta = –40 - +105°C; AVDD = 3.0 - 3.6V, DVDD = 1.7 - 1.98V (LDOE pin = "L"), 3.0 - 3.6V (LDOE pin = "H"), VDD18 = 1.7 - 1.98V (LDOE pin = "L"), CPVDD = 3.0 - 3.6V, HVDD = CPOUT (CPEN pin = "L") / HVDD = 14.5V (CPEN pin = "H"), C_L = 20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK Input Timing					
(Note 36, Note 37)					
Frequency	fMCLK	4.096	-	36.864	MHz
Pulse Width Low	tMCLKL	40		60	%
Pulse Width High	tMCLKH	40		60	%
LRCK Output Timing					
Stereo Mode					
Frequency					
Normal Speed	fsn				
MCLK 1024fs, 2048fs		8	-	16	kHz
MCLK 256fs, 384fs 512fs		8	-	48	kHz
Double Speed	fsd				
MCLK 256fs		48	-	96	kHz
MCLK 384fs		48	-	96	
Quad Speed	fsq				
MCLK 128fs		96	-	192	kHz
MCLK 192fs		96	-	192	kHz
Duty Cycle	dLRCK		50		%
TDM128 Mode					
Frequency					
Normal Speed	fsn	8	-	48	kHz
Double Speed	Fsd	48	-	96	kHz
Quad Speed	fsq	96	-	192	kHz
Pulse Width Low	tLRCKL	-	1/(4fsn)	-	s
		-	1/(4fsd)	-	s
		-	1/(4fsq)	-	
Pulse Width High	tLRCKH	-	1/(4fsn)	-	s
		-	1/(4fsd)	-	s
		-	1/(4fsq)	-	

Note 36. Refer to Table 5, Table 6, Table 7, Table 8 and Table 9 for supported MCLK frequencies in each operation mode.

Note 37. The minimum value of "Pulse Width Low/High" is inversely proportional to the MCLK frequency, with a proportionality constant of 11 x 36.864. Note that 11ns is the minimum supported pulse width when MCLK is 36.864MHz (the maximum supported MCLK frequency).

ex) When MCLK = 18.432 MHz, the minimum value of "Pulse Width Low/High" is 11×36.864/18.432 = 22ns.

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LRCK Output Timing (Continued)						
TDM256 Mode (Note 38)						
Frequency						
Normal Speed		fsn	8	-	48	kHz
Double Speed		fsd	48	-	96	kHz
Pulse Width Low		tLRCKL	-	1/(8fsn)	-	s
			-	1/(8fsd)	-	s
Pulse Width High		tLRCKH	-	1/(8fsn)	-	s
			-	1/(8fsd)	-	s
TDM512 Mode (Note 38)						
Frequency						
Normal Speed			8		48	kHz
Pulse Width Low		tLRCKL	-	1/(16fsn)	-	s
Pulse Width High		tLRCKH	-	1/(16fsn)	-	s
BICK Output Timing						
Stereo Mode						
Period		tBICK	-	1/(64fs)	-	s
Duty Cycle		dBICK	-	50	-	%
TDM128 Mode						
Period		tBICK	-	1/(128fs)	-	s
Duty Cycle		dBICK	-	50	-	%
TDM256 Mode						
Period		tBICK	-	1/(256fs)	-	s
Duty Cycle (MCLK=512fs)		dBICK	-	50	-	%
Duty Cycle (MCLK=256fs)		dBICK	-	50	-	%
TDM512 Mode						
Period		tBICK	-	1/(512fs)	-	s
Duty Cycle		dBICK	-	50	-	%

Note 38: BICK duty depends on MCLK duty in TDM mode.

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■ Audio Interface

□ Slave Mode

(Ta = –40 - +105°C; AVDD = 3.0 - 3.6V, DVDD = 1.7 - 1.98V (LDOE pin = “L”), 3.0 - 3.6V (LDOE pin = “H”), VDD18 = 1.7 - 1.98V (LDOE pin = “L”), CPVDD = 3.0 - 3.6V, HVDD = CPOUT (CPEN pin = “L”) / HVDD = 14.5V (CPEN pin = “H”), C_L = 20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Stereo Mode					
Normal Speed, Double Speed, Quad Speed Mode					
DVDD=1.7V - 1.98V					
LRCK to BICK “↑”	tLRB	30	-	-	ns
BICK “↑” to LRCK	tBLR	30	-	-	ns
LRCK to SDTO (MSB Justified)	tLRS	-	-	30	ns
BICK “↓” to SDTO	tBSD	-	-	30	ns
DVDD=3.0V - 3.6V					
LRCK to BICK “↑”	tLRB	33	-	-	ns
BICK “↑” to LRCK	tBLR	33	-	-	ns
LRCK to SDTO (MSB Justified)	tLRS	-	-	28	ns
BICK “↓” to SDTO	tBSD	-	-	28	ns
TDM128 (Normal Speed Mode, Double Speed Mode), TDM256 (Normal Speed Mode)					
DVDD=1.7V - 1.98V					
LRCK to BICK “↑”	tLRB	33	-	-	ns
BICK “↑” to LRCK	tBLR	33	-	-	ns
BICK “↑” to SDTO	tBSDD	5	-	30	ns
TDMI Setup time to BICK “↑”	tSDS	5	-	-	ns
TDMI Hold time to BICK “↑”	tSDH	5	-	-	ns
DVDD=3.0V - 3.6V					
LRCK to BICK “↑”	tLRB	33	-	-	ns
BICK “↑” to LRCK	tBLR	33	-	-	ns
BICK “↓” to SDTO	tBSD	-	-	14	ns
TDMI Setup time to BICK “↑”	tSDS	5	-		ns
TDMI Hold time to BICK “↑”	tSDH	5	-		ns
TDM128 Mode					
Quad Speed Mode					
LRCK to BICK “↑”	tLRB	16	-	-	ns
BICK “↑” to LRCK	tBLR	16	-	-	ns
BICK “↑” to SDTO	tBSDD	5	-	30	ns
TDMI Setup time to BICK “↑”	tSDS	5	-	-	ns
TDMI Hold time to BICK “↑”	tSDH	5	-	-	ns
TDM256 Mode					
Double Speed Mode					
LRCK to BICK “↑”	tLRB	16	-	-	ns
BICK “↑” to LRCK	tBLR	16	-	-	ns
BICK “↑” to SDTO	tBSDD	5	-	30	ns
TDMI Setup time to BICK “↑”	tSDS	5	-	-	ns
TDMI Hold time to BICK “↑”	tSDH	5	-	-	ns
TDM512 Mode					
Normal Speed Mode					
LRCK to BICK “↑”	tLRB	16	-	-	ns
BICK “↑” to LRCK	tBLR	16	-	-	ns
BICK “↑” to SDTO	tBSDD	5	-	30	ns
TDMI Setup time to BICK “↑”	tSDS	5	-	-	ns
TDMI Hold time to BICK “↑”	tSDH	5	-	-	ns

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□ Master Mode

(Ta=−40 - +105°C; AVDD = 3.0 - 3.6V, DVDD = 1.7 - 1.98V (LDOE pin = “L”), 3.0 - 3.6V (LDOE pin = “H”), VDD18 = 1.7 - 1.98V (LDOE pin = “L”), CPVDD = 3.0 - 3.6V, HVDD = CPOUT (CPEN pin = “L”) / HVDD = 14.5V (CPEN pin = “H”), C_L = 20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Stereo Mode					
Normal Speed, Double Speed, Quad Speed Mode					
DVDD=1.7V - 1.98V					
BICK “↓” to LRCK	tMBLR	-10	-	10	ns
LRCK to SDTO (MSB Justified)	tLRS	-20	-	20	ns
BICK “↓” to SDTO	tBSD	-20	-	20	ns
DVDD=3.0V - 3.6V					
BICK “↓” to LRCK	tMBLR	-10	-	10	ns
LRCK to SDTO (MSB Justified)	tLRS	-20	-	20	ns
BICK “↓” to SDTO	tBSD	-20	-	20	ns
TDM128, TDM256 Mode, TDM512 Mode					
Normal Speed, Double Speed, Quad Speed Mode					
BICK “↓” to LRCK	tMBLR	-6		6	ns
BICK “↓” to SDTO	tBSD	-10	-	10	ns
TDMI Setup time to BICK “↑”	tSDS	5	-	-	ns
TDMI Hold time to BICK “↑”	tSDH	5	-	-	ns

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■ Control Interface, Power-down, Reset

(Ta = –40 - 105°C; AVDD = 3.0 - 3.6V, DVDD = 1.7 - 1.98V (LDOE pin = “L”), 3.0 - 3.6V (LDOE pin = “H”), VDD18 = 1.7 - 1.98V (LDOE pin = “L”), CPVDD=3.0 - 3.6V, HVDD = 14.5V (CPEN pin = “H”), HVDD = CPOUT(CPEN pin = “L”))

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (4-wire Serial)					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
CCLK pulse Width High	tCCKH	80	-	-	ns
CDTI Setup Time	tCDS	40	-	-	ns
CDTI Hold Time	tCDH	40	-	-	ns
CCSN “H” Time	tCSW	150	-	-	ns
CSN Edge to CCLK “↑” (Note 39)	tCSS	50	-	-	ns
CCLK “↑” to CSN Edge (Note 39)	tCSH	50	-	-	ns
CCLK “↓” to CDTO, (at Read Command)	tDCD	-	-	70	ns
CSN “↑” to CDTO (Hi-z), (at Read Command) (Note 40)	tCCZ	-	-	70	ns
Control Interface Timing (I^2C Bus):					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 41)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	1.0	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Capacitive load on bus	Cb	-	-	400	pF
Power-down & Reset Timing					
PDN Accept Pulse Width (Note 42)	tAPD	150	-	-	ns
PDN Reject Pulse Width	tRPD	-	-	30	ns
RSTN bit “1” to SDTO valid (CPEN pin = “H”) (Note 43)	tRSTNV	-	2262	-	1/fs
RSTN bit “1” to SDTO valid (CPEN pin = “L”) (Note 43)	tRSTNV	-	3224	-	1/fs

Note 39: CCLK rising edge must not occur at the same time as CSN edge.

Note 40: Hi-z level is defined at the point when the CDTO pin voltage is changed for 10% from “L” level while it is pulled up to DVDD by 1kΩ.

Note 41: Data must be held for long enough to account for the 300ns rise/fall time of SCL.

Note 42: The AK5734 can be reset by setting the PDN pin to “L” upon power-up. The PDN pin must be held “L”, for more than 150ns for a certain reset. The AK5734 is not reset by an “L” pulse less than 30ns.

Note 43: This cycle is the number of LRCK rising edges from writing RSTN bit = “1” when MSN bit is set to “0”. It will be -3/fs times shorter if MSN bit is set to “1”.

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■ Timing Diagram

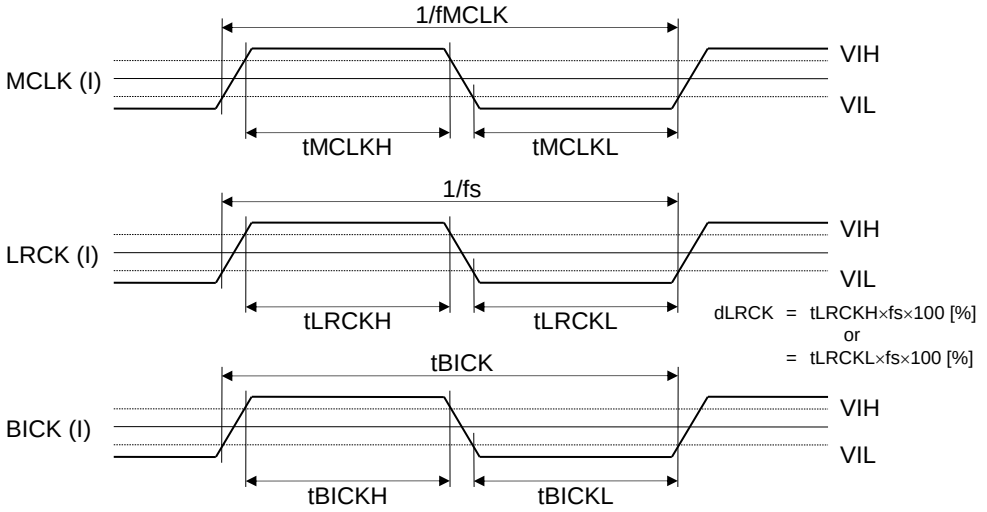

Figure 15. Clock Timing (External Slave Mode)

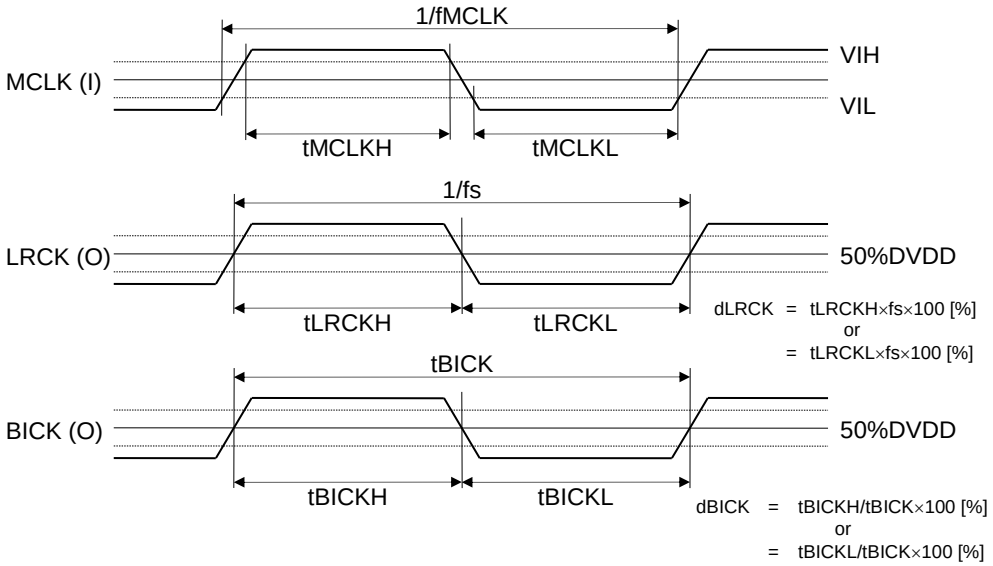

Figure 16. Clock Timing (External Master Mode)

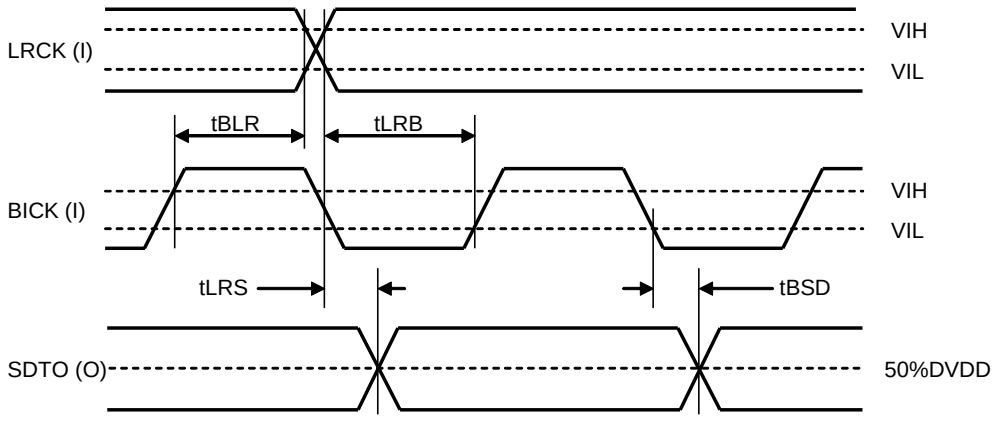

Figure 17. Audio Interface Timing (External Slave Mode)

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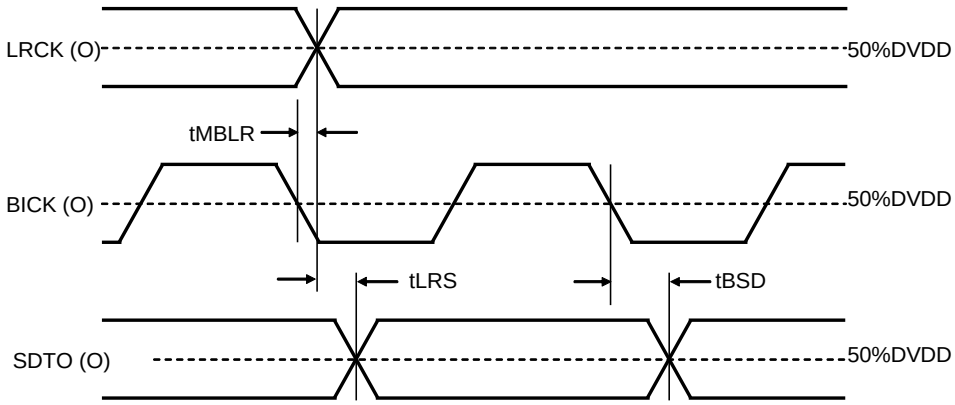

Figure 18. Audio Interface Timing (External Master Mode)

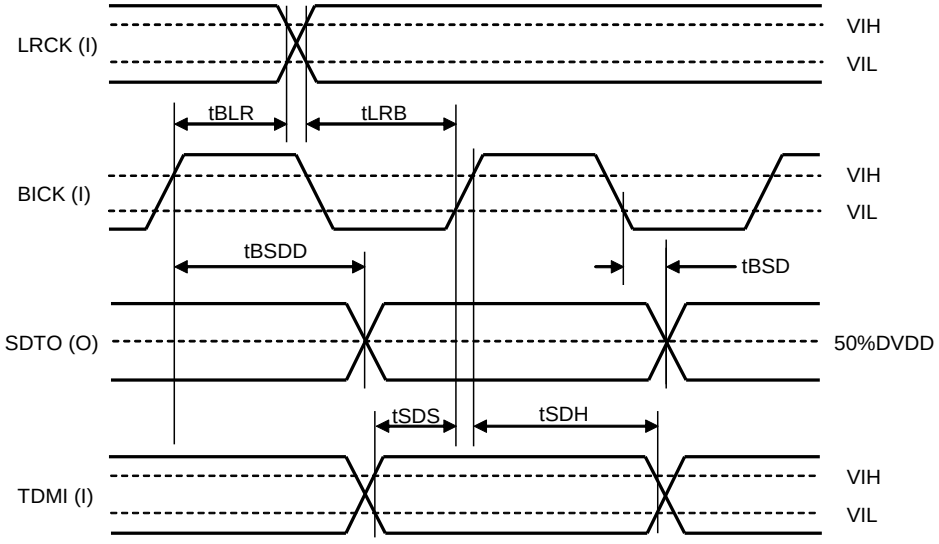

Figure 19. Audio Interface Timing (TDM mode & Slave mode)

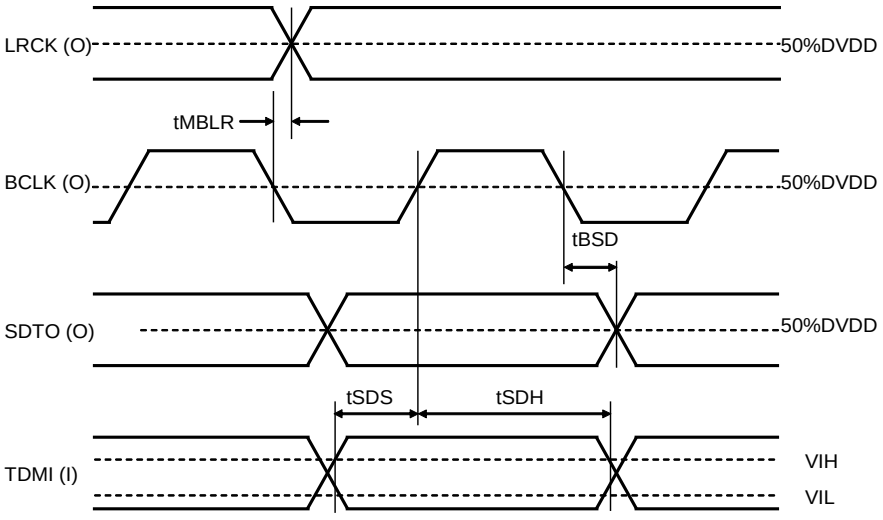

Figure 20. Audio Interface Timing (TDM mode & Master mode)

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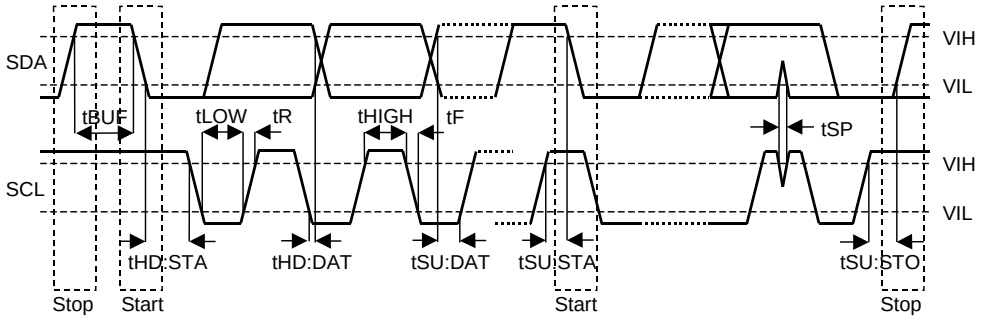

Figure 21. I²C Bus Timing

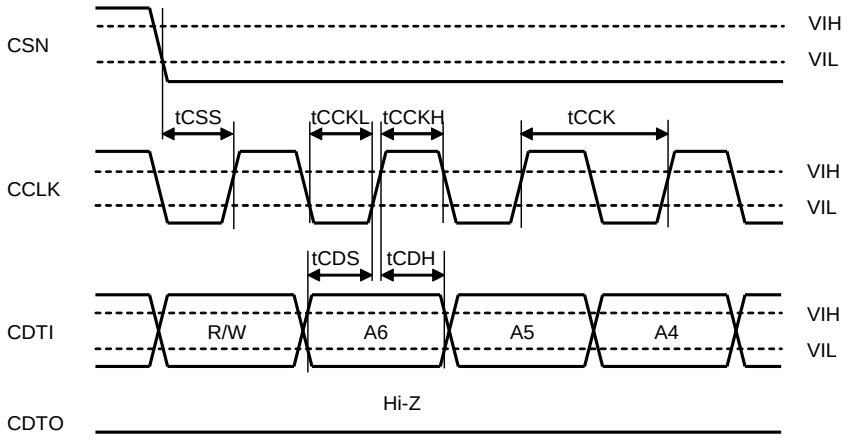

Figure 22. WRITE/READ Command Input Timing (4-wire serial mode)

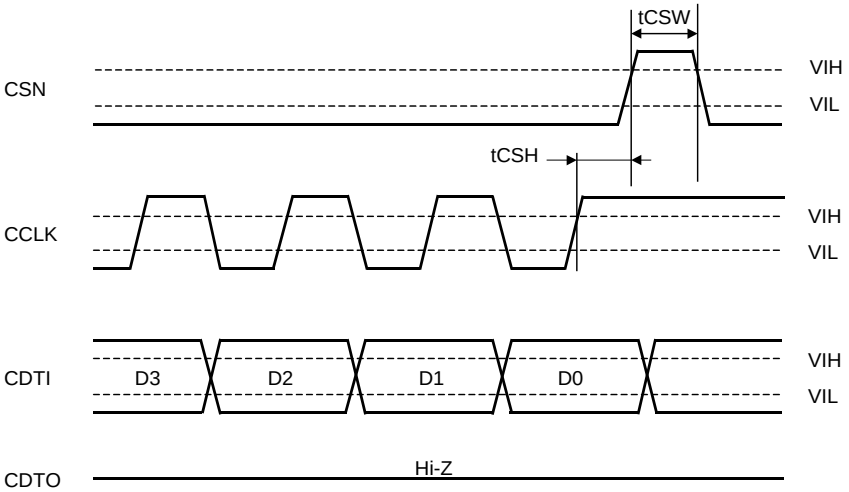

Figure 23. WRITE Data Input Timing (4-wire serial mode)

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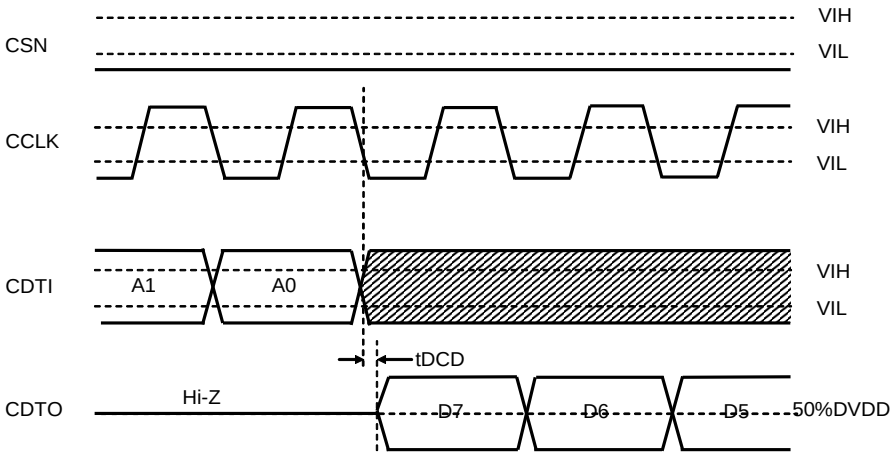

Figure 24. READ Data Output Timing 1 (4-wire serial mode)

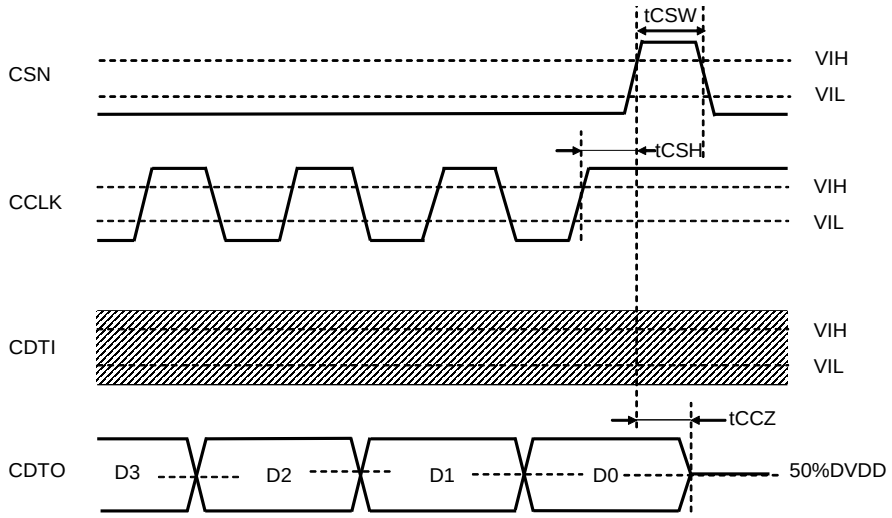

Figure 25. READ Data Output Timing 2 (4-wire serial mode)

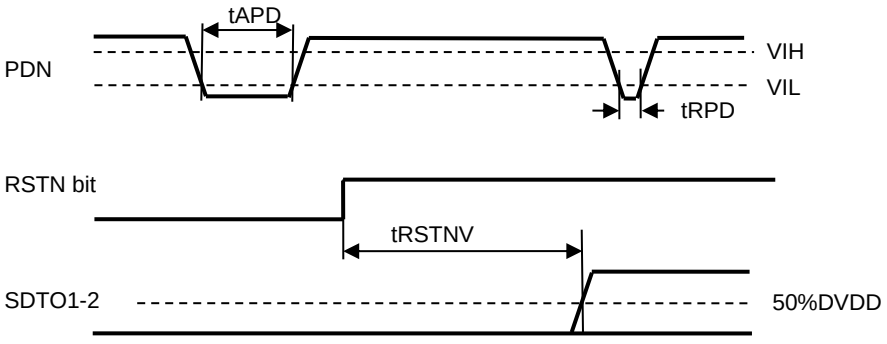

Figure 26. Power-down & Reset Timing

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12. Functional Descriptions

■ Digital Core Power Supply

The digital core of the AK5734 operates with a 1.8V power supply. This 1.8V is generated from DVDD, (3.3V), by an internal LDO regulator. The LDO is powered ON by setting the LDOE pin = "H" and OFF by setting the LDOE pin = "L". When using a 1.8V power supply for DVDD, set the LDOE pin = "L" and input the 1.8V power to the VDD18 pin. When LDOE pin = "H", the control register can be accessed up to 4ms after PDN pin goes "H". When LDOE pin = "L", the control register can be accessed max.2ms after PDN pin goes "H".

■ Master Mode and Slave Mode

Master Mode and Slave Mode are selected by setting the MSN bit. ["1" = Master Mode, "0" = Slave Mode (default)]. In Master mode, the LRCK pin and the BICK pin become output pins. In Slave mode, the LRCK pin and the BICK pins become input pins.

Clock Mode	MSN bit	Clock Pin Status			Connection Diagram
		MCLK	BICK	LRCK	
Master	1	In	Out	Out	Figure 27
Slave	0	In	In	In	Figure 28

Table 1. Clock Mode

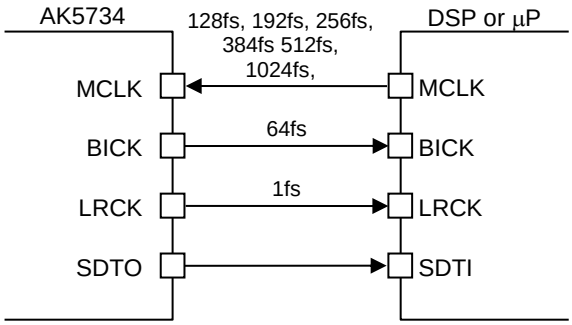

Figure 27: Master Mode

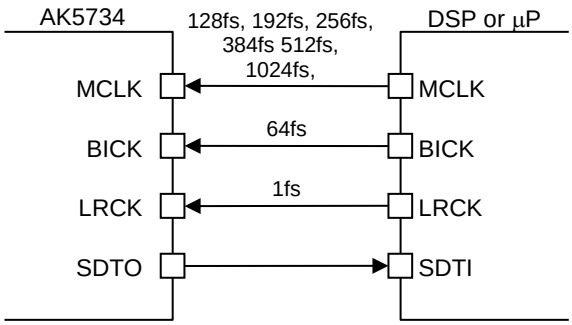

Figure 28: Slave Mode

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■ System Clock

The AK5736's system clocks (MCLK, BICK and LRCK) are configured via the CKS2-0, FS12K, OSR and FS2-0 bits.
OSR bit is recommended to set to "1" when 8kHz ≤ fs ≤ 24kHz. By setting the OSR bit = "1", the influence of noise around 1 MHz on the audio band can be reduced. If the setting of FS2-0 bits is over 24kHz, the noise around 1MHz can be reduced regardless of OSR bit setting. The charge pump frequency can be change by CPCK1-0 bits. (Table 4)
Stable clock must be supplied during operation. Mode switching (e.g. clock frequency change during operation), should be executed when the PDN pin = "L" or RSTN bit = "0". Changing the clock frequency or clock settings during operation may cause sound skipping or incorrect detection of the diagnostic circuit.

CKS2 bit	CKS1 bit	CKS0 bit	Clock Speed	
0	0	0	128fs	
0	0	1	192fs	
0	1	0	256fs	
0	1	1	384fs	
1	0	0	512fs	(default)
1	0	1	1024fs	
1	1	0	2048fs	

Table2: Master Clock Control

FS12K bit	FS2 bit	FS1 bit	FS0 bit	Sampling Rate (fs)	Sampling Speed mode	
0	0	0	0	8kHz	Normal	
1	0	0	0	12kHz		
0	0	0	1	16kHz		
1	0	0	1	24kHz		
0	0	1	0	32kHz		
1	0	1	0	44.1kHz, 48kHz		(default)
0	0	1	1	72kHz	Double	
1	0	1	1	96kHz		
0	1	0	0	144kHz	Quad	
1	1	0	0	192kHz		

Table 3. Sampling Rate Setting

CPCK1 bit	CPCK0 bit	Charge Pump Switching Frequency				
		fs=8k, 16k, 32kHz	fs=72k, 144kHz	fs=12k, 24k,48k, 96k, 192kHz	fs=44.1kHz	
0	0	0.512 MHz	0.576 MHz	0.768 MHz	0.706 MHz	(default)
0	1	2.048 MHz	2.304 MHz	2.048 MHz	1.882 MHz	
1	0	2.731 MHz	3.072 MHz	3.072 MHz	2.822 MHz	
1	1	2.048 MHz	2.304 MHz	3.072 MHz	2.822 MHz	

Table 4. Charge Pump Frequency Setting

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LRCK	MCLK (MHz)						
fs	128fs	192fs	256fs	384fs	512fs	1024fs	2048fs
8kHz	-	-	-	-	4.096	-	-
12kHz	-	-	-	-	6.144	-	-
16kHz	-	-	4.096	6.144	8.192	-	-
24kHz	-	-	6.144	9.216	12.288	-	-
32kHz	-	-	8.192	12.288	16.384	-	-
44.1kHz	-	-	11.2896	16.9344	22.5792	-	-
48kHz	-	-	12.288	18.432	24.576	-	-
72kHz	-	-	18.432	27.648	-	-	-
96kHz	-	-	24.576	36.864	-	-	-
144kHz	18.432	27.648	-	-	-	-	-
192kHz	24.576	36.864	-	-	-	-	-

(-: Not available)

Table 5. System Clock Example (OSR bit = “0”, CPCK1-0 bits = ”00”) (default)

LRCK	MCLK (MHz)						
fs	128fs	192fs	256fs	384fs	512fs	1024fs	2048fs
8kHz	-	-	-	-	-	8.192	-
12kHz	-	-	-	-	-	12.288	-
16kHz	-	-	-	-	8.192	-	-
24kHz	-	-	-	-	12.288	-	-
32kHz	-	-	8.192	12.288	16.384	-	-
44.1kHz	-	-	11.2896	16.9344	22.5792	-	-
48kHz	-	-	12.288	18.432	24.576	-	-
72kHz	-	-	18.432	27.648	-	-	-
96kHz	-	-	24.576	36.864	-	-	-
144kHz	18.432	27.648	-	-	-	-	-
192kHz	24.576	36.864	-	-	-	-	-

Table 6. System Clock Example (OSR bit = “1”, CPCK1-0 bits = ”00”)

LRCK	MCLK (MHz)						
fs	128fs	192fs	256fs	384fs	512fs	1024fs	2048fs
8kHz	-	-	-	-	-	8.192	-
12kHz	-	-	-	-	-	12.288	-
16kHz	-	-	-	-	8.192	-	-
24kHz	-	-	-	-	12.288	-	-
32kHz	-	-	8.192	12.288	16.384	-	-
44.1kHz	-	-	11.2896	16.9344	22.5792	-	-
48kHz	-	-	12.288	18.432	24.576	-	-
72kHz	-	-	18.432	27.648	-	-	-
96kHz	-	-	24.576	36.864	-	-	-
144kHz	18.432	27.648	-	-	-	-	-
192kHz	24.576	36.864	-	-	-	-	-

Table 7. System Clock Example (OSR bit = “0” or “1”, CPCK1-0 bits = ”01”)

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LRCK	MCLK (MHz)						
fs	128fs	192fs	256fs	384fs	512fs	1024fs	2048fs
8kHz	-	-	-	-	-	-	16.384
12kHz	-	-	-	-	-	12.288	
16kHz	-	-	-	-	-	16.384	
24kHz	-	-	-	-	12.288	-	
32kHz	-	-	-	-	16.384	-	
44.1kHz	-	-	11.2896	16.9344	22.5792	-	
48kHz	-	-	12.288	18.432	24.576	-	
72kHz	-	-	18.432	27.648	-	-	-
96kHz	-	-	24.576	36.864	-	-	-
144kHz	18.432	27.648	-	-	-	-	-
192kHz	24.576	36.864	-	-	-	-	-

Table 8. System Clock Example (OSR bit = “0” or “1”, CPCK1-0 bits = ”10”)

LRCK	MCLK (MHz)						
fs	128fs	192fs	256fs	384fs	512fs	1024fs	2048fs
8kHz	-	-	-	-	-	8.192	-
12kHz	-	-	-	-	-	12.288	-
16kHz	-	-	-	-	8.192	-	-
24kHz	-	-	-	-	12.288	-	-
32kHz	-	-	8.192	12.288	16.384	-	-
44.1kHz	-	-	11.2896	16.9344	22.5792	-	-
48kHz	-	-	12.288	18.432	24.576	-	-
72kHz	-	-	18.432	27.648	-	-	-
96kHz	-	-	24.576	36.864	-	-	-
144kHz	18.432	27.648	-	-	-	-	-
192kHz	24.576	36.864	-	-	-	-	-

Table 9. System Clock Example (OSR bit = “0” or “1”, CPCK1-0 bits = ”11”)

Relationship between MCLK and TDM mode in TDM master mode is shown in Table 10. The MCLK is divided by 2 and output as BICK in modes marked with a white dot. In these modes, BICK duty cycle is typically 50%. In modes described with a black dot, BICK duty cycle depends on the duty cycle of the MCLK input. Modes described with, “-”, are not available since the clock frequency of MCLK input is slower than BICK output.

MCLK Speed	TDM128	TDM256	TDM512
128fs	●	-	-
192fs	-	-	-
256fs	○	●	-
384fs	-	-	-
512fs	○	○	●
1024fs	○	○	○
2048fs	○	○	○

(-: Not available)

Table 10: Relationship between MCLK and TDM Modes

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■ Clock Stop Detection Circuit

The AK5734 has MCLK, BICK and LRCK stop detection circuits. The MCLK stop detection circuit is engaged when the MCLK frequency drops under 660kHz. In this case, internal circuits except for clock detection circuits, control registers, internal bias generation circuit and LDO (when LDOE pin = "H") are stopped.
BICK, LRCK stop detection circuits are engaged after 8192 MCLK cycles are received with no activity on BICK and LRCK. In this case, internal circuits except for clock detection circuits, control registers, the internal bias generation circuit, and LDO (when LDOE pin = "H") are stopped.

■ Audio Interface Formats

14 types of audio interface formats are selectable with the DIF, TDM1-0 and SLOT bits. In all modes the serial data format is MSB first, 2's complement.

Available audio interface formats are different depending on the operation mode (Normal, Double or Quad). Modes described as "Yes" in the table below are supported.

When the data length is 16-bits, the AK5734 supports up to 8ch outputs in TDM128 mode (4ch AK5734 x 2). In TDM256 and 512 modes, the AK5734 supports up to 16ch outputs (4ch AK5734 x 4).
When the data length is 24-bits, the AK5734 supports up to 4ch outputs in TDM128 mode. 8ch outputs and 16ch outputs can be supported in TDM256 mode and TDM512 mode, respectively by using two AK5734s or four AK5734s.
In TDM mode, the slot length can be set to 16BICK or 32BICK by SLOT bit.
When SLOT bit ="0", the slot length is 32BICK, and it is 16BICK when SLOT bit = "1".

Note: SDTO1-2 data should be captured on a rising edge of BICK.

Mode		SLOT bit	TDM1 bit	TDM0 bit	DIF bit	BICK Freq.	Speed mode			Data Format
							Normal	Double	Quad	
Stereo	0	*	0	0	0	64fs	Yes	Yes	Yes	24-bits I²S (Figure 29) Default
	1	*			1					24-bits Left Justified (Figure 30)
TDM128	2	0	0	1	0	128fs	Yes	Yes	Yes	24-bits I²S (Figure 31)
	3	0			1					24-bits Left Justified (Figure 32)
	4	1			0					16-bits I²S (Figure 33)
	5	1			1					16-bits Left Justified (Figure 34)
TDM256	6	0	1	0	0	256fs	Yes	Yes	-	24-bits I²S (Figure 35)
	7	0			1					24-bits Left Justified (Figure 36)
	8	1			0					16-bits I²S (Figure 37)
	9	1			1					16-bits Left Justified (Figure 38)
TDM512	10	0	1	1	0	512fs	Yes	-	-	24-bits I²S (Figure 39)
	11	0			1					24-bits Left Justified (Figure 40)
	12	1			0					16-bits I²S (Figure 41)
	13	1			1					16-bits Left Justified (Figure 42)

(-: Not available)

Table 11. Audio Data Interface Modes Setting

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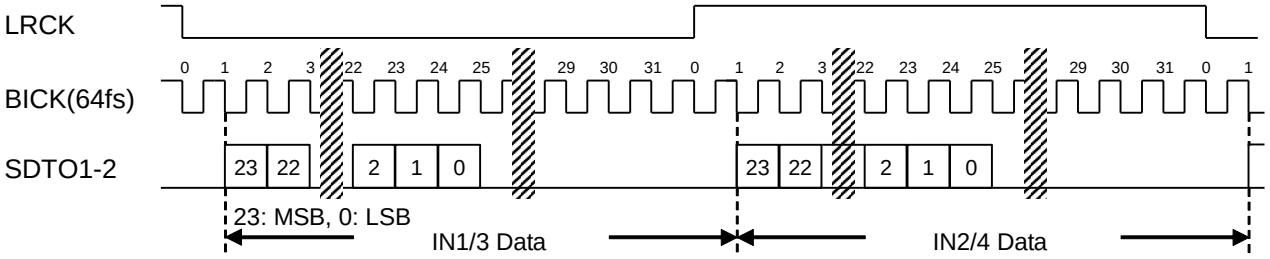

Figure 29. Mode 0 Timing (Stereo Mode (24-bits I²S))

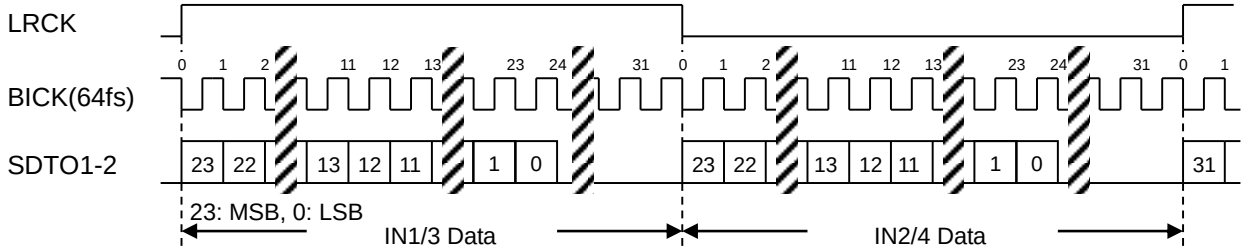

Figure 30. Mode 1 Timing (Stereo Mode, 24-bits MSB Justified)

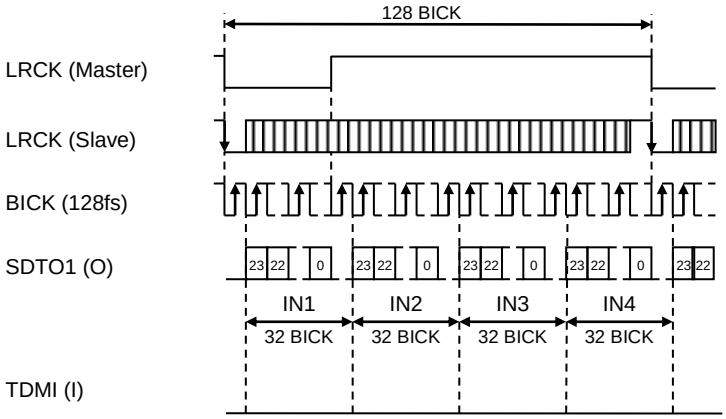

Figure 31 Mode 2 Timing (TDM128 Mode, 24-bits I²S Compatible)

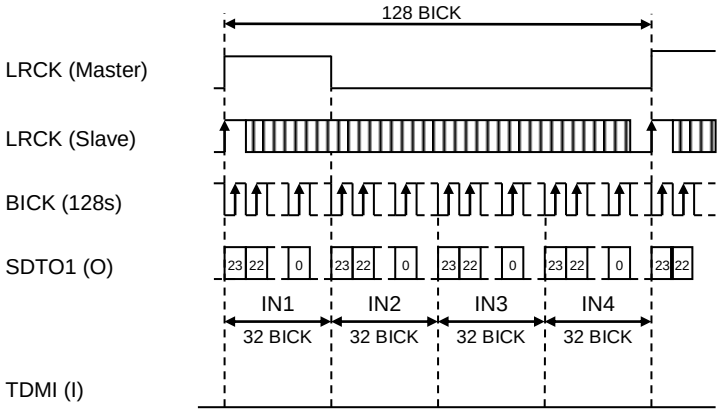

Figure 32. Mode 3 Timing (TDM128 Mode, 24-bits MSB Justified)

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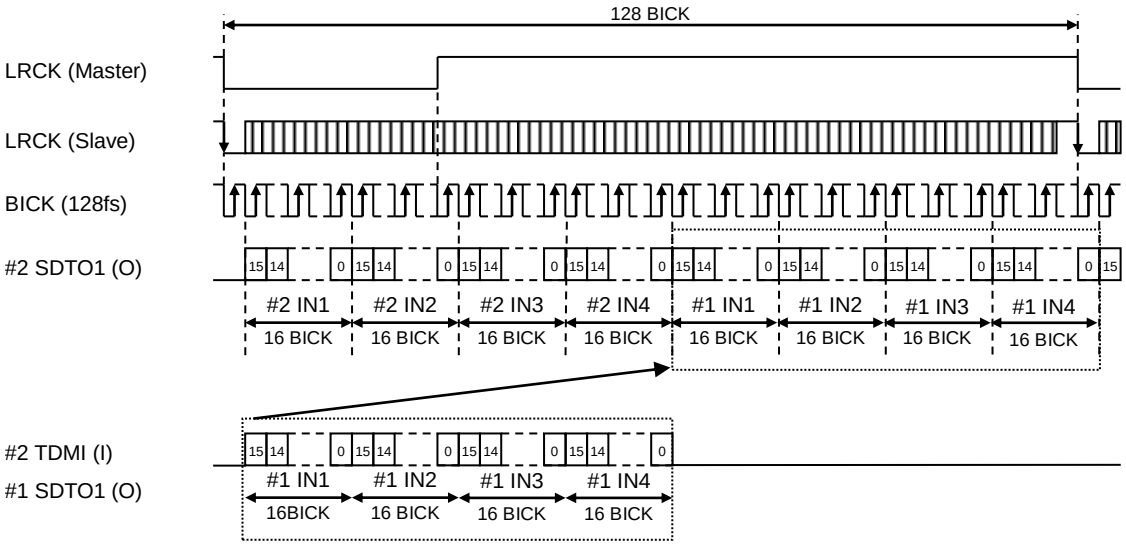

Figure 33. Mode 4 Timing (TDM128 Mode, 16-bits I²S Compatible)

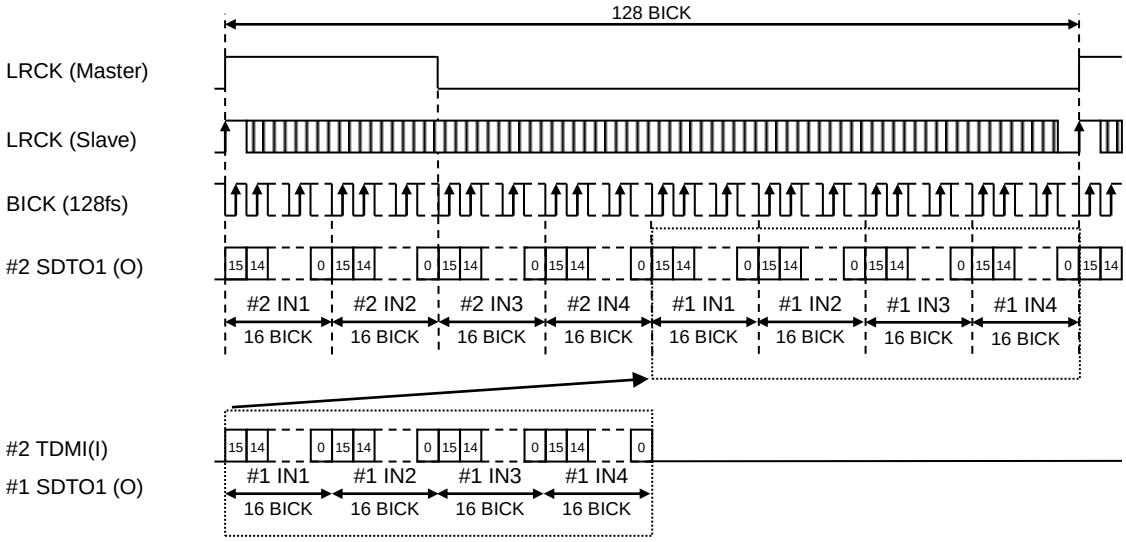

Figure 34. Mode 5 Timing (TDM128 Mode, 16-bits MSB Justified)

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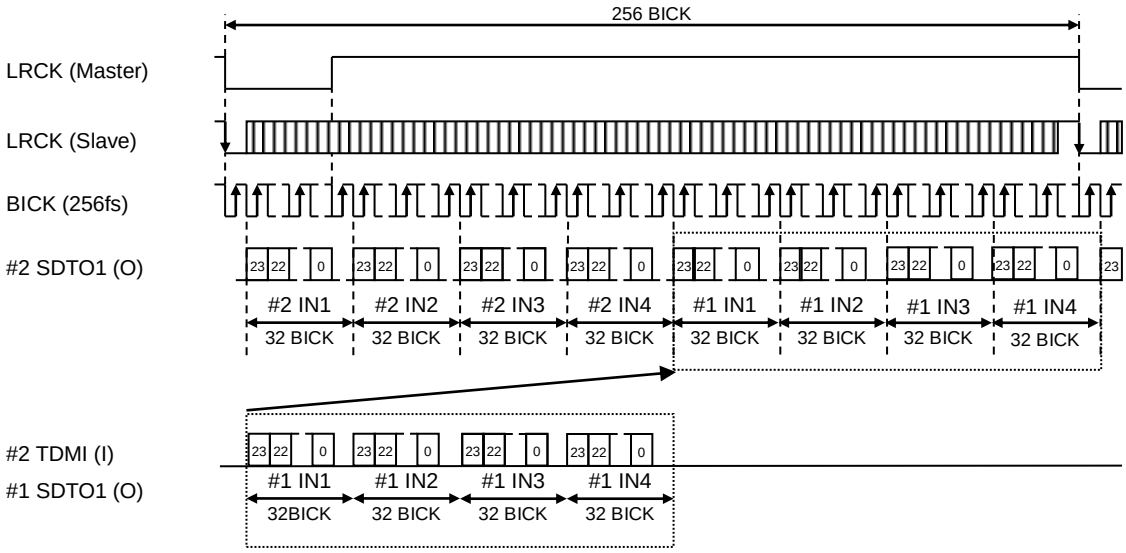

Figure 35. Mode 6 Timing (TDM256 Mode, 24-bits I²S Compatible)

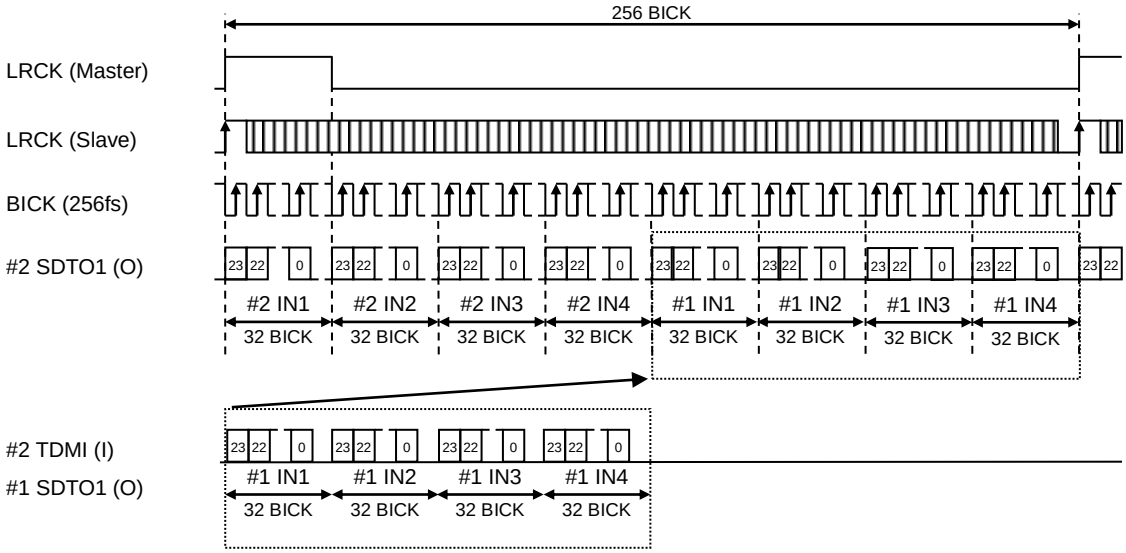

Figure 36. Mode 7 Timing (TDM256 Mode, 24-bits MSB Justified)

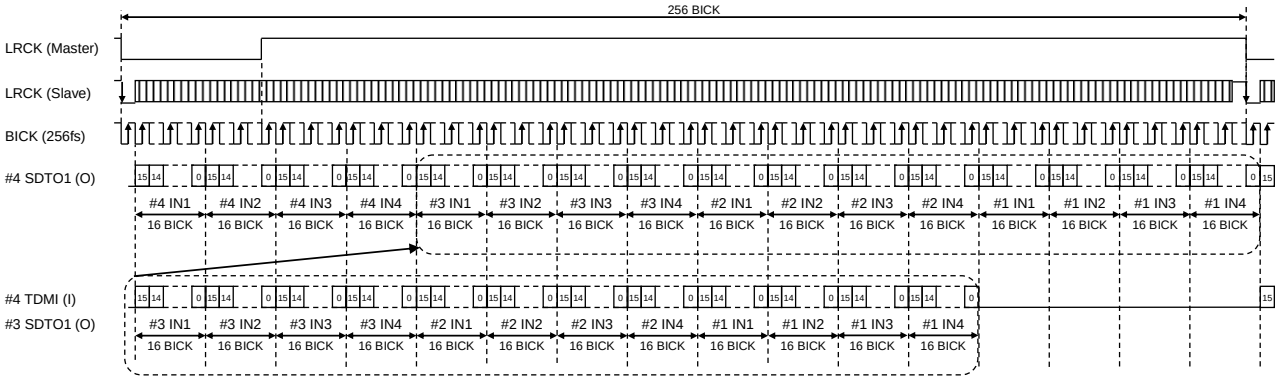

Figure 37. Mode 8 Timing (TDM256 Mode, 16-bits I²S Compatible)

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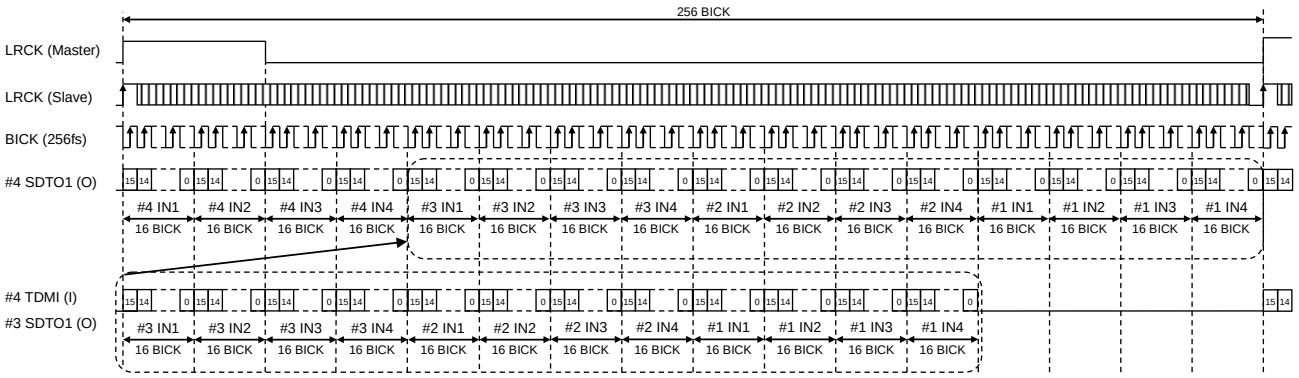

Figure 38. Mode 9 Timing (TDM256 Mode, 16-bits MSB Justified)

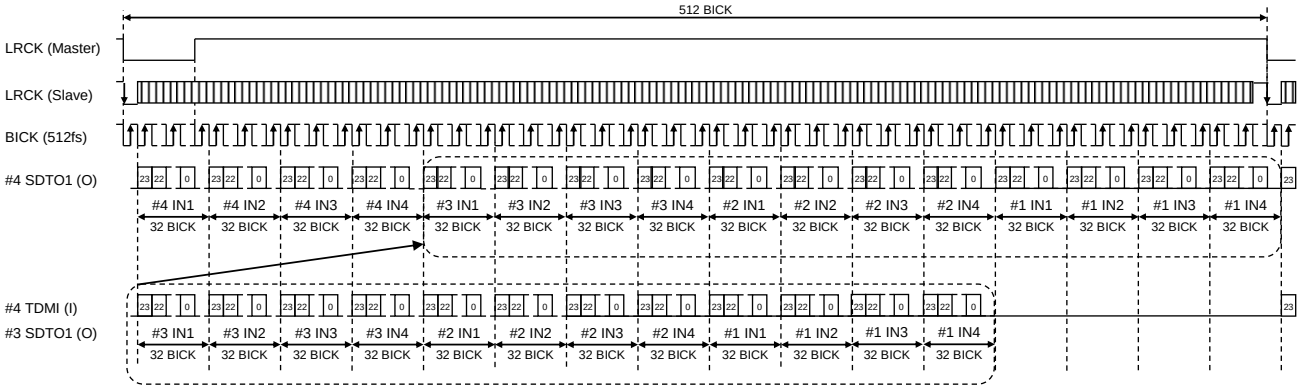

Figure 39. Mode 10 Timing (TDM512 Mode, 24-bits I^{2}S Compatible)

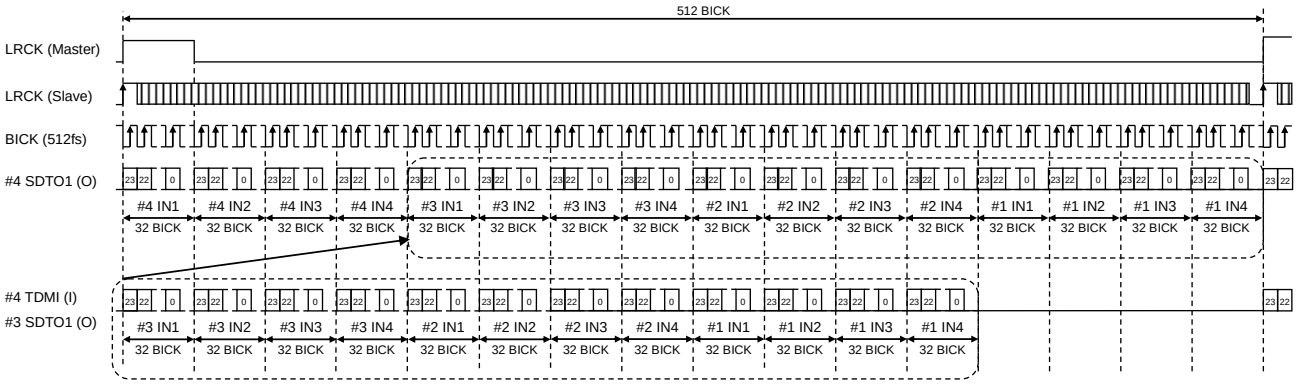

Figure 40. Mode 11 Timing (TDM512 Mode, 24-bits MSB Justified)

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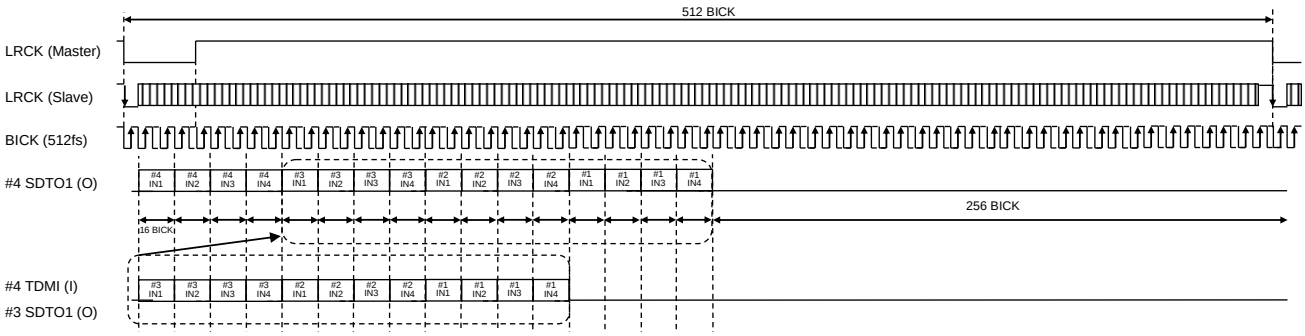

Figure 41. Mode 12 Timing (TDM512 Mode, 16-bits I^{2}S Compatible, 1SLOT = 16BICK)

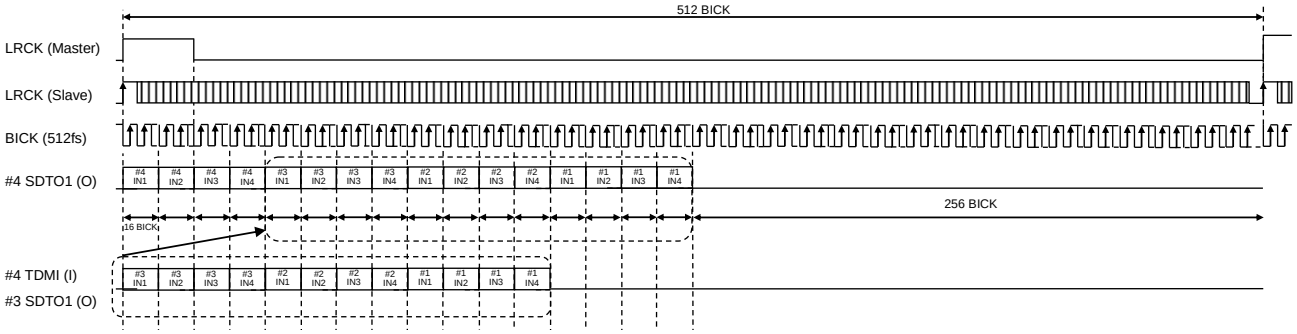

Figure 42. Mode 13 Timing (TDM512 Mode, 16-bits MSB Justified, 1SLOT = 16BICK)

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■ Cascade Connection in TDM Mode

The AK5734 supports the connection of two cascaded devices in TDM128 and TDM256 modes. And it supports the connection of four cascaded devices in TDM256 and 512 modes. Figure 43 shows a connection example. The A/D converted data of all connected AK5734s is output from the SDTO1 pin of the last AK5734, via this cascaded connection.

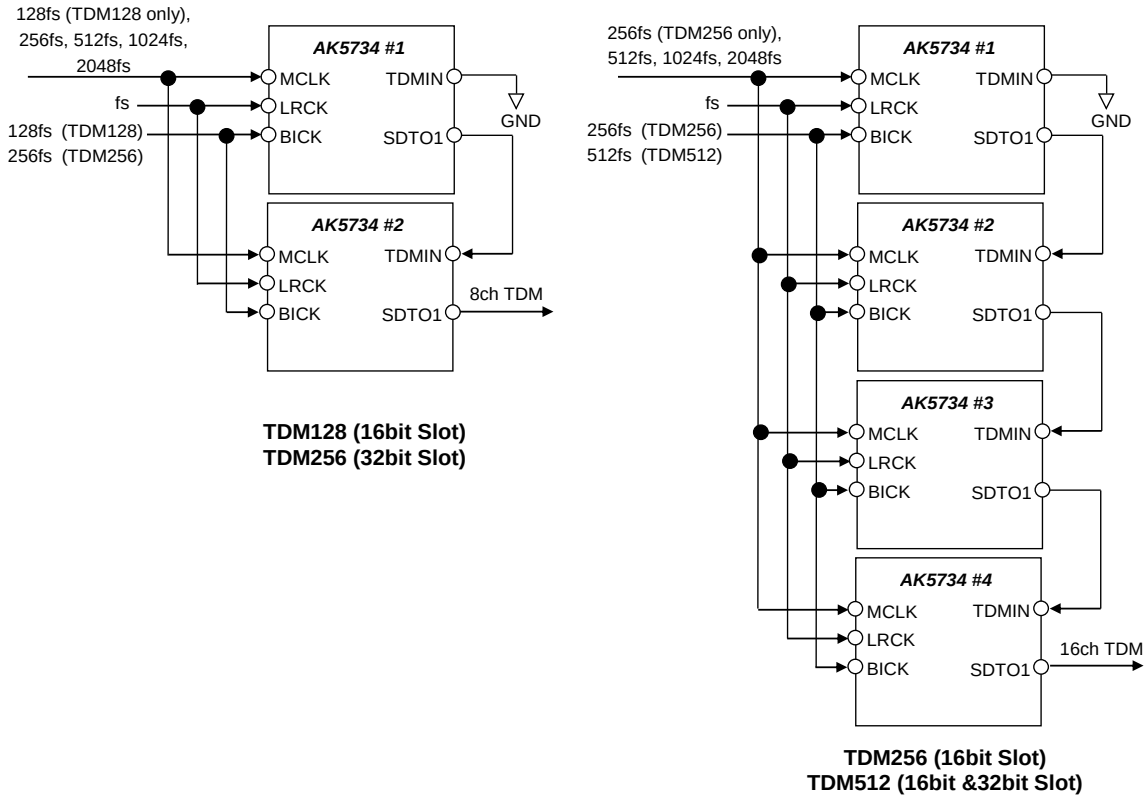

Figure 43: Cascade Connection

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■ Digital HPF

The AK5734 has a digital high-pass filter (HPF) for DC offset cancellation. The cut-off frequency fc of the high-pass filter is 2.0Hz with the maximum sampling frequency in each range of fs.

When 8kHz ≤ fs ≤ 12kHz, fc = 2Hz @ fs=12kHz.

When 12kHz < fs ≤ 24kHz, fc = 2Hz @ fs=24kHz

When 24kHz < fs ≤ 48kHz, fc = 2Hz @ fs=48kHz

When 48kHz < fs ≤ 96kHz, fc = 2Hz @ fs=96kHz

When 96kHz < fs ≤ 192kHz, fc = 2Hz @ fs=192kHz

The cut-off frequency fc is proportional to the sampling frequency fs for each range of fs.

For example:
When fs is 44.1kHz, the fs is satisfied with 24kHz < fs ≤ 48kHz. Thus, fc is proportional to the 48kHz.
The cutoff frequency fc = 2Hz x 44.1/48 = 1.84Hz.

■ Digital Filter Setting

The AK5734 has five types of digital filters. They are selected by the VOICE, SD and SLOW bits. VOICE bit is valid only when fs ≤ 48kHz. If the fs is over 48kHz, VOICE bit is invalid, and the digital filter is set according to SD and SLOW bits.

VOICE bit	SD bit	SLOW bit	Filter	
0	0	0	Sharp Roll-off Filter	(default)
0	0	1	Slow Roll-off Filter	
0	1	0	Short Delay Sharp Roll-off Filter	
0	1	1	Short Delay Slow Roll-off Filter	
1	*	*	Voice Filter	

Table 12: Digital Filter Setting (*: Don't care)

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■ Digital Volume

The AK5734 has a digital volume setting (168 levels, 1dB per step) that can configured independently for each channel. The digital volume for each channel can be set via the register ATT17-10 bits (1ch), ATT27-20 bits (2ch), …, ATT47-40 bits (4ch), (Table 13). The value that is set while RSTN bit = "0" will be the default value for the digital volume. The AK5734 starts operation from this default value when the RSTN bit is set to "1". ATT*7-0 bits (*=1-4) are initialized to 34H by setting the PDN pin to "L".

ATT* bits (*1-4ch)	Volume	
00H	52dB	
01H	51dB	
:	:	
32H	2dB	
33H	1dB	
34H	0dB	(default)
35H	-1dB	
36H	-2dB	
37H	-3dB	
:	:	
A6H	-114dB	
A7H	-115dB	
A8H	MUTE	
A9H	MUTE	
:	MUTE	
FFH	MUTE	

Table 13: Gain of Digital Volume

The volume transition set by ATT*7-0 bits (*=1-4) is a soft transition, thus no switching noise occurs during the transition. Digital volume transition speed is set by ATS1-0 bits (Table 14).

Mode	ATS1	ATS0	Gain Change per 1/fs	Transition Time +52dB ↔ Mute	
0	0	0	0.03125dB	5376/fs	(default)
1	0	1	0.0625dB	2688/fs	
2	1	0	0.25dB	672/fs	
3	1	1	0.5dB	336/fs	

Table 14: Digital Volume Transition Speed

In Mode 0, it takes 5376/fs (112ms@fs=48kHz) to change the volume from +52dB (00H) to MUTE (A8H-FFH) or from MUTE (A8H-FFH) to +52dB (00H).

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■ Power Up/Down Sequence Example

In slave mode, the device is released from reset by setting RSTN bit = "1" after MCLK, BICK and LRCK inputs are applied, following the PDN pin = "H". After that, power down state is released by detecting a rising edge of LRCK following a rising edge of MCLK.

In master mode, the device is released from reset when a rising edge of MCLK is detected following RSTN bit = "1" after setting the PDN pin = "H". The initialization cycle begins at this point.

When the CPEN pin = "L" (charge pump enabled), data is shifted out on the SDTO pin 3324 × 1/fs (in slave mode) or 3321 × 1/fs (in master mode) after the device is released from reset by setting RSTN bit = "1".
When the CPEN pin = "H" (charge pump disabled), data is shifted out on the SDTO pin 2262 × 1/fs (in slave mode) or 2259 × 1/fs (in master mode) after the device is released from reset by setting RSTN bit = "1".

During initialization, the ADC output data is "0" in 2's complement. Output data corresponds to the analog input content only after initialization (this takes about one group delay period).

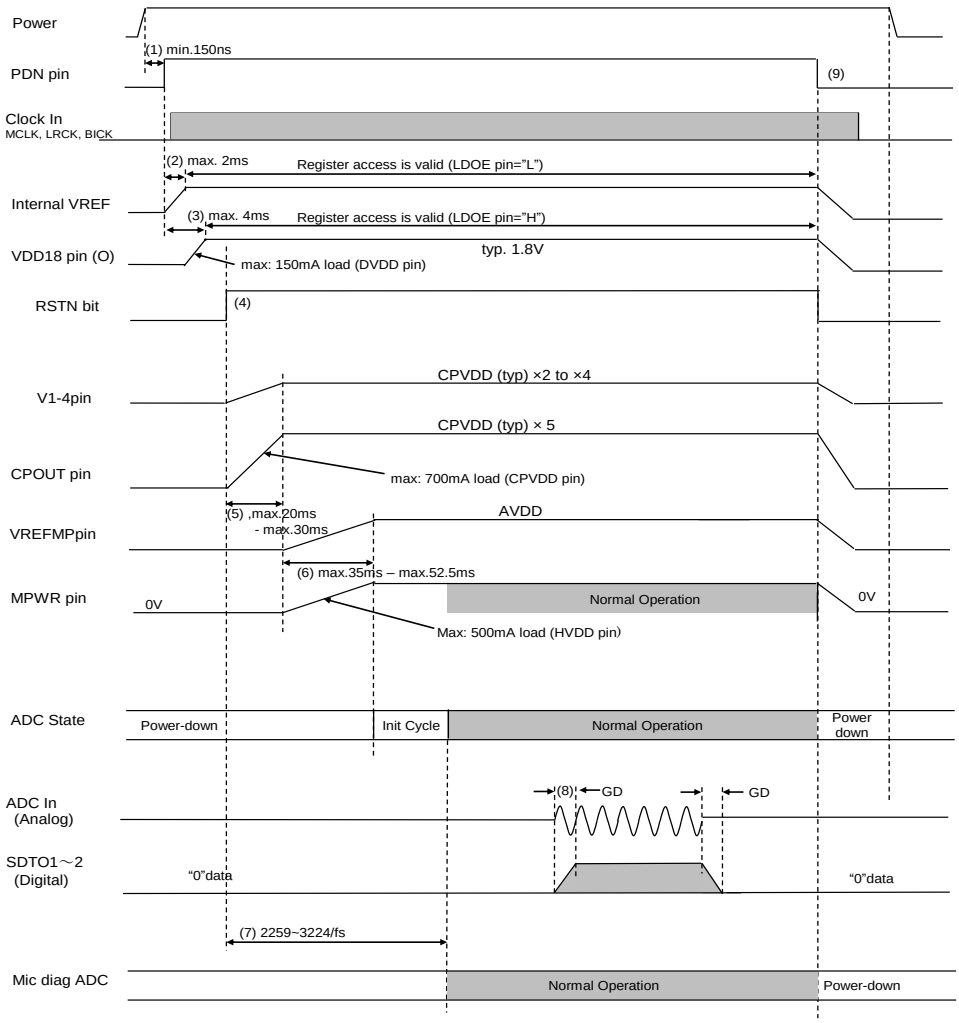

Figure 44: Power Up/Down Sequence

(1) Set the PDN pin = "L" → "H" after powering on all the power supplies. The PDN pin must be held at "L" for at least 150ns before setting to "H" after all power is supplied.

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(2) When the LDOE pin = “L” (1.8V power supply is supplied externally), the internal VREF circuit rises up to 2ms after the PDN pin = “H” and the register can be accessed.
(3) When the LDOE pin = “H” (using the internal 1.8V LDO), the internal LDO is powered up and the register access will be available in 4ms after the PDN pin = “H”.
(4) Make necessary register settings such as setting of clocks, audio IF, error diagnosis function, output level of microphone bias voltage, etc., and set RSTN bit = “1”. It is prohibited to change the clock mode while RSTN bit = “1”.
(5) The internal charge pump powers up after 20msec when the CPEN pin = “L” and fs = 48kHz. With a 48kHz based sampling frequency, 12kHz, 24kHz, 48kHz, 96kHz, and 192kHz power up time is 20msec. With a 32kHz based sampling frequency, 8kHz, 16kHz, 32kHz, 72kHz, and 144kHz the time becomes 30msec. When fs = 44.1kHz, the time is 21.8ms.
The internal charge pump will not be powered up when the CPEN pin = “H”. This power-up time is not necessary when not using the internal charge pump and supplying HVDD externally.
(6) When fs = 48kHz, the MPWR pin and the VREFMP pin rise in max.35ms after the internal charge pump is powered up. With a 48kHz based sampling frequency (12kHz, 24kHz, 48kHz, 96kHz, and 192kHz), the power up time is max.35msec. With a 32kHz based sampling frequency (8kHz, 16kHz, 32kHz, 72kHz and 144kHz), the time is max.52.5msec. When fs = 44.1kHz, the time is max.38.1ms.
(7) The AK5734 outputs data and error detections become enabled after max.67ms (@fs=48kHz) by setting the RSTN bit = “1” when the CPEN pin = “L”. It will be after max.47ms (@fs=48kHz) if the CPEN pin = “H”.
(8) There is a group delay (GD) on the SDTO1-2 output from the ADC input.
(9) All circuits are powered down by setting the PDN pin = “H” → “L”.

Note:
The wait time of (7) is inversely proportional to the maximum sampling frequency fs of the operation mode set by FS2-0 bits.

Example: When the CPEN pin = "L" and fs = 32kHz, the wait time of 67ms × (48/32) = 100.5ms is required. The reference wait time at 48kHz is 67ms. When the CPEN pin = "L" and fs = 16kHz, a wait time of 79ms × (24/16) = 118.5ms is required. The reference wait time at 24kHz is 79ms.

fs	Wait time until Output
8kHz ≤ fs ≤ 12kHz	103 ms @ 12kHz
12kHz < fs ≤ 24kHz	79 ms @ 24kHz
24kHz < fs ≤ 48kHz	67 ms @ 48kHz
48kHz < fs ≤ 96kHz	61 ms @ 96kHz
98kHz < fs ≤ 192kHz	58 ms @ 192kHz

Table 15: Wait Time until Data is Output, (CPEN pin = “L”)

fs	Wait time until Output
8kHz ≤ fs ≤ 12kHz	83 ms @ 12kHz
12kHz < fs ≤ 24kHz	59 ms @ 24kHz
24kHz < fs ≤ 48kHz	47 ms @ 48kHz
48kHz < fs ≤ 96kHz	41 ms @ 96kHz
98kHz < fs ≤ 192kHz	38 ms @ 192kHz

Table 16: Wait Time until Data is Output, (CPEN pin = “H”)

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■ Analog Input Connection

The analog input connection method is shown in this section. The AK5734 supports line and microphone inputs. 4 differential analog input channels are available. AC or DC connections are selectable at each channel by setting the AC4-1 bits. Analog signals are input into the PGA via differential input pins of each channel. The voltage difference of IN*P and IN*N pins will be the input voltage (* = 1-4). The ADC input range is 2.0Vrms (typ.).

The Input DC operating point of the IN*P pin must be higher than the IN*N pin.

□ Microphone Inputs

The connection method for a microphone input application and the AK5734 is shown below. Please follow the diagram of the connected ECM for the MIC bias voltage. The AK5734 is capable of supplying 5 - 9V, (in 0.5V steps). Voltage is supplied from the MPWR pin. In the use case of connecting multiple microphones, you must not exceed the maximum current of the MIC Power Supply.

Electret Condenser Microphone (ECM) DC Connection Differential Input

Set AC4-1 bits = “0” when using a DC connection. Normally, the output signal amplitude is proportional to MIC bias voltage with an electric capacitor microphone (ECM). When supplying 9V to the MIC bias voltage, the 2Vrms differential signal can be output from the ECM. In this case, 1Vrms (2.8V p-p) is input to both the IN*P pin and the IN*N pin of the AK5734. Common voltage depends on the connected ECM but normally it will be equivalent to “2/3 x MIC bias voltage” at the IN*P pin and “1/3 x MIC bias voltage” at the IN*N pin.

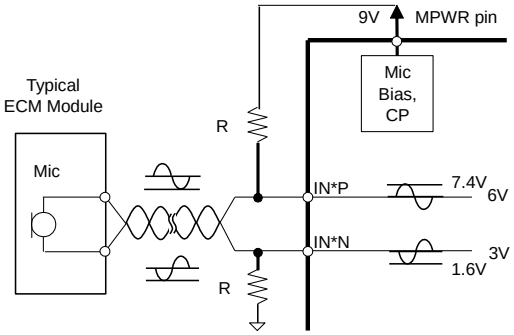

Figure 45: DC Connection Differential Input

Dynamic MIC AC Connection Differential Input

Set AC4-1 bits = “1” when using AC connection. Common voltage is 2.5V, (typ.), and generated internally.

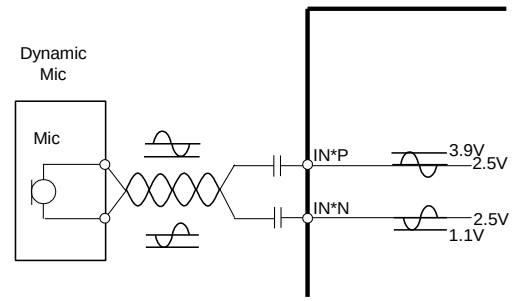

Figure 46: AC Connection Differential Input

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Electret Condenser Microphone (ECM) DC connection Single-ended Input

Set AC4-1 bits = “0” when using a DC connection. With single-ended input, signal amplitude will be half of the differential input since a signal is input to the IN*P pin. The available input signal amplitude of the IN*P pin is 1Vrms (typ.) Common voltage depends on the connected ECM but normally it will be about “1/2 x MIC bias voltage”.

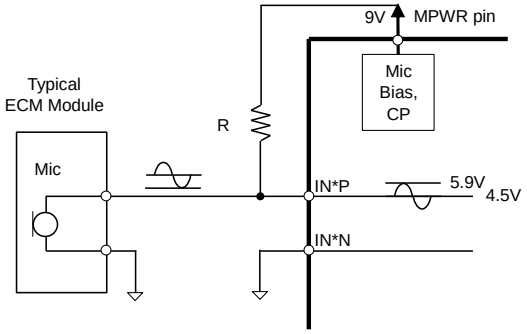

Figure 47: Single-ended Input DC Connection, (IN*P/N pins)

Dynamic MIC AC Connection Single-ended Input

Set AC4-1 bits = “1” when using an AC connection. Common voltage is 2.5V, (typ.) and generated internally.

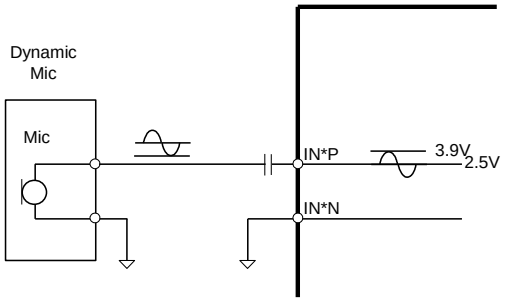

Figure 48: Single-ended Input AC Connection, (IN*P/N pins)

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□ Line Input

Normally the output amplitude of an automotive power amplifier is about 10Vrms (differential), and common voltage is about 7.2V, (assuming a BTL connection with a 14.4V battery). In this case, the input signal amplitude of each IN*P pin and IN*N pin is 5Vrms (14.14Vp-p) and common voltage is 7.2V. The amplitude range is from 14.27V (7.2V + 7.07V) to 0.13V (7.2V − 7.07V). External resistance values (R1 and R2) should be adjusted so that the input signal to IN*P pin and IN*N pin will not exceed 2.0Vrms.

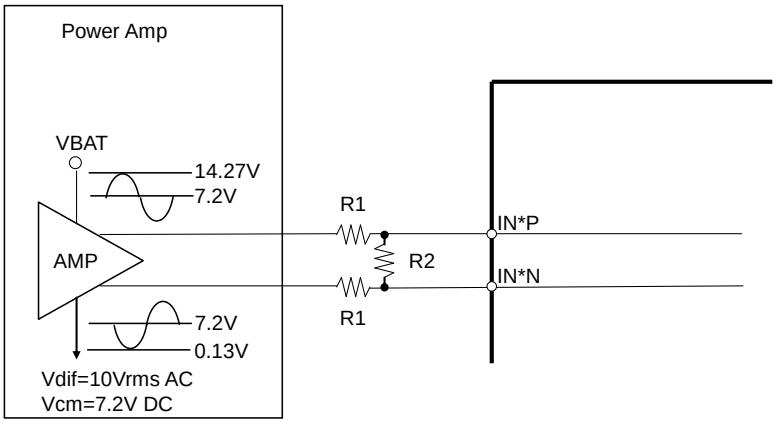

Figure 49: Differential Input DC Connection, (IN*P/N pins)

■ Full Scale Clip Function

As shown in Figure 50, the output becomes full scale when the analog input is over 0dBFS.

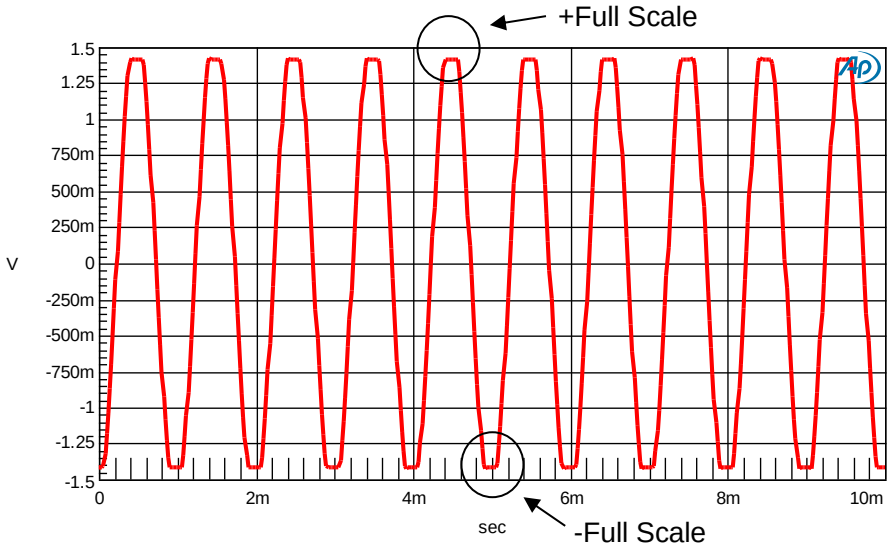

Figure 50: Output Signal with an input of 1kHz 2.3Vrms Signal (2.0Vrms = 0dBFS)

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■ Pre-Gain Amplifier (PGA) for MIC Input

The AK5734 has a PGA for microphone input. Each microphone input gain can be set with the PG13-10 bits, (1ch), PG23-20 bits (2ch), …, PG43-40 bits (4ch) in the range of 0dB, +6dB - +20dB, (1dB Step). Set the PG* bits (*=1-4) so that the input voltage to the ADC block will not exceed 2.0 Vrms, (ADC full-scale).

PG*3	PG*2	PG*1	PG*0	Input Gain	
0	0	0	0	0dB	(default)
0	0	0	1	6dB	
0	0	1	0	7dB	
0	0	1	1	8dB	
0	1	0	0	9dB	
0	1	0	1	10dB	
0	1	1	0	11dB	
0	1	1	1	12dB	
1	0	0	0	13dB	
1	0	0	1	14dB	
1	0	1	0	15dB	
1	0	1	1	16dB	
1	1	0	0	17dB	
1	1	0	1	18dB	
1	1	1	0	19dB	
1	1	1	1	20dB	

Table 17: PGA for Microphone Input Gain Setting (*=channel number)

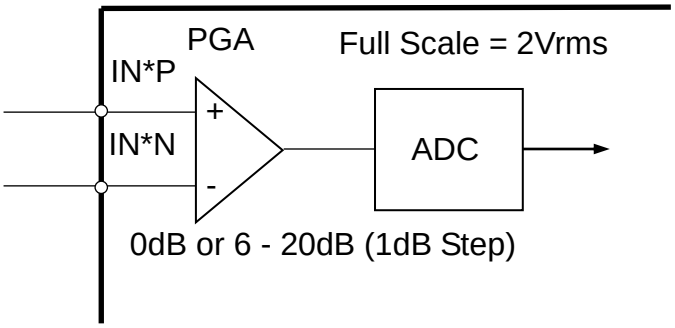

Figure 51: Input Step Construction

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■ Charge Pump

The AK5734 has an integrated charge pump to generate the MIC bias voltage and analog voltage such as for a PGA, etc. When use the charge pump, external capacitors should be connected to as shown in Figure 52 and set CPEN pin = "L". The charge pump boosts the CPVDD voltage and output it from the CPOUT pin. Connect the CPOUT pin with the HVDD pin.

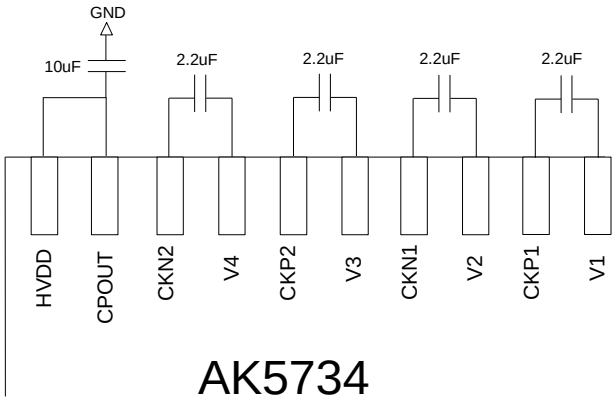

Figure 52: Charge Pump Connection Diagram (CPEN pin = "L")

When the CPEN pin = "L", it is recommended that the trace which connects the CPOUT pin with the HVDD pin is close as physically possible to a 10uF capacitor.

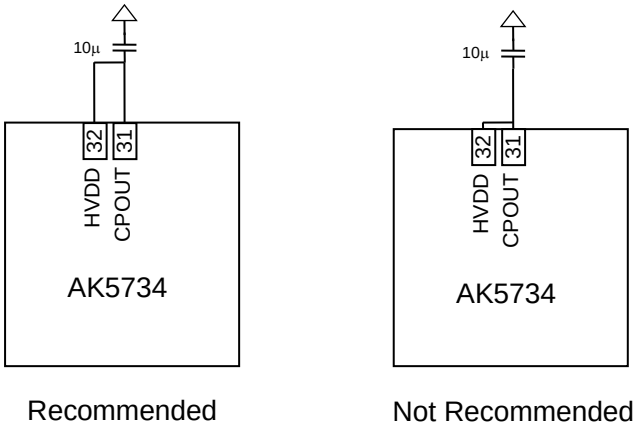

Figure 53: Connection position between CPOUT pin and HVDD pin (CPEN pin = "L")

The charge pump switching frequency is 512kHz or 768kHz in default setting. The switching frequency can be shifted to around 2MHz or 3MHz by CPCK1-0 bits (Table 4). This function can prevent the frequency interference with a radio IC.

The charge pump is not powered up when setting the CPEN pin = "H". In this case, the external power supply (typ.14.5V) should be connected to the HVDD pin. Connect the CPVDD pin to the AVDD pin, and leave the V1-4 pins, CKP1-2 pins, and CKN1-2 pins open.

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■ MIC Bias Voltage

MIC bias voltage is set by the MBS3-0 bits in a range of 5 - 9 V (0.5V steps), and is output on the MPWR pin. The MPWR pin should be connected to AVSS via a 1Ω resistor and a 10μF ceramic capacitor. The VREFMP pin should be connected to AVSS via a 2.2μF ceramic capacitor. (Figure 75)

MBS3-0	Mic Bias Voltage	
00H	5V	(default)
01H	5.5V	
02H	6V	
03H	6.5V	
04H	7V	
05H	7.5V	
06H	8V	
07H	8.5V	
08H	9V	
09H-0FH	Pulled-down by 4.5kΩ (typ) (Power down state)	

Table 18: MIC Bias Voltage Setting

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■ Error Detection Function

The AK5734 drives the INT pin “L” when one of the following nine error conditions is detected. The error status registers (11H - 15H), which reflect the ADC input’s error status, are updated simultaneously. Errors 1-5 are detectable only in DC connection mode. Errors 6-9 can be detected at any time. The INT pin outputs an OR-ed signal based on the below nine interrupt events. The INT pin should be pulled up to DVDD via a 10kΩ resistor.
Error status registers can be masked by setting the appropriate mask bit (18H - 1BH). When a mask bit is set to “0” (error condition not masked), the corresponding error status register bit will be set to “1” when an error is detected. If the mask register bit is set to “1” (error condition masked), the corresponding error status register bit remains “0.” In this case, the masked error will not be reflected at the INT pin.

Table 19: Error Statuses, Error Status Registers, and Mask Registers

No.	Error Status	Error Status Register	Mask Register
1	OPEN: Input Open	OPEN* (*1-4)	MOPEN* (*1-4)
2	SHTD: Short between Positive and Negative Inputs	SHTD* (*1-4)	MSHTD* (*1-4)
3	SHTG: Short to Ground	SHTG* (*1-4)	MSHTG* (*1-4)
4	SHMB: Short to MIC Bias Voltage	SHMB* (*1-4)	MSHMB* (*1-4)
5	SHTV: Short to Battery	SHTV* (*1-4)	MSHTV* (*1-4)
6	OVDET: MIC Bias Overvoltage Threshold is 11.9V (typ.). It not depending on the setting of MIC bias voltage (MBS3-0 bits).	OVDET	-
7	OIDET: MIC Bias Overcurrent Threshold is 280mA (typ.).	OIDET	-
8	OVCP: Charge Pump Under Voltage Threshold is CPOUT Voltage = 5-7V.	OVCP	-
9	OVTP: Over temperature Threshold is 160ºC or more.	OVTP	-

Table 20. Detectable Error Status

No.	Error Status	DC Connection (Differential/Single-end)	AC Connection (Differential/Single-end)
1	OPEN	Yes	N/A
2	SHTD	Yes	N/A
3	SHTG	Yes	N/A
4	SHMB	Yes	N/A
5	SHTV	Yes	N/A
6	OVDET	Yes	Yes
7	OIDET	Yes	Yes
8	OVCP	Yes	Yes
9	OVTP	Yes	Yes

N/A: Not Available

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□ Internal circuit status at error detection and error release method

Analog Input Connection Error (Error 1-5)
Internal circuits are not powered down when errors are detected. These error statuses can be released by setting INTR bit = “1”, or RSTN bit = “0”.

MIC Bias Over Voltage, MIC Bias Over Current, Charge Pump Under Voltage (Error 6-8)
The behavior of internal circuits upon detection of an error condition is selected by ERRPDSEL bit (2EH).
If ERRPDSEL bit = “0”, internal circuits are not powered down when errors are detected. It is recommended that the ERRPDSEL bit is changed during RSTN bit = “0”. These error statuses can be cleared by setting INTR bit = “1”, or RSTN bit = “L”.
If ERRPDSEL bit = “1”, internal circuits are powered down when errors are detected. In this mode, error status registers are not reset since control registers are not powered down. The INT pin drives “L“. These error statuses can be cleared by setting RSTN bit = “0” or PDN pin = “L”.

Over Temperature (Error 9)
Internal circuits are powered down when this error is detected. At this time, error status registers are not reset since control registers are not powered down, and the INT pin outputs “L“. There are two types of power-down due to over temperature, latch type and automatic reset type, which can be selected by OVTPSEL bit.
When OVTPSEL bit = “0”, set RSTN bit = “0” or the PDN pin = “L” to reset error status. When OVTPSEL bit = “1”, RSTN bit = “0” → “1” sequence is automatically executed, and the error status is reset when the internal temperature drops 110ºC or lower up to the number of times according to automatic recovery count set by OVTPCNT bit. It is also possible to reset the error status by setting RSTN bit = “0” or the PDN pin = “L”.
If the number of automatic recovering set by OVTPCNT bit is exceeded, the error status is not reset until setting RSTN bit = “0”, the PDN pin = “L”, or reading OVTPCM bit.

Table 21: State of the Internal Circuit and How to Reset Error Status

No	Error Status	Internal Circuit States (Note 44)	Error Release Conditions
1 - 5	OPEN, SHTD, SHTG, SHMB, SHTV	Not powered down	INTR bit = “1” or RSTN bit =”0”
6 - 8	OVDET, OIDET, OVCP	Case: ERRPDSEL bit = “0” Not powered down Case: ERRPDSEL bit = “1” Powered down	Case: ERRPDSEL bit = “0” INTR bit = “1” or RSTN bit = “0” Case: ERRPDSEL bit = “1” RSTN bit = “0” or PDN pin = “L”
9	OVTP	Powered down	Case: OVTPSEL bit = “0” RSTN bit = “0” or PDN pin = “L” Case: OVTPSEL bit = “1” RSTN bit =”0” or PDN pin = “L” or read OVTPCM bit

Note 44: The internal circuit includes the ADC, Error detection circuits 1-8, MIC bias voltage generator, and charge pump.

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□ Detectable Error State

The integrated error detection circuit detects connection errors for the microphone by monitoring the DC level of the microphone input signal. The detectable error status is described below.

OPEN: Input Open

An Input open is detected when the voltage of an IN*P pin approaches the MPWR pin level (MIC bias voltage) and the electrical potential of an IN*N pin approaches GND level. The error status is detected when the voltage of an IN*P pin is within the range of MPWR ± Vth and the voltage of an IN*N pin is under Vth. The threshold voltage Vth can be set via TOP3-0 bits for simple detection (SARTH bit = "0") and is set from THOP12-01 bits for high accuracy detection (SARTH bit = "1"). When using an external microphone bias power supply, connect the microphone bias power supply to the VBATM pin and set REFSEL bit = "1".

Short to MIC Bias Voltage (SHMB) is detected If only IN*P pin is open. Short to ground (SHTG) is detected if only IN*N pin is open.

Error detection criteria is the readout value of MPWR voltage (Address: 4AH and 4BH) when REFSEL bit = "0".

Fault Conditions	Conditions
Positive and Negative Input Open	MPWR – Vth ≤ IN*P ≤ MPWR + Vth and IN*N ≤ Vth

Error detection criteria is the readout value of VBATM voltage (Address: 48H and 49H) when the REFSEL bit = "1".

Fault Conditions	Conditions
Positive and Negative Input Open	VBATM – Vth ≤ IN*P ≤ VBATM + Vth and IN*N ≤ Vth

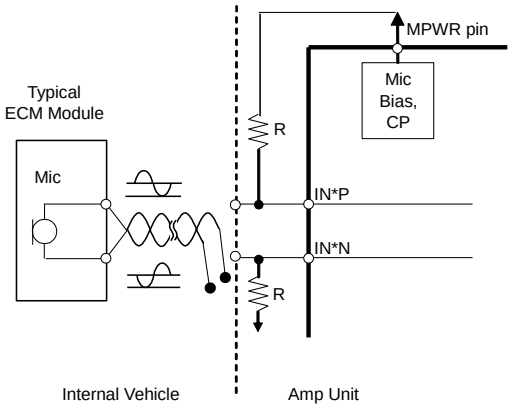

Figure 54: Positive and Negative Input OPEN

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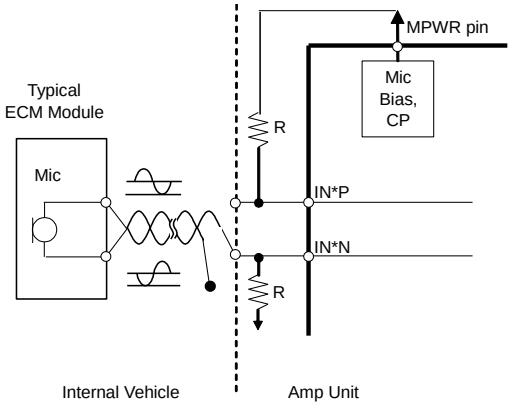
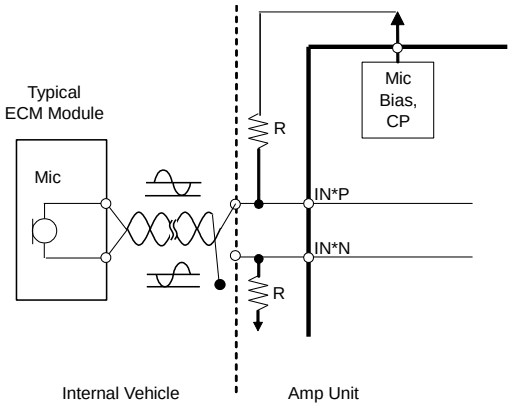


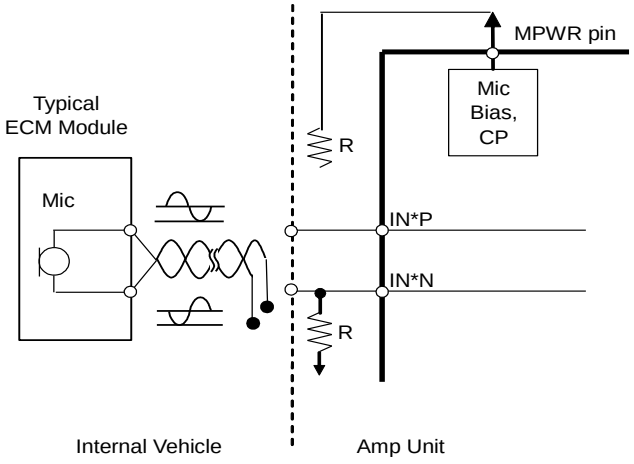
Note: Short to MIC Bias Voltage (SHMB) is detected if only an IN*P pin is open.

Figure 55: Positive Input OPEN



Note: Short to Ground (SHTG) is detected if only an IN*N pin is open.

Figure 56: Negative Input OPEN



If both resistance elements that are connected to microphone input and MPWR pin are open, the INT pin is pulled down by internal resistance (Typ. 1.4 MΩ) and short to ground is detected.

Figure 57: Positive and Negative Input OPEN with MPWR pin Open

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SHTD: Short between Positive and Negative Inputs

The voltage of each pin will be equal to (MIC bias voltage/2) when the positive input pin (IN*P pin) and a negative input pin (IN*N pin) are shorted together. The error status is detected when the voltage difference of IN*P and IN*N pins goes below the threshold voltage Vth set in the registers. The Vth can be set via TSD3-0 bits for simple detection (SARTH bit = “0”) and set by THSD12-01 bits for high accuracy detection (SARTH bit = “1”).

Fault Condition	Condition
Short Between Positive and Negative Inputs	|IN*P – IN*N| ≤ Vth

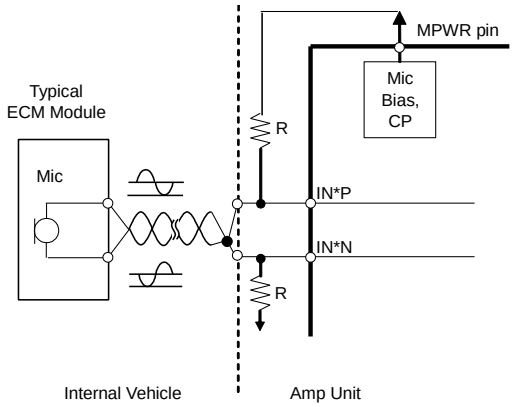

Figure 58: Positive and Negative Input Shorted

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SHTG: Short to Ground

When input pins (IN*P/N pins) are shorted to ground, the voltage approaches 0V. An error status is detected if the voltage of the pin goes under the threshold voltage Vth. The Vth can be set via register TSG3-0 bits for simple detection (SARTH bit = “0”) and it is set by THSG12-01 bits for high accuracy detection (SARTH bit = “1”).

Fault Condition	Condition
Positive Input Short to Ground	IN*P ≤ Vth

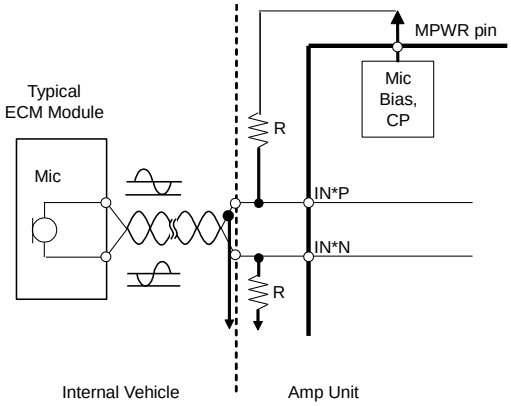

Figure 59: Positive Input Short to GND

Fault Condition	Condition
Negative Input Short to Ground	IN*N ≤ Vth

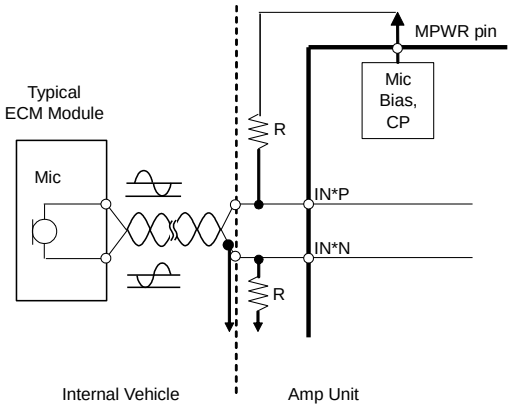

Figure 60: Negative Input Short to GND

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SHMB: Short to MIC Bias Voltage

When input pins (IN*P/N pins) are shorted to MPWR (MIC bias voltage), the input approaches to the MIC bias voltage. An error status is detected if the voltage of the pin goes higher than “MPWR – Vth”. The threshold voltage Vth can be set via register TSB3-0 bits for simple detection (SARTH bit = “0”) and it is set by THSM12-01 bits for high accuracy detection (SARTH bit = “1”).

Error detection criteria is the readout value of MPWR voltage (Address: 4AH and 4BH) when REFSEL bit = “0”.

Fault Conditions	Conditions
Short to MIC bias voltage	IN*P ≥ MPWR – Vth and/or IN*N ≥ MPWR – Vth

Error detection criteria is the readout value of VBATM voltage (Address: 48H and 49H) when REFSEL bit = “1”.

Fault Conditions	Conditions
Short to MIC bias voltage	IN*P ≥ VBATM – Vth and/or IN*N ≥ VBATM – Vth

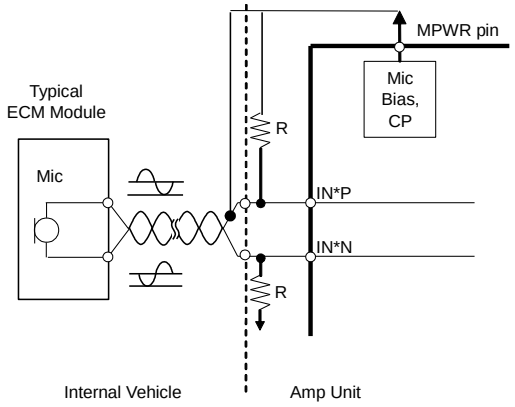

Figure 61: Short to Mic Bias Voltage

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SHTV: Short to Battery

When the input pins (IN*P/N pins) are shorted to the battery, their voltage approaches the battery voltage. An error status is detected if the voltage at the pin becomes higher than “MPWR – Vth”. The threshold voltage Vth can be set via TSV3-0 bits for simple detection (SARTH bit = “0”) and set via THSV12-01 bits for high accuracy detection (SARTH bit = “1”). If there is a possibility of short circuit with the battery, insert a protection resistor between the signal input terminal and INxP/N pin to avoid electrical stress on the device. (See Table 25)

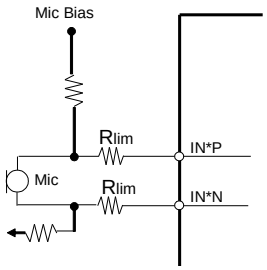

Figure 62: External Protection Circuit for Battery Short

Error detection criteria is the readout value of MPWR voltage (Address: 4AH and 4BH) when REFSEL bit = “0”.

Fault Conditions	Conditions
Short to Battery	IN*P ≥ MPWR + Vth and/or IN*N ≥ MPWR + Vth

Error detection criteria is the readout value of VBATM voltage (Address: 48H and 49H) when REFSEL bit = “1”.

Fault Conditions	Conditions
Short to Battery	IN*P ≥ VBATM + Vth and/or IN*N ≥ VBATM + Vth

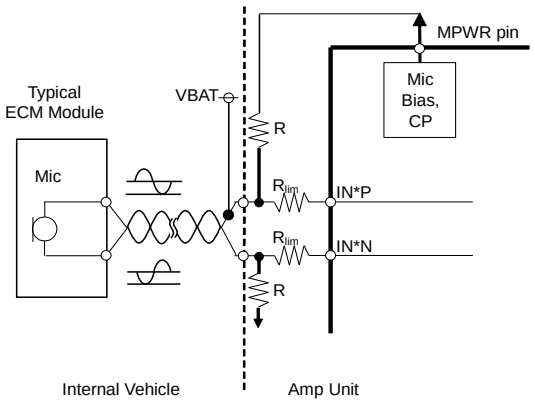

Figure 63: Short to Battery

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□ Threshold Voltage Vth Settings

There are two ways to set the threshold voltage Vth for error detection. When SARTH bit = "0", nine threshold voltage settings (Table 22) are available by setting TOP3-0, TSD3-0, TSG3-0, TSB3-0 and TSV3-0 bits. When the SARTH bit = "1", threshold Voltage can be set with a 12-bit straight binary code with full scale of AVDD for high accuracy error detection.

Simple Error Detection with Nine Threshold Steps (SARTH bit = "0")

Threshold voltage Vth for error detection can be set from the TOP3-0, TSD3-0, TSG3-0, TSB3-0 and TSV3-0 bits. Input signals to the IN*P pin and IN*N pin will be attenuated by 0.3 times the internal resistance and input to the SAR ADC. Therefore, the threshold voltage range at SAR ADC input is from 30mV to 270mV.

bit3-0	Threshold Voltage (Vth)	
00H	100mV	
01H	200mV	
02H	300mV	(default)
03H	400mV	
04H	500mV	
05H	600mV	
06H	700mV	
07H	800mV	
08H	900mV	
09H-0FH	(Reserved)	

Table 22: Error Monitor Threshold Setting

High Accuracy Setting via 12-bit Code (SARTH bit = "1")

The threshold voltage in the high accuracy mode can be set from a 12-bit straight binary code, (Address: 24H-2DH), which the full scale is AVDD. When AVDD = 3.3V, the minimum value of the threshold voltage is 3.3V/4095 = 0.81mV. Vth becomes "n/4095× 3.3V". The "n" is the set value in 24H-2DH. This is the voltage seen at the input of the diagnostic SAR ADC. The signal input to IN*P/N pins (*=1-4) is internally multiplied by 0.3 and enters the SAR ADC. Therefore, Vth seen at IN*P/N pins is Vth = (n / 4095) × 3.3 / 0.3V.

e.g.) When THOP12-1 bits are "000000000011b", Vth = 3/4095 × 3.3 = 2.43mV.

□ Continuous Error Detection Setting

To prevent false triggering of a fault event, continuous detection times to distinguish the error status can be set. The AK5734 detects error status when detecting an error for the number of times set by INT1-0 bits, and outputs to error status registers (11-15H) and the INT pin drives "L".

INT1 bit	INT0 bit	Error Detection Number	
0	0	Error determination is made by 1 times Detection	(default)
0	1	Error determination is made by 5 times Detection	
1	*	Error determination is made by 10 times Detection	

(*: Don't care)

Table 23: Number of Times for Continuous Error Detection

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□ Error Detection Sequence

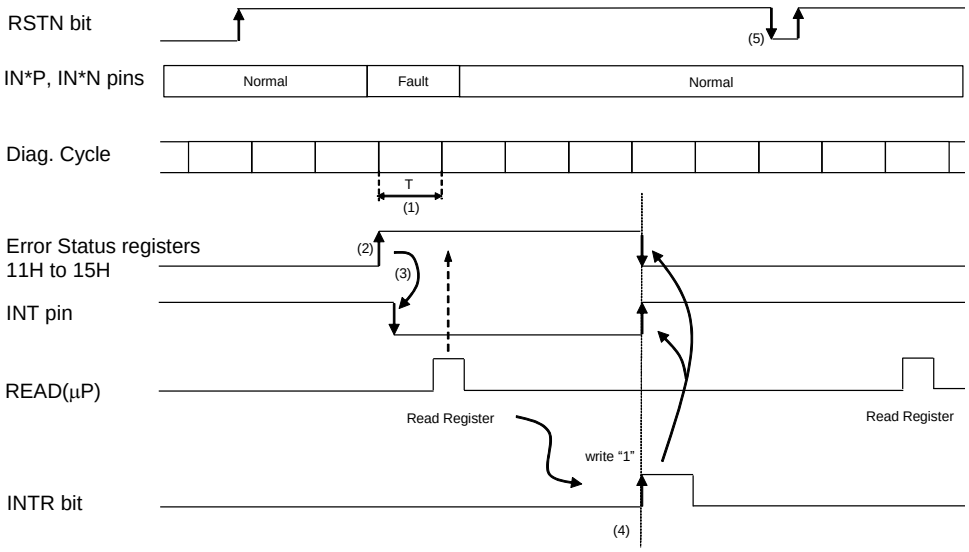

Figure 64: Error Detection Timing

(1) During the diagnostic cycle T, the AK5734 reads the DC level with the SAR ADC in the order of VBATM, MPWR, IN1P, IN1N, IN2P, IN2N ... IN4N and performs error diagnosis. The diagnostic cycle T depends on fs and CPCK1-0 bits (charge pump frequency).

	Diagnostic Cycle T [sec]			
fs	CPCK="00"	CPCK="11"	CPCK="01"	CPCK="10"
8kHz	12 × 1/fs	6 × 1/fs	6 × 1/fs	5 × 1/fs
12kHz	12 × 1/fs	6 × 1/fs	9 × 1/fs	6 × 1/fs
16kHz	23 × 1/fs	12 × 1/fs	12 × 1/fs	9 × 1/fs
24kHz	23 × 1/fs	12 × 1/fs	17 × 1/fs	12 × 1/fs
32kHz	23 × 1/fs	23 × 1/fs	23 × 1/fs	17 × 1/fs
44kHz	23 × 1/fs	23 × 1/fs	34 × 1/fs	23 × 1/fs
48kHz	23 × 1/fs	23 × 1/fs	34 × 1/fs	23 × 1/fs
72kHz	45 × 1/fs	45 × 1/fs	45 × 1/fs	34 × 1/fs
96kHz	45 × 1/fs	45 × 1/fs	67 × 1/fs	45 × 1/fs
144kHz	89 × 1/fs	89 × 1/fs	89 × 1/fs	67 × 1/fs
192kHz	89 × 1/fs	89 × 1/fs	134 × 1/fs	89 × 1/fs

Table 24. Diagnostic Cycle T

(2) The error status register becomes "1" if input pins, MIC bias, charge pump or over temperature errors are detected. Once the error status register becomes "1", it holds that status until it is reset by the INTR bit = "1". The 4-channel ADC is not reset by INTR bit = "1".
(3) An OR-ed result is output to the INT pin. The errors can be masked via MSHTV*, MSHTG*, MSHMB*, MSHTD* and MOPEN* (*=1-4) bits and masked error will not reflect to the error status registers.
(4) Status of the INT pin and error status registers are reset by setting INTR bit = "1" or RSTN bit = "0". Refer to Table 21 for details. When write "1" to the INTR bit, the INTR bit automatically return to "0" within one diagnostic cycle.
(5) If the internal circuit is automatically powered down due to error detection (Table 21), reset the AK5734 by setting RSTN bit = "0" or the PDN pin = "L".

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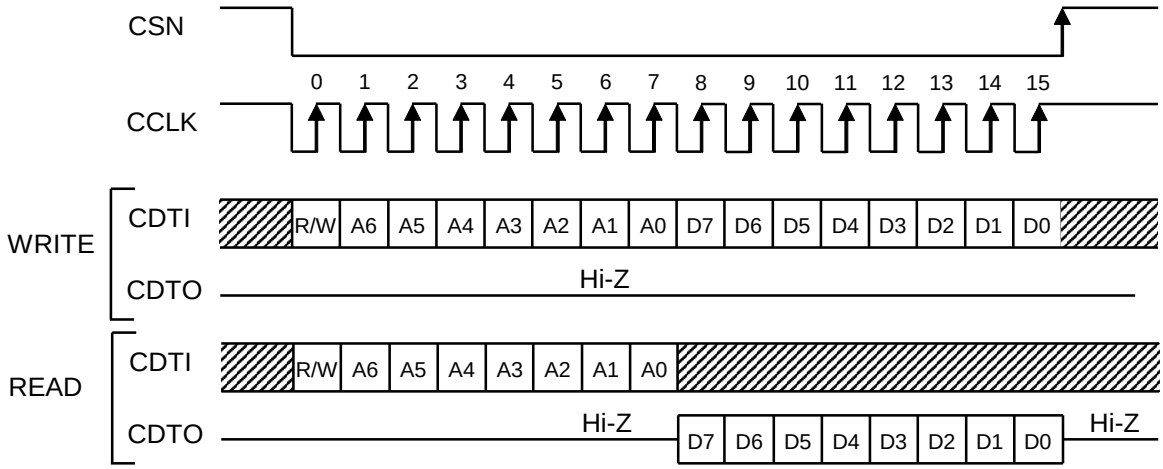
■ Register Control Interface

By using the SPI pin, it is possible to switch the operation mode between, “4-wire serial control mode, (SPI pin =’H’)”, and, “I2C Bus control mode, (SPI pin = ‘L’)”. The SPI pin state must not be changed while the AK5734 is in operation.

□ 4-wire Serial Control Mode, (SPI pin = “H”)

The internal registers may be either written or read from the 4-wire µP interface pins: CSN, CCLK, CDTI & CDTO. The data consists of Chip address, (1bit, C1 is fixed to “1”), Read/Write (1bit), Register address (MSB first, 7bits) and Control data (MSB first, 7bits). Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge. For write operations, data is written on a rising edge of CSN after the 16th rising edge of CCLK counting from a falling edge of CSN. For read operations, the CDTO output goes to high impedance state after a low-to-high transition of CSN. The maximum speed of CCLK is 5MHz. Setting the PDN pin= “L” resets the registers to their default values.
Data will not be written with a format other than 16 times CCLK while CSN is, “L”, such as 15 times CCLK or 17 times CCLK.
For read operations, data will be output after a rising edge of CSN if CCLK is not transitioned 16 times while CSN is “L”. The AK5734 outputs data until D1, (Figure 65), if the CCLK cycle is finished in 15 times and CSN rises.



R/W: READ/WRITE (0: READ, 1: WRITE)
A6-A0: Register Address
D7-D0: Control Data

Figure 65: 4-wire Serial Control I/F Timing

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□ I²C Bus Control Mode (SPI pin = "L")

The AK5734 supports the fast-mode I²C bus, (max: 400kHz).

WRITE Operation

Figure 66 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition, (Figure 72). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant five bits of the slave address are fixed as "00100". The next bits are CAD1 and CAD0, (device address bits). These bits identify the specific device on the bus. The hard-wired input pins, (CAD1/0 pins), set these device address bits, (Figure 67). If the slave address matches that of the AK5734, the AK5734 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line, (HIGH), during the acknowledge clock pulse, (Figure 73). R/W bit = "1" indicates that the read operation is to be executed. "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK5734. The format is MSB first, and those most significant 1-bit is fixed to zero, (Figure 68). The data after the second byte contains control data. The format is MSB first, 8bits, (Figure 69). The AK5734 generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition, (Figure 72).

The AK5734 can perform more than one byte write operation per sequence. After receipt of the third byte the AK5734 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet, the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds "4BH" prior to generating a stop condition, the address counter will "roll over" to "00H" and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW, (Figure 74), except for the START and STOP conditions.

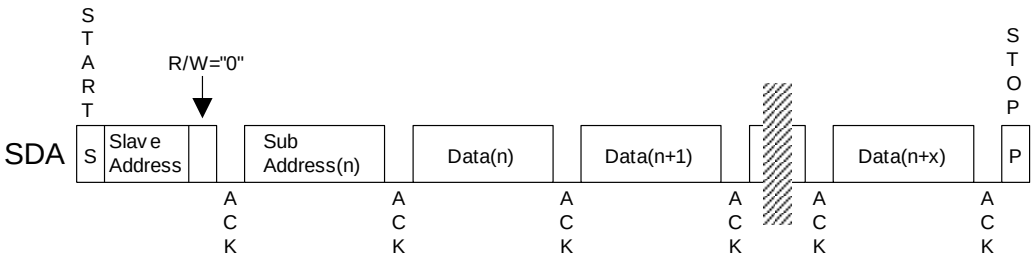

Figure 66: Data Transfer Sequence at the I²C Bus Mode

0	0	1	0	0	CAD1	CAD0	R/W

(CAD bits are set by the CAD pins)

Figure 67: The First Byte

0	A6	A5	A4	A3	A2	A1	A0

Figure 68: The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 69: Byte Structure after the Second Byte

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READ Operation

Set the R/W bit = “1” for the READ operation of the AK5734. After transmission of data, the master can read the next address’ data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet, the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds, “4BH”, prior to generating a stop condition, the address counter will “roll over” to “00H” and the data of 00H will be read out.

The AK5734 supports two basic read operations: Current Address Read and Random Address Read.

Current Address Read

The AK5734 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access, (either a read or write), was to address, “n”, the next CURRENT READ operation would access data from the address, “n+1”. After receipt of the slave address with R/W bit “1”, the AK5734 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK5734 ceases transmission.

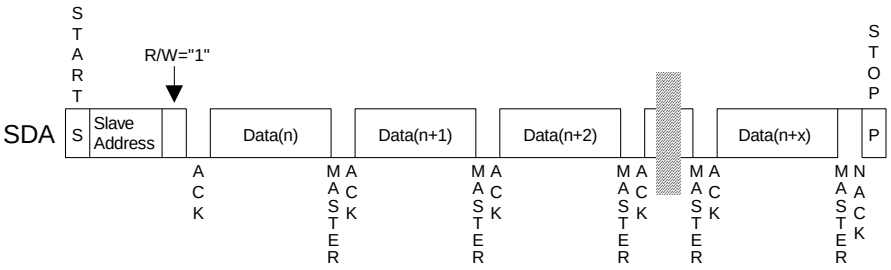

Figure 70. Current Address Read

Random Address Read

The random read operation allows the master to access any memory location at random. Prior to issuing a slave address with the R/W bit =“1”, the master must execute a “dummy” write operation first. The master issues a start request, a slave address, (R/W bit = “0”), and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit =“1”. The AK5734 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK5734 ceases transmission.

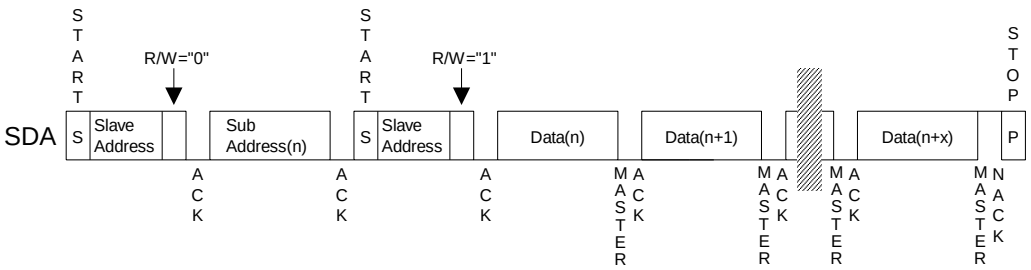

Figure 71: Random Address Read

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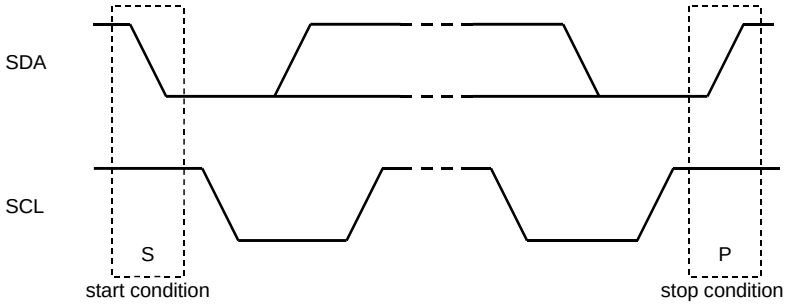

Figure 72: START and STOP Conditions

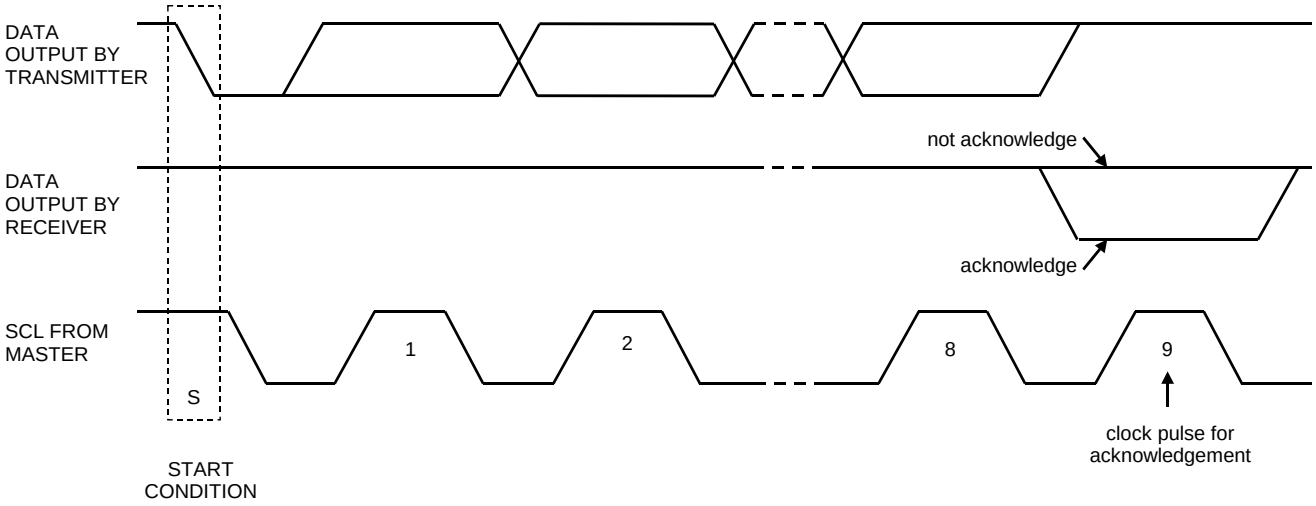

Figure 73: Acknowledge on the I²C-Bus

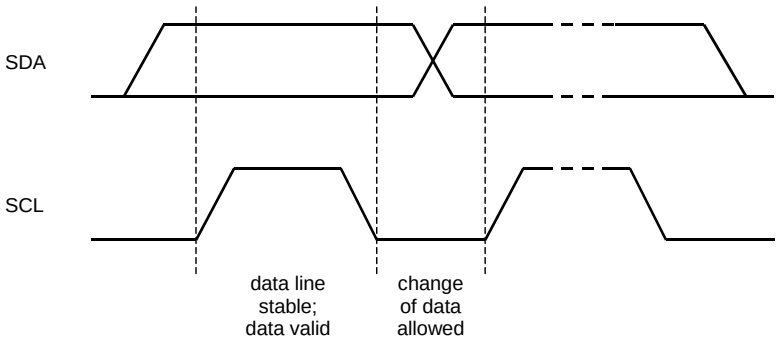

Figure 74: Bit Transfer on the I²C Bus

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■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
00H	Mic. PGA1	0	0	STD1	0	PG13	PG12	PG11	PG10	R/W	00H
01H	Mic. PGA2	0	0	STD2	0	PG23	PG22	PG21	PG20	R/W	00H
02H	Mic. PGA3	0	0	STD3	0	PG33	PG32	PG31	PG30	R/W	00H
03H	Mic. PGA4	0	0	STD4	0	PG43	PG42	PG41	PG40	R/W	00H
04H	Reserved	0	0	0	0	0	0	0	0	R/W	00H
05H	Reserved	0	0	0	0	0	0	0	0	R/W	00H
06H	General Setting 1	SLOW	SD	ATS1	ATS0	DIF	TDM1	TDM0	RSTN	R/W	00H
07H	General Setting 2	0	FS2	FS1	FS0	CKS2	CKS1	CKS0	SARTH	R/W	28H
08H	General Setting 3	MBS3	MBS2	MBS1	MBS0	0	0	REFSEL	ATTVB	R/W	00H
09H	Master Slave	0	MSN	0	0	CPCK1	CPCK0	0	0	R/W	00H
0AH	General Setting 4	OSR	SLOT	FS12K	0	VOICE	0	0	INTR	R/W	20H
0BH	ADC1 Digital Volume Control	ATT17	ATT16	ATT15	ATT14	ATT13	ATT12	ATT11	ATT10	R/W	34H
0CH	ADC2 Digital Volume Control	ATT27	ATT26	ATT25	ATT24	ATT23	ATT22	ATT21	ATT20	R/W	34H
0DH	ADC3 Digital Volume Control	ATT37	ATT36	ATT35	ATT34	ATT33	ATT32	ATT31	ATT30	R/W	34H
0EH	ADC4 Digital Volume Control	ATT47	ATT46	ATT45	ATT44	ATT43	ATT42	ATT41	ATT40	R/W	34H
0FH	Reserved	0	0	0	0	0	0	0	0	R/W	00H
10H	Reserved	0	0	0	0	0	0	0	0	R/W	00H
11H	Monitor Summary	0	0	0	0	ADC4	ADC3	ADC2	ADC1	R	00H
12H	Monitor ADC1	0	OVDET	OIDET	SHTV1	SHMB1	SHTG1	SHTD1	OPEN1	R	00H
13H	Monitor ADC2	OVTPCM	OVTP	OVCP	SHTV2	SHMB2	SHTG2	SHTD2	OPEN2	R	00H
14H	Monitor ADC3	0	0	0	SHTV3	SHMB3	SHTG3	SHTD3	OPEN3	R	00H
15H	Monitor ADC4	0	0	0	SHTV4	SHMB4	SHTG4	SHTD4	OPEN4	R	00H
16H	Reserved	0	0	0	0	0	0	0	0	R	00H
17H	Reserved	0	0	0	0	0	0	0	0	R	00H
18H	Mask ADC1	DETST	INT1	INT0	MSHTV1	MSHMB1	MSHTG1	MSHTD1	MOPEN1	R/W	00H
19H	Mask ADC2	0	0	0	MSHTV2	MSHMB2	MSHTG2	MSHTD2	MOPEN2	R/W	00H
1AH	Mask ADC3	0	0	0	MSHTV3	MSHMB3	MSHTG3	MSHTD3	MOPEN3	R/W	00H
1BH	Mask ADC4	0	0	0	MSHTV4	MSHMB4	MSHTG4	MSHTD4	MOPEN4	R/W	00H
1CH	Reserved	0	0	0	0	0	0	0	0	R/W	00H
1DH	Reserved	0	0	0	0	0	0	0	0	R/W	00H

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Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
1EH	Input Mode Select	0	0	0	0	AC4	AC3	AC2	AC1	R/W	00H
1FH	SAR Threshold setting OPEN	0	0	0	0	TOP3	TOP2	TOP1	TOP0	R/W	02H
20H	SAR Threshold setting SHTD	0	0	0	0	TSD3	TSD2	TSD1	TSD0	R/W	02H
21H	SAR Threshold setting SHTG	0	0	0	0	TSG3	TSG2	TSG1	TSG0	R/W	02H
22H	SAR Threshold setting SHMB	0	0	0	0	TSB3	TSB2	TSB1	TSB0	R/W	02H
23H	SAR Threshold setting SHTV	0	0	0	0	TSV3	TSV2	TSV1	TSV0	R/W	02H
24H	SAR OPEN Threshold High byte	THOP12	THOP11	THOP10	THOP09	THOP08	THOP07	THOP06	THOP05	R/W	06H
25H	SAR OPEN Threshold Low byte	THOP04	THOP03	THOP02	THOP01	0	0	0	0	R/W	F0H
26H	SAR P/N SHORT Threshold High byte	THSD12	THSD11	THSD10	THSD09	THSD08	THSD07	THSD06	THSD05	R/W	06H
27H	SAR P/N SHORT Threshold Low byte	THSD04	THSD03	THSD02	THSD01	0	0	0	0	R/W	F0H
28H	SAR GND SHORT Threshold High byte	THSG12	THSG11	THSG10	THSG09	THSG08	THSG07	THSG06	THSG05	R/W	06H
29H	SAR GND SHORT Threshold Low byte	THSG04	THSG03	THSG02	THSG01	0	0	0	0	R/W	F0H
2AH	SAR VBAT SHORT Threshold High byte	THSV12	THSV11	THSV10	THSV09	THSV08	THSV07	THSV06	THSV05	R/W	06H
2BH	SAR VBAT SHORT Threshold Low byte	THSV04	THSV03	THSV02	THSV01	0	0	0	0	R/W	F0H
2CH	SAR VBIAS SHORT Threshold High byte	THSM12	THSM11	THSM10	THSM09	THSM08	THSM07	THSM06	THSM05	R/W	06H
2DH	SAR VBIAS SHORT Threshold Low byte	THSM04	THSM03	THSM02	THSM01	0	0	0	0	R/W	F0H
2EH	Error State Select	ERRPDSEL	0	0	0	0	0	0	0	R/W	00H
2FH	OVTP setting	OVTPCNT	OVTPSEL	0	0	0	0	0	0	R/W	00H
30H	SAR IN1+ High byte	A1P12	A1P11	A1P10	A1P09	A1P08	A1P07	A1P06	A1P05	R	00H
31H	SAR IN1+ Low byte	A1P04	A1P03	A1P02	A1P01	0	0	0	0	R	00H
32H	SAR IN1- High byte	A1N12	A1N11	A1N10	A1N09	A1N08	A1N07	A1N06	A1N05	R	00H
33H	SAR IN1- Low byte	A1N04	A1N03	A1N02	A1N01	0	0	0	0	R	00H
34H	SAR IN2+ High byte	A2P12	A2P11	A2P10	A2P09	A2P08	A2P07	A2P06	A2P05	R	00H
35H	SAR IN2+ Low byte	A2P04	A2P03	A2P02	A2P01	0	0	0	0	R	00H
36H	SAR IN2- High byte	A2N12	A2N11	A2N10	A2N09	A2N08	A2N07	A2N06	A2N05	R	00H
37H	SAR IN2- Low byte	A2N04	A2N03	A2N02	A2N01	0	0	0	0	R	00H
38H	SAR IN3+ High byte	A3P12	A3P11	A3P10	A3P09	A3P08	A3P07	A3P06	A3P05	R	00H
39H	SAR IN3+ Low byte	A3P04	A3P03	A3P02	A3P01	0	0	0	0	R	00H
3AH	SAR IN3- High byte	A3N12	1N11	A3N10	A3N09	A3N08	A3N07	A3N06	A3N05	R	00H
3BH	SAR IN3- Low byte	A3N04	A3N03	A3N02	A3N01	0	0	0	0	R	00H

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Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
3CH	SAR IN4+ High byte	A4P12	A4P11	A4P10	A4P09	A4P08	A4P07	A4P06	A4P05	R	00H
3DH	SAR IN4+ Low byte	A4P04	A4P03	A4P02	A4P01	0	0	0	0	R	00H
3EH	SAR IN4- High byte	A4N12	A4N11	A4N10	A4N09	A4N08	A4N07	A4N06	A4N05	R	00H
3FH	SAR IN4- Low byte	A4N04	A4N03	A4N02	A4N01	0	0	0	0	R	00H
40H	Reserved	0	0	0	0	0	0	0	0	R	00H
41H	Reserved	0	0	0	0	0	0	0	0	R	00H
42H	Reserved	0	0	0	0	0	0	0	0	R	00H
43H	Reserved	0	0	0	0	0	0	0	0	R	00H
44H	Reserved	0	0	0	0	0	0	0	0	R	00H
45H	Reserved	0	0	0	0	0	0	0	0	R	00H
46H	Reserved	0	0	0	0	0	0	0	0	R	00H
47H	Reserved	0	0	0	0	0	0	0	0	R	00H
48H	SAR VBAT High byte	VBAT12	VBAT11	VBAT10	VBAT09	VBAT08	VBAT07	VBAT06	VBAT05	R	00H
49H	SAR VBAT Low byte	VBAT04	VBAT03	VBAT02	VBAT01	0	0	0	0	R	00H
4AH	SAR VBIAS High byte	VBIAS12	VBAIS11	VBIAS10	VBIAS09	VBIAS08	VBIAS07	VBIAS06	VBIAS05	R	00H
4BH	SAR VBIAS Low byte	VBIAS04	VBIAS03	VBIAS02	VBIAS01	0	0	0	0	R	00H
5AH	Test	0	0	0	0	0	0	0	0	R/W	00H
5BH	Test	0	0	0	0	0	0	0	0	R/W	00H
5CH	Test	0	0	0	0	0	0	0	0	R/W	00H
5DH	Test	0	0	0	0	0	0	0	0	R/W	00H
5EH	Power down control	PDMPN	1	1	1	1	1	1	1	R/W	FFH
5FH	Test	1	1	1	1	1	1	1	1	R/W	FFH

Note:
- Do not write to the registers called, “Test”, and” or to any addresses after beyond “5FH”. Leave them to at the default setting. Malfunctions may occur by writing “0” to these bits.
- Auto increment function is functional until the address “4BH”, so the address counter will be set to “00H” after accessing “4BH”. Therefore, the address “5EH” must be accessed explicitly.
- Bits indicated as 0 in each address must contain a “0” value. Malfunctions may occur by writing “1” to those bits. Bits indicated as 1 in each address must contain a “1” value. Malfunctions May occur by writing, “0”, to those bits.
- When the PDN pin is pulled “L” all registers are initialized to their default values.
- When RSTN bit is set to “0” the internal timing is reset, but registers are not initialized to their default values.

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■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Mic. PGA1	0	0	STD1	0	PG13	PG12	PG11	PG10
01H	Mic. PGA2	0	0	STD2	0	PG23	PG22	PG21	PG20
02H	Mic. PGA3	0	0	STD3	0	PG33	PG32	PG31	PG30
03H	Mic. PGA4	0	0	STD4	0	PG43	PG42	PG41	PG40
04H	Reserved	0	0	0	0	0	0	0	0
05H	Reserved	0	0	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

STD*: Input Select (single–ended or differential)
0: Differential (default)
1: Single–ended

PGA*3-*0: Microphone Pre-Gain Amplifier Gain Setting, (Table 17)
Default value is “0000b” (0dB).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	General Setting 1	SLOW	SD	ATS1	ATS0	DIF	TDM1	TDM0	RSTN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SLOW: Slow Roll-off Filter Enable (Table 12)
0: Sharp roll-off filter (default)
1: Slow roll-off filter

SD: Short delay Filter Enable (Table 12)
0: Sharp roll-off filter (default)
1: Short delay filter

ATS1-0: Digital attenuator transition time setting (Table 14)
Default value is “00”.

DIF: Audio Data Interface Mode Select (Table 11)
0: IIS (default)
1: Left Justified

TDM: TDM Mode Select (Table 11)
00: Normal mode (default)
01: TDM128 mode
10: TDM256 mode
11: TDM512 mode

RSTN: Internal Timing Reset
0: Reset (default)
Internal clock timings are reset, but all other registers are not reset to their default value and R/W access is still allowed.
1: Normal Operation

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Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	General Setting 2	0	FS2	FS1	FS0	CKS2	CKS1	CKS0	SARTH
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	0	1	0	0	0

SARTH: Diagnosis Accuracy Select
0: Simple (9 steps) (default)
1: High Accuracy (12bit code)

CKS2-0: Master Clock Frequency Setting (Table2)
Default value is “100b” (512fs).

FS2-0: Sampling Rate Setting (Table 3)
Default value is “010b” (24kHz < fs ≤ 48kHz).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	General Setting 3	MBS3	MBS2	MBS1	MBS0	0	0	REFSEL	ATTVB
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ATTVB: VBATM pin Attenuation (Note 22)
0: 10% Attenuation (default)
1: 30% Attenuation

REFSEL: Criteria Setting

0: Using MIC bias voltage for OPEN*, SHMB*, SHTV* error detection (default)

Error Name	Fault Conditions	Conditions
OPEN*	Positive and Negative Input Open	MPWR - Vth ≤ IN*P ≤ MPWR + Vth and IN*N ≤ Vth
SHMB*	Short to MIC Bias Voltage	IN*P/N ≥ MPWR - Vth
SHTV*	Short to Battery	IN*P/N ≥ MPWR + Vth

1: Using VBATM for OPEN*, SHMB*, SHTV* error detection

Error Name	Fault Conditions	Conditions
OPEN*	Positive and Negative Input Open	VBATM - Vth ≤ IN*P ≤ VBATM + Vth and IN*N ≤ Vth
SHMB*	Short to MIC Bias Voltage	IN*P/N ≥ VBATM - Vth
SHTV*	Short to Battery	IN*P/N ≥ VBATM + Vth

MBS3-0: MIC Bias Voltage Setting (Table 18)
Default value is “0000b” (5V).

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Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Master Slave	0	MSN	0	0	CPCK1	CPCK0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

MSN: Master & Slave Mode Select (Table 1)
0: Slave Mode (default)
1: Master Mode

CPCK1-0: Charge Pump CLK Frequency select (Table 4)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	General Setting	OSR	SLOT	FS12K	0	VOICE	0	0	INTR
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	0	0	0	0	0

OSR: Reducing Noise around 1MHz when 8kHz ≤ fs ≤ 24kHz.
0: Disable (default)
1: Enable
*When fs > 24kHz, noise around 1MHz is reduced regardless of the setting.

SLOT: Data SLOT Length Select
0: 32BICK (default)
1: 16BICK

FS12K: Sampling Rate setting
0: fs=8kHz, 16kHz, 32kHz, 72kHz, 144kHz
1: fs=12kHz, 24kHz, 44.1kHz, 48kHz, 96kHz, 192kHz

VOICE: Voice Filter Select (Table 12)
0: Depend on SLOW and SD bits (default)
1: Voice Filter

INTR: INT pin Reset
0: Normal Operation (default)
1: Reset Error Status Registers (11-15H) and INT pin

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	ADC1 Digital Volume Control	ATT17	ATT16	ATT15	ATT14	ATT13	ATT12	ATT11	ATT10
0CH	ADC2 Digital Volume Control	ATT27	ATT26	ATT25	ATT24	ATT23	ATT22	ATT21	ATT20
0DH	ADC3 Digital Volume Control	ATT37	ATT36	ATT35	ATT34	ATT33	ATT32	ATT31	ATT30
0EH	ADC4 Digital Volume Control	ATT47	ATT46	ATT45	ATT44	ATT43	ATT42	ATT41	ATT40
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	1	0	1	0	0

ATT*7-0: Digital Volume Setting (Table 13)
Default value is “00110100b” (0dB).

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Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0FH	Reserved	0	0	0	0	0	0	0	0
10H	Reserved	0	0	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
11H	Monitor Summary	0	0	0	0	ADC4	ADC3	ADC2	ADC1
R/W		R	R	R	R	R	R	R	R
Default		0	0	0	0	0	0	0	0

ADC4-1: Error Status for each ADC
0: No Error Detected. (default)
1: Error Detected.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
12H	Monitor ADC1	0	OVDET	OIDET	SHTV1	SHMB1	SHTG1	SHTD1	OPEN1
13H	Monitor ADC2	OVTPCM	OVTP	OVCP	SHTV2	SHMB2	SHTG2	SHTD2	OPEN2
14H	Monitor ADC3	0	0	0	SHTV3	SHMB3	SHTG3	SHTD3	OPEN3
15H	Monitor ADC4	0	0	0	SHTV4	SHMB4	SHTG4	SHTD4	OPEN4
16H	Reserved	0	0	0	0	0	0	0	0
17H	Reserved	0	0	0	0	0	0	0	0
R/W		R	R	R	R	R	R	R	R
Default		0	0	0	0	0	0	0	0

OVDET, OIDET, OVTP, OVCP, SHTV1-4, SHMB1-4, SHTG1-4, SHTD1-4, OPEN1-4: Error Status
0: No Error Detected (default)
1: Error Detected.

OVTPCM: OVTP Automatic Recovery Count Monitor
0: Less than the Upper Limit (default)
1: Reaches Upper Limit

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
18H	Mask ADC1	DETST	INT1	INT0	MSHTV1	MSHMB1	MSHTG1	MSHTD1	MOPEN1
19H	Mask ADC2	0	0	0	MSHTV2	MSHMB2	MSHTG2	MSHTD2	MOPEN2
1AH	Mask ADC3	0	0	0	MSHTV3	MSHMB3	MSHTG3	MSHTD3	MOPEN3
1BH	Mask ADC4	0	0	0	MSHTV4	MSHMB4	MSHTG4	MSHTD4	MOPEN4
1CH	Reserved	0	0	0	0	0	0	0	0
1DH	Reserved	0	0	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

MSHTV1-4, MSHMB1-4, MSHTG1-4, MSHTD1-4, MOPEN1-4: Error Status Bit Mask
0: No Mask (default)
1: Mask Error Status Bit

INT1-0: Number of Consecutive Error Detections that Determine Error Occurred (Table 23)

DETST: Diagnostic Circuit Operation after Error Detection
0: Diagnostic circuit and SAR ADC keep operation. (default)
1: Diagnostic circuit and SAR ADC stop operation.

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Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1EH	Input Mode Select	0	0	0	0	AC4	AC3	AC2	AC1
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

AC4-1: Analog Input Mode (AC or DC Connection) Select
0: DC Connection Mode (default)
1: AC Connection Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1FH	Threshold setting OPEN	0	0	0	0	TOP3	TOP2	TOP1	TOP0
20H	Threshold setting SHTD	0	0	0	0	TSD3	TSD2	TSD1	TSD0
21H	Threshold setting SHTG	0	0	0	0	TSG3	TSG2	TSG1	TSG0
22H	Threshold setting SHMB	0	0	0	0	TSB3	TSB2	TSB1	TSB0
23H	Threshold setting SHTV	0	0	0	0	TSV3	TSV2	TSV1	TSV0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	0

TOP3-0, TSD3-0, TSG3-0, TSB3-0, TSV3-0: Simple Error Detection Threshold Setting (Table 22)
Default value is “0010b” (300mV).
This setting is valid when SARTH bit = “0”. Nine values of threshold voltage can be selected.
The threshold setting is applied to all channels.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
24H	OPEN Threshold High byte	THOP12	THOP11	THOP10	THOP09	THOP08	THOP07	THOP06	THOP05
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	1	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
25H	OPEN Threshold Low byte	THOP04	THOP03	THOP02	THOP01	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	0	0	0	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
26H	P/N SHORT Threshold High byte	THSD12	THSD11	THSD10	THSD09	THSD08	THSD07	THSD06	THSD05
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	1	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
27H	P/N SHORT Threshold Low byte	THSD04	THSD03	THSD02	THSD01	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	0	0	0	0

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Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
28H	GND SHORT Threshold High byte	THSG12	THSG11	THSG10	THSG09	THSG08	THSG07	THSG06	THSG05
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	1	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
29H	GND SHORT Threshold Low byte	THSG04	THSG03	THSG02	THSG01	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	0	0	0	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2AH	VBAT SHORT Threshold High byte	THSV12	THSV11	THSV10	THSV09	THSV08	THSV07	THSV06	THSV05
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	1	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2BH	VBAT SHORT Threshold Low byte	THSV04	THSV03	THSV02	THSV01	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	0	0	0	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2CH	VBIAS SHORT Threshold High byte	THSM12	THSM11	THSM10	THSM09	THSM08	THSM07	THSM06	THSM05
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	1	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2DH	VBIAS SHORT Threshold Low byte	THSM04	THSM03	THSM02	THSM01	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	0	0	0	0

THOP12-01, THSD12-01, THSG12-01, THSV12-01, THSM12-01: High Accuracy Error Detection Threshold Setting

Default value of high byte is “00000110b”
Default value of low byte is “11110000b”
This setting is valid when SARTH bit = “1”. Threshold voltage of the diagnostic circuit can be set by the 12-bit straight binary code with AVDD full scale. The threshold setting is applied to all channels.

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Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2EH	Error State Select	ERRPDSEL	0	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ERRPDSEL: Error State Select (Table 21)

Error state of internal circuits (Note 44)when MIC bias overvoltage, MIC bias overcurrent or charge pump under voltage is detected can be selected.

0: Active (default)
1: Power down

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2FH	OVTP Setting	OVTPCNT	OVTPSEL	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

OVTPSEL: Type of Over Temperature detection

0: Latch type
1: Automatic return type

OVTPCNT: Limit Count of Automatic Recovering

0: 3 times
1: 7 times

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Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30H	SAR IN1P High byte	A1P12	A1P11	A1P10	A1P09	A1P08	A1P07	A1P06	A1P05
31H	SAR IN1P Low byte	A1P04	A1P03	A1P02	A1P01	0	0	0	0
32H	SAR IN1N High byte	A1N12	A1N11	A1N10	A1N09	A1N08	A1N07	A1N06	A1N05
33H	SAR IN1N Low byte	A1N04	A1N03	A1N02	A1N01	0	0	0	0
34H	SAR IN2P High byte	A2P12	A2P11	A2P10	A2P09	A2P08	A2P07	A2P06	A2P05
35H	SAR IN2P Low byte	A2P04	A2P03	A2P02	A2P01	0	0	0	0
36H	SAR IN2N High byte	A2N12	A2N11	A2N10	A2N09	A2N08	A2N07	A2N06	A2N05
37H	SAR IN2N Low byte	A2N04	A2N03	A2N02	A2N01	0	0	0	0
38H	SAR IN3P High byte	A3P12	A3P11	A3P10	A3P09	A3P08	A3P07	A3P06	A3P05
39H	SAR IN3P Low byte	A3P04	A3P03	A3P02	A3P01	0	0	0	0
3AH	SAR IN3N High byte	A3N12	A3N11	A3N10	A3N09	A3N08	A3N07	A3N06	A3N05
3BH	SAR IN3N Low byte	A3N04	A3N03	A3N02	A3N01	0	0	0	0
3CH	SAR IN4P High byte	A4P12	A4P11	A4P10	A4P09	A4P08	A4P07	A4P06	A4P05
3DH	SAR IN4P Low byte	A4P04	A4P03	A4P02	A4P01	0	0	0	0
3EH	SAR IN4N High byte	A4N12	A4N11	A4N10	A4N09	A4N08	A4N07	A4N06	A4N05
3FH	SAR IN4N Low byte	A4N04	A5N03	A4N02	A4N01	0	0	0	0
40H	Reserved	0	0	0	0	0	0	0	0
41H	Reserved	0	0	0	0	0	0	0	0
42H	Reserved	0	0	0	0	0	0	0	0
43H	Reserved	0	0	0	0	0	0	0	0
44H	Reserved	0	0	0	0	0	0	0	0
45H	Reserved	0	0	0	0	0	0	0	0
46H	Reserved	0	0	0	0	0	0	0	0
47H	Reserved	0	0	0	0	0	0	0	0
48H	SAR VBAT High byte	VBAT12	VBAT11	VBAT10	VBAT09	VBAT08	VBAT07	VBAT06	VBAT05
49H	SAR VBAT Low byte	VBAT04	VBAT03	VBAT02	VBAT01	0	0	0	0
4AH	SAR VBIAS High byte	VBIAS12	VBAIS11	VBIAS10	VBIAS09	VBIAS08	VBIAS07	VBIAS06	VBIAS05
4BH	SAR VBIAS Low byte	VBIAS04	VBIAS03	VBIAS02	VBIAS01	0	0	0	0
R/W		R	R	R	R	R	R	R	R
Default		0	0	0	0	0	0	0	0

A*P12-01 (*=1-4), A*N12-01, VBAT12-01, VBIAS12-01: SAR Raw Data Read

Default value is, “00000000b”.

Read out Low bytes before High bytes when reading the addresses above. To prevent data mismatch of Low byte and High byte, the AK5734 High byte and Low byte will not be updated once High byte is read until reading other addresses. Therefore, addresses from 30H to 4BH should be read continuously. Do not stop the data read; there is a possibility of data mismatch of High and Low bytes, or the data might not be updated.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
5EH	Power Down Control	PDMPN	1	1	1	1	1	1	1
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	1	1	1	1

PDMPN: MIC Bias Circut Power Down

0: Power down

1: Power up (default)

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13. Recommended External Circuits

Figure 75 shows recommended external connection. An evaluation board (AKD5734) is available for fast evaluation as well as suggestions for peripheral circuitry.

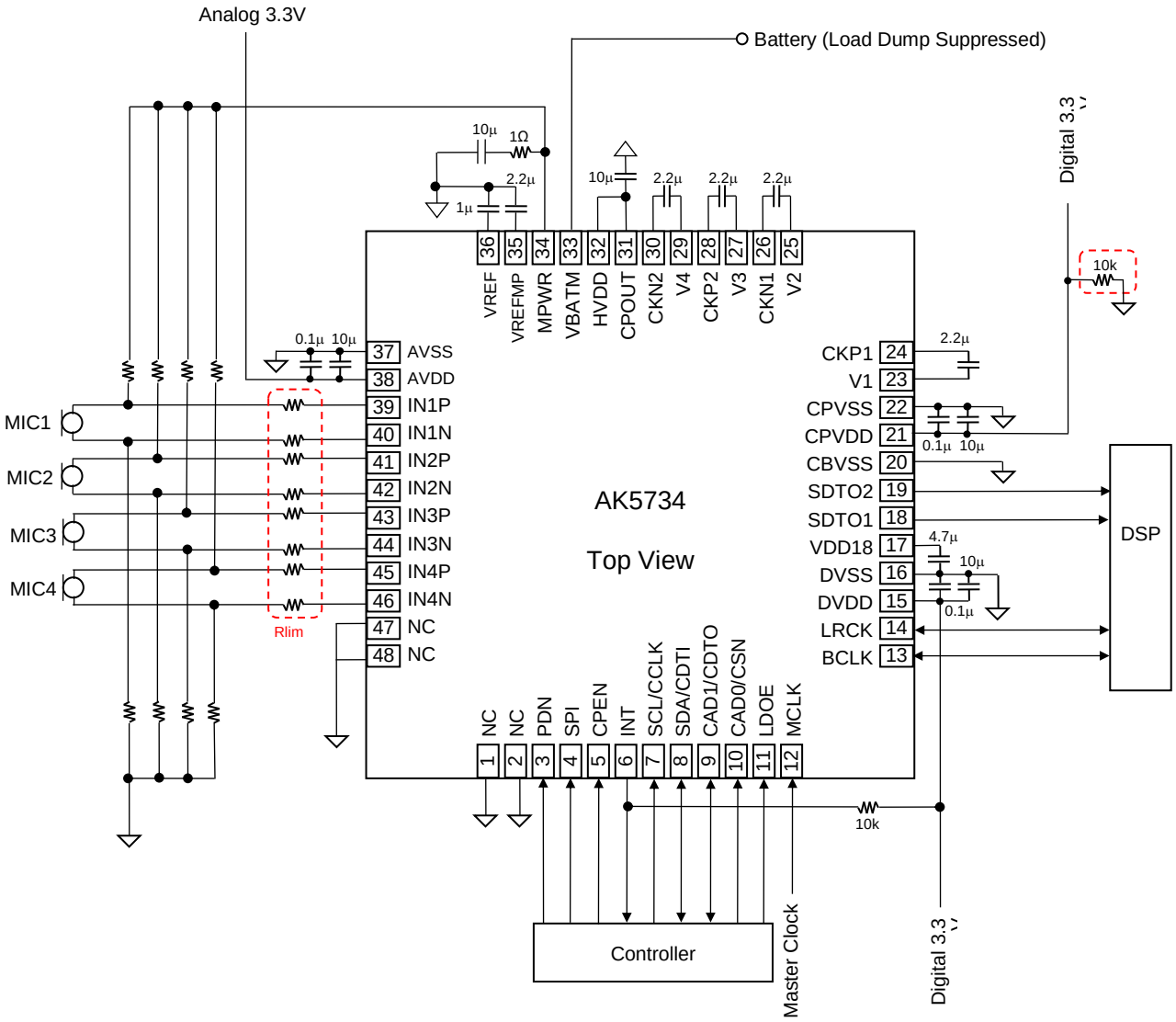

Figure 75: Typical Connection Diagram

The resistors surrounded by the dotted line are protection resistors, intended to address a potential short between the battery and the analog input pins. These resistors are not necessary when a battery short is not expected.

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■ Analog Input Pin Protection Resistor

If a battery short at the INxP / N pin input is expected, insert a protection resistor R_{lim} between the signal input terminal and the INxP / N pins.

Battery short is not assumed

When the voltage applied to INxP / N pins is up to 10.1V, no protection resistor is required.

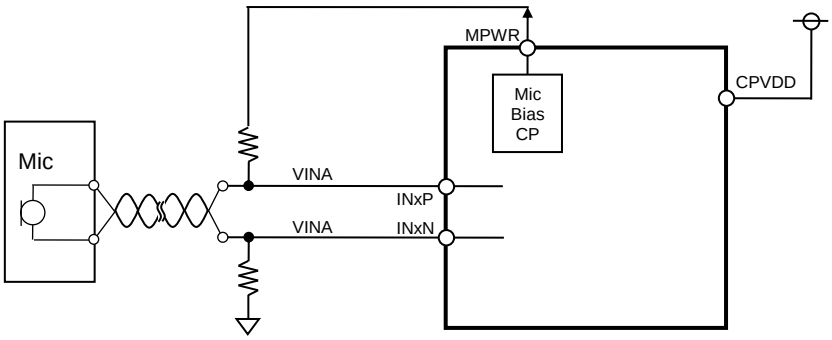

Figure 76. No Battery Short

Battery short is assumed

Insert a protection resistor R_{lim} between the signal input terminal and INxP / N pins. The voltage VINR that can be applied to the input terminal is up to 18V.

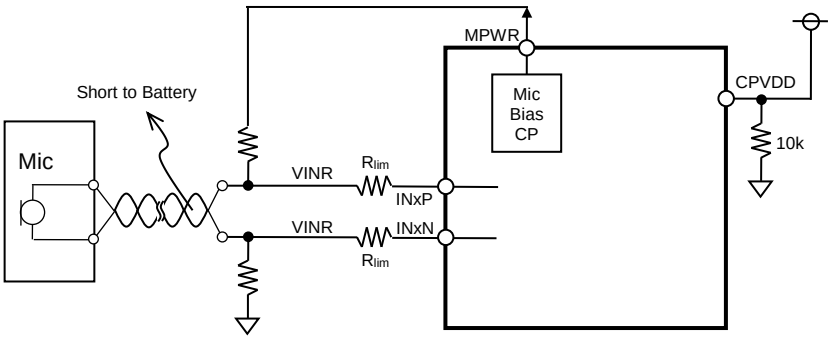

Figure 77. Battery Short using Built-in Microphone Bias

When the internal mic. bias circuit is not used, the voltage VINR is up to 48V.

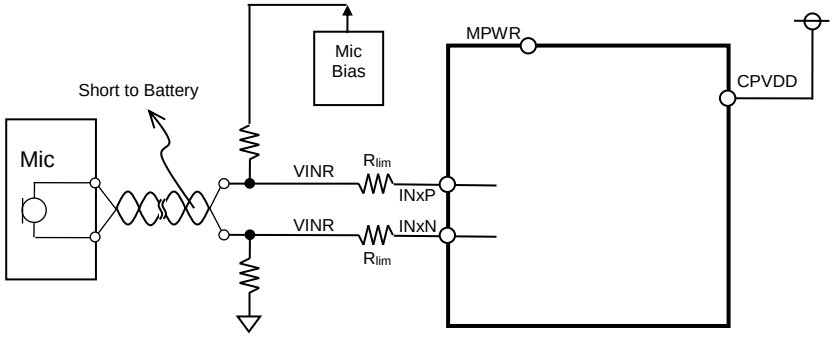

Figure 78. Battery Short using Built-in Microphone Bias

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Choose protection resistor

The recommended resistance value of the protection resistor Rlim and the required rated power are shown in the table below. Use resistors with a tolerance of 10% or less.

R_{lim}	Short Voltage			
	18V	30V	42V	48V
220Ω	≥ 0.25W	-	-	-
270Ω	≥ 0.2W	-	-	-
330Ω	≥ 0.2W	-	-	-
390Ω	≥ 0.125W	-	-	-
470Ω	≥ 0.125W	-	-	-
560Ω	≥ 0.1W	-	-	-
680Ω	≥ 0.1W	≥ 1W	-	-
820Ω	≥ 0.063W	≥ 1W	-	-
1000Ω	≥ 0.05W	≥ 0.5W	-	-
1200Ω	≥ 0.05W	≥ 0.5W	≥ 1.5W	-
1500Ω	≥ 0.05W	≥ 0.5W	≥ 1W	≥ 1.5W

-: Not Available

Table 25. Rated Power of Protection Resistor

■ Internal circuit protection resistor

If a battery short at the INxP / N pin input is expected, pull down the CPVDD pin with a resistor of 10k□ or less.

If the INxP / N pin input is shorted to the battery while the CPVDD power is off, the voltage from the battery is applied to the internal circuitry (which has a low tolerance for high voltages) through the internal path from the MPWR pin. This may damage the internal circuitry. By pulling down the CPVDD pin with 10k□ or less, destruction can be prevented. If the internal mic bias circuit (MPWR pin) is not used, the CPVDD pin pull-down resistor is not required, even if a battery short is expected.

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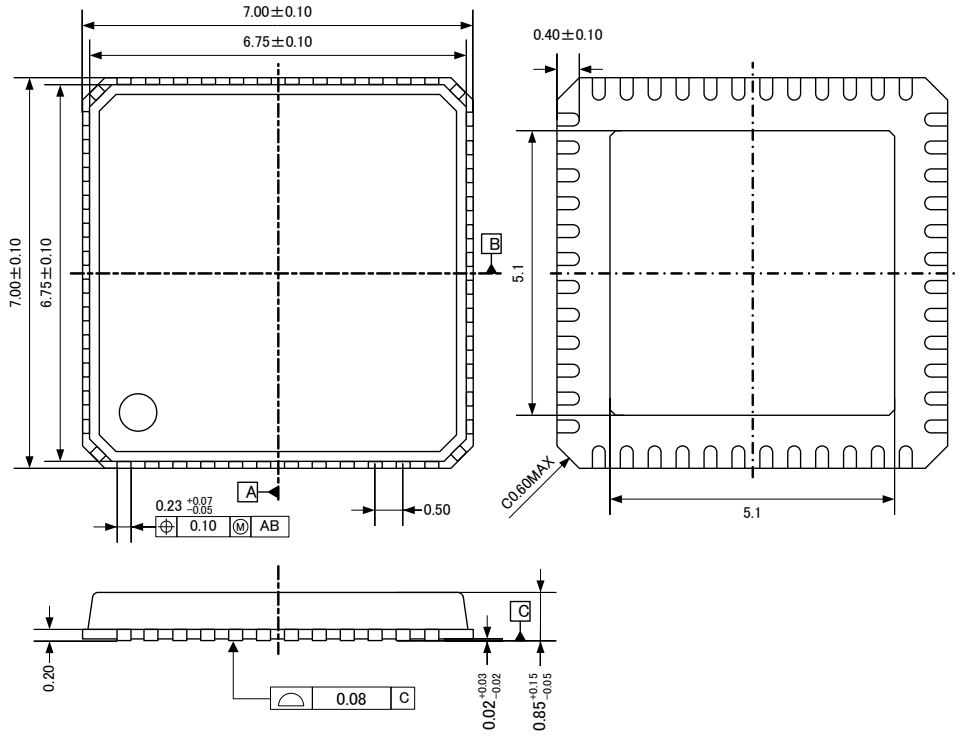
14. Package

■ Outline Dimensions

48-pin QFN (Unit: mm)



■ Material & Lead Finish

Package Molding Compound: Epoxy Resin
Lead Frame Material: Cu
Pin Surface Treatment: Solder, (Pb free), Plate

■ Marking

1) Pin #1 indication
2) Date Code: XXXXXXX (7 digits)
3) Marketing Code: AK5734VN
4) AKM Logo

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15. Ordering Guide

AK5734VN	−40 - 105°C	48-pin QFN
AKD5734	Evaluation Board for AK5734	

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16. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
20/02/12	00	First Edition		

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