

74LVT02

3.3 V Quad 2-input NOR gate

Rev. 5 — 18 April 2024

Product data sheet

1. General description

The 74LVT02 is a quad 2-input NOR gate. This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

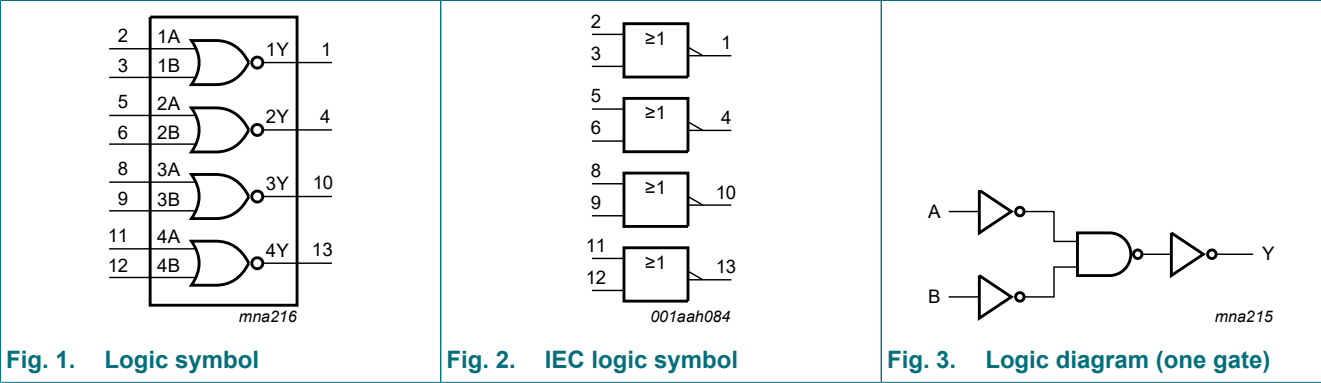
- Wide supply voltage range from 2.7 V to 3.6 V
- Output capability: +64 mA and -32 mA
- Direct interface with TTL levels
- Overvoltage tolerant inputs to 5.5 V
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 500 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to 85 °C

3. Ordering information

Table 1. Ordering information

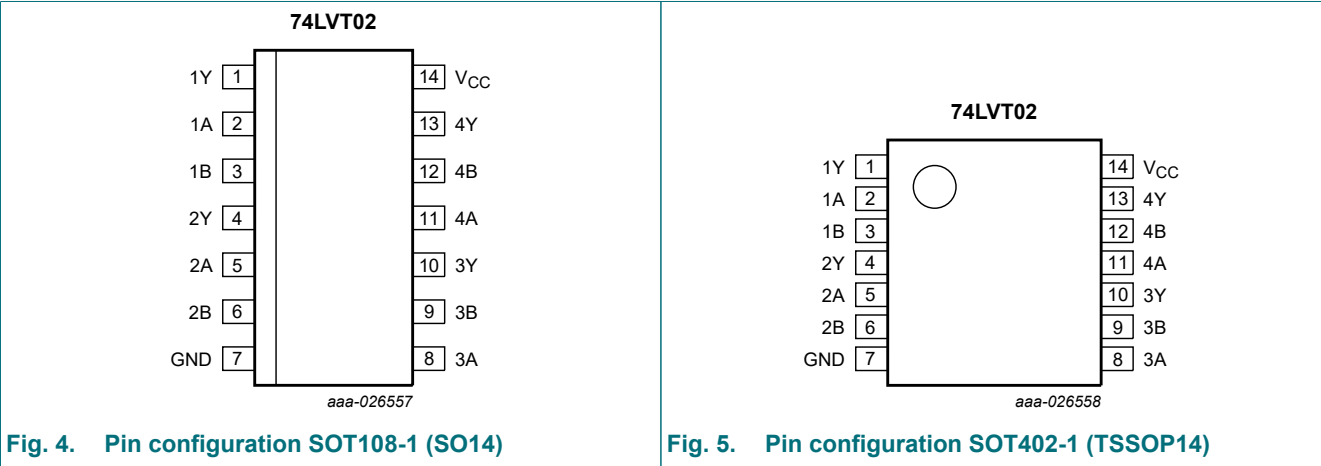
Type number	Package			
	Temperature range	Name	Description	Version
74LVT02D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVT02PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1Y, 2Y, 3Y, 4Y	1, 4, 10, 13	data output
1A, 2A, 3A, 4A	2, 5, 8, 11	data input
1B, 2B, 3B, 4B	3, 6, 9, 12	data input
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level

Input		Output
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage	[1]	-0.5	+7.0	V
V _O	output voltage	output in OFF-state or HIGH-state [1]	-0.5	+7.0	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
I _O	output current	output in LOW-state	-	64	mA
		output in HIGH-state	-32	-	mA
T _{stg}	storage temperature		-65	+150	°C
T _j	junction temperature	[2]	-	150	°C
P _{tot}	total power dissipation	T _{amb} = -40 to +85 °C [3]	-	500	mW

- [1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
- [2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.
- [3] For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		2.7	-	3.6	V
V _I	input voltage		0	-	5.5	V
I _{OH}	HIGH-level output current		-20	-	-	mA
I _{OL}	LOW-level output current		-	-	32	mA
T _{amb}	ambient temperature	in free-air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T _{amb} = -40 °C to +85 °C						
V _{IK}	input clamping voltage	V _{CC} = 2.7 V; I _{IK} = -18 mA	-1.2		-	V
V _{IH}	HIGH-level input voltage		2.0	-	-	V
V _{IL}	LOW-level input voltage		-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _{CC} = 2.7 V to 3.6 V; I _{OH} = -100 µA	V _{CC} - 0.2		-	V
		V _{CC} = 2.7 V; I _{OH} = -6 mA	2.4	-	-	V
		V _{CC} = 3.0 V; I _{OH} = -20 mA	2.0	-	-	V
V _{OL}	LOW-level output voltage	V _{CC} = 2.7 V; I _{OL} = 100 µA	-		0.2	V
		V _{CC} = 2.7 V; I _{OL} = 24 mA	-		0.5	V
		V _{CC} = 3.0 V; I _{OL} = 32 mA	-		0.5	V
I _I	input leakage current	V _{CC} = 0 V or 3.6 V; V _I = 5.5 V	-	-	10	µA
		V _{CC} = 3.6 V; V _I = V _{CC} or GND		-	±1	µA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 0 V to 4.5 V			±100	µA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = GND or V _{CC} ; I _O = 0 A				
		output HIGH	-	-	0.02	mA
		output LOW	-	1	2	mA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 3.0 V to 3.6 V; one input at V _{CC} - 0.6 V and other inputs at V _{CC} or GND [2]	-		0.2	mA
C _I	input capacitance	V _I = 0 V or 3.0 V	-	3	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 3.3 V.
[2] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T _{amb} = -40 °C to +85 °C						
t _{PLH}	LOW to HIGH propagation delay	nA or nB to nY; see Fig. 6				
		V _{CC} = 2.7 V	-	-	5.2	ns
		V _{CC} = 3.0 V to 3.6 V	1	2.8	4.4	ns
t _{PHL}	HIGH to LOW propagation delay	nA or nB to nY; see Fig. 6				
		V _{CC} = 2.7 V	-	-	3.4	ns
		V _{CC} = 3.0 V to 3.6 V	1	2.6	3.6	ns

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 3.3 V.

10.1. Waveforms and test circuit

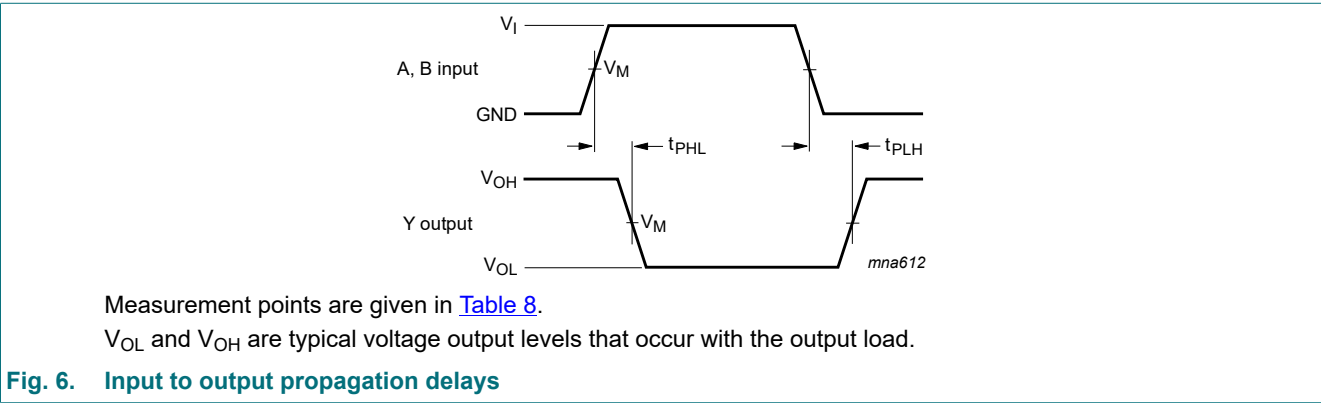


Table 8. Measurement points

Input		Output
V_M	V_I	V_M
1.5 V	2.7 V	1.5 V

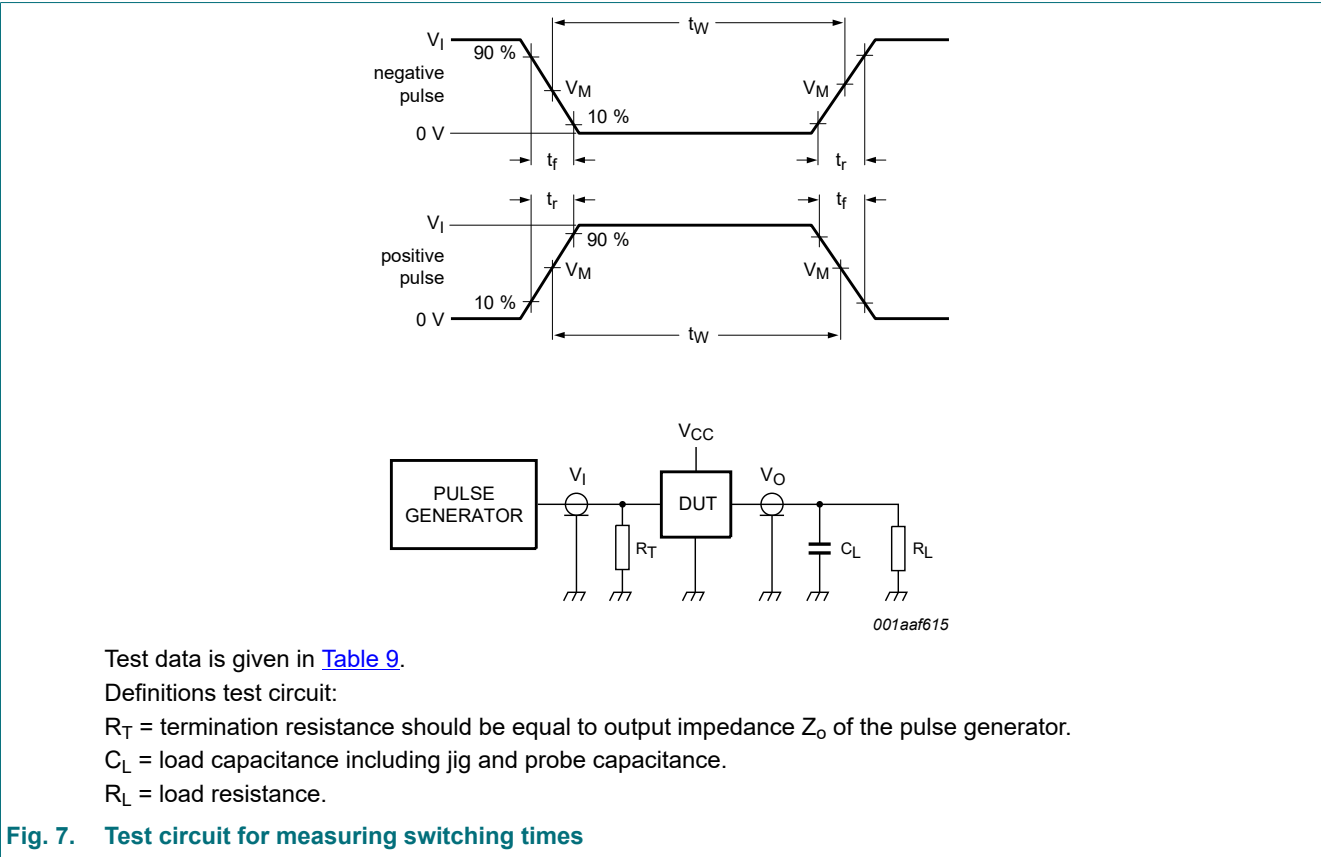


Table 9. Test data

Input				Load		Test
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

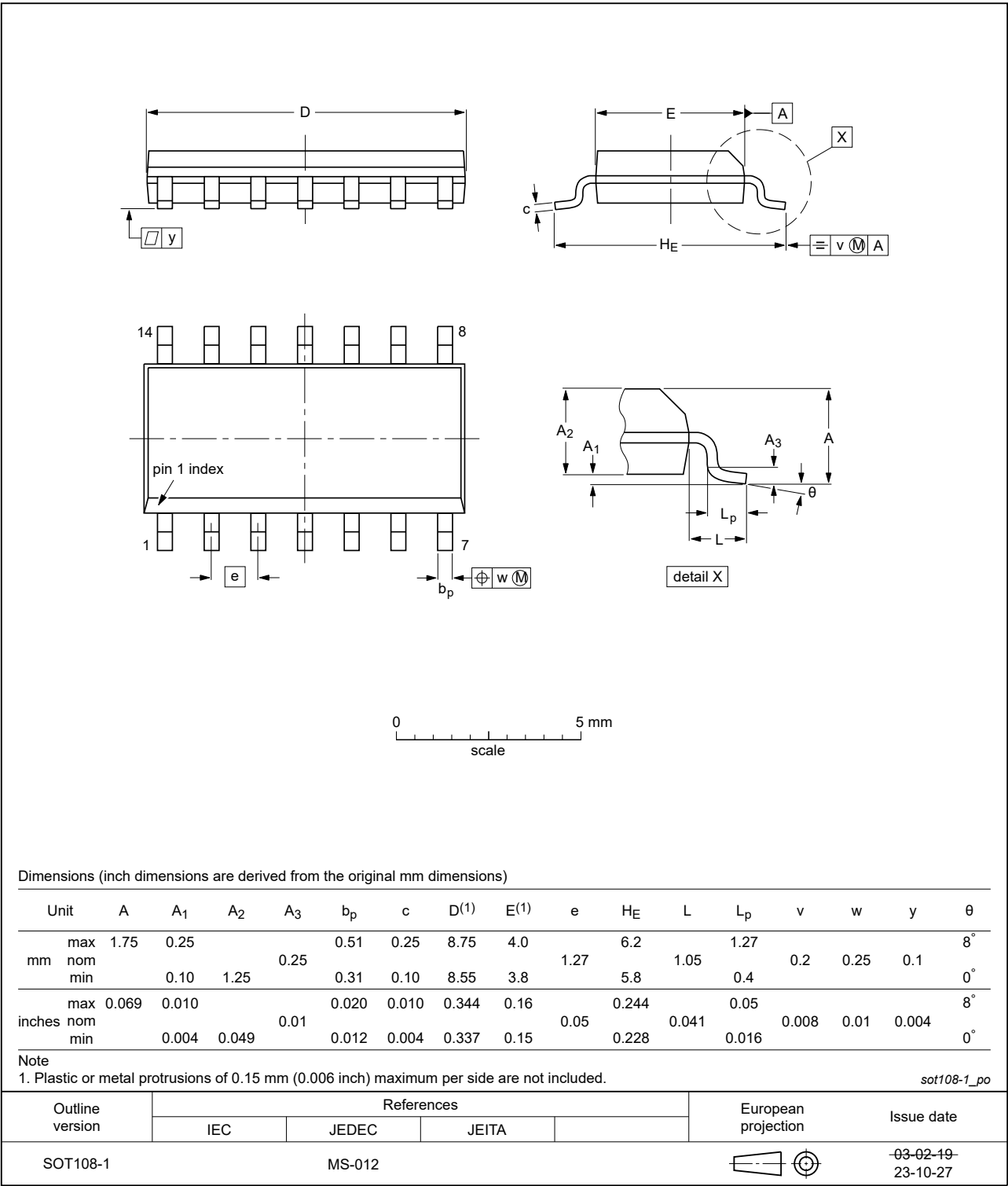


Fig. 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

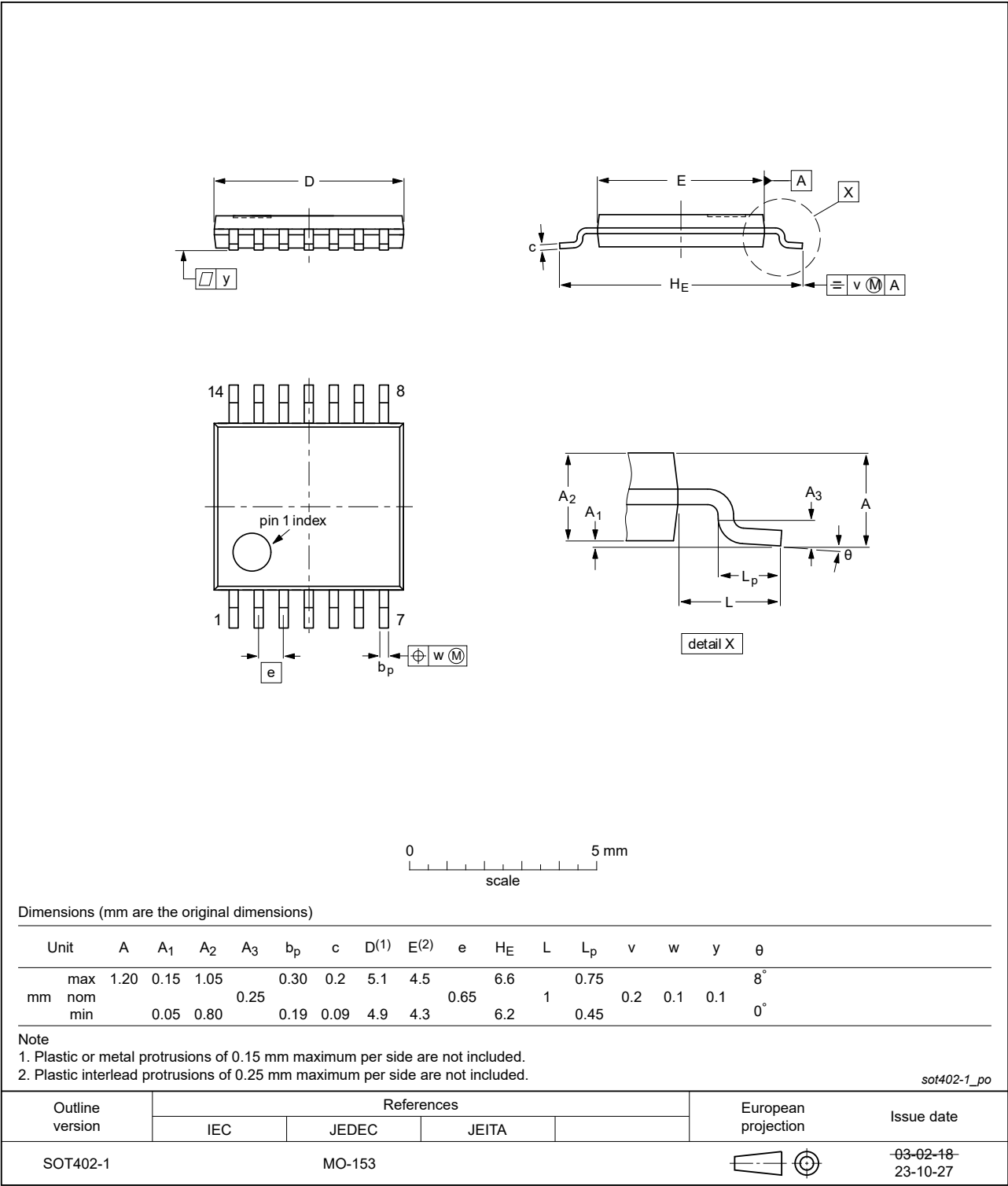


Fig. 9. Package outline SOT402-1 (TSSOP14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT02 v.5	20240418	Product data sheet	-	74LVT02 v.4
Modifications:	<ul style="list-style-type: none">Fig. 8, Fig. 9: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.Section 2: ESD specification updated according to the latest JEDEC standard.Section 9: ΔI_{CC} specification updated (errata).			
74LVT02 v.4	20210301	Product data sheet	-	74LVT02 v.3
Modifications:	<ul style="list-style-type: none">Type number 74LVT02DB (SOT337-1 / SSOP14) removed.Section 1 and Section 2 updated.Section 7: Derating value for P_{tot} total power dissipation updated.			
74LVT02 v.3	20170407	Product data sheet	-	74LVT02 v.2
Modifications:	<ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.Legal texts have been adapted to the new company name where appropriate.			
74LVT02 v.2	19960815	Product specification	-	74LVT02 v.1

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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