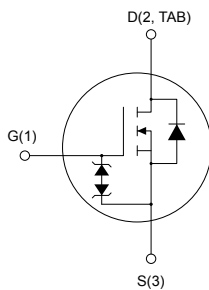
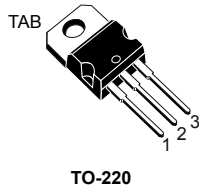


N-channel 900 V, 210 mΩ typ., 20 A MDmesh K5 Power MOSFET in a TO-220 package

Features



AM01476v1_tab

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STP20N90K5	900 V	250 mΩ	20 A

- Very low FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.



Product status link

[STP20N90K5](#)

Product summary

Order code	STP20N90K5
Marking	20N90K5
Package	TO-220
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	20	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	13	A
$I_{DM}^{(1)}$	Drain current (pulsed)	80	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	250	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	
T_J	Operating junction temperature range	-55 to 150	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 20\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$; $V_{DS(peak)} \leq V_{(BR)DSS}$, $V_{DD} = 450\text{ V}$.
3. $V_{DD} \leq 720\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.5	$^{\circ}\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	$^{\circ}\text{C}/\text{W}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	6.5	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	500	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Table 4. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	900			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 900\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 900\text{ V}$			50	μA
		$T_C = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾				
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$		210	250	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	1500	-	pF
C_{oss}	Output capacitance		-	120	-	pF
C_{rss}	Reverse transfer capacitance		-	1	-	pF
$C_{o(er)}$ ⁽¹⁾	Equivalent capacitance energy related	$V_{DS} = 0\text{ to }720\text{ V}$, $V_{GS} = 0\text{ V}$	-	78	-	pF
$C_{o(tr)}$ ⁽²⁾	Equivalent capacitance time related			220	-	pF
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	3.7	-	Ω
Q_g	Total gate charge	$V_{DD} = 720\text{ V}$, $I_D = 20\text{ A}$	-	40	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 0\text{ to }10\text{ V}$	-	14	-	nC
Q_{gd}	Gate-drain charge	(see Figure 14. Test circuit for gate charge behavior)	-	17	-	nC

- $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 450\text{ V}$, $I_D = 10\text{ A}$, $R_G = 4.7\text{ }\Omega$ $V_{GS} = 10\text{ V}$ (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	20.2	-	ns
t_r	Rise time		-	13.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	64.7	-	ns
t_f	Fall time		-	16	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		20	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		80	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 20\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 20\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	517		ns
Q_{rr}	Reverse recovery charge		-	11.4		μC
I_{RRM}	Reverse recovery current		-	44		A
t_{rr}	Reverse recovery time		-	674		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	14		μC
I_{RRM}	Reverse recovery current		-	41.6		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics curves

Figure 1. Safe operating area

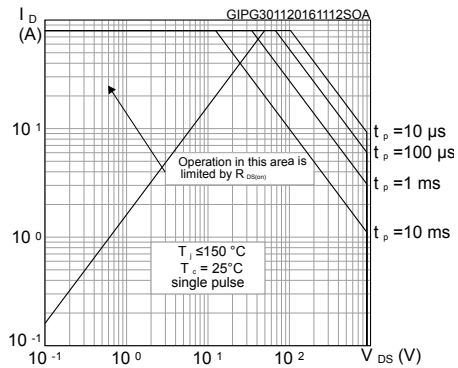


Figure 2. Thermal impedance

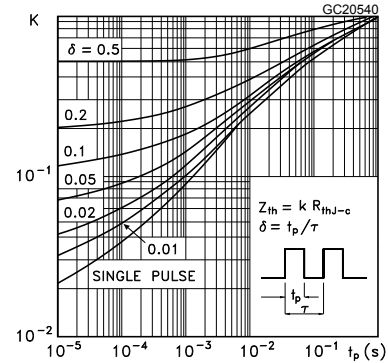


Figure 3. Output characteristics

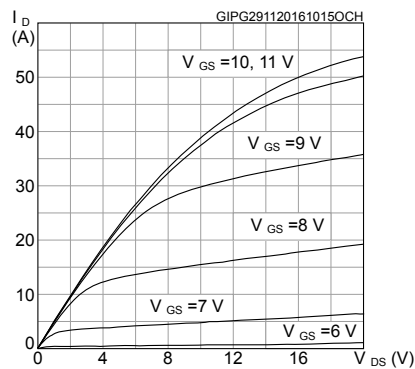


Figure 4. Transfer characteristics

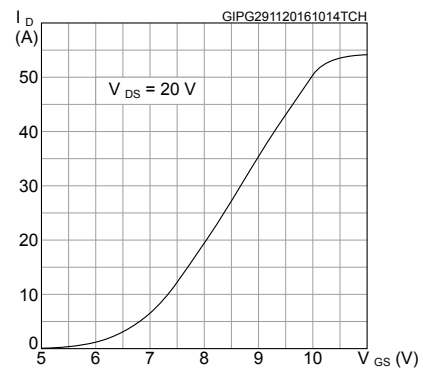


Figure 5. Normalized $V_{(BR)DSS}$ vs temperature

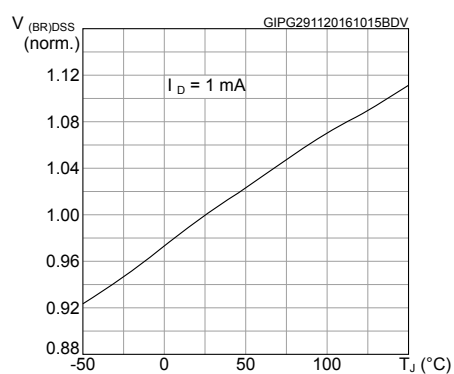


Figure 6. Static drain-source on-resistance

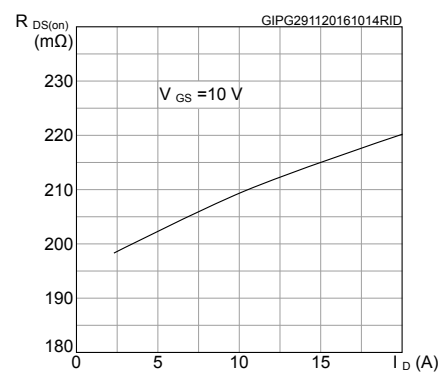
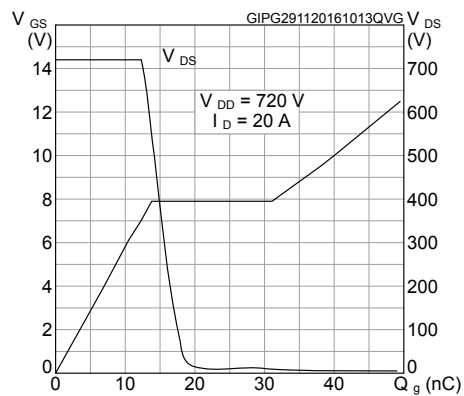
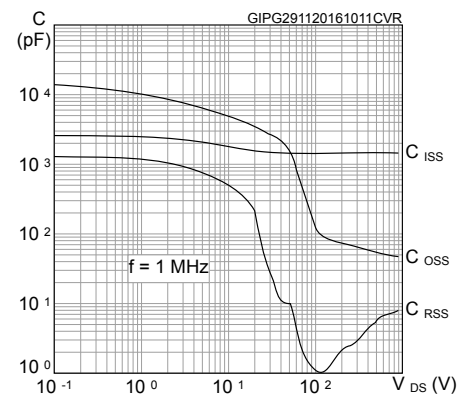
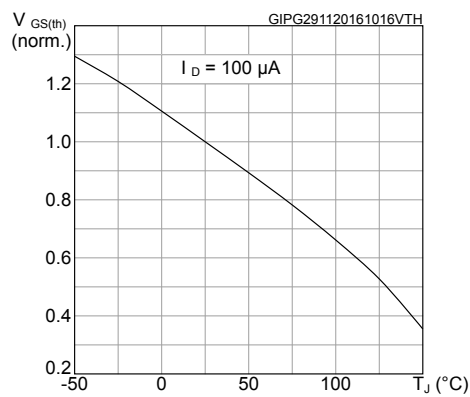
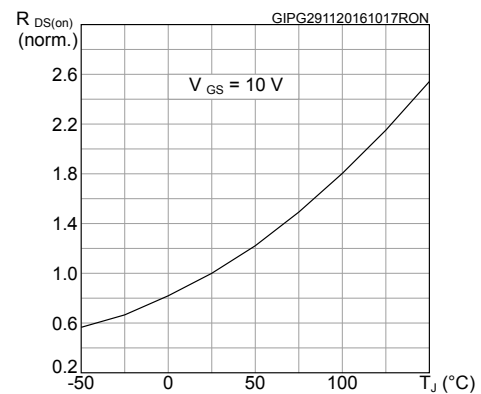
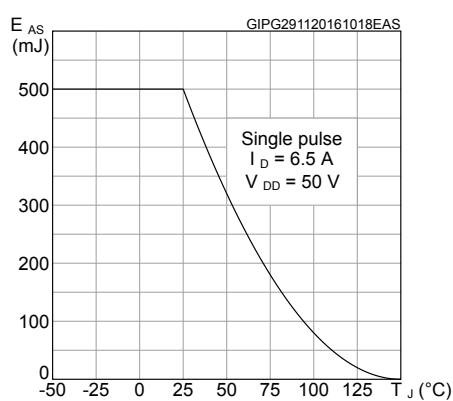
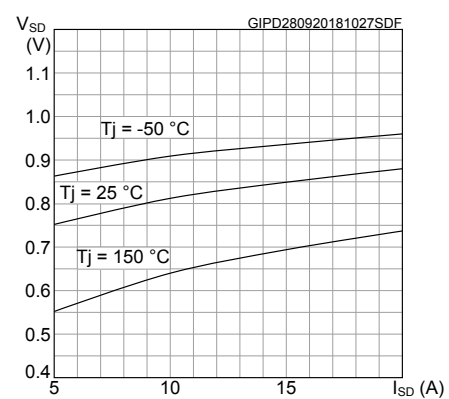
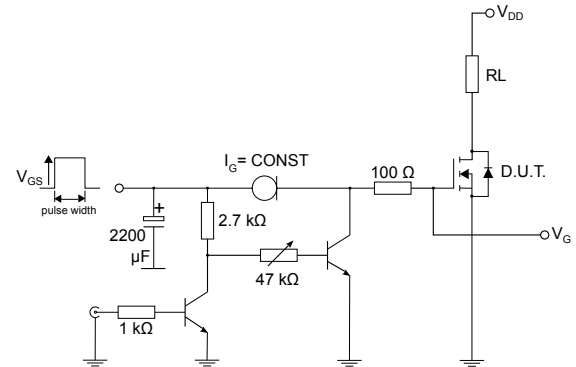


Figure 7. Gate charge vs gate-source voltage

Figure 8. Capacitance variation

Figure 9. Normalized gate threshold voltage vs temperature

Figure 10. Normalized on-resistance vs temperature

Figure 11. Maximum avalanche energy vs. starting T_J

Figure 12. Source-drain diode forward characteristics


3 Test circuits

Figure 13. Test circuit for resistive load switching times


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Figure 14. Test circuit for gate charge behavior


AM01469v10

Figure 15. Test circuit for inductive load switching and diode recovery times

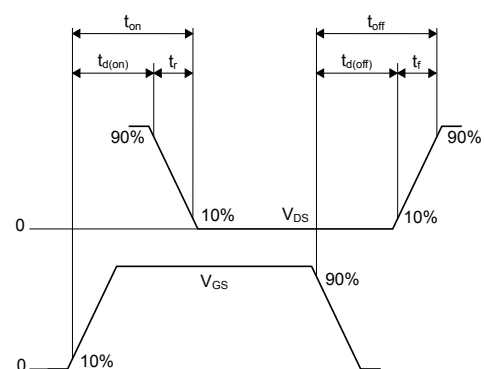

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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


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Figure 18. Switching time waveform


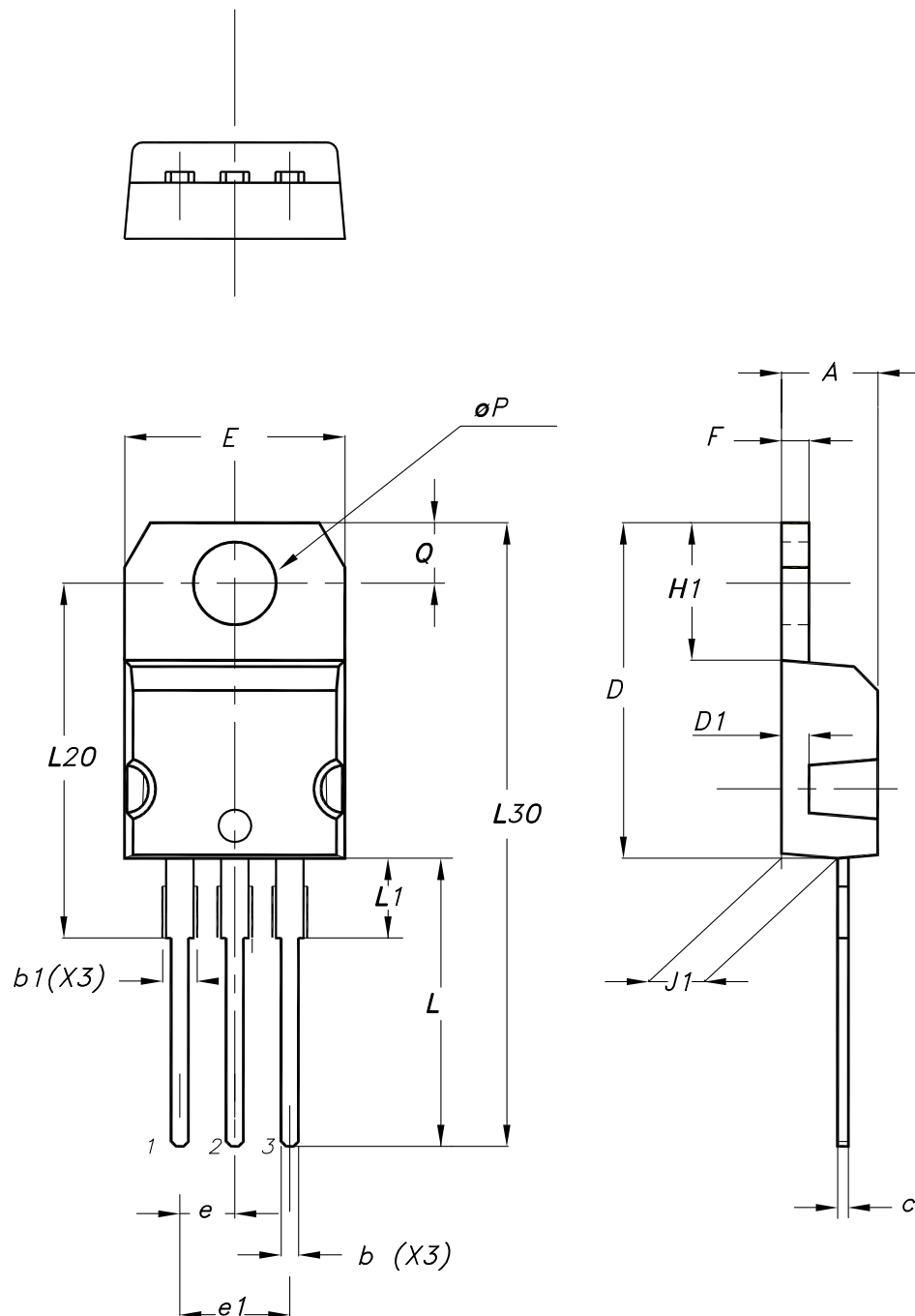
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220 type A package information

Figure 19. TO-220 type A package outline



0015988_typeA_Rev_24

Table 8. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

Revision history

Table 9. Document revision history

Date	Revision	Changes
10-May-2016	1	First release.
01-Dec-2016	2	Modified: title and $R_{DS(on)}$ value in cover page Modified <i>Table 4: "Avalanche characteristics"</i> , <i>Table 5: "On/off-state"</i> , <i>Table 6: "Dynamic"</i> , <i>Table 7: "Switching times"</i> and <i>Table 8: "Sourcedrain diode"</i> Added <i>Section 2.1: "Electrical characteristics (curves)"</i> Modified <i>Section 3: "Test circuits"</i> Datasheet promoted from preliminary data to production data Minor text changes
24-Jan-2017	3	Modified <i>Table 6: "Dynamic"</i> . Minor text changes.
05-Oct-2018	4	Removed maturity status indication from cover page. Added <i>Figure 12. Source-drain diode forward characteristics</i> . Minor text changes.
24-Feb-2026	5	Updated <i>Section 4.1: TO-220 type A package information</i> . Minor text changes.

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