### **STL3N80K5**



# N-channel 800 V, 2.8 Ω typ., 2 A MDmesh™ K5 Power MOSFET in a PowerFLAT™ 5x6 VHV package

Datasheet - production data

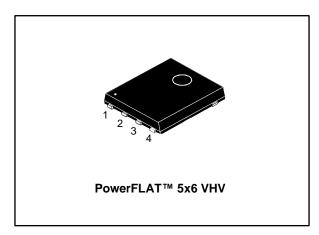
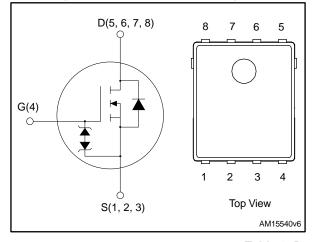


Figure 1: Internal schematic diagram



#### **Features**

Order code	Order code V <sub>DS</sub> R <sub>DS</sub>		lο	Ртот
STL3N80K5	800 V	3.5 Ω	2 A	38 W

- Industry's lowest R<sub>DS(on)</sub> x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

### **Applications**

• Switching applications

### **Description**

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

**Table 1: Device summary** 

Order code	Marking	Package	Packing
STL3N80K5	3N80K5	PowerFLAT™ 5x6 VHV	Tape and reel

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STL3N80K5 Electrical ratings

# 1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>G</sub> s	Gate-source voltage	±30	V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	2	Α
ΙD	Drain current (continuous) at T <sub>C</sub> = 100 °C	1.3	Α
I <sub>DM</sub> <sup>(1)</sup>	Drain current (pulsed)	8	Α
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	38	
dv/dt (2)	Peak diode recovery voltage slope	4.5	\//n a
dv/dt (3)	dv/dt (3) MOSFET dv/dt ruggedness		V/ns
Tj	Operating junction temperature range	FF to 150	°C
T <sub>stg</sub>	Storage temperature range	- 55 to 150	

#### Notes:

Table 3: Thermal data

Symbol Parameter		Value	Unit	
R <sub>thj-case</sub>	R <sub>thj-case</sub> Thermal resistance junction-case			
R <sub>thj-pcb</sub> <sup>(1)</sup>	Thermal resistance junction-pcb	59	°C/W	

#### Notes

**Table 4: Avalanche characteristics** 

Symbol	Parameter	Value	Unit
lar	$I_{AR} \qquad \begin{array}{l} \text{Avalanche current, repetitive or not repetitive} \\ \text{(pulse width limited by } T_{jmax}) \\ \\ \text{E}_{AS} \qquad \begin{array}{l} \text{Single pulse avalanche energy} \\ \text{(starting Tj} = 25 \ ^{\circ}\text{C}, \ I_{D} = I_{AR}, \ V_{DD} = 50 \ V) \end{array}$		А
Eas			mJ

<sup>&</sup>lt;sup>(1)</sup>Pulse width limited by safe operating area.

 $<sup>^{(2)}</sup>I_{SD} \le 2 \text{ A, di/dt} = 100 \text{ A/}\mu\text{s; V}_{DS} \text{ peak} < V_{(BR)DSS}$ 

 $<sup>^{(3)}</sup>V_{DS} \le 640 \text{ V}.$ 

 $<sup>^{(1)}</sup>$ When mounted on FR-4 board of 1 inch², 2 oz Cu

Electrical characteristics STL3N80K5

### 2 Electrical characteristics

T<sub>C</sub> = 25 °C unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	800			V
	I <sub>DSS</sub> Zero gate voltage drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 800 \text{ V}$			1	μΑ
I <sub>DSS</sub>		$V_{GS} = 0 \text{ V}, V_{DS} = 800 \text{ V}$ $T_{C} = 125 \text{ °C}^{(1)}$			50	μΑ
Igss	Gate body leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			±10	μΑ
V <sub>GS(th)</sub>	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100 \mu A$	3	4	5	V
R <sub>DS(on)</sub>	Static drain-source on- resistance	V <sub>G</sub> S = 10 V, I <sub>D</sub> = 1 A		2.8	3.5	Ω

#### Notes:

**Table 6: Dynamic** 

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
Ciss	Input capacitance		ı	130	1	pF
Coss	Output capacitance	$V_{DS} = 100 \text{ V}, f = 1 \text{ MHz},$ $V_{GS} = 0 \text{ V}$	1	14	ı	pF
Crss	Reverse transfer capacitance		ı	0.6	ı	pF
C <sub>o(tr)</sub> <sup>(1)</sup>	Equivalent capacitance time related	V <sub>DS</sub> = 0 to 640 V, V <sub>GS</sub> = 0 V	1	20	ı	pF
C <sub>o(er)</sub> <sup>(2)</sup>	Equivalent capacitance energy related		1	9	ı	pF
Rg	Intrinsic gate resistance	f = 1 MHz , I <sub>D</sub> =0 A	-	15.5	-	Ω
Qg	Total gate charge	V <sub>DD</sub> = 640 V, I <sub>D</sub> = 2.5 A	-	9.5	-	nC
Qgs	Gate-source charge	V <sub>GS</sub> = 0 to 10 V (see Figure 15: "Test circuit for gate charge behavior")	-	1.5	-	nC
Q <sub>gd</sub>	Gate-drain charge		-	7.5	-	nC

#### Notes:

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<sup>&</sup>lt;sup>(1)</sup>Defined by design, not subject to production test.

 $<sup>^{(1)}</sup>$ Time related is defined as a constant equivalent capacitance giving the same charging time as Coss when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ 

 $<sup>^{(2)}</sup>$ Energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ 

Table 7: Switching times

Table 1. Ownering times						
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 400 V, I <sub>D</sub> = 1.25 A,	-	8.5	-	ns
tr	Rise time	$R_G = 4.7 \Omega$	ı	7.5	-	ns
$t_{d(off)}$	Turn-off delay time	V <sub>GS</sub> = 10 V (see Figure 14: "Test circuit for	-	20.5	-	ns
t <sub>f</sub>	Fall time	resistive load switching times" and Figure 19: "Switching time waveform")	-	25	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I <sub>SD</sub>	Source-drain current		-		2	Α
I <sub>SDM</sub> <sup>(1)</sup>	Source-drain current (pulsed)		-		8	А
V <sub>SD</sub> <sup>(2)</sup>	Forward on voltage	I <sub>SD</sub> = 2 A, V <sub>GS</sub> = 0 V	-		1.5	V
t <sub>rr</sub>	Reverse recovery time	I <sub>SD</sub> = 2 A, di/dt = 100 A/µs,	-	265		ns
Q <sub>rr</sub>	Reverse recovery charge	$V_{DD} = 60 \text{ V}$ (see Figure 16: "Test circuit for	-	1.2		μC
I <sub>RRM</sub>	Reverse recovery current	inductive load switching and diode recovery times")	-	9.2		А
t <sub>rr</sub>	Reverse recovery time	I <sub>SD</sub> = 2 A, di/dt = 100 A/µs,	-	430		ns
Qrr	Reverse recovery charge	V <sub>DD</sub> = 60 V, T <sub>j</sub> = 150 °C (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	1.9		μC
I <sub>RRM</sub>	Reverse recovery current		-	8.8		А

#### Notes:

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I <sub>GS</sub> = ±1 mA, I <sub>D</sub> = 0 A	30		1	V

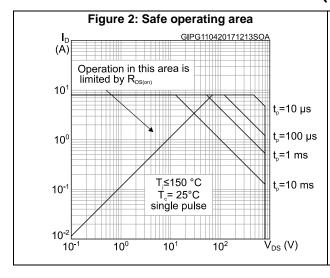
The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.



<sup>&</sup>lt;sup>(1)</sup>Pulse width limited by safe operating area

 $<sup>^{(2)}</sup>$ Pulsed: pulse duration = 300  $\mu$ s, duty cycle 1.5%

### 2.1 Electrical characteristics (curves)



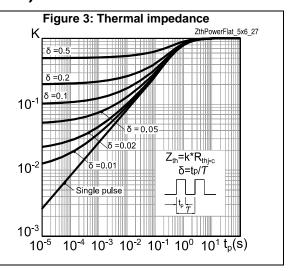


Figure 4: Output characteristics

AM18012v1

VGS=10,11V

9V

3

2

1

7V

0

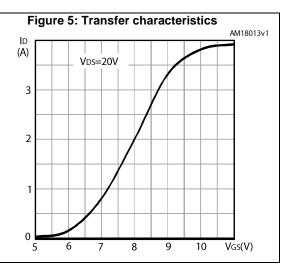
4

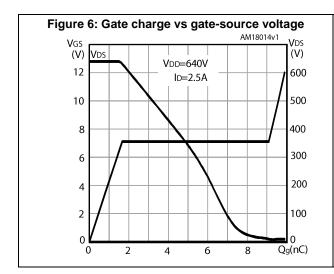
8

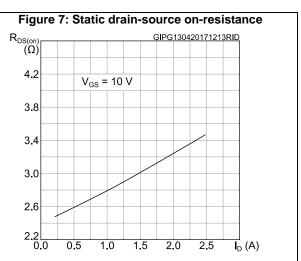
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VDS(V)



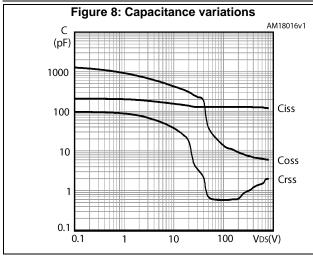




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STL3N80K5 Electrical characteristics



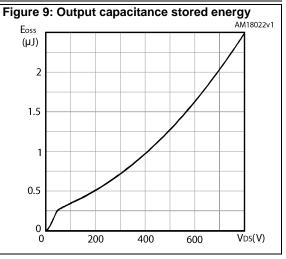
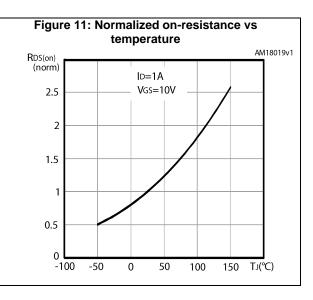
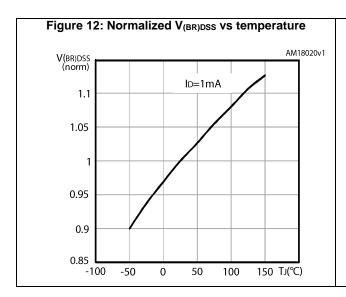
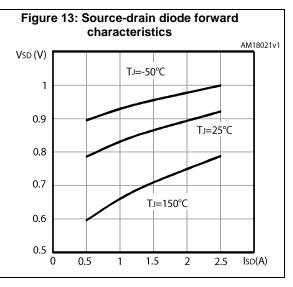


Figure 10: Normalized gate threshold voltage vs temperature AM18017v1 (norm) 1.2 ID=100μA 1.1 0.9 0.8 0.7 0.6 0.5 0.4 -50 50 100 150 TJ(°C)



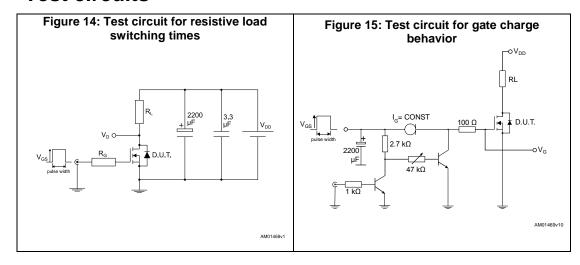


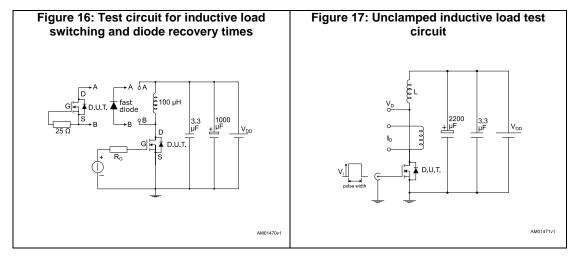


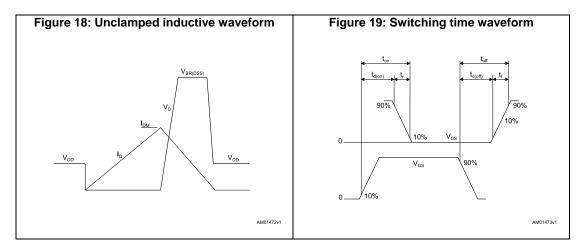


Test circuits STL3N80K5

### 3 Test circuits







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STL3N80K5 Package information

# 4 Package information

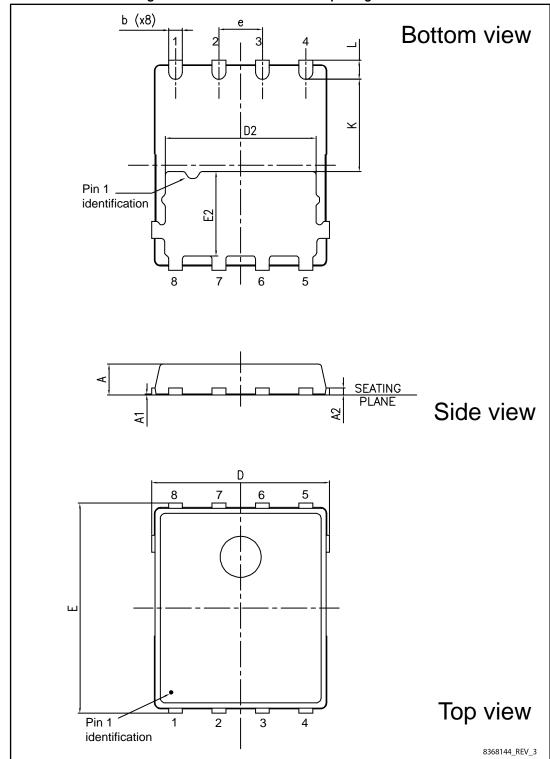
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.



Package information STL3N80K5

# 4.1 PowerFLAT™ 5x6 VHV package information

Figure 20: PowerFLAT™ 5x6 VHV package outline



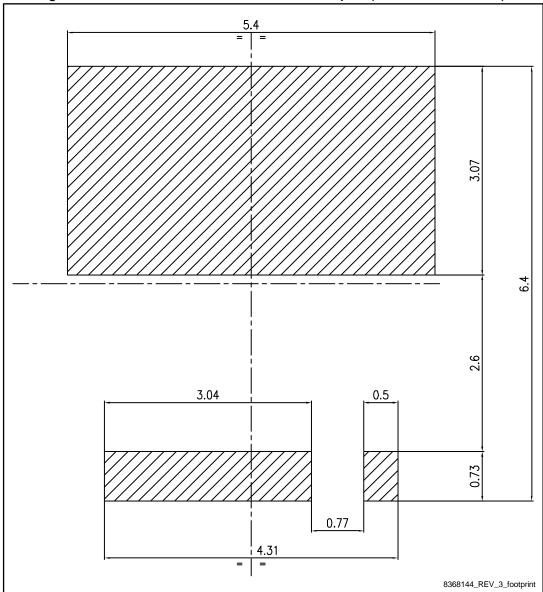
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Table 10: PowerFLAT™ 5x6 VHV package mechanical data

Dim.	mm			
Dilli.	Min.	Тур.	Max.	
А	0.80		1.00	
A1	0.02		0.05	
A2		0.25		
b	0.30		0.50	
D	5.00	5.20	5.40	
Е	5.95	6.15	6.35	
D2	4.30	4.40	4.50	
E2	2.40	2.50	2.60	
е		1.27		
L	0.50	0.55	0.60	
K	2.60	2.70	2.80	

Figure 21: PowerFLAT™ 5x6 VHV recommended footprint (dimensions are in mm)



STL3N80K5 Package information

# 4.2 PowerFLAT™ 5x6 VHV packing information

Figure 22: PowerFLAT™ 5x6 tape (dimensions are in mm)

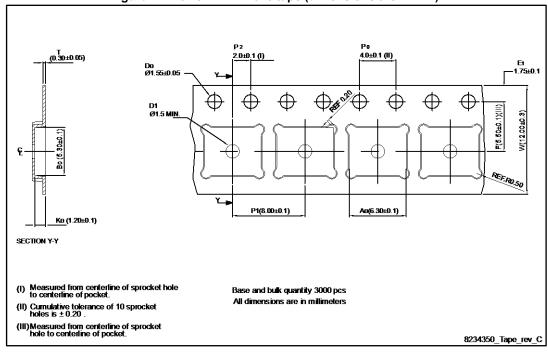
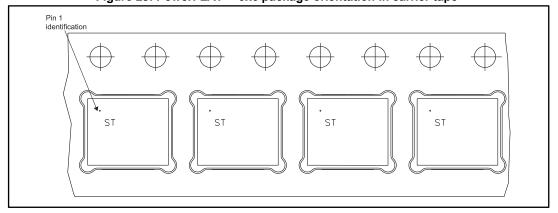


Figure 23: PowerFLAT™ 5x6 package orientation in carrier tape



8234350\_Reel\_rev\_C

Figure 24: PowerFLAT™ 5x6 reel PART NO. A 330 (+0/-4.0) ESD LOGO All dimensions are in millimeters

STL3N80K5 Revision history

# 5 Revision history

Table 11: Document revision history

Date	Revision	Changes
10-Apr-2017	1	First release.

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