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FDD5690

60V N-Channel PowerTrench® MOSFET

General Description

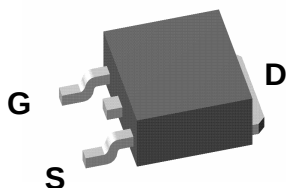
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable $R_{DS(ON)}$ specifications.

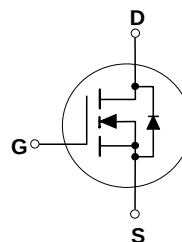
The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

Features

- 30 A, 60 V. $R_{DS(ON)} = 0.027\Omega$ @ $V_{GS} = 10$ V
 $R_{DS(ON)} = 0.032\Omega$ @ $V_{GS} = 6$ V.
- Low gate charge (23nC typical).
- Fast switching speed.
- High performance trench technology for extremely low $R_{DS(ON)}$.



TO-252



Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Maximum Drain Current -Continuous (Note 1) (Note 1a)	30	A
	Maximum Drain Current -Pulsed	9	
P_D	Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ (Note 1)	100	W
	$T_A = 25^\circ\text{C}$ (Note 1a)	50	
	$T_A = 25^\circ\text{C}$ (Note 1b)	3.2	
T_J, T_{stg}	Operating and Storage Junction Temperature Range	1.3	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to- Case (Note 1)	2.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to- Ambient (Note 1a) (Note 1b)	40	$^\circ\text{C/W}$
		96	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDD5690	FDD5690	13"	16mm	2500

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 30\text{ V}, I_D = 30\text{ A}$			90	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				30	A
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		57		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}$			1	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	2.5	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		-6		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 9\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 9\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = 6\text{ V}, I_D = 8\text{ A}$		0.023 0.032 0.026	0.027 0.048 0.032	Ω
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	25			A
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 9\text{ A}$		24		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}$ $f = 1.0\text{ MHz}$		1110		pF
C_{oss}	Output Capacitance			150		pF
C_{rss}	Reverse Transfer Capacitance			75		pF

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{ V}, I_D = 1\text{ A}$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		10	18	ns
t_r	Turn-On Rise Time			9	18	ns
$t_{d(off)}$	Turn-Off Delay Time			24	39	ns
t_f	Turn-Off Fall Time			10	18	ns
Q_g	Total Gate Charge	$V_{DS} = 30\text{ V}, I_D = 9\text{ A}$ $V_{GS} = 10\text{ V},$		23	32	nC
Q_{gs}	Gate-Source Charge			4		nC
Q_{gd}	Gate-Drain Charge			6.8		nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current				2.3	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.3\text{ A}$ (Note 2)		0.75	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the drain tab.

$R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



■ a) $R_{\theta JA} = 40^\circ\text{C/W}$ when mounted on a 1 in^2 pad of 2oz copper.

■ b) $R_{\theta JA} = 96^\circ\text{C/W}$ on a minimum mounting pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$

Typical Characteristics

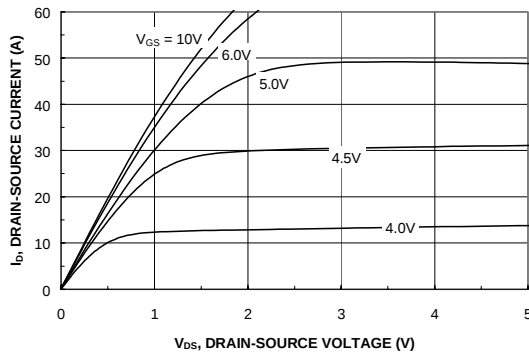


Figure 1. On-Region Characteristics.

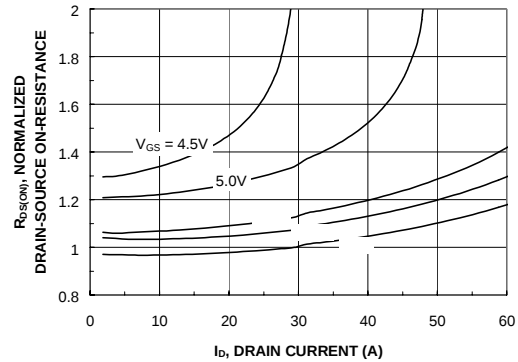


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

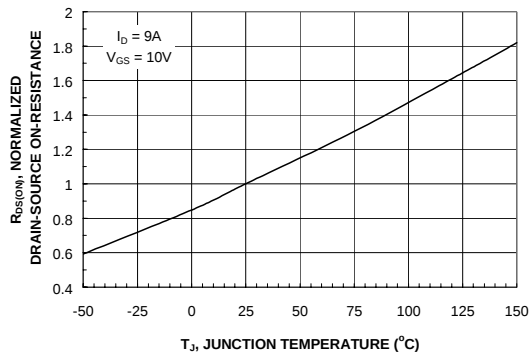


Figure 3. On-Resistance Variation with Temperature.

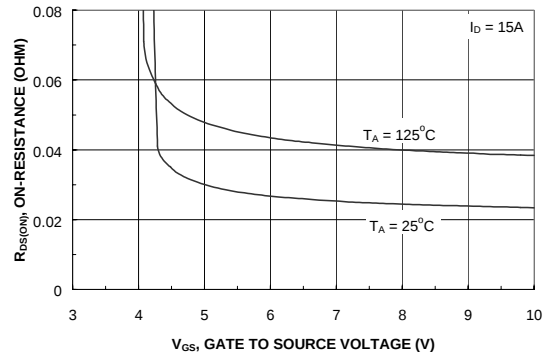


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

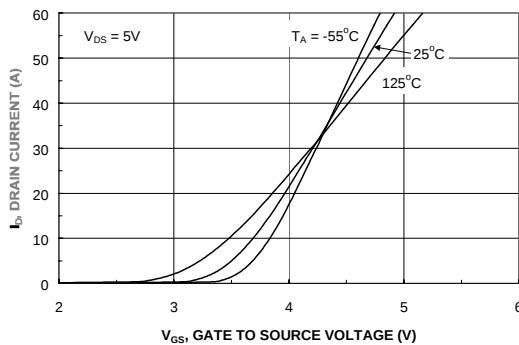


Figure 5. Transfer Characteristics.

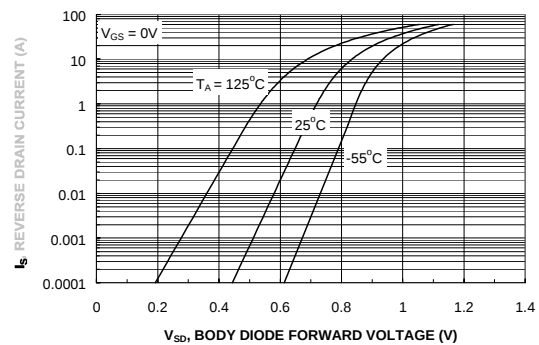


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)

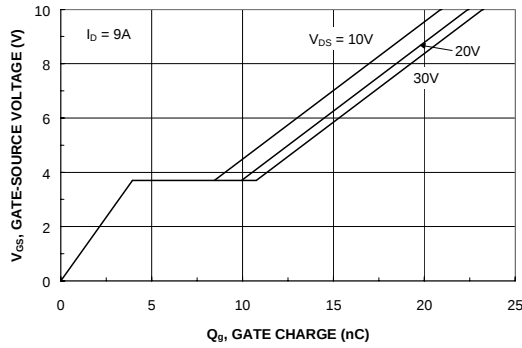


Figure 7. Gate-Charge Characteristics.

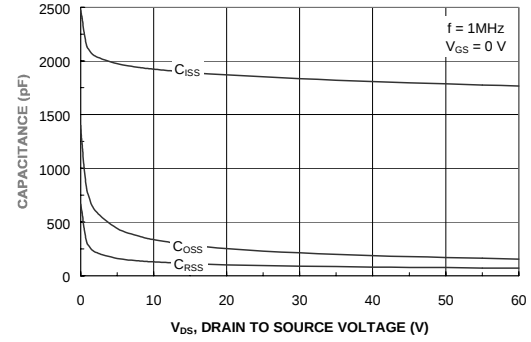


Figure 8. Capacitance Characteristics.

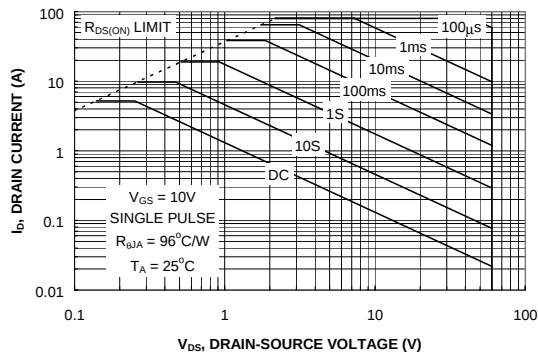


Figure 9. Maximum Safe Operating Area.

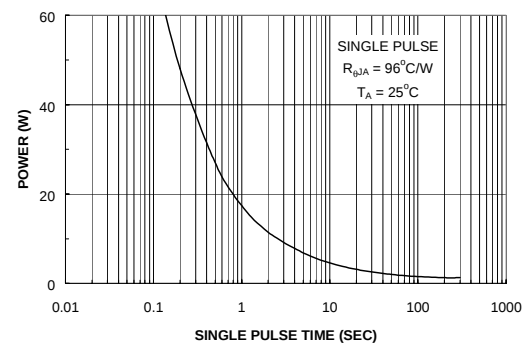


Figure 10. Single Pulse Maximum Power Dissipation.

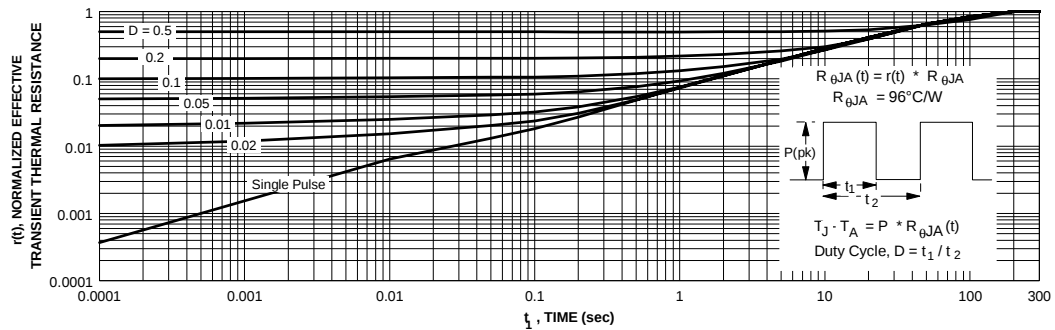


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

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