LED Drivers for LCD Backlights

White LED Driver for large LCD panel

BD9397EFV

●General Description

BD9397EFV is a high efficiency driver for white LEDs and designed for large LCD panel. This IC is built-in high current drive and high responsibility type 6ch LED drivers and 1ch boost DCDC converter. BD9397EFV has some protect function against fault conditions, such as the over-voltage protection (OVP), LED OPEN and SHORT protection, the over current limit protection of DCDC (OCP). Therefore BD9397EFV is available for the fail-safe design over a wide range output voltage.

●Key Specification

- Operating power supply voltage range: 9.0V to 35.0V
- Oscillator frequency: 500kHz (RT=30kΩ)
- Operating Current: 9mA (typ.)
- Operating temperature range: -40°C to +85°C

●Applications

TV, Computer Display, Notebook, LCD Backlighting

●Features

- 6ch Constant LED drivers, available 400mA drive per 1ch.
- Constant current accuracy ±1.8% (IC only)
- Each 6ch external PWM inputs can control independent dimming .
- Current analog (linear) dimming by VREF
- 1ch boost controller with current mode (external FET)
- Several protection functions
  DCDC part : OCP/OVP/UVLO/TSD
  LED driver part :OPEN,SHORT detection
- SHORT detection voltage is set by LSP terminal.
- Error detection output FAIL terminal inside (normal=Open, error=Drain)

●Package

	W(Typ.)	D(Typ.)	H(Max.)
HTSSOP-B40	13.60mm	x 7.80mm	x 1.00mm
Pin Pitch:			0.65mm

●Typical Application Circuit

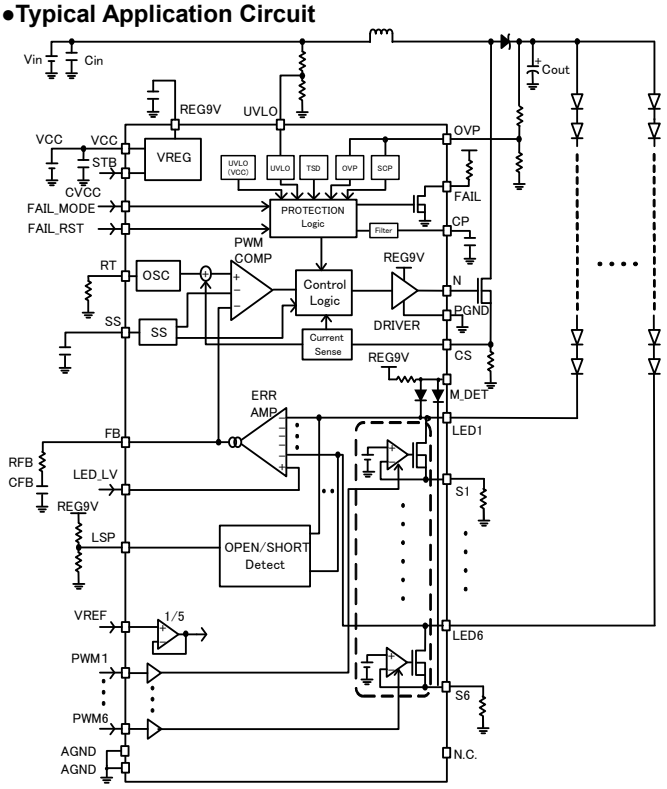


Figure 1. Typical Application Circuit

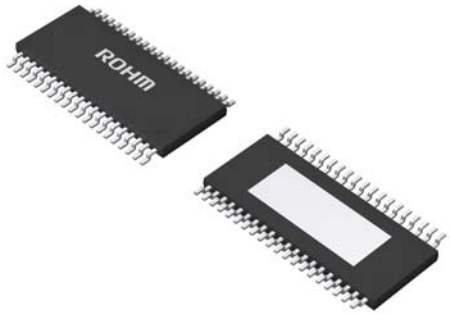


Figure 2. HTSSOP-B40

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●**Absolute maximum ratings** (Ta=25°C)

Parameter	Symbol	Ratings	Unit
Operating Temperature Range	Ta(opr)	-40 to +85	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Power Dissipation	Pd	4.7 *1	W
Thermal resistance between junction and case	θjc	7 *2	°C/W
Maximum Junction Temperature	Tjmax	150	°C
Maximum LED output current	ILED	400 *3 *4	mA

*1 In the case of mounting 4 layer glass epoxy base-plate of 70mm×70mm×1.6mm, 37.6mW is reduced at 1°C above Ta=25℃.
*2 In the case of mounting 4 layer glass epoxy base-plate of 70mm×70mm×1.6mm.
*3 Wide VF variation of LED increases loss at the driver, which results in rise in package temperature. Therefore, the board needs to be designed with attention paid to heat radiation.
*4 This current value is per 1ch. It needs be used within a range not exceeding Pd.

●**Operating Ratings** (Ta = 25°C)

Parameter	Symbol	Range	Unit
Power supply voltage	VCC	9 to 35	V
DC/DC oscillation frequency	FCT	100 to 1250 *5	kHz
VREF input voltage	VREF	0.2 to 2.5	V
LSP terminal input voltage	VLSP	0.8 to 3	V
FB terminal output voltage	VFB	0 to 3.3	V
M_DET terminal output voltage	VM_DET	0 to REG9V	V

The operating conditions written above are constants of the IC unit. Be careful enough when setting the constant in the actual set.

●**External Components Recommended Range**

Item	Symbol	Setting Range	Unit
VCC terminal connection capacitance	CVCC	1.0 to 10	μF
Soft-start set capacitance	SS	0.001 to 1.0	μF
Timer latch set capacitance	CP	0.001 to 2.7	μF
Operating frequency set resistance	RT	12 to 150	kΩ
REG9V terminal connection capacitance	CREG9V	2.2 to 10	μF

The values described above are constants for a single IC. Adequate attention must be paid to setting of a constant for an actual set of parts

●**Pin Configuration**

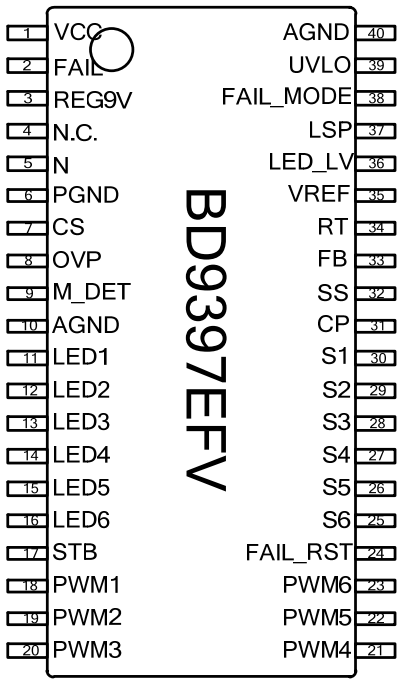


Figure 3.

●**Physical Dimension Tape and Marking Diagram**

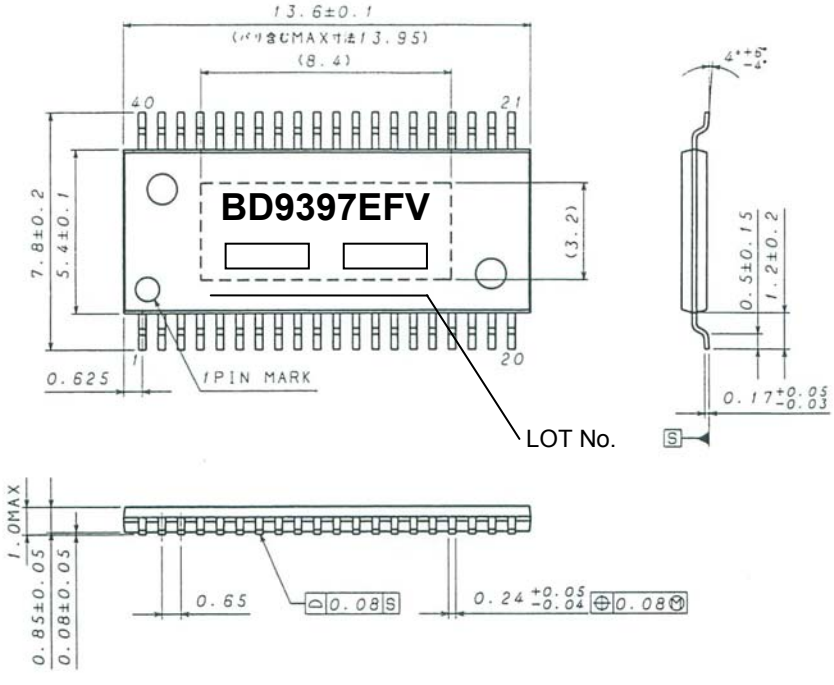


Figure 4. HTSSOP-B40

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●**1.1 Electrical Characteristics 1**(Unless otherwise specified, Ta=25°C, VCC=24V)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
【Whole device】						
Operating circuit current	ICC	-	9	16	mA	STB=3V,LED1-6=ON, RT=30kΩ
Stand-by circuit current	ISTB	-	12	20	μA	STB=0V
【REG9V block】						
REG9V output voltage	REG9V	8.9	9.0	9.1	V	IO=0mA
Maximum REG9V output current	IREG9V	20	-	-	mA	
【Switching block】						
N terminal source resistance	RONH	-	2.5	3.5	Ω	ION=-10mA
N terminal sink resistance	RONL	-	3.0	4.2	Ω	ION=10mA
【Over current protection (OCP) block】						
Over current protection voltage	VOCP	0.40	0.45	0.50	V	VCS=SWEEP UP
【Soft-start block】						
SS terminal source current	ISS	-1.4	-1.0	-0.6	μA	
SS terminal release voltage	VSS	2.9	3.0	3.1	V	SS=SWEEP UP
【Error amplifier block】						
LED control voltage	VLED	0.66	0.7	0.74	V	LED_LV=0.7V
FB sink current	IFBSINK	55	100	155	μA	LED=2.0V, VFB=1.0V
FB source current	IFBSOURCE	-155	-100	-55	μA	LED=0V, VFB=1.0V
LED_LV terminal input current	ILED_LV	-2	0	2	uA	VLED_LV=3V
【CT oscillator block】						
Oscillation frequency	FCT	440	500	560	kHz	RT=30kΩ
MAX DUTY	DMAX	78	84	91	%	
【Over voltage protection (OVP) block】						
OVP detection voltage	VOVP	2.34	2.43	2.52	V	VOVP=SWEEP UP
OVP hysteresis voltage	VOVPHYS	10	50	100	mV	VOVP=SWEEP DOWN
OVP feedback voltage	FBOVP	0.93	1.05	1.17	V	PMW1-6=0V,SS=2.8V, VLED_LV=0.7V
【Short current protection (SCP) block】						
Short circuit protection voltage	VSCPmL	0.12	0.20	0.28	V	VOVP=SWEEP DOWN, FAILMODE=0V
	VSCPmH	0.74	0.79	0.84	V	VOVP=SWEEP DOWN, FAILMODE=3V
【M_LED block】						
Diode forward voltage	VFLED	1120	1340	1560	mV	VLED=0V
Forward voltage offset each ch	VFOFFSET	-	-	20	mV	VLED=0V
REG9V pull up resistance	RM_DET	60	100	140	kΩ	

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●**1.2 Electrical Characteristics 2**(Unless otherwise specified, Ta=25°C, VCC=24V)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
【UVLO block】						
Operation power source voltage (VCC)	VUVLO_VCC	7.0	7.5	8.0	V	VCC=SWEEP UP
Hysteresis voltage (VCC)	VUHYS_VCC	150	300	600	mV	VCC=SWEEP DOWN
UVLO Release voltage	VUVLO_U	2.375	2.5	2.625	V	VUVLO=SWEEP UP
Hysteresis voltage (UVLO)	VUHYS_U	50	100	150	mV	VUVLO=SWEEP DOWN
UVLO terminal input resistance	RUVLO	370	610	850	kΩ	VUVLO=3V
【Filter block】						
CP detection voltage	VCP	1.9	2.0	2.1	V	CP=SWEEP UP
CP source current	ICP	-1.2	-1.0	-0.8	μA	VCP=0V
【LED driver block】						
S terminal voltage	VSLED	196	200	204	mV	VREF=1.0V
		294.6	300	305.4	mV	VREF=1.5V
		392.8	400	407.2	mV	VREF=2.0V
		491	500	509	mV	VREF=2.5V
LED current rise time	ILEDtr	-	400	760	ns	VREF=0.3V,RS=2Ω
LED current fall time	ILEDtf	-	100	280	ns	VREF=0.3V,RS=2Ω
OPEN detection voltage	VOPEN	0.12	0.20	0.28	V	VLED=SWEEP DOWN
SHORT detection voltage	VSHORT	5.7	6.0	6.3	V	VLED=SWEEPUP, VLSP=1.2V
SHORT MASK voltage	VSHTMASK	2.85	3.0	3.15	V	
VREF terminal input current	IVREF	-2	0	2	μA	VVREF=3V
LSP terminal input current	ILSP	-2	0	2	μA	VLSP=3V
【STB block】						
STB terminal HIGH voltage	STBH	2.0	-	VCC	V	
STB terminal LOW voltage	STBL	-0.3	-	0.8	V	
STB terminal Pull Down resistance	RSTB	0.5	1.0	1.5	MΩ	STB=3V
【PWM IN block】						
PWM terminal HIGH voltage	PWMH	2.0	-	20	V	
PWM terminal LOW voltage	PWML	-0.3	-	0.8	V	
PWM terminal Pull Down resistance	RPWM	200	300	400	kΩ	PWM=3V
【FAIL_MODE,FAIL_RST,SUMPWM block】						
Input terminal High voltage	VINH	2.0	-	20	V	
Input terminal Low voltage	VINL	-0.3	-	0.8	V	
Input terminal Pull Down resistance	RVIN	60	100	140	kΩ	VIN=3V
【FAIL block（OPEN DRAIN）】						
FAIL LOW output voltage	VOL	0.25	0.5	1.0	V	IOL=1mA

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●1.3 Pin Descriptions

No	Pin name	In/Out	Function	rating [V]
1	VCC	IN	Power source terminal	-0.3 to 36
2	FAIL	OUT	Abnormality detection output terminal (OPEN DRAIN)	-0.3 to 36
3	REG9V	OUT	9V regulator output terminal	-0.3 to 13
4	N.C.	-	Non connection terminal	-
5	N	OUT	DC/DC switching output terminal	-0.3 to 13
6	PGND	IN	Power GND terminal	-
7	CS	IN	DC/DC FET output current detection terminal	-0.3 to 7
8	OVP	IN	Overvoltage protection detection terminal	-0.3 to 7
9	M_DET	OUT	LED Diode OR output terminal	-0.3 to 13
10	AGND	IN	GND terminal for analog part	-
11	LED1	OUT	LED output 1	-0.3 to 50
12	LED2	OUT	LED output 2	-0.3 to 50
13	LED3	OUT	LED output 3	-0.3 to 50
14	LED4	OUT	LED output 4	-0.3 to 50
15	LED5	OUT	LED output 5	-0.3 to 50
16	LED6	OUT	LED output 6	-0.3 to 50
17	STB	IN	Standby control terminal	-0.3 to 36
18	PWM1	IN	PWM dimming input signal terminal for LED 1	-0.3 to 22
19	PWM2	IN	PWM dimming input signal terminal for LED 2	-0.3 to 22
20	PWM3	IN	PWM dimming input signal terminal for LED 3	-0.3 to 22
21	PWM4	IN	PWM dimming input signal terminal for LED 4	-0.3 to 22
22	PWM5	IN	PWM dimming input signal terminal for LED 5	-0.3 to 22
23	PWM6	IN	PWM dimming input signal terminal for LED 6	-0.3 to 22
24	FAIL_RST	IN	FAIL output reset terminal	-0.3 to 22
25	S6	IN	Connecting terminal for LED 6 constant current setting resistor	-0.3 to 7
26	S5	IN	Connecting terminal for LED 5 constant current setting resistor	-0.3 to 7
27	S4	IN	Connecting terminal for LED 4 constant current setting resistor	-0.3 to 7
28	S3	IN	Connecting terminal for LED 3 constant current setting resistor	-0.3 to 7
29	S2	IN	Connecting terminal for LED 2 constant current setting resistor	-0.3 to 7
30	S1	IN	Connecting terminal for LED 1 constant current setting resistor	-0.3 to 7
31	CP	OUT	Connecting terminal for non-reaction time setting capacitor	-0.3 to 7
32	SS	OUT	Connecting terminal for soft-start time setting capacitor	-0.3 to 7
33	FB	OUT	Error amplifier output terminal	-0.3 to 7
34	RT	OUT	Connecting terminal for DC/DC frequency setting resistor	-0.3 to 7
35	VREF	IN	Analog dimming DC voltage input terminal	-0.3 to 7
36	LED_LV	IN	LED control voltage set terminal	-0.3 to 7
37	LSP	IN	LED SHORT detection voltage setting terminal	-0.3 to 7
38	FAIL_MODE	IN	FAIL function change terminal	-0.3 to 7
39	UVLO	IN	Low voltage malfunction prevention detection terminal	-0.3 to 10.5
40	AGND	IN	GND terminal for analog part	-

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●1.4.1 I/O equivalence circuit

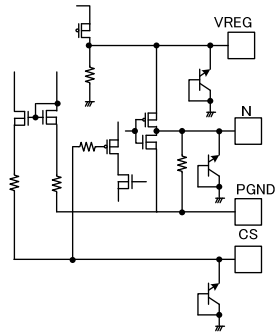
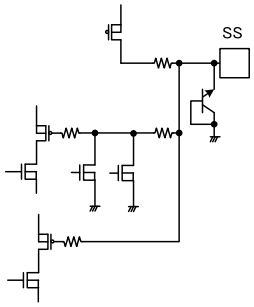
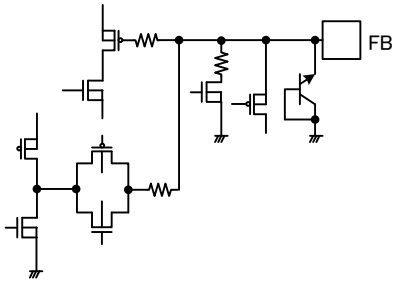
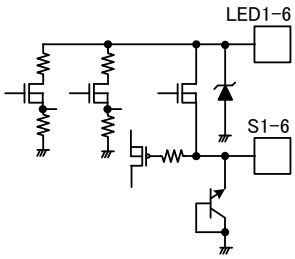
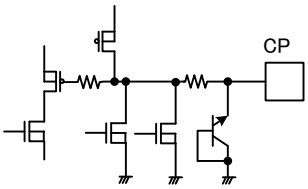
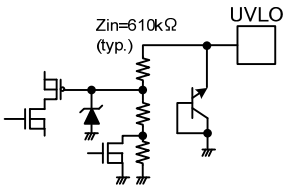
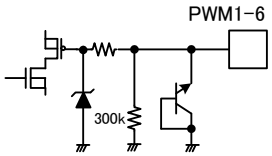
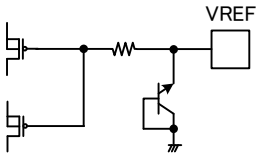
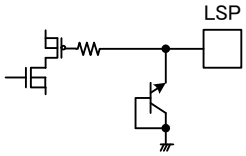
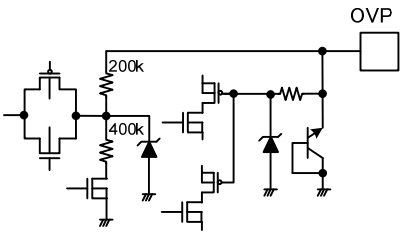
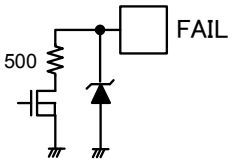
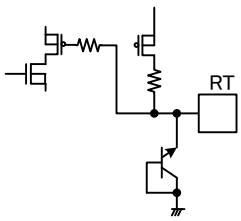
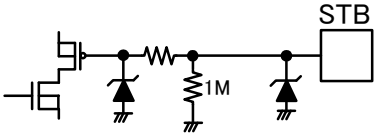
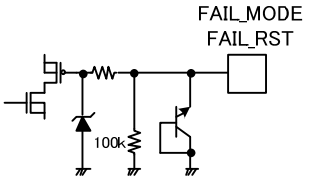
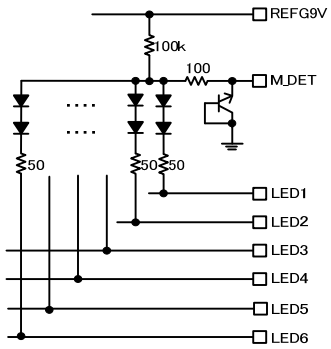
REG9V / N / PGND / CS	SS	FB
		
LED1 to LED6, S1 to S6	**CP**	**UVLO**
		
PWM1 to PWM6	**VREF**	**LSP,LED_LV**
		
OVP	**FAIL**	**RT**
		
STB	**FAIL_MODE / FAIL_RST**	**M_DET**
		

Figure 5. I/O equivalence circuit

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●1.5Typical Performance Curves（reference data）

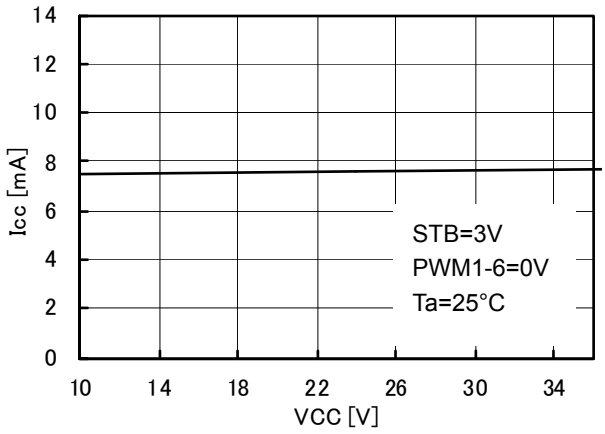


Figure 6. Circuit current

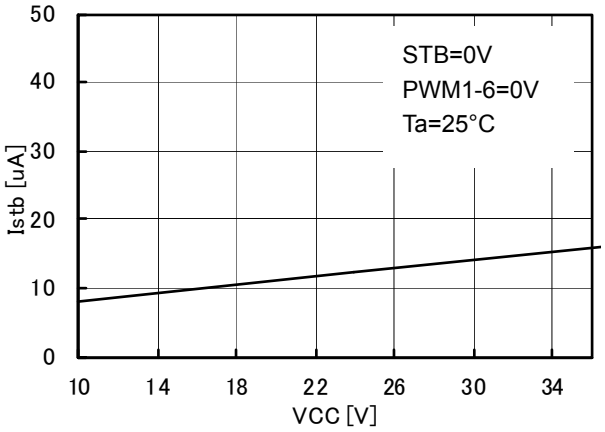


Figure 7. Stand-by circuit current

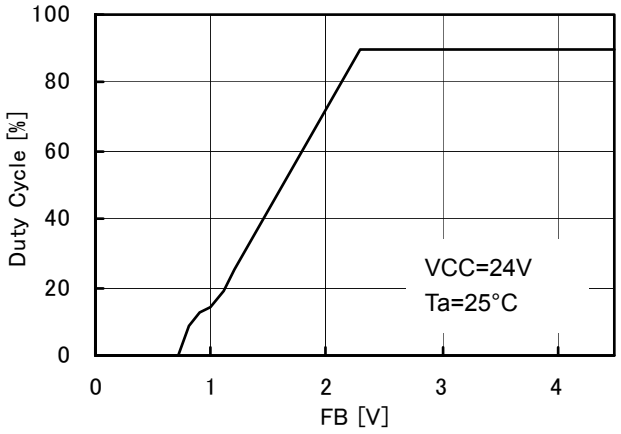


Figure 8. FB v.s. Duty Cycle

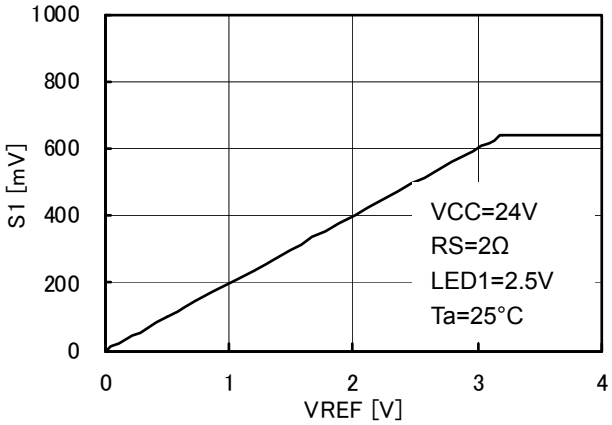


Figure 9. VREF v.s. Sx

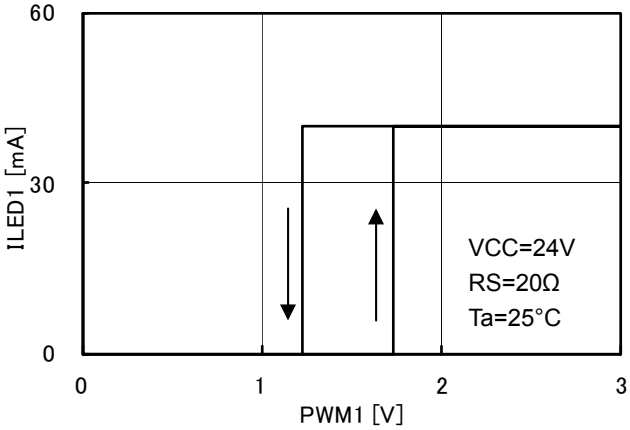


Figure 10. PWM terminal threshold voltage

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●2 Block Diagram

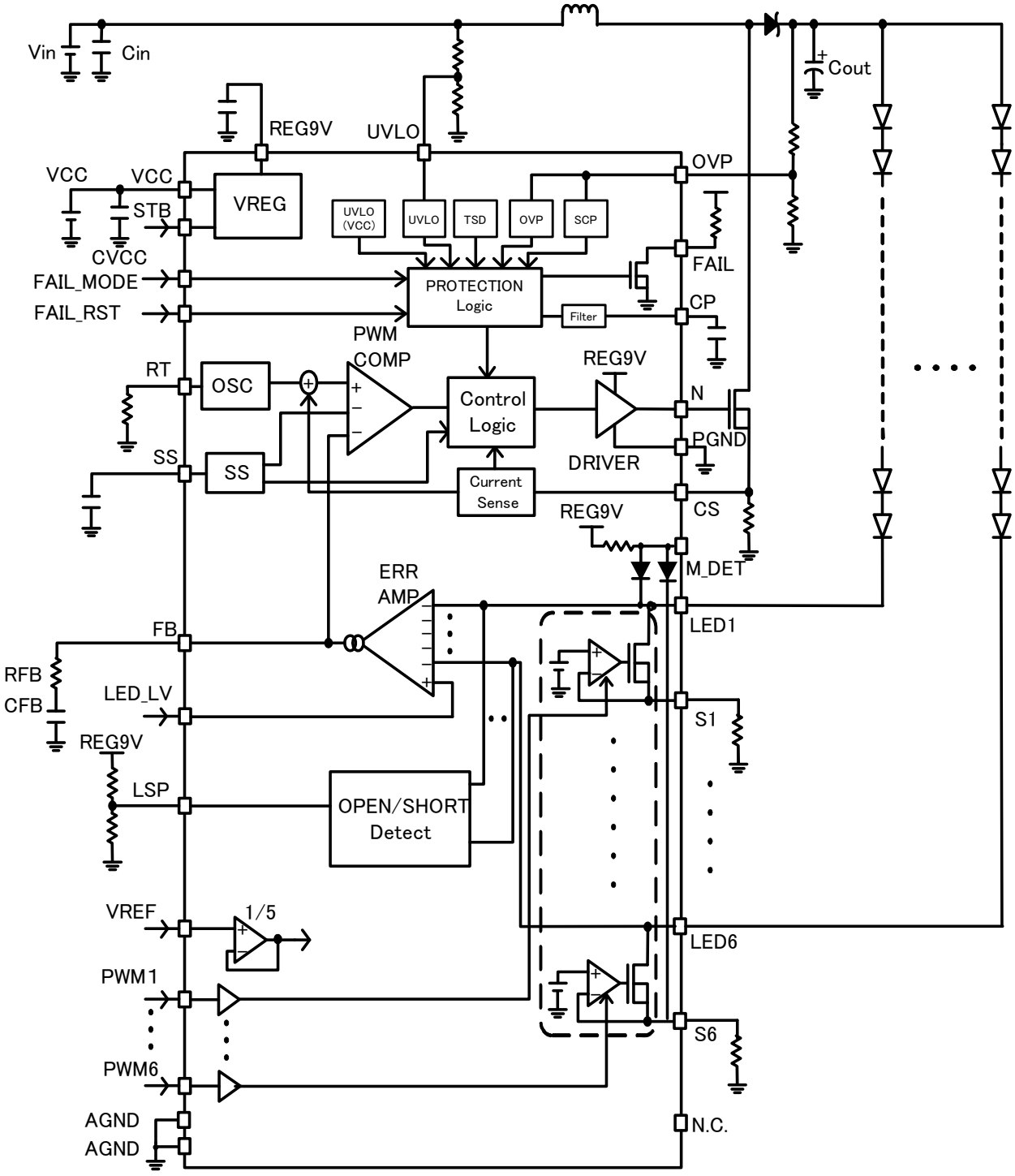


Figure 11. Block Diagram

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●3.1 Pin Configuration

1 pin. VCC

Power supply terminal of IC. The input range is 9 to 35V.
The operation starts over VCC＝7.5V(typ.) and the system stops under VCC=7.2V(typ.).

2 pin. FAIL

FAIL signal output terminal (NMOS open-drain). NMOS is OPEN at the normal operation so FAIL pin is Hi-Z. NMOS becomes ON state (500 ohm typ.) at the abnormal detection. It is possible to select the FAIL type from latch type (FAIL_MODE=L) or one shot pulse (FAIL_MODE=H).Please refer to the detail explanation＜38pin. FAIL_MODE terminal＞

3 pin. REG9V

REG9V is a 9 V output pin used delivering 20mA at maximum for switching power supply of N terminal.
Use at a current higher than 20mA may affect the reference voltage within IC, which may result in malfunction. It will also cause heating of IC itself. Therefore it is recommended to set the load as small as possible.
The characteristic of VCC line regulation at REG9V is shown as figure. VCC must be used in more than 10.5V for stable 9V output.
Install an oscillation prevention ceramic capacitor (2.2 to 10μF) nearest to VREG between VREG-AGND terminals.

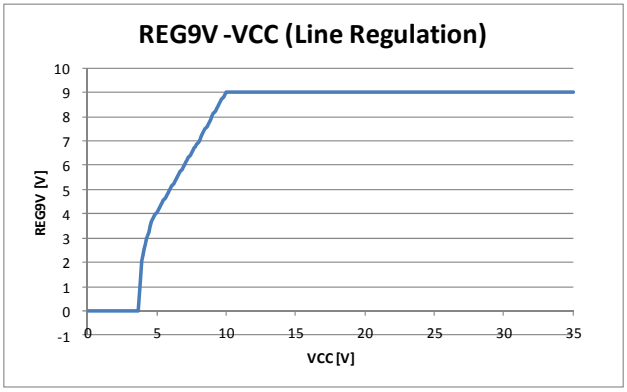


Figure 12.

4 pin. N.C

Non connect pin. Please set it the open state or deal with connecting the GND.

5 pin. N

Gate driving output pin of external NMOS of DC/DC converter with 0 to 9V (REG9V) swing. Output resistance of High side is 2.5 ohm(typ.), Low side is 3.0 ohm(typ.) in ON state. The oscillation frequency is set by a resistance connected to RT pin. For details, see the explanation of <34pin. RT terminal>.

6pin. PGND

Power GND terminal of output terminal, N driver:

7pin. CS

Inductor current detection resistor connecting terminal of DC/DC current mode: it transforms the current flowing through the inductor into voltage by sense resistor R_{CS} connected to CS terminal, and this voltage is compared with that set in the error amplifier by current detection comparator to control DC/DC output voltage. RCS also performs over current protection (OCP) and stops switching action when the voltage of CS terminal is 0.45 V (typ.) or higher (Pulse by Pulse).

8 pin. OVP

OVP terminal is the detection terminal of overvoltage protection (OVP) and short circuit protection (SCP) for DC/DC output voltage. Depending on the setting of the FAIL_MODE terminal, FAIL and CP terminal behave differently when an abnormality is detected. For details, see the table for each protection operation is described in ●3.2 and ●3.3.
During the soft start (SS), there is a function which returns the OVP voltage to error amplifier to boost DC/DC output voltage at all Low PWM (OVPFB function). After completion of SS, this function is disabled.

9 pin. M_DET

The Di OR output terminal of LED 1 to 6. The output is the voltage which is added a diode forward voltage(two diode stack) to the lowest voltage among 6 LED terminals.

10pin. AGND

Analog GND for IC

11 to 16pin. LED1 to LED6

LED constant current driver output terminal. Setting of LED current value is adjustable by setting the VREF voltage and connecting a resistor to S terminal. For details, see the explanation of <25 to 30pin. S1 to S6, 35pin. VREF >.
The PWM dimming frequency of LED current driver and upper/lower limit of the duty need to be set in a manner that necessary linearity of PWM dimming characteristics can be secured referring to the following figures:

Start/Stop time of constant current driver (PWM pulse response)
Start-up time depends on the VREF value; the response becomes quick, so that voltage is high.
In the way of reference, the current response upon application of current rise rate and pulse PWM1us (current pulse) to describe the dependence of VREF. It needs to be adequately verified with an actual device because the response rate may vary with application conditions.

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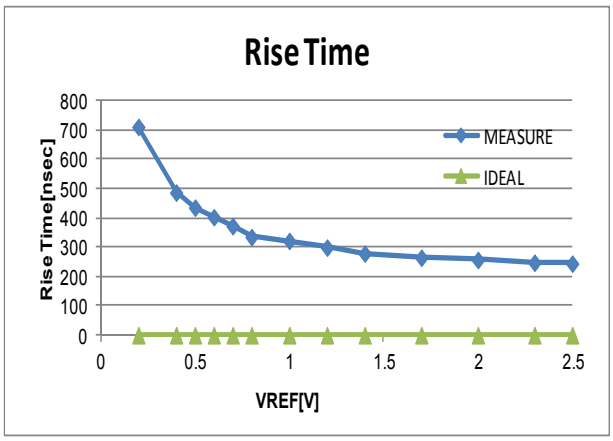


Figure 13.

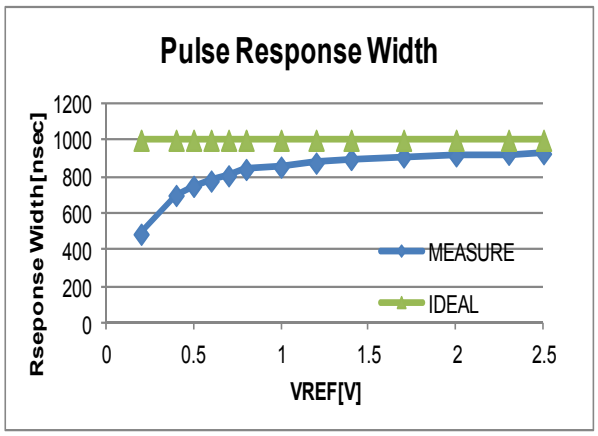


Figure 14.

17pin. STB

ON/OFF setting terminal for IC, which can be used perform a reset at shutdown.

* The voltage of STB input in the sequence of VCC → STB.
* Voltage input in STB terminal switches the state of IC (IC ON/OFF). Using the terminal between the 2 states (0.8 to 2.0 V) needs to be avoided.

18 to 23pin. PWM1 to PWM6

ON/OFF terminal of LED driver: it inputs PWM dimming signal directly to PWM terminal and change of DUTY enables dimming. High/Low level of PWM terminal is shown as follows:

State	PWM voltage
LED ON	PWM= 2.0 to 20V
LED OFF	PWM= -0.3 to 0.8V

24pin.FAIL_RST

Reset terminal of the protection circuit and FAIL terminal:
Return the latch stopped protection block by setting the FAIL_RST to High. During High state, operation is masked by the latch system protection.

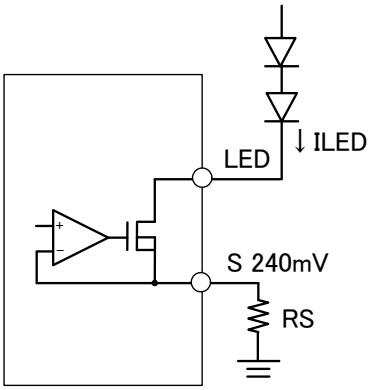
25 to 30pin. S1 to S6, 35pin. VREF

S terminal is a connecting terminal for LED constant current setting resistor, output current ILED is in an inverse relationship to the resistance value.
VREF terminal is a terminal for analog dimming; output current ILED is in a proportional relationship to the voltage value to be input.
VREF terminal is assumed that it is set by dividing the resistance with a high degree of accuracy, VREF terminal inside the IC is in open state (High Impedance). It is necessary to input voltage to divide the resistance from the output of REG9V or use external power source. Using the terminal in open state needs to be avoided.
The relationship among output current ILED, VREF input voltage, and RS resistance has the following equation:

$$I_{LED} = \frac{VREF[\mathrm{V}]}{\mathrm{RS}[\Omega]} \times 0.2[\mathrm{A}]$$

The voltage of S terminal is following equation:

$$\mathrm{VS} = 0.2 \times VREF[V]$$



VREF=1.2V, RS=2 [Ω]
ILED=120[mA]

Figure 15.

*Attention: Rises LED current accelerate heat generation of IC. Adequate consideration needs to be taken to thermal design in use.

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* For the adjustment of LED current with analog dimming by VREF, note that the output voltage of the DC/DC converter largely changes accompanied by LED VF changes if the VREF voltage is changed rapidly. In particularly, when the VREF voltages become high to low, it makes the LED terminal voltage seem higher transiently, which may influence application such as activation of the LED short circuit protection. It needs to be adequately verified with an actual device when analog dimming is used.

31pin. CP

Terminal which sets the time from detection of abnormality until shutdown (Timer latch). When the LED short protection, LED open protection or SCP is detected, it perform s constant current charge of 1.0uA (typ.) to external capacitor. When the CP terminal voltage reaches 2.0V (typ.), the IC is latched and FAIL terminal operates (at FAIL_MODE = L).

32pin. SS

Terminal which sets soft-start time of DC/DC converter: it performs constant current charge of 1.0uA to the external capacitor connected with SS terminal, which enables soft-start of DC/DC converter.
Since the LED protection function (OPEN/SHORT detection) works when the SS terminal voltage reaches 3.0 V (typ.) or higher, it must be set to bring stability to conditions such as DC/DC output voltage and LED constant current drive operation, etc. before the voltage of 3.0 V is detected.

33pin. FB

Output terminal of the error amplifier of DC/DC converter which controls current mode:
The voltage of LED terminal which is the highest VF voltage among 6 LED strings and the voltage of LED_LV terminal become input of the error amplifier. The DC/DC output voltage is kept constant to control the duty of the output N terminal by adjusting the FB voltage.
The voltage of other LED terminals is, as a result, higher by the variation of Vf. Phase compensation setting is separately described in ●3.7 How to set phase compensation.

A resistor and a capacitor need to be connected in series nearest to the terminal between FB and AGND.
The state in which all PWM signals are in LOW state brings high Impedance, keeping FB voltage. This action removes the time of charge to the specified voltage, which results in speed-up in DC/DC conversion.

34pin. RT

RT sets charge/discharge current determining frequency inside IC.
Only a resistor connected to RT determines the drive frequency inside IC, the relationship has the following equation: FCT is 500 kHz at RT= 30 kohm.

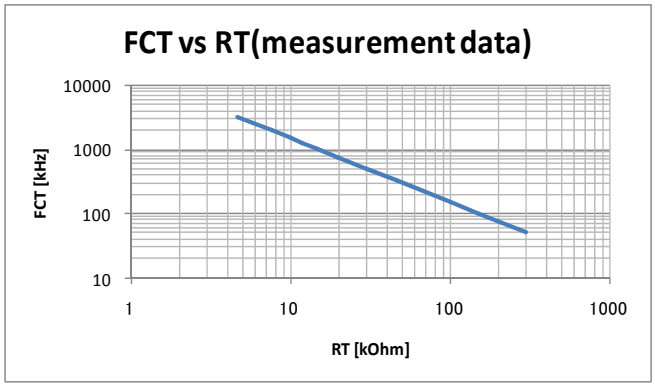


Figure 16.

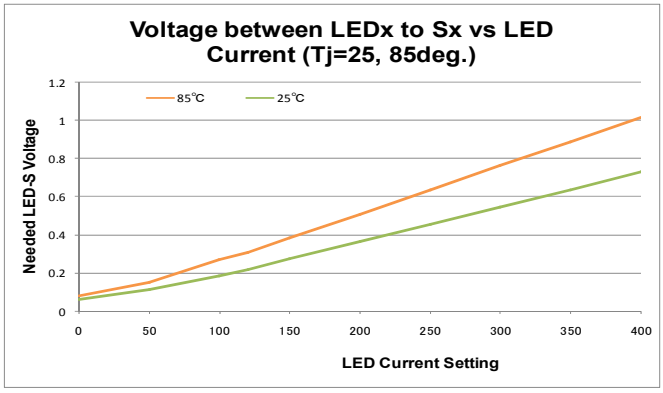


Figure 17.

36pin. LED_LV

LED_LV terminal sets the reference voltage error amplifier. LED_LV terminal is assumed that it is set by dividing the resistance with a high degree of accuracy, LED_LV terminal inside the IC is in open state (High Impedance). It is necessary to input voltage to divide the resistance from the output of REG9V or use external power source. Using the terminal in open state needs to be avoided.
According to output current, lowering LED_LV voltage can reduce the loss and heat generation inside IC. However, it is necessary to ensure the voltage between drain and source of FET inside IC, so LED_LV voltage has restriction on the following equation.

VLED_LV ≧ (LED-S terminal voltage) + 0.2×VREF [V]

For example, at ILED = 100mA setting by VREF = 1V, from figure the voltage between LED and S terminal is required 0.27 V at Tj = 85°C, so LED_LV voltage must be at least a minimum 0.47V.

Note: Rises in VLED_LV voltage and LED current accelerate heat generation of IC. Adequate consideration needs to be taken to thermal design in use.
Note: LED_LV voltage is not allowed setting below 0.3V.
Note: LED current by raising LED_LV voltage can flow to MAX 400mA, use with care in the dissipation of the package.

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37pin. LSP

Terminal which sets LED SHORT detection voltage: The input impedance of LSP pin is High Impedance, because it is assumed that the input of LSP terminal is set by dividing the resistance with a high degree of accuracy.
The LSP terminal is assumed that it is set by dividing the resistance with a high degree of accuracy, LSP terminal inside the IC is in open state (High Impedance). It is necessary to input voltage to divide the resistance from the output of REG9V or use external power source. Using the terminal in open state needs to be avoided. Set LSP voltage in the range of 0.8V to 3.0V.

$$LED_{SHORT} = 5 \times VLSP \quad [V]$$

LED_{SHORT} : LSP detection Voltage, VLSP : LSP terminal voltage

The conditions there are restrictions on short LED detection. For details, see the explanation of section ●3.5.2 Setting the LED short detect voltage (LSP pin).

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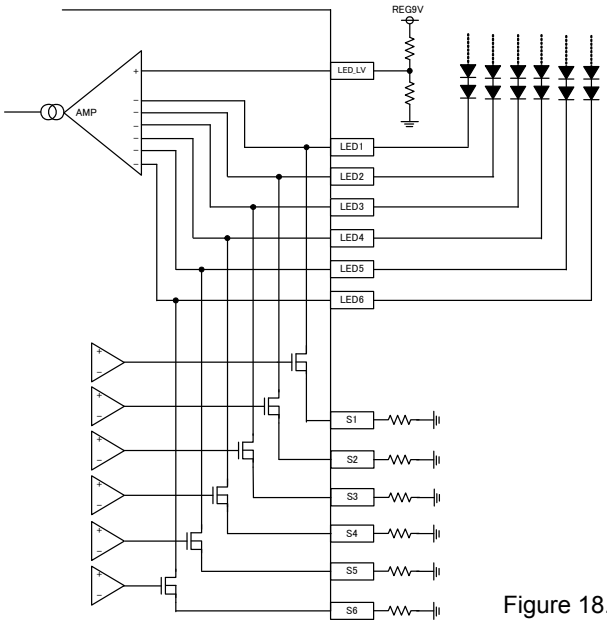


Figure 18.

38pin. FAIL_MODE

Output mode of FAIL can be change by FAIL_MODE terminal. When FAIL_MODE is in Low state, the output of FAIL terminal is the latch mode. FAIL terminal is latched after the CP charge time from detection of abnormal state. When FAIL_MODE is in High state, the output of FAIL terminal is one-shot-pulse mode. At detected abnormality, firstly FAIL is in Low state (Drain state). FAIL returns to High state (Open state) if abnormality is cleared after CP charge time, In this mode, there is no latch stop for protection operation in IC. Monitoring the FAIL with the Microcomputer, decide to stop working IC.
For FAIL_MODE = H when the detection sequence, see the explanation of section ●3.8.3 Protective operation sequence at FAIL_MODE=H. On application to change modes is prohibited.

39pin. UVLO

UVLO terminal of the power of step-up DC/DC converter: at 2.5 V (typ.) or higher, IC starts step-up operation and stops at 2.4V or lower (typ.). (It is not shutdown of IC.) UVLO can be used to perform a reset after latch stop of the protections.
The power of step-up DC/DC converter needs to be set detection level by dividing the resistance. If any problem on the application causes noise on UVLO terminal which results in unstable operation of DC/DC converter, a capacitance of approximately 1000 pF needs to be connected between UVLO and AGND terminals.

40pin. AGND

Analog GND for IC

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●3.2 Protection Operation at FAIL Latch output (FAILMODE=L)

●3.2.1 List of the Threshold Function terminal（typ. condition）

Please decide the resistance divider of the various protection detection using the following table.

Protection name	Detection Pin name	Detection condition	PWM	Release condition	Protection type
LED Open	**LEDx**	LEDx < 0.2V(4clk) SS>3V	High	LEDx > 0.2V(*1)	Stop the CH latch after the CP charge is completed.
LED short	**LEDx**	LEDx > 5×VLSP(4clk) SS>3V	High	LEDx < 5×VLSP(3clk)	Stop the CH latch after the CP charge is completed.
UVLO	**UVLO**	UVLO < 2.4V	—	UVLO > 2.5V	Stop the system
OVP	**OVP**	OVP > 2.43V	—	OVP < 2.4V	Stop the N output
SCP	**OVP**	OVP < 0.2V	—	OVP > 0.2V	Stop the N output. Stop the system after the CP charge is completed.
OCP	**CS**	CS > 0.45V	—	CS < 0.45V	Stop the N output under the detection.（Pulse by Pulse）

It is possible to reset with the FAIL_RST terminal to release the latch stop.

(*1) The release condition of OPEN protection is depend on its release timing.

No.	The timing of release of LEDx voltage (LEDx 0.2V)	The release condition
1	LED pin voltage is released during PWM=H.	LED pin voltage is normal range during 3clk(3 positive edge)
2	LED pin voltage is released during PWM=L.	As PWM=L, LED pin voltage do not exceed Short protection voltage (VLSP) during more than 3clk. or PWM positive edge is input when LED pin voltage do not exceed VLSP for more than 3clk.

●3.2.2 List of Protection function

Protection function	Action when protection function is detected			
	DC/DC converter	LED driver	Soft-start	FAIL terminal
STB	Stop	Stop	Discharge	OPEN
LED Open	Normal operation (Stop when all LED CH stop)	Stop after CP charge (Latch operation)	Normal operation	DRAIN after the CP charge is completed. (Latch operation)
LED short	Normal operation *1	Stop after CP charge (Latch operation)	Normal operation	DRAIN after the CP charge is completed. (Latch operation)
UVLO	Stop	Stop	Discharge	GND
OVP	Stop N output	Normal operation	Normal operation	OPEN
SCP	Stop N output	Stop after CP charge (Latch operation)	Discharge after latch	DRAIN after the CP charge is completed. (Latch operation)
OCP	Stop the N output (Pulse by Pulse)	Normal operation	Normal operation	OPEN

（*1）Short protection doesn't hang when becoming remainder 1ch. DCDC output falls as LED short.

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●3.3 Protection operation when the FAIL one shot outputs(FAILMODE=H)

●3.3.1 List of the threshold function terminal（typ. condition）

Please decide the resistance divider of the various protection detection using the following table.

Protection name	Detection Pin name	Detection condition	PWM	Release condition	Protection type
LED Open	LEDx	LEDx < 0.2V(4clk) SS>3V	High	LEDx > 0.2V(3clk)	FAIL drain state under the detection.
LED short	**LEDx**	LEDx > 5×VLSP(4clk) SS>3V	High	LEDx < 5×VLSP(3clk)	FAIL drain state under the detection.
UVLO	**UVLO**	UVLO < 2.4V	—	UVLO > 2.5V	Stop the system.
OVP	**OVP**	OVP > 2.43V	—	OVP < 2.4V	Stop the system FAIL drain state under the detection..
SCP	**OVP**	OVP < 0.79V	—	OVP > 0.79V	Stop the system. FAIL drain state under the detection..
OCP	**CS**	CS > 0.45V	—	CS < 0.45V	Stop the N output under the detection. （Pulse by Pulse）

●3.3.2 List of the protection function

Protection function	Action when protection function is detected			
	DC/DC converter	LED driver	Soft-start	FAIL terminal
STB	Stop	Stop	Discharge	OPEN
LED Open	Normal operation (Stop when the all CH stop)	Normal operation	Normal operation	DRAIN under the detection
LED short	Normal operation	Normal operation	Normal operation	DRAIN under the detection
UVLO	Stop	Stop	Discharge	DRAIN
OVP	Stop the N output	Normal operation	Normal operation	DRAIN
SCP	Stop the N output	Normal operation	Normal operation	DRAIN
OCP	Stop the N output (Pulse by Pulse)	Normal operation	Normal operation	OPEN

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●3.4 Setting of the external components.(typ. condition)

●3.4.1 Setting the LED current (VREF and Sx pin)

First, VREF pin voltage is determined. When performing Analog dimming, be careful of VREF pin input range (0.2 to 2.5V) and decide typical voltage.

In BD9397EFV, LED constant current is controlled by Sx terminal voltage as a reference point. Sx terminal is controlled to become one fifth of the voltage of VREF terminal voltage. In the case of VREF=1V, it is set to Sx=0.2V.

Therefore, when the resistance to Sx terminal versus GND is set to "RS", the relationship between RS, VREF and ILED is as follows

$$R_S\ [ohm] = \frac{V_{VREF}\ [V]}{I_{LED}\ [A] \times 5}$$

●3.4.2 Setting the LED short detect voltage (LSP pin)

The voltage of LED short detection can be arbitrarily set up with LSP pin voltage.

LSP pin cannot be used by OPEN because of High Impedance. Please be sure to applied voltage from the exterior. About LED short detection voltage, if "VLEDshort" and LSP pin voltage are set to "VLSP", it is as follows.

$$V_{LSP}\ [V] = \frac{VLED_{short}\ [V]}{5}$$

Since the setting range of a LSP pin is set to 0.8V to 3.0V, VLEDshort can be set up in 4Vto15V.

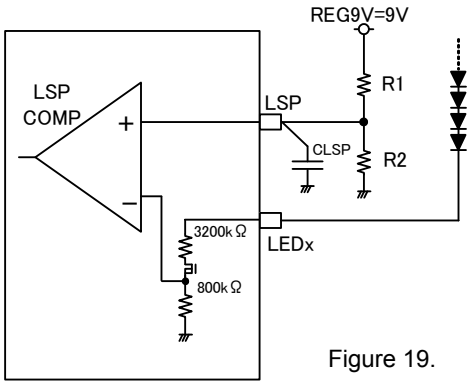


Figure 19.

○Equation of setting LSP detect Voltage

When the detection voltage VLSP of LSP is set up by resistance division of R1 and R2 using REG9V, it becomes like the following formula.

$$VLED_{short} = \left(REG9V \times \frac{R2}{R1 + R2} \right) \times 5 \quad [V]$$

*Also including the variation in IC, please also take the part variation in a set into consideration for an actual constant setup, and inquire enough to it.

●3.4.3 Timer latch time(CP pin)

When various abnormalities are detected, the source current of 1.0uA is first flowed from CP pin.

BD9397EFV don't stop by latch, unless abnormal state is continues and CP pin voltage reaches continues 2V.

With the capacity linked to CP pin, the unresponded time from detection to a latch stop. The relationship between the unresponded time "Tcp" and CP pin connection capacitor "Ccp" is as follows.

$$C_{CP}\ [F] = \frac{T_{CP}\ [S] \times 1.0 \times 10^{-6} [A]}{2.0\ [V]}$$

●3.4.4 Setting the soft-start time (SS pin)

The starting time of a DCDC output is dependent on SS pin connection capacity.

Moreover, although SS pin is charged by source current of 1uA, IC does not perform LED protection as under DCDC starting state until SS pin voltage arrive to 3.0V.

(The soft starting time set up here should be the mask time of a under [starting], and please keep in mind that it differs from time until a DCDC output is stabilized.)

Time until a DCDC output is stabilized is greatly dependent on a ratio of step-up or load.

The relationship between soft starting time "TSS" and SS pin connection capacity "CSS" is as follows.

$$C_{SS}\ [F] = \frac{T_{SS}\ [S] \times 1.0 \times 10^{-6} [A]}{3.0\ [V]}$$

●3.4.5 DCDC operation frequency (RT pin)

The oscillation frequency of the DCDC output is decided by RT resistance.

BD9397EFV is designed to become a 500-kHz setup at the time of 30kohm.

RT resistance and frequency have a relation of an inverse proportion, and become settled as the following formula.

$$R_{RT} = \frac{1.5 \times 10^{10}}{f_{SW}} [\Omega]$$

f_{sw} =DCDC convertor oscillation frequency [Hz]

Please connect RT resistance close as much as possible from RT pin and an AGND pin.

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●3.4.6 Maximum DCDC output voltage(Vout ,Max)

The DCDC output maximum voltage is restricted by Max Duty of N output.
Moreover, the voltage needed in order that Vf may modulate by LED current also with the same number of LEDs.
Vf becomes high, so that there is generally much current.
When you have grasped the variation factor of everythings, such as variation in a DCDC input voltage range, the variation and temperature characteristics of LED load, and external parts, please carry out a margin setup.

●3.4.7 Setting the OVP

In BD9397EFV, when over voltage in VOUT line is detected, the instant stop of the N pin output is carried out, and voltage rise operation is stopped. But the latch stop by CP charge is not performed. If VOUT drops by naturally discharge, it is less than the hysteresis voltage of OVP detection and the oscillation condition is fulfilled, N output will be resumed again.

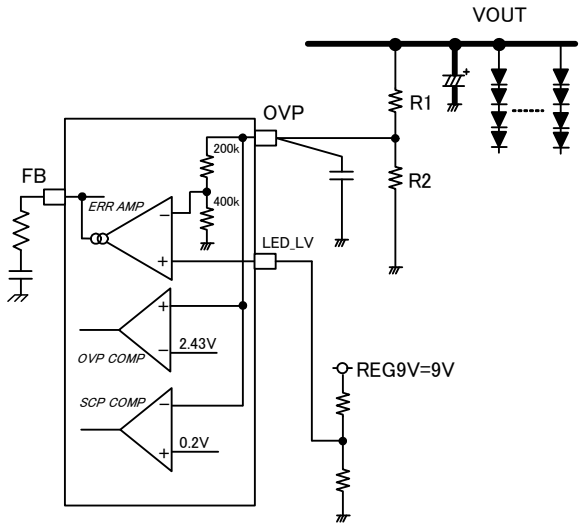


Figure 20.

○Equation of setting OVP detect

$$VOVP = 2.43 \times \frac{R1+R2}{R2} \quad [V]$$

N pin output is suspended at the time of SCP detection, it stops step-up operation, and the latch protection by CP timer.

○Equation of setting SCP detect

$$VSCP = 0.2 \times \frac{R1+R2}{R2} \quad [V]$$

Moreover, there is an OVPFB function which returns OVP voltage and controls error amplifier so that output voltage may be raised, even when there is no PWM signal during a soft start.

○The VOUT setting formula by OVPFB in Soft Start

$$VOUT = \left(\frac{3}{2} \frac{R1+R2}{R2} + \frac{R1}{400} \right) \times V_{LED_LV} \quad [V]$$

●3.4.8 FAIL Logic

FAIL signal output pin (OPEN DRAIN); when an abnormality is detected, NMOS is brought into GND Level.
The rating of this pin is 36V.

State	FAIL output
In normal state, In STB	OPEN
In completion of an abnormality, when the UVLO is detected(after CP latch)	GND Level (500ohm typ.)

●3.4.9 How to set the UVLO

UVLO pin detect the power supply voltage: Vin for step-up DC/DC converters. Operation starts operation on more than 2.5V (typ.) and Operation stops on less than 2.4V (typ.) .
Since internal impedance exists in UVLO pin, cautions are needed for selection of resistance for resistance division.
A Vin voltage level to make it detecting becomes settled like the following formula by resistance division of R1 and R2 (unit: kΩ).

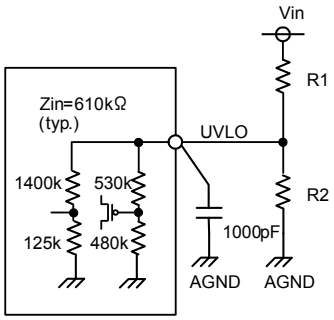


Figure 21.

○Equation of setting UVLO release

$$Vin_{DET} = 2.5 \times \left\{ \frac{R1+R2}{R2} + \left(\frac{1}{1400k+125k} + \frac{1}{530k+480k} \right) \times R1 \right\} \quad [V]$$

○ Equation of setting UVLO lock

$$Vin_{lock} = 2.4 \times \left\{ \frac{R1+R2}{R2} + \left(\frac{1}{1400k+125k} + \frac{1}{530k+480k+40k} \right) \times R1 \right\} \quad [V]$$

*Also including the variation in IC, please also take the part variation in a set into consideration for an actual constant setup, and inquire enough to it.

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●3.4.10 Setting of the LED_LV voltage (LED_LV pin)

LED_LV pin is in the OPEN (High Impedance) state.
Please be sure to use an external seal of approval, carrying out by inputting REG9V output by resistance division. It cannot use in the state of OPEN.

○Equation of Setting LED_LV voltage

When LED_LV voltage is set up by resistance division of R1 and R2 using REG9V, it becomes like the following formula.

$$V_{LED_LV} = REG9V \times \frac{R2}{R1+R2}[V]$$

*Also including the variation in IC, please also take the part variation in a set into consideration for an actual constant setup, and inquire enough to it.

●3.5 Selecting of DCDC part

Selecting inductor L

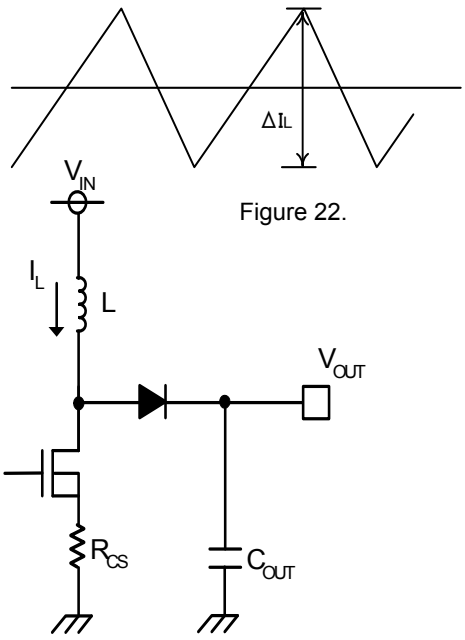


Figure 22.

Figure 23.

The value of inductor has a great influence on input ripple current. As shown in Equation (1), as the inductor becomes large and switching frequency becomes high, the ripple current of an inductor ⊿IL becomes low.

$$\Delta IL = \frac{(V_{OUT} - V_{IN}) \times V_{IN}}{L \times V_{OUT} \times f_{SW}}[A] \quad \cdots\cdots \quad (1)$$

When the efficiency is expressed by Equation (2), input peak current will be given by Equation (3).

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \quad \cdots\cdots \quad (2)$$

$$IL_{MAX} = I_{IN} + \frac{\Delta IL}{2} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} + \frac{\Delta IL}{2} \quad \cdots\cdots \quad (3)$$

Here,

L: reactance value [H] V_{OUT}: DC/DC output voltage [V]

V_{IN}: input voltage [V]

I_{OUT}: output load current (total of LED current) [A]

I_{IN}: input current [A] F_{SW}: oscillation frequency [Hz]

Generally, ⊿IL is set at around 30 to 50 % of output load current.

* Current exceeding the rated current value of inductor flown through the coil causes magnetic saturation, resulting in decrease in efficiency. Inductor needs to be selected to have such adequate margin that peak current does not exceed the rated current value of the inductor.
* To reduce inductor loss and improve efficiency, inductor with low resistance components (DCR, ACR) needs to be selected.

Selecting output capacitor C_{OUT}

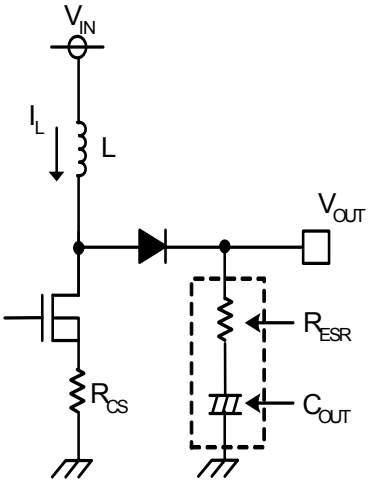


Figure 24.

Output capacitor needs to be selected in consideration of equivalent series resistance required to even the stable area of output voltage or ripple voltage. Be aware that set LED current may not be flown due to decrease in LED terminal voltage if output ripple voltage is high.

Output ripple voltage ⊿V_{OUT} is determined by Equation (4):

$$\Delta V_{OUT} = ILMAX \times R_{ESR} + \frac{1}{C_{OUT}} \times \frac{I_{OUT}}{\eta} \times \frac{1}{f_{SW}}[V] \quad \cdots\cdots \quad (4)$$

R_{ESR}: equivalent series resistance of C_{OUT}

* Rating of capacitor needs to be selected to have adequate margin against output voltage.
* To use an electrolytic capacitor, adequate margin against allowable current is also necessary. Be aware that current larger than set value flows transitionally in case that LED is provided with PWM dimming especially.

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Selecting switching MOSFET

Though there is no problem if the absolute maximum rating is the rated current of L or (withstand voltage of C_{OUT} + rectifying diode) VF or higher, one with small gate capacitance (injected charge) needs to be selected to achieve high-speed switching.

* One with over current protection setting or higher is recommended.
* Selection of one with small ON resistance results in high efficiency.

Selecting rectifying diode

A schottky barrier diode which has current ability higher than the rated current of L, reverse voltage larger than withstand voltage of C_{OUT}, and low forward voltage VF especially needs to be selected.

Selecting MOSFET for load switch and its soft-start

As a normal step-up DC/DC converter does not have a switch on the path from V_{IN} to V_{OUT}, output voltage is generated even though IC is OFF. To keep output voltage at 0 V until IC works, PMOSFET for load switch needs to be inserted between V_{IN} and the inductor. FAIL terminal needs to be used to drive the load switch. PMOSFET for the load switch of which gate-source withstand voltage and drain-source withstand voltage are both higher than V_{IN} needs to be selected.
To provide soft-start for the load switch, a capacitor must be inserted among gates and sources.

●3.6 How to set phase compensation

DC/DC converter application controlling current mode has each one pole (phase lag) f_p due to CR filter composed of output capacitor and output resistance (= LED current) and ZERO (phase lead) f_Z by output capacitor and ESR of the capacitor. Moreover, step-up DC/DC converter has RHP ZERO f_{ZRHP} as another ZERO. Since RHP ZERO has a characteristic of phase lag (-90°) as pole does, cross-over frequency f_c needs to be set at RHP ZERO or lower.

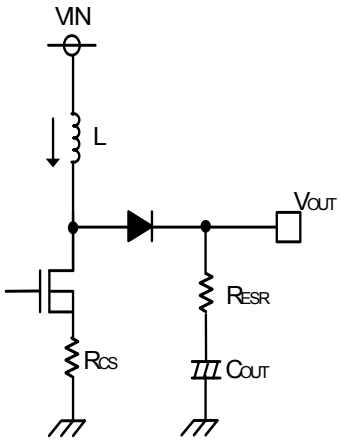


Figure 25. Output part

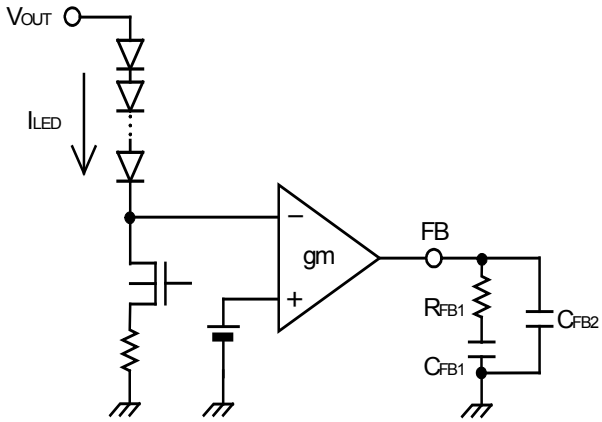


Figure 26. Error Amplifier

i. Determine Pole f_p and RHPZERO f_{ZRHP} of DC/DC converter:

$$f_p = \frac{I_{LED}}{2\pi \times V_{OUT} \times C_{OUT}} [Hz] \qquad f_{ZRHP} = \frac{V_{OUT} \times (1-D)^2}{2\pi \times L \times I_{LED}} [Hz]$$

Here,、 I_{LED}==sum of LED current, $D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$

ii. Determine Phase compensation to be inserted into error amplifier (with f_c set at 1/5 of f_{ZRHP})

$$R_{FB1} = \frac{f_{RHZP} \times R_{CS} \times I_{LED}}{5 \times f_p \times gm \times V_{OUT} \times (1-D)} [\Omega] \qquad C_{FB1} = \frac{1}{2\pi \times R_{FB1} \times f_p} [F]$$

Here,

$$gm = 1.036 \times 10^{-3} [S]$$

iii. Determine ZERO to compensate ESR (R_{ESR}) of C_{OUT} (electrolytic capacitor)

$$C_{FB2} = \frac{R_{ESR} \times C_{OUT}}{R_{FB1}} [F]$$

* When a ceramic capacitor (with R_{ESR} of the order of millimeters) is used to C_{OUT}, too, operation is stabilized by insertion of R_{ESR} and C_{FB2}.

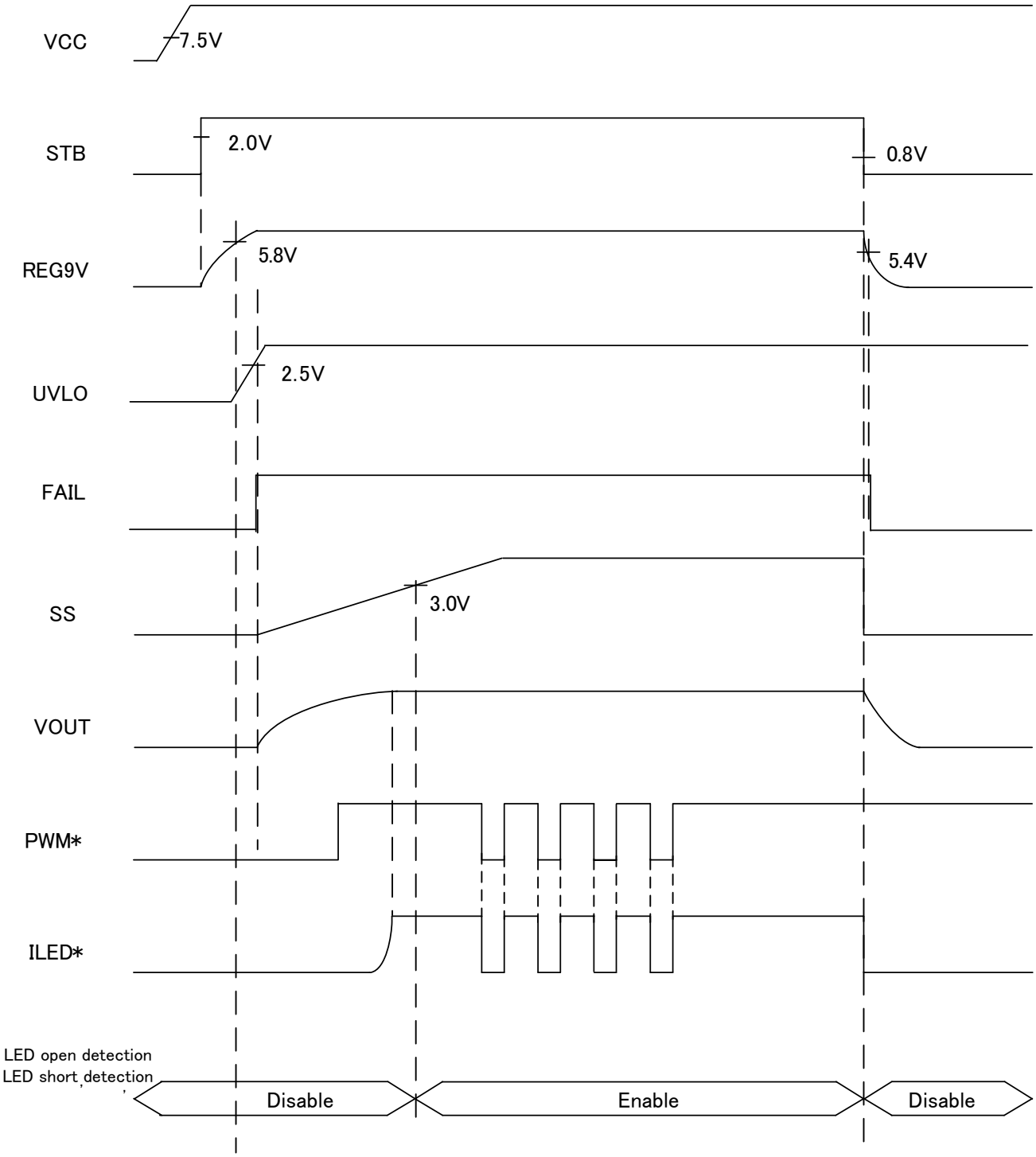
Though increase in R_{FB1} and decrease in C_{FB1} are necessary to improve transient response, it needs to be adequately verified with an actual device in consideration of variation between external parts since phase margin is decreased.

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●3.7 Timing chart

●3.7.1 Normal operation sequence



・ILED* current is independent controlled by each PWM* pin.

・FAIL pin is pulled up.

Figure 27.

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●3.8.2 Protective operation state transition table at FAIL_MODE=L

(Open detection)

before CP charge		→	CP charge		→	CP=2V arrival		end of state
PWM	Error state		PWM	Error state		PWM	Error state	
L(no pulse) or pulse less than 4cnt.	don't care	discharge	-	-		-	-	normal state
pulse over 4cnt.	Not detect	discharge	-	-		-	-	normal state
	detect	start charge	L(no pulse)	Not detect	discharge	-	-	normal state
				detect	charge	L(no pulse)	Not detect	normal state
							detect	**CH latch FAIL latch**
						H(input pulse)	Not detect	normal state
							detect	**CH latch FAIL latch**
			H(input pulse)	Not detect	discharge	-	-	normal state
				detect	charge	L(no pulse)	Not detect	normal state
							detect	**CH latch FAIL latch**
						H(input pulse)	Not detect	normal state
							detect	**CH latch FAIL latch**

(Short detection)

before CP charge		→	CP charge		→	CP=2V arrival		end of state
PWM	Error state		PWM	Error state		PWM	Error state	
L(no pulse) or puse less than 4cnt.	don't care	discharge	-	-		-	-	normal state
pulse over 4cnt.	Not detect	discharge	-	-		-	-	normal state
	detect	start charge	L(no pulse)	don't care	charge	L(no pulse)	don't care	**CH latch FAIL latch**
						H(input pulse)	Not deetect	normal state
							detect	**CH latch** FAIL latch
			H(input pulse)	Not detect	discharge	-	-	normal state
				detect	charge	L(no pulse)	don't care	**CH latch** FAIL latch
						H(input pulse)	Not deetect	normal state
							detect	**CH latch** FAIL latch

With "the pulse of less than 4 cnt", it is defined as the pulse width from (100n)sec to (Hi time of less than 4 cnt of DCDC frequency). In the pulse below (100n)sec, since delay from a PWM pin input to internal logic exists, it becomes unfixed.

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●3.7.3 Protective operation sequence at FAIL_MODE=H

・**Basic sequence**

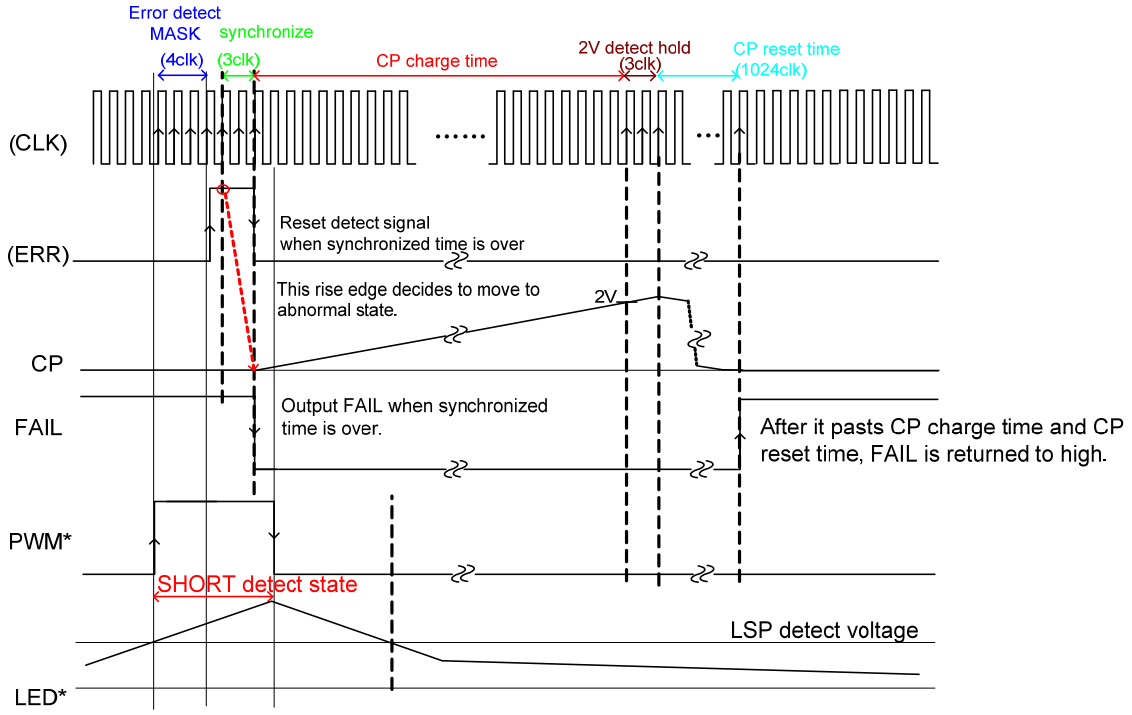


Figure 28.

・**Actual sequence**

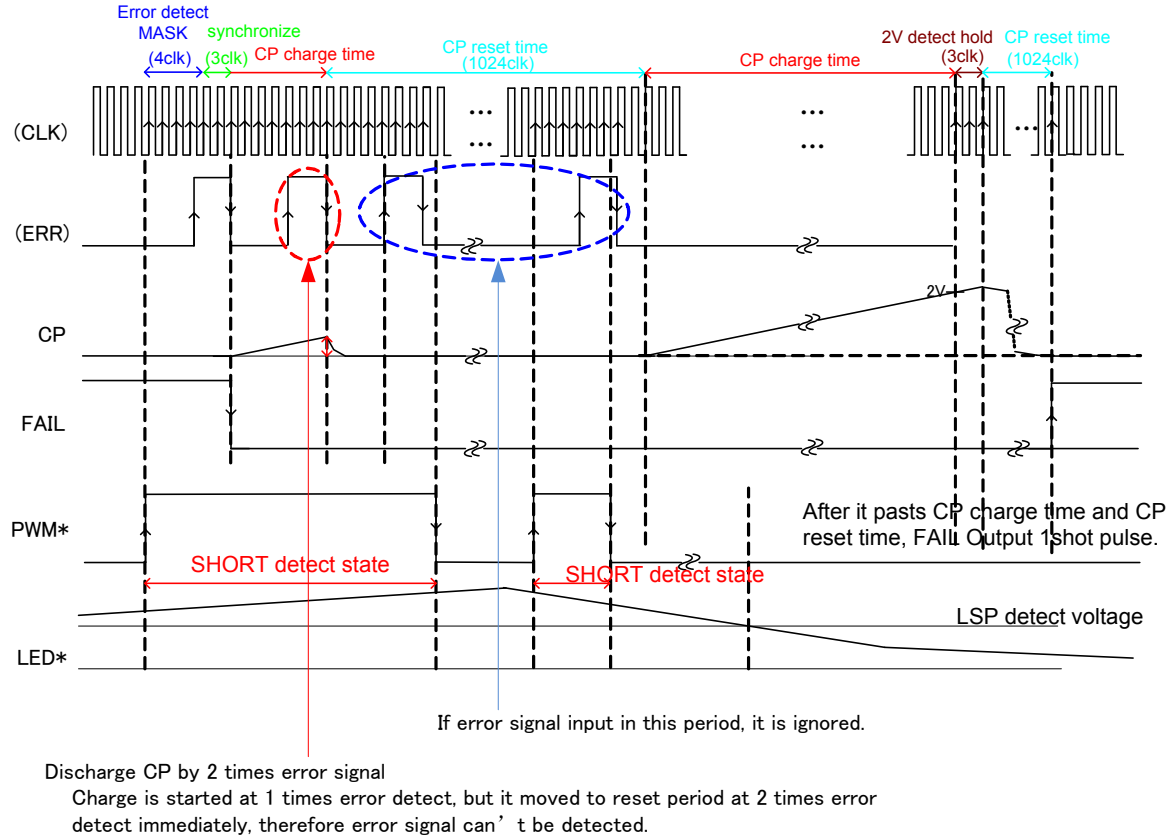


Figure 29.

The above chart is sample of SHORT detection, but the chart of OPEN detection is also same structure.

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●3.7.4 About LED SHORT detection

LED SHORT detection don't work by individual ch. The followings are needed for detection.

- Detection channel is PWM=H and LED terminal voltage is over LED SHORT detection threshold voltage.
- Except for detection ch, any 1ch is PWM=H and LED terminal voltage is under 3V.
- The above-mentioned 2 states continue over 4clk of DCDC oscillation frequency.

Detection sequence is the followings.(omit 4clk mask)

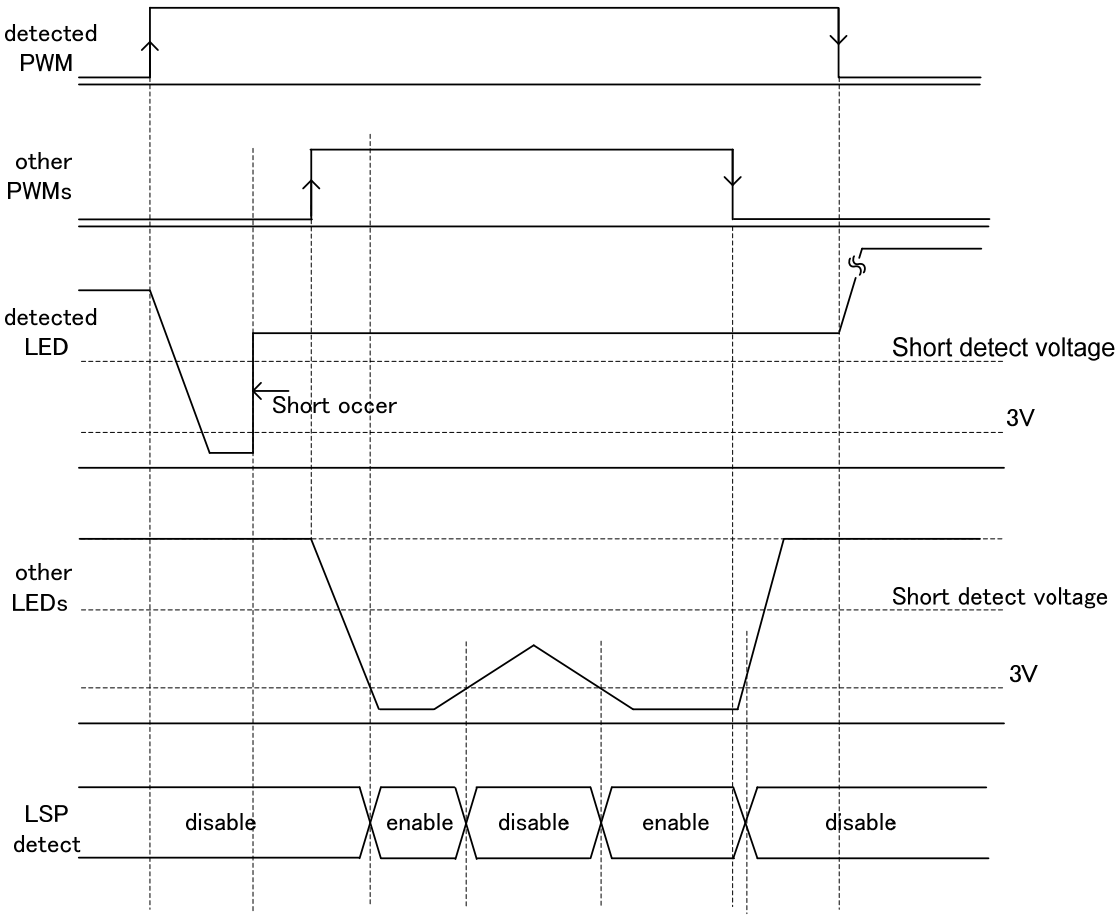


Figure 30.

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Rush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes – continued

10. Unused Input Terminals

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

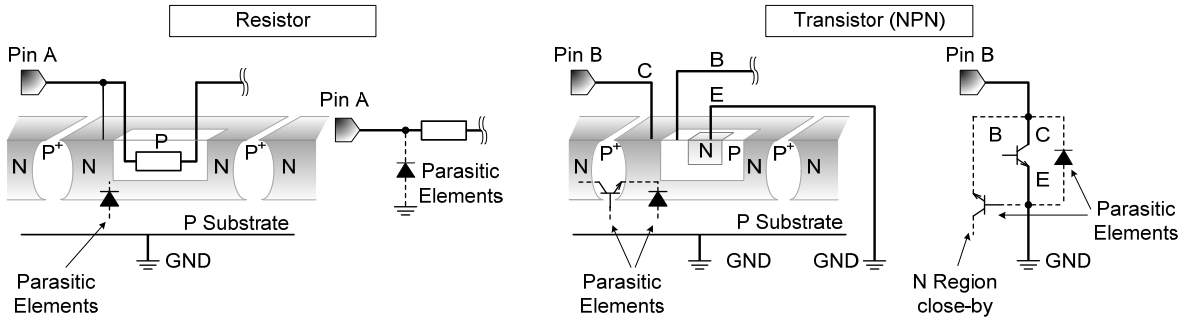


Figure 31. Example of monolithic IC structure

12. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

14. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

15. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

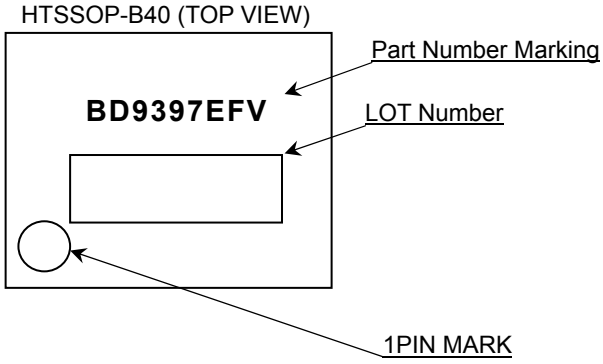
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●**Ordering Information**

B D 9 3 9 7 E F V	-	E2
Part Number		Packaging and forming specification E2: Embossed tape and reel
Package EFV:HTSSOP-B		

●**Marking Diagram**

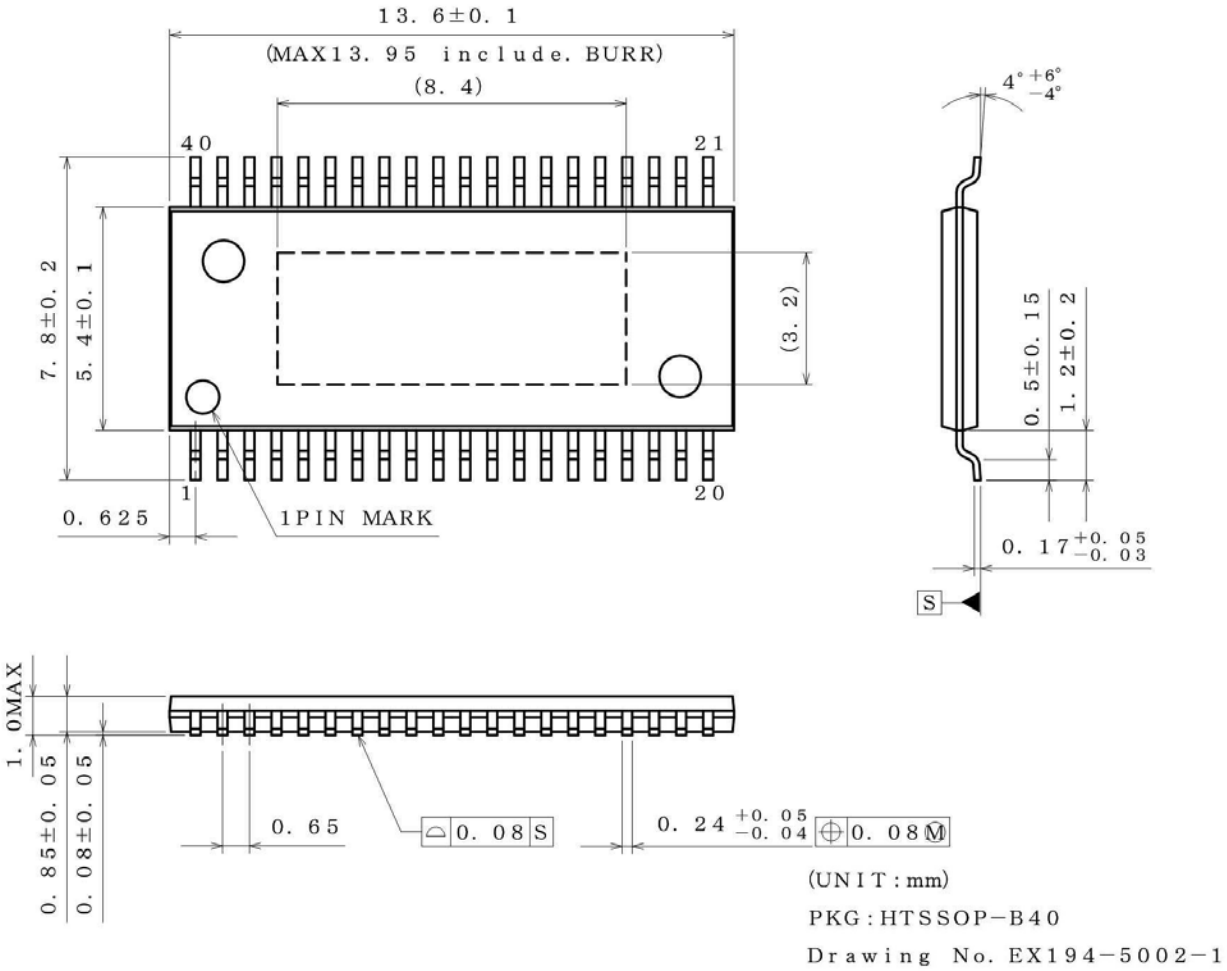


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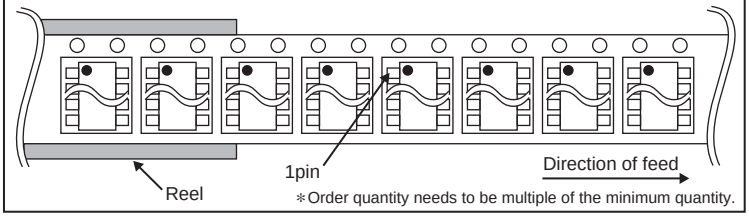
Physical Dimension, Tape and Reel Information

Package Name	HTSSOP-B40



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

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Revision History

Date	Revision	Changes
9.Jan.2014	001	Draft Version
10.Mar.2014	002	p.5 1.3 Pin Descriptions No.11-16 LED1-LED6 rating -0.3 to 60 [V] → -0.3 to 50 [V]
26.May.2014	003	p.3 Short circuit protection voltage add condition(FAILMODE=3V) p.13 UVLO detection condition UVLO<2.4V→2.3V p.14 UVLO detection condition UVLO<2.4V→2.3V SCP detection condition OVP<0.2V→0.79V release condition OVP>0.2V→0.79V
22.Dec.2014	004	p.2 Pin Configuration 37pin LPS→LSP
2.Jul.2015	005	p.14 ●3.3.2 List of the protection function modify table's contents
1.Sep.2015	006	p.13,14 The detailed timing condition for protections is added.

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

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8. Confirm that operation temperature is within the specified range described in the product specification.

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   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

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