MOSFET – Power, Single, N-Channel, μ8FL

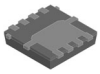
30 V, 71 A, 4.2 mΩ

NVTFS4C06N

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
30 V	4.2 mΩ @ 10 V	71 A
	6.1 mΩ @ 4.5 V	



WDFN8 3.3x3.3, 0.65P
CASE 511AB

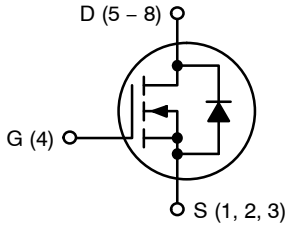


WDFNW8 3.3x3.3, 0.65P (Full-Cut μ8FL WF)
CASE 515AN

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- NVTFS4C06NWF – Wettable Flanks Product
- NVT Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

N-Channel

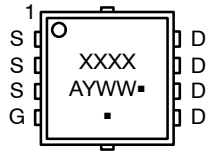


MAXIMUM RATINGS (T_J = 25 °C unless otherwise stated)

Symbol	Parameter			Value	Unit
V_{DSS}	Drain-to-Source Voltage			30	V
V_{GS}	Gate-to-Source Voltage			±20	V
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 4)	Steady State	T_A = 25 °C	21	A
			T_A = 100 °C	15	
P_D	Power Dissipation $R_{\theta JA}$ (Note 1, 2, 4)		T_A = 25 °C	3.1	W
			T_A = 100 °C	1.6	
I_D	Continuous Drain Current $R_{\theta JC}$ (Note 1, 3, 4)		T_A = 25 °C	71	
			T_A = 100 °C	50	A
P_D	Power Dissipation $R_{\theta JC}$ (Note 1, 3, 4)		T_A = 25 °C	37	W
			T_A = 100 °C	18	
I_{DM}	Pulsed Drain Current	T_A = 25 °C, t_p = 10 μs		367	A
T_J, T_{stg}	Operating Junction and Storage Temperature			−55 to +175	°C
I_S	Source Current (Body Diode)			33	A
E_{AS}	Single Pulse Drain-to-Source Avalanche Energy (T_J = 25 °C, I_L = 26 A_{pk}, L = 0.1 mH)			34	mJ
T_L	Lead Temperature for Soldering Purposes (1/8″ from Case for 10 s)			260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAM



4C06	= Specific Device Code for NVMTS4C06N
06WF	= Specific Device Code of NVTFS4C06NWF
A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 6 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 6.

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THERMAL RESISTANCE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State (Drain) (Notes 1 and 4)	4.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Notes 1 and 2)	48	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm^2 2 oz. Cu pad.
3. Assumes heat-sink sufficiently large to maintain constant case temperature independent of device power.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA		30	–	–	V
$V_{(BR)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient			–	14.4	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25 °C	–	–	1.0	μA
			T_J = 125 °C	–	–	10	
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = ±20 V		–	–	±100	nA
ON CHARACTERISTICS (Note 5)							
$V_{GS(TH)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA		1.3	–	2.2	V
$V_{GS(TH)}/T_J$	Negative Threshold Temperature Coefficient			–	3.8	–	mV/°C
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 10 V	I_D = 30 A	–	3.4	4.2	mΩ
		V_{GS} = 4.5 V	I_D = 30 A	–	4.9	6.1	
g_{FS}	Forward Transconductance	V_{DS} = 1.5 V, I_D = 15 A		–	58	–	S
R_G	Gate Resistance	T_A = 25 °C		–	1.0	–	Ω
CHARGES AND CAPACITANCES							
C_{ISS}	Input Capacitance	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 15 V		–	1683	–	pF
C_{OSS}	Output Capacitance			–	841	–	
C_{RSS}	Reverse Transfer Capacitance			–	40	–	
C_{RSS}/C_{ISS}	Capacitance Ratio	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		–	0.023	–	
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 4.5 V, V_{DS} = 15 V; I_D = 30 A		–	11.6	–	nC
$Q_{G(TH)}$	Threshold Gate Charge			–	2.6	–	
Q_{GS}	Gate-to-Source Charge			–	4.7	–	
Q_{GD}	Gate-to-Drain Charge			–	4.0	–	
V_{GP}	Gate Plateau Voltage			–	3.1	–	V
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 10 V, V_{DS} = 15 V; I_D = 30 A		–	26	–	nC
SWITCHING CHARACTERISTICS (Note 6)							
$t_{d(ON)}$	Turn-On Delay Time	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 15 A, R_G = 3.0 Ω		–	10	–	ns
t_r	Rise Time			–	32	–	
$t_{d(OFF)}$	Turn-Off Delay Time			–	18	–	
t_f	Fall Time			–	5.0	–	
$t_{d(ON)}$	Turn-On Delay Time	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 15 A, R_G = 3.0 Ω		–	8.0	–	ns
t_r	Rise Time			–	28	–	
$t_{d(OFF)}$	Turn-Off Delay Time			–	24	–	
t_f	Fall Time			–	3.0	–	

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified) (continued)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS							
V_{SD}	Forward Diode Voltage	V_{GS} = 0 V, I_S = 10 A	T_J = 25 °C	–	0.8	1.1	V
			T_J = 125 °C	–	0.63	–	
t_{RR}	Reverse Recovery Time	V_{GS} = 0 V, dIS/dt = 100 A/μs, I_S = 30 A		–	34	–	ns
t_a	Charge Time			–	17	–	
t_b	Discharge Time			–	17	–	
Q_{RR}	Reverse Recovery Charge			–	22	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

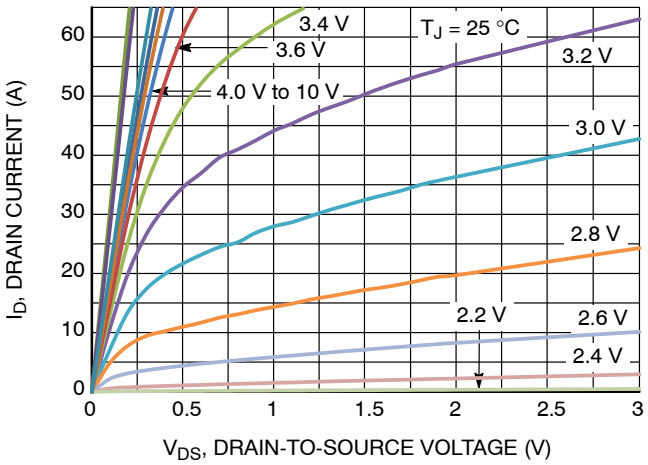


Figure 1. On-Region Characteristics

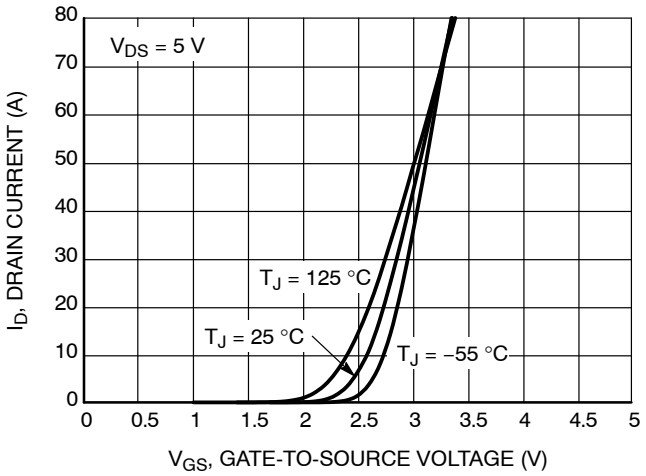


Figure 2. Transfer Characteristics

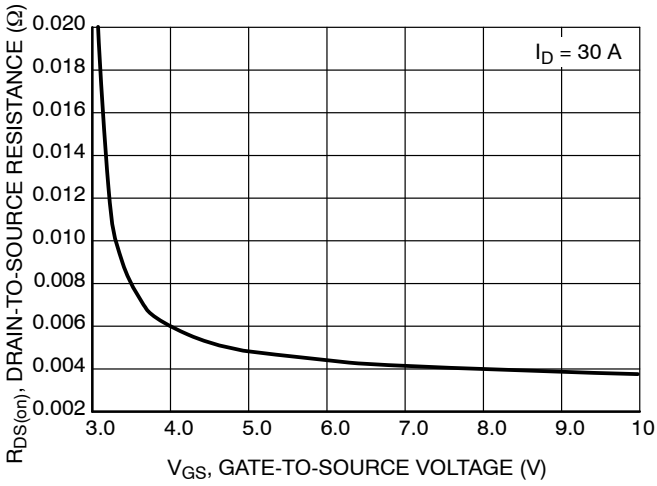


Figure 3. On-Resistance vs. V_{GS}

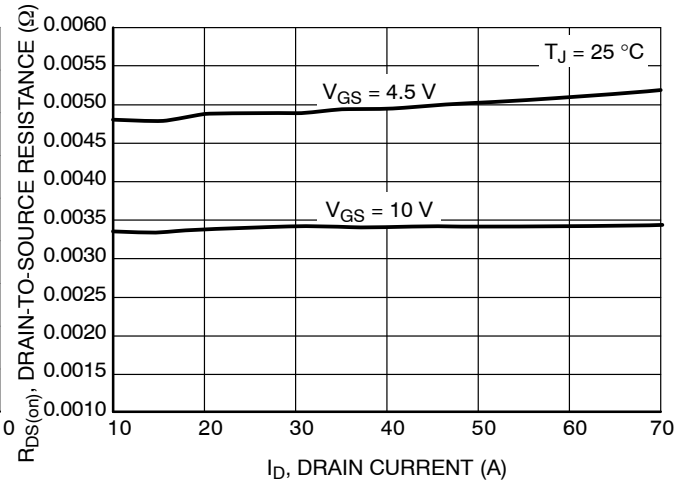


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

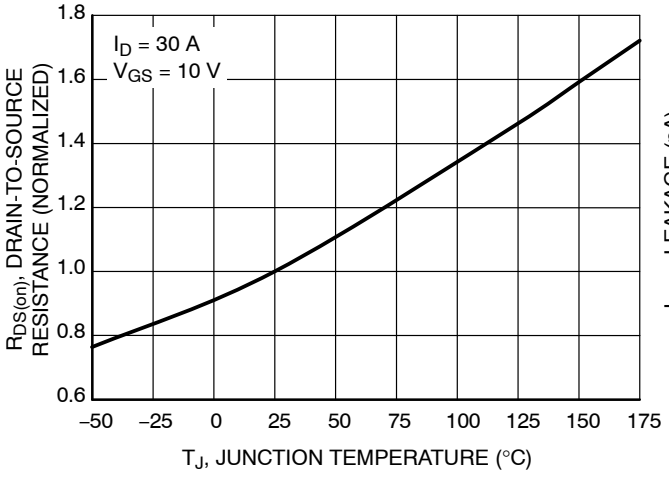


Figure 5. On-Resistance Variation with Temperature

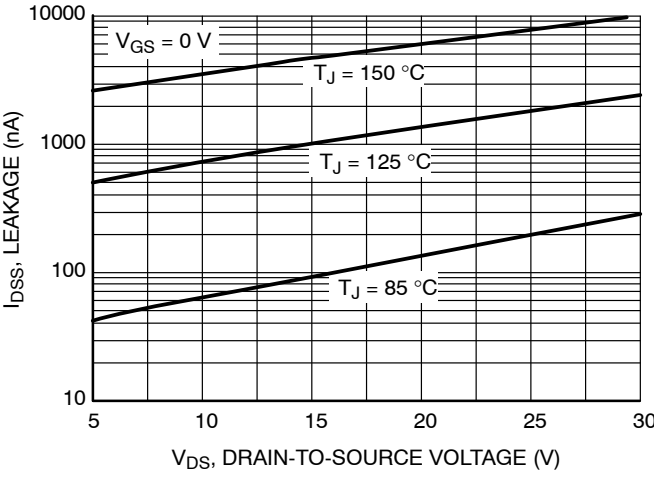


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS (continued)

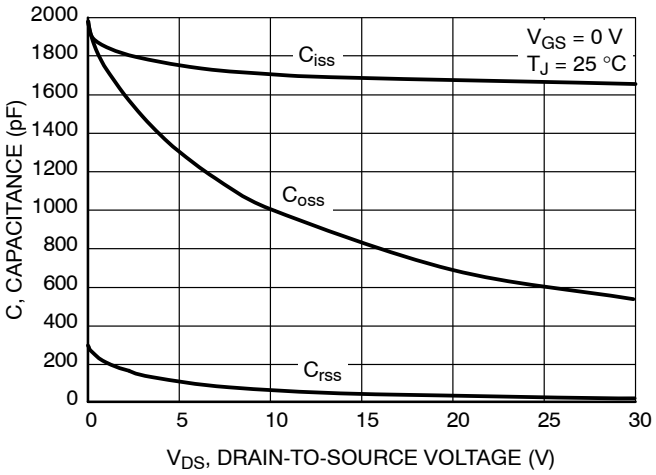


Figure 7. Capacitance Variation

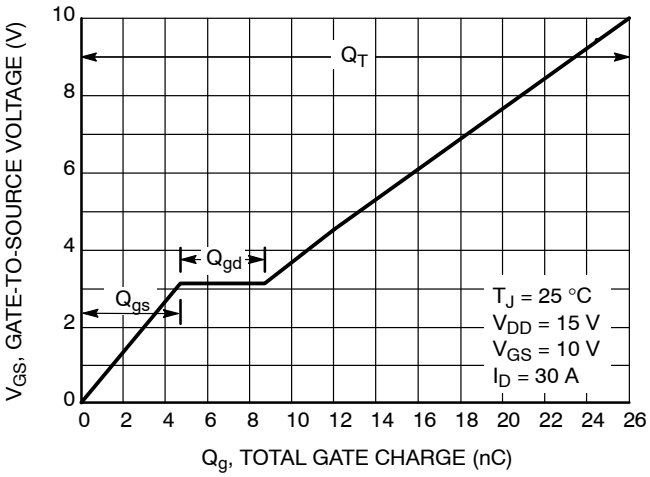


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

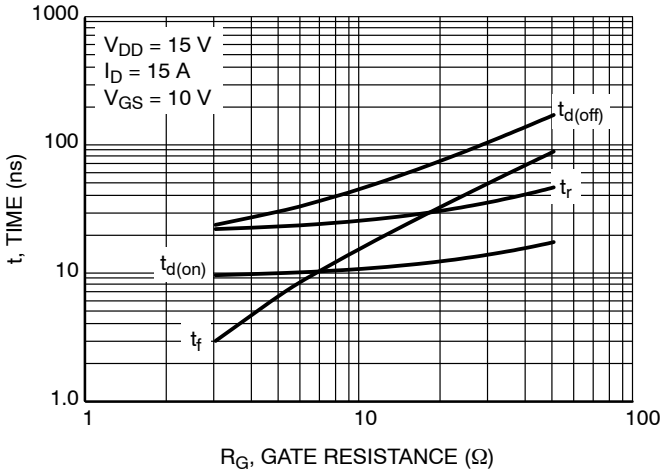


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

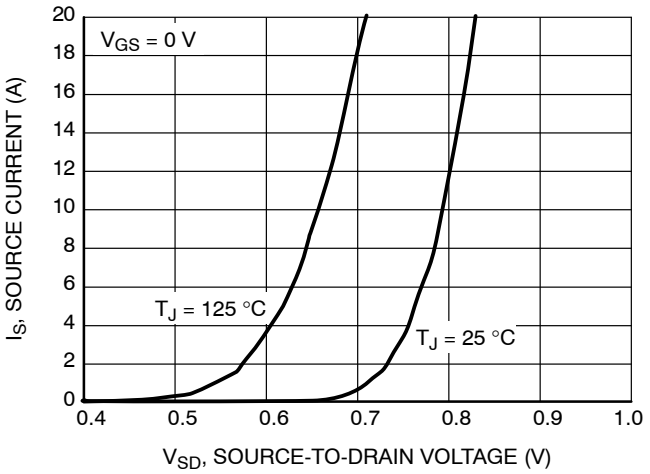


Figure 10. Diode Forward Voltage vs. Current

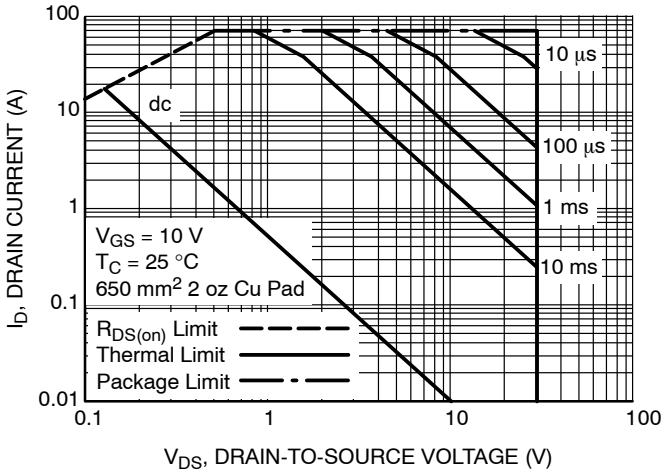


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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TYPICAL CHARACTERISTICS (continued)

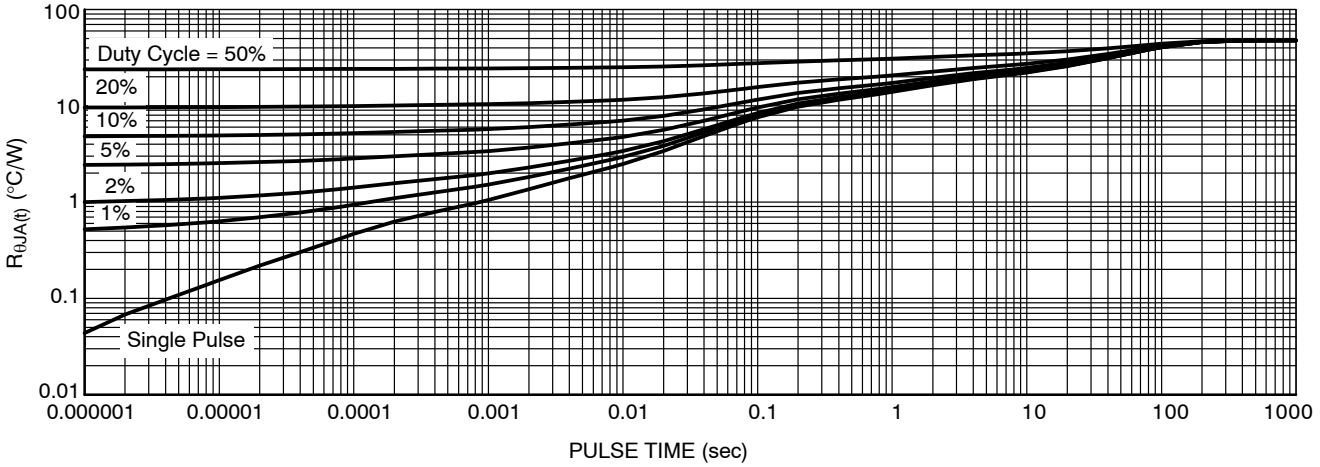


Figure 12. Thermal Response

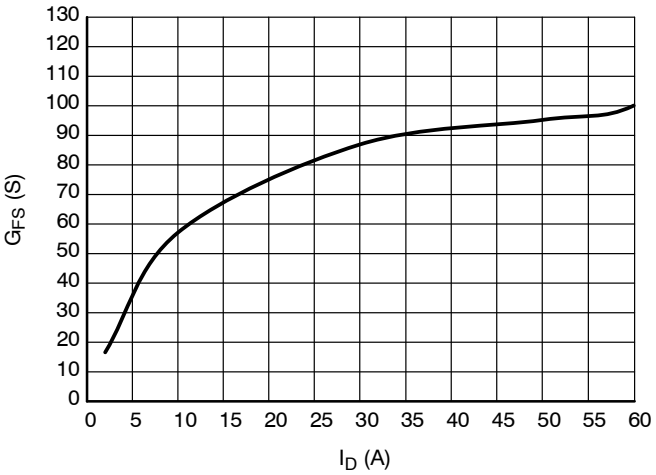


Figure 13. G_{FS} vs. I_D

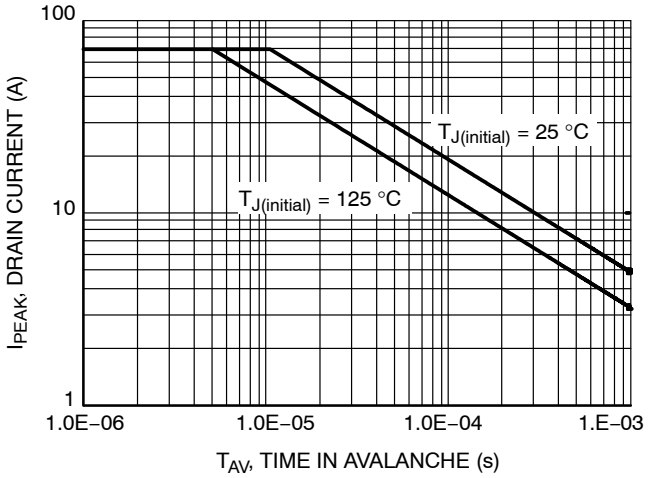


Figure 14. Avalanche Characteristics

ORDERING INFORMATION

Device	Package	Shipping†
NVTFS4C06NTAG	WDFN8 3.3x3.3, 0.65P (Pb-Free)	1500 / Tape & Reel
NVTFS4C06NTWG	WDFN8 3.3x3.3, 0.65P (Pb-Free)	5000 / Tape & Reel
NVTFS4C306NTAG	WDFN8 3.3x3.3, 0.65P (Pb-Free)	1500 / Tape & Reel

DISCONTINUED (Note 7)

NVTFS4C06NWFTAG	WDFNW8 3.3x3.3, 0.65P (Full-Cut μ8FL WF) (Pb-Free)	1500 / Tape & Reel
NVTFS4C06NWFTWG	WDFNW8 3.3x3.3, 0.65P (Full-Cut μ8FL WF) (Pb-Free)	5000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

7. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

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REVISION HISTORY

Revision	Description of Changes	Date
5	Device NVTFS4C306NTAG added to the Ordering Information table.	1/26/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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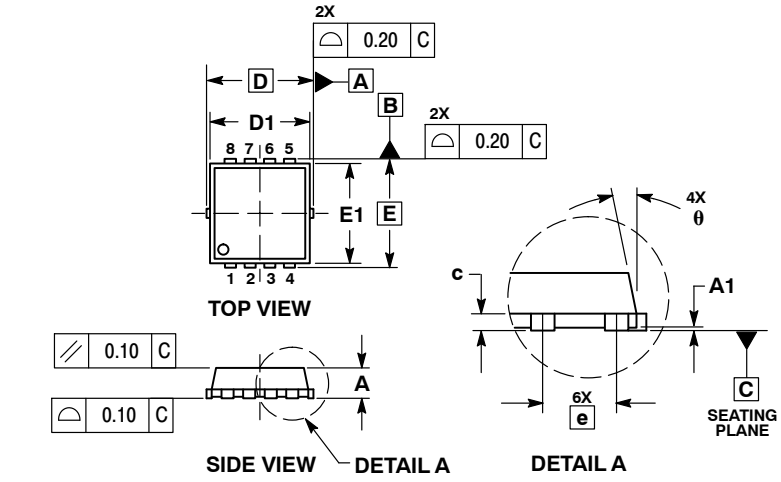
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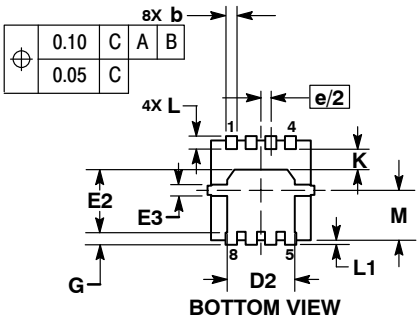
WDFN8 3.3x3.3, 0.65P
CASE 511AB
ISSUE D

DATE 23 APR 2012



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D		3.30 BSC			0.130 BSC	
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E		3.30 BSC			0.130 BSC	
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e		0.65 BSC			0.026 BSC	
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0 °	---	12 °	0 °	---	12 °



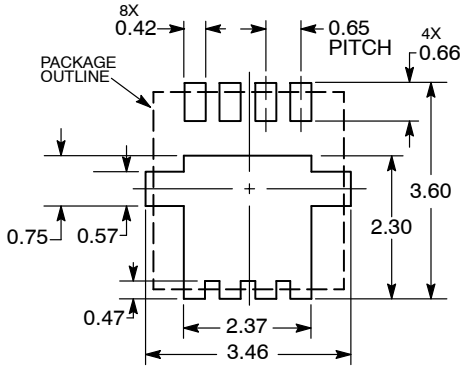
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT*



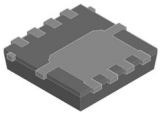
DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**WDFN8 3.3X3.3, 0.65P**	**PAGE 1 OF 1**

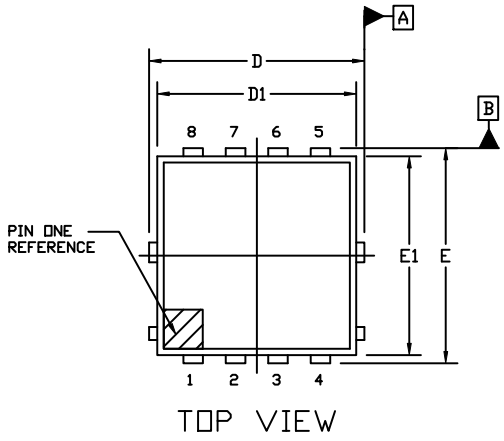
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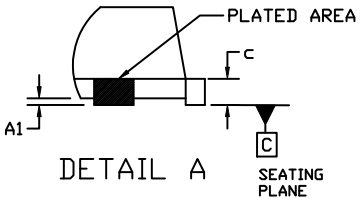


WDFNW8 3.3x3.3, 0.65P (Full−Cut µ8FL WF)
CASE 515AN
ISSUE O

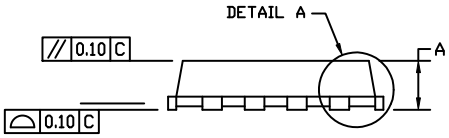
DATE 25 AUG 2020



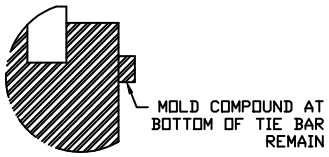
TOP VIEW



DETAIL A



SIDE VIEW

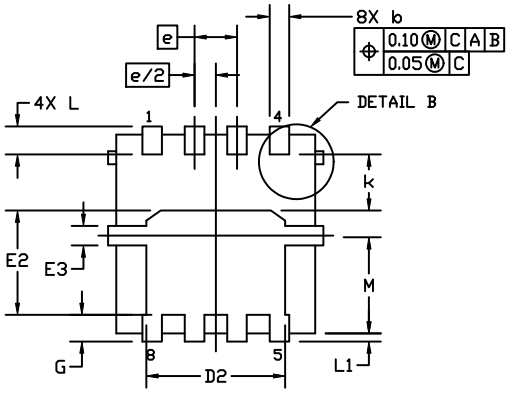


DETAIL B

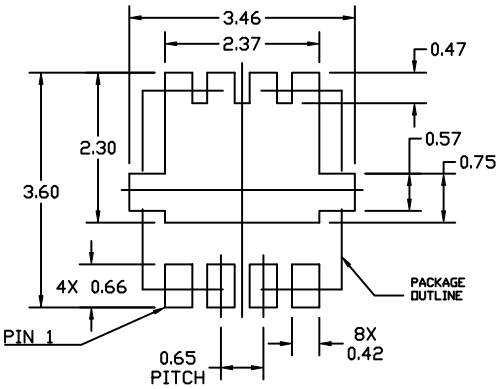
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	----	0.05
b	0.23	0.30	0.40
c	0.15	0.20	0.25
D	3.05	3.30	3.55
D1	2.95	3.05	3.15
D2	1.98	2.11	2.24
E	3.05	3.30	3.55
E1	2.95	3.05	3.15
E2	1.47	1.60	1.73
E3	0.23	0.30	0.40
e	0.65 BSC		
G	0.30	0.41	0.51
K	0.65	0.80	0.95
L	0.30	0.43	0.59
L1	0.06	0.13	0.20
M	1.40	1.50	1.60



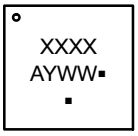
BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WDFNW8 3.3x3.3, 0.65P (Full−Cut µ8FL WF)**	**PAGE 1 OF 1**

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