Octal 75V, 700 mA Source Driver for Space Data Sheet

AAHS298B

Description

The AAHS298B is an 8-channel 75V, 700 mA source driver with internal thermal shutdown that is radiation-hardened by design. It is typically used as a companion device to the LX7710 diode array to build redundant power switches.

Each output is capable of sourcing 700 mA with a withstand voltage of 75V to interface control systems to relays, motors, solenoids, and other loads. Outputs include integrated diodes for protection against transients and inductive kick-back. Built-in thermal shutdown provides protection during over-current and soft-start occurrences.

The AAHS298B is packaged in a 20 pin ceramic hermetic CSOIC package and is QML-V and QML-Q certified. It operates over a –55°C to 125°C temperature range and is radiation tolerant to a minimum of 100 krad(Si) TID and a minimum of 50 krad (Si) ELDRS, as well as single event effects.

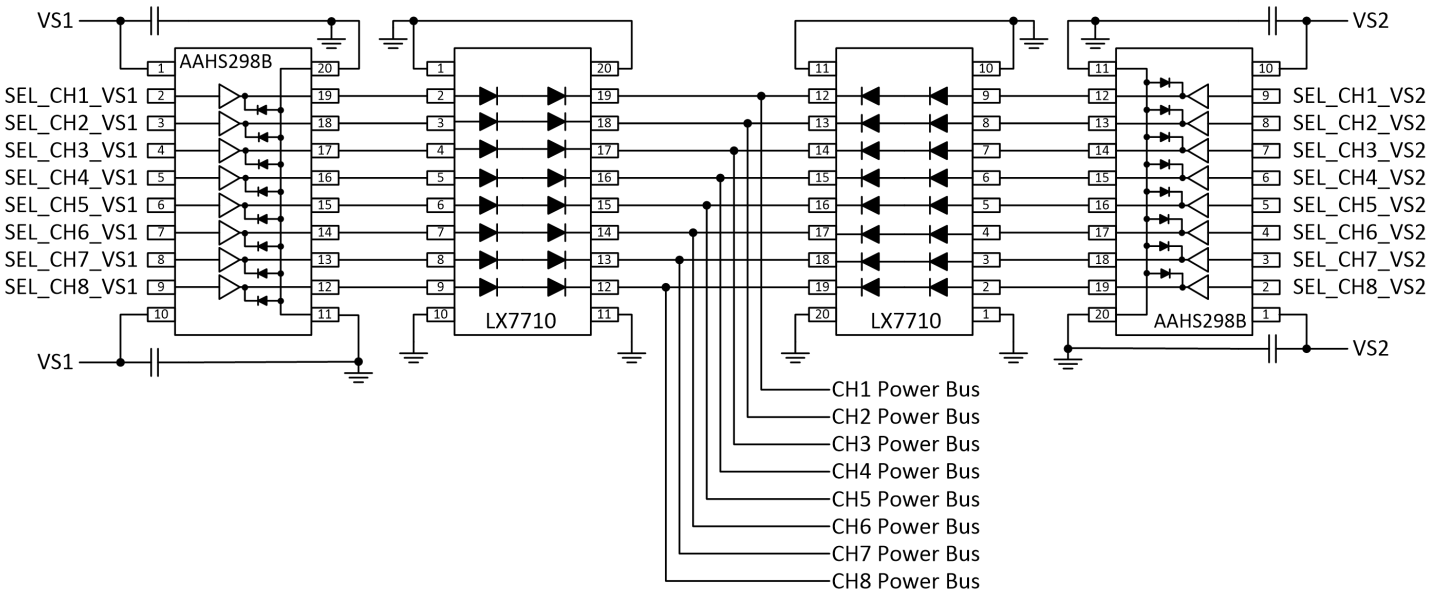
Features

- 700 mA source current capability per output
- 20 µA max supply current with all outputs off
- Channel isolation to prevent fault propagation
- Internal ground clamp diodes
- 75V output breakdown voltage
- 2.5V to 12V logic compatible inputs
- Internal thermal shutdown
- Radiation tolerant: 100 krad(Si) TID, 50krad (Si) ELDRS, and SEL immune to 117 MeV.cm²/mg and 125°C (fluence of 10^7 particles/cm²)

Applications

- Relay/Solenoid drivers
- Lamp/LED drivers
- Stepper and/or servo motor drivers
- Aerospace satellite manufacturers
- Military power electronics control

Figure 1. AAHS298B Example Redundant Power Bus Switch System with LX7710



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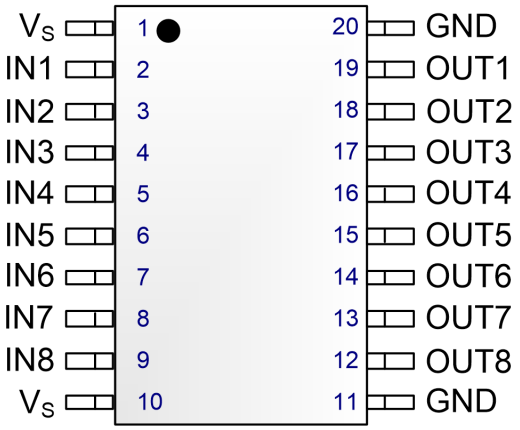
1. Pin Configuration and Pinout

Figure 1-1. Pin Configuration and Pinout



1.1. Ordering Information

Table 1-1. Ordering Information (Subject to Export Compliance Under EAR9A515.e)

Operating Temperature	Package Type	Package	Part Number	SMD Number	Flow	Shipping Type
–55°C to 125°C	Hermetic Ceramic	CSOIC 20L Flat leads	AAHS298B-07-4020A-V	SMD 5962-1523101VYC	QML-V	Tray
			AAHS298B-06-4020A-Q	SMD 5962-1523101QYC	QML- Q	
	Ceramic		MECH-SAMPLE-CSOICF20	—	Empty Package Sample	
	Hermetic Ceramic	CSOIC 20L Formed leads	AAHS298B-S-S20B-S	SMD 5962-1523101VXC	QML-V	
			AAHS298B-S-S20B-B	SMD 5962-1523101QXC	QML- Q	
	Ceramic		AAHS298B-S-S20B-ENGR(1)	—	Engineering Samples	
			MECH-SAMPLE-CSOIC20	—	Empty Package Sample	

Note:

1. Engineering samples are tested at room temperature only and do not undergo thermal, environmental or hermeticity testing.

2. CSOIC-20 Pin Numbering and Pin Descriptions

Table 2-1. CSOIC-20 Pin Numbering and Pin Descriptions

Pin	Name	Pin Type	Description
1	VS	Power	Both VS pins 1 and 10 must be used, connected together to the common supply (10V to 50V)
2	IN1	Logic Input	Active high to turn on source driver 1
3	IN2	Logic Input	Active high to turn on source driver 2
4	IN3	Logic Input	Active high to turn on source driver 3
5	IN4	Logic Input	Active high to turn on source driver 4
6	IN5	Logic Input	Active high to turn on source driver 5
7	IN6	Logic Input	Active high to turn on source driver 6
8	IN7	Logic Input	Active high to turn on source driver 7
9	IN8	Logic Input	Active high to turn on source driver 8
10	VS	Power	Both VS pins 1 and 10 must be used, connected together to the common supply (10V to 50V)
11	GND	Ground	Both GND pins 11 and 20 must be used, connected together to GND
12	OUT1	Output	Output of source driver 1
13	OUT2	Output	Output of source driver 2
14	OUT3	Output	Output of source driver 3
15	OUT4	Output	Output of source driver 4
16	OUT5	Output	Output of source driver 5
17	OUT6	Output	Output of source driver 6
18	OUT7	Output	Output of source driver 7
19	OUT8	Output	Output of source driver 8
20	GND	Ground	Both GND pins 11 and 20 must be used, connected together to GND

3. Electrostatic Discharge Ratings

Table 3-1. Electrostatic Discharge Ratings

ESD Test	Minimum Capability
HBM: Human Body Model, per MIL-STD-883 TM3015, all pins	±2000V

3.1. Absolute Maximum Ratings

Exceeding these ratings could cause damage to the device. All voltages are with respect to GND. Currents are positive into, negative out of specified terminal. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions are not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 3-2. Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Supply Voltage (VS, Max voltage between VS and GND)	–0.5	75	V
Digital Inputs (IN[1:8], Max voltage between INPUT and GND)	–0.5	75	V
Output Voltage (OUT[1:8], Maximum voltage between OUT[1:8] and GND)	—	75	V
Single Output Continuous Current (OUT[1:8])	—	–700	mA
Single Output Peak Current (OUT[1:8], ≤ 1 second)	—	–1200	mA
Multiple Output Simultaneously Continuous Current (OUT[1:8])	—	–2800	mA
ESD (all pins, HBM)	—	2000	V
Operating Junction Temperature	–55	150	°C
Storage Junction Temperature	–65	150	°C
Peak Lead Solder Temperature (10 seconds)	—	260 (+0, –5)	°C

4. Electrical Characteristics

The following specifications apply over the operating ambient temperature of –55°C ≤ T_A ≤ 125°C except where otherwise noted with the following test conditions: V_S = 50V. Typical parameters refer to T_J = 25°C. Positive currents flow into pins. The numbers in the Test Setup column refer to Parameter Test Configurations.

Table 4-1. Electrical Characteristics

Symbol	Parameter	Test Conditions	Test Setup	Min.	Typ.	Max.	Units
Operating Supply Current							
I_{SLEEP}	Standby Supply Current	IN[1:8] = 0.0V, No Output Load	1	—	1	20	µA
$I_{VS2.5}$	Active Supply Current	IN[1:8] = 2.5V, No Output Load	2	—	5	25	mA
I_{VS5}	Active Supply Current	IN[1:8] = 5.0V, No Output Load	3	—	7	25	mA
AC Characteristics							
t_{on}	Output Turn On Delay Time	Load = 470Ω, 100 pF, V_S = 45V	—	—	—	2	µs
t_{off}	Output Turn Off Delay Time	V_{IL} = 0.8; V_{IH} = 2.5V	—	—	—	10	µs
t_R	Output Rise Time (10% to 90%)		—	—	—	2	µs
t_F	Output Fall Time (90% to 10%)		—	—	—	10	µs
DC Characteristics							
V_S	Supply Voltage Range	—	—	10	—	50	V
$THSD_{TRIP}$	Thermal Shutdown Trip Temperature	—	—	135	155	175	°C
$THSD_{RST}$	Thermal Shutdown Reset Temperature	Restarts at 125°C	—	125	—	—	°C
V_{IH}	Input High Level	—	—	2.5	—	—	V
V_{IL}	Input Low Level	—	3	—	—	0.8	V
$V_{CE(SAT)}$	Output Saturation at 350 mA	IN[1:8] = 2.5V	4	—	1.7	2.2	V
	Output Saturation at 500 mA		4	—	1.8	2.3	V
	Output Saturation at 700 mA		4	—	2.1	2.7	V
I_{IH}	Input High Leakage	IN[1:8] = 5.0V	5	—	60	100	µA
I_{IL}	Input Low Leakage	IN[1:8] = 0.0V	5	—	0.1	10	µA
I_{OL}	Output Low Leakage	Output OFF, VOUTX = 0.0V	6	—	2	50	µA
V_F	Clamp Diode Forward Voltage	I_F = 200 mA	7	—	—	2.5	V
		I_F = 700 mA	7	—	—	3.0	V
I_R	Clamp Diode Leakage Current	V_R = 50V	8	—	—	50	µA

5. Thermal Properties

The θ_{JB} number is for conduction only to the ceramic base of the package. It assumes that the ceramic base has a thermal epoxy underneath the ceramic package to exhaust the heat from the package into the PCB or other surface.

Table 5-1. Thermal Properties

Thermal Resistance	Typ	Units
θ_{JB}	2.24	°C/W

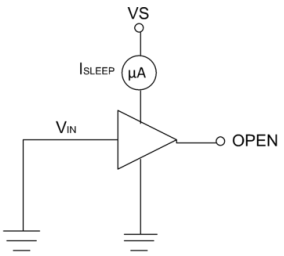
5.1. Heatsinking Recommendations

The AAHS298B dissipates up to around 7.5W ({2.7V per output} x 2800 mA) at full load, and so thermal considerations are usually necessary. The base of the ceramic package should be used as the heat conducting surface for all but light duty applications. The metal package top is attached to the package body at the top of relatively thin cavity walls and so has a much higher thermal resistance from the die than the base of the package. It is recommended to apply a thermal interface material between either package or its heat dissipater. The heat dissipater can be copper layers within a multilayer circuit board to spread heat laterally across the board or a direct mounted dissipation element.

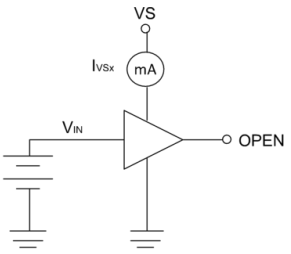
6. Parameter Test Configurations

The test setup numbers correspond to the Test Setup column in Table 4-1.

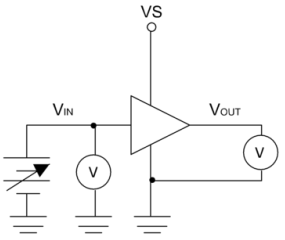
Figure 6-1. Parameter Test Configurations



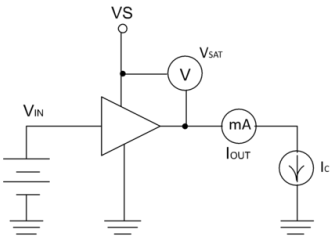
Test Setup 1
Standby Supply Current



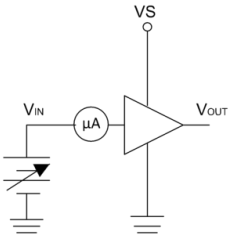
Test Setup 2
Active Supply Current



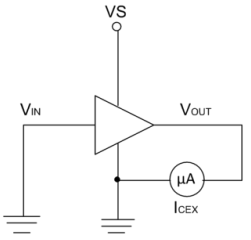
Test Setup 3
Input Threshold Voltage



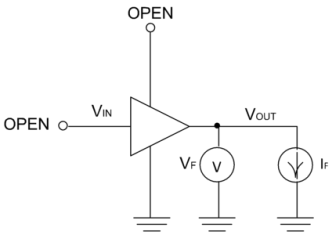
Test Setup 4
$V_{CE(sat)}$Test Circuit



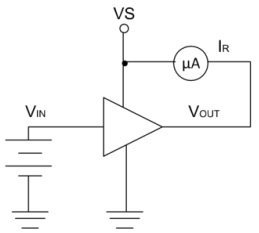
Test Setup 5
Input Bias Current



Test Setup 6
Output Leakage Current



Test Setup 7
Clamp Diode Forward Voltage



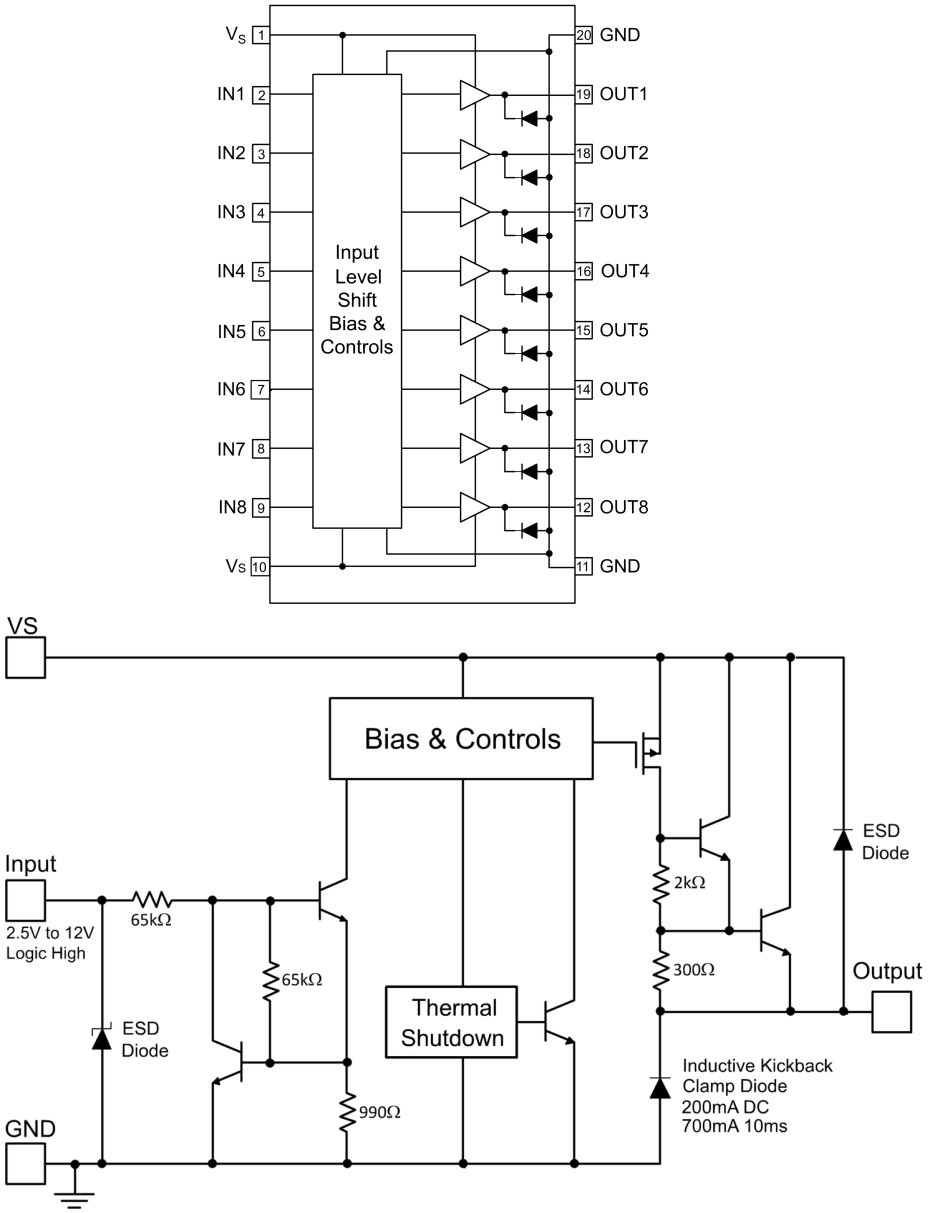
Test Setup 8
Clamp Diode Leakage Current

7. AAHS298B Operation and Application

The AAHS298B contains eight 75V, 700 mA source drivers as shown in the block diagram in the following figure. The drivers switch outputs from a common input supply, V_S. Both V_S input supply pins 1 and 10 must be used, connected to the loads' 10V to 50V supply.

The logic inputs share the GND connection with the anodes of the load outputs clamp diodes, which may carry high peak currents when an inductive load is switched off. Avoid ground bounce by either using a ground plane or routing GND to a star ground point. The clamp diodes protect against transients and kick-backs from inductive loads. Each diode is rated for 200 mA DC current, and can withstand 700 mA for about 10 ms. Both GND pins 11 and 20 must be connected to the system GND. The internal clamp diodes may be enough to manage voltage kick-backs from local inductive loads, but an additional snubber, diode, or transorb may be necessary across an inductive loads located at a distance from the driver.

Figure 7-1. AAHS298B Block Diagram and Single Channel Simplified Block Diagram



7.1. Logic Inputs

The logic inputs IN1 to IN8 are compatible with 2.5V to 12V logic levels over the full supply and temperature ranges. When all INx pins are low, all drivers are off and the AAHS298B draws a 1 µA typical 20 µA maximum standby current.

The variation with temperature of logic inputs' high threshold for V_S = 50V is shown in Figure 8-1. The threshold rises with decreasing temperature. The worst case is at V_S =10V, I_{LOAD} = 700 mA, and T_A = –55°C. Here, the output stage's PFET pre-driver (Figure 7-1) has the highest gate threshold, lowest supply voltage, and needs to drive the most current into the base of the output NPN transistor. By relaxing one or more of these parameters, the input logic level can be reduced from 2.5V to 2.2V, enabling compatibility with 2.5V logic outputs. This is not production tested or characterized, but for the conditions $V_{IH} \geq 2.2V$, $V_S \geq 20V$, I_{LOAD} = 350 mA, and T_A = –55°C to +125°C, the outputs will switch, but the output drive voltage $V_{CE(SAT)}$ may worsen up to 600 mV worst case (from 2.2V to 2.8V) at T_A = –55°C.

If any logic input is high when the input power is applied, its respective output will start to turn on at some point below the supply voltage minimum $V_{S(min)}$ = 10V, following the supply dV/dt. Above 10V, the output will follow the supply up and down with a time constant of the power switch's on-resistance and the switch load's bulk capacitance.

If any logic input is high when the input power is removed, the load's bulk capacitance will discharge back to the supply through the internal ESD diode. If the input supply drops very fast and the load capacitance is large, fit a silicon or schottky diode across the switch (cathode to VS, anode to output) paralleling the ESD diode to manage this reverse current flow.

7.2. Source Driver Outputs

The source driver outputs OUT1 to OUT8 are switched high-side drivers capable of 700 mA continuous current with a typical saturation voltage drop of 2.1V. Figure 8-2 shows the typical variation of saturation voltage with output current and temperature. The saturation voltage has a negative temperature coefficient, reducing driver power dissipation with increasing temperature. The negative temperature coefficient also means that directly paralleled driver outputs will **not** current share. The paralleled output with the lowest voltage drop initially will take the most current. That output's current share will continue to rise as the driver gets hotter than the others, and its voltage drop continues to reduce.

Above 700 mA source current, the saturation voltage increases more rapidly across a source driver output, and due to the design of the output stage the output current self-limits around 1.4A for a slow overload. The 700 mA channel continuous current rating is therefore a nominal 50% derating of the maximum drive capability of the output transistors.

An instantaneous short-circuit condition from a driver output to ground could cause the driver output current to reach the output's bond-wire fusing current of 2A. This can be used as a protection feature to permanently isolate a shorted load while allowing the remaining outputs to function normally.

There is a 2800 mA limit for the total current from the 8 source drivers OUT1 to OUT8. This limit is due to the bond wire current capability on the two supply pins, V_S, as these bond wires will fuse open around 2A each. The 2800 mA limit allows all 8 drivers to source 350 mA continuously, or high currents with pulsed loads. The relationship between maximum channel output current and load duty cycle is shown in Figure 8-3.

7.3. Thermal Shutdown

The thermal shut-down circuitry is located in the center of the die between drivers 4 and 5. Since silicon is a good heat conductor, the temperature gradient at the surface of the die remains within a few degrees centigrade from the center of die (drivers 4 and 5) and each end of the die (driver 1 and driver 8). The thermal trip has a time constant in the order of seconds and cannot protect against a short-circuit on a driver output. A shorted output's bond wire will fuse open in a few 10s of milliseconds before the overload has caused the extra dissipation to be detected.

When all channels are dissipating power, the die junction-to-package-bottom (θ_{JB}) thermal resistance is less than 3°C/W. θ_{JB} for one channel only is under 20°C/W.

When the AAHS298B is mounted using a heat pad under the package to transfer heat to a PCB equipped with an integral heat-sink, the junction to PCB thermal resistance is typically around 10°C/W. This makes it unlikely for the thermal shut-down circuitry to trip. If the part is simply mounted on the PCB with no heat sinking, a 6W load (4 channels enabled sourcing 700 mA each) can be enough to trip the thermal shutdown trip at room temperature. The AAHS298B is also available with flat leads, which can be formed to mount the part upside down. This approach allows external heatsinking to be applied directly to the package bottom.

8. Characteristic Curves

Figure 8-1. AAHS298B Input Logic High Threshold Variation With Temperature

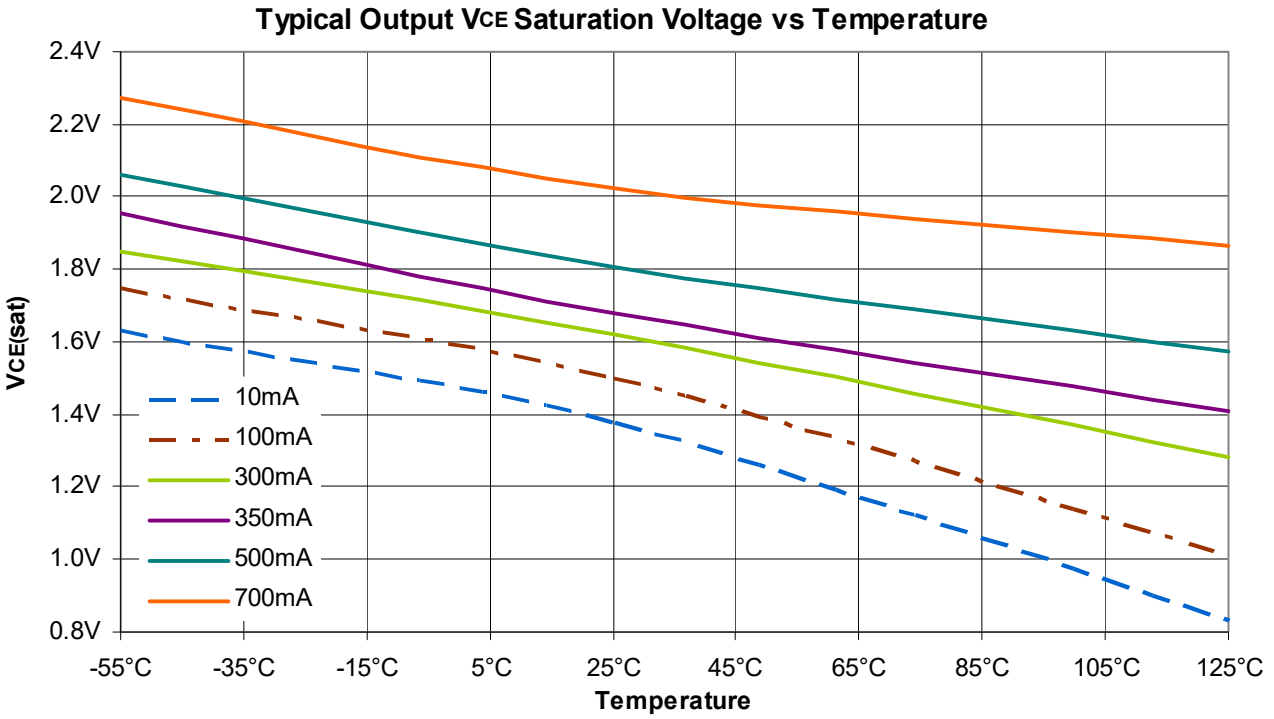


Figure 8-2. Typical Output V_{CE} Vs. Saturation Voltage

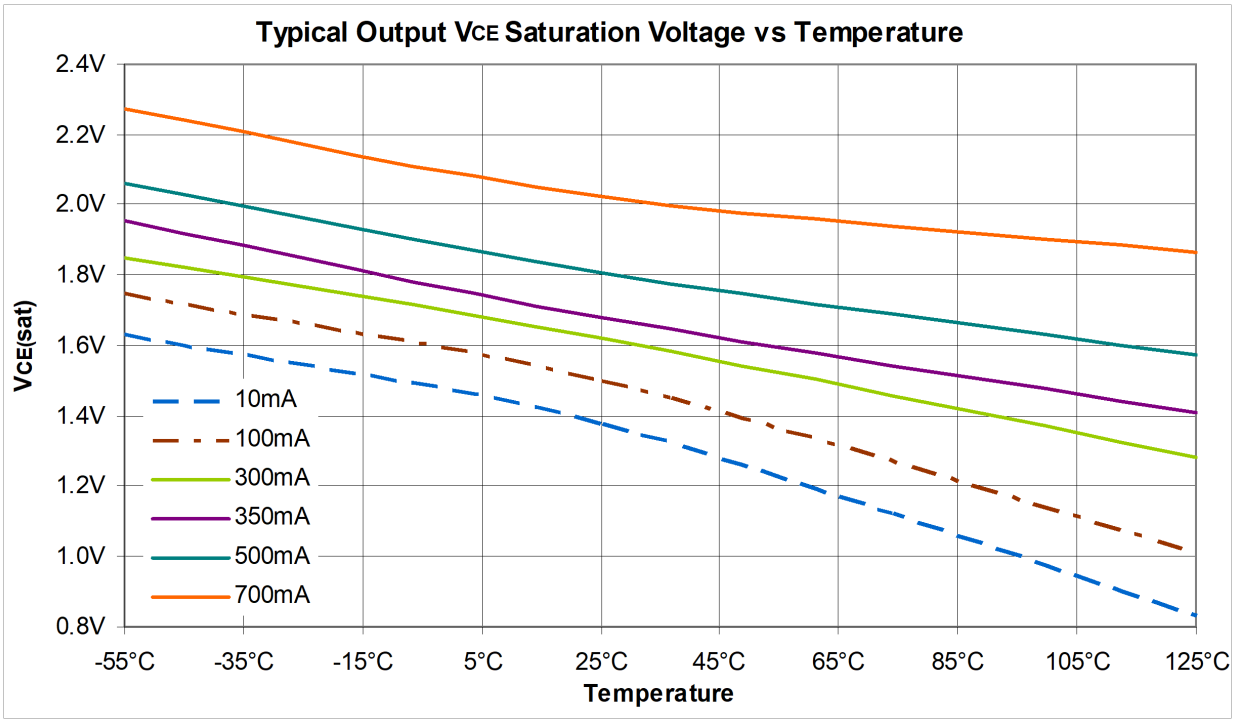
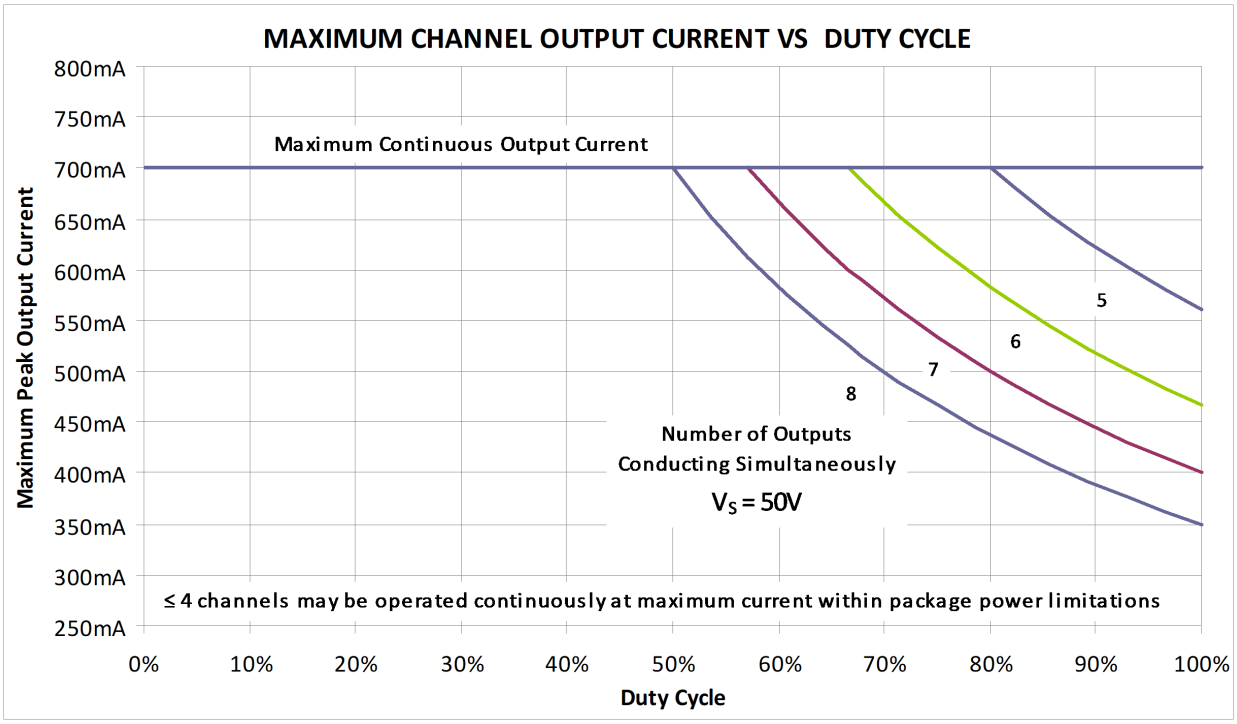
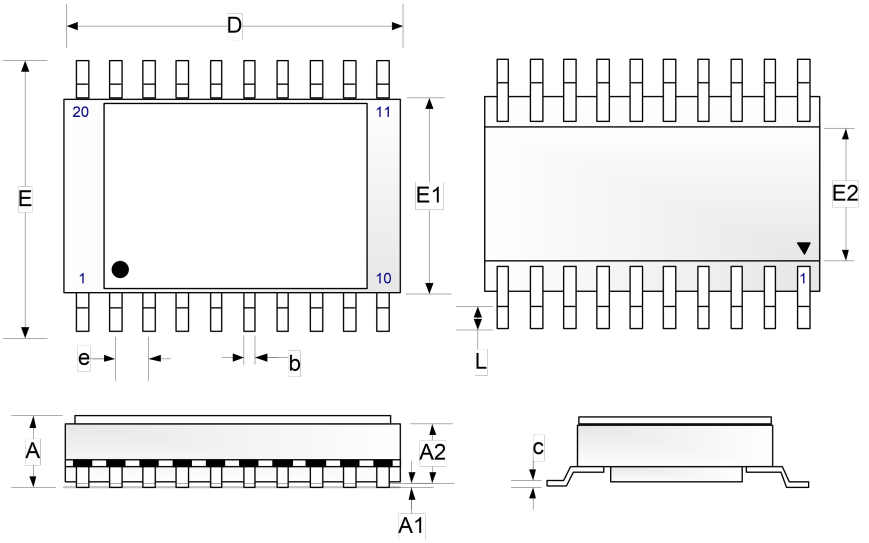


Figure 8-3. Maximum Channel Output Current Vs. Duty Cycle



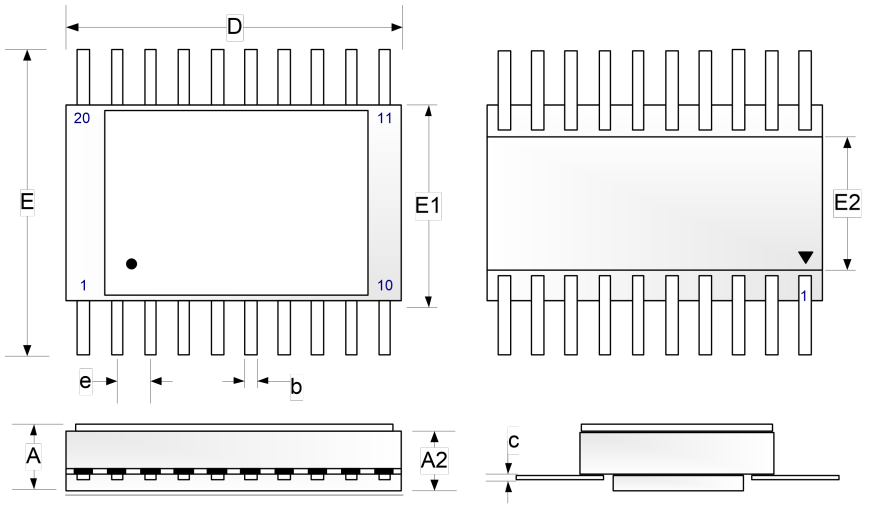
9. CSOIC 20L (Ceramic Small Outline) Dimensions

Figure 9-1. CSOIC-20 (Formed Leads) Package Dimensions



Dim.	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	2.28	2.92	0.090	0.115
A1	—	0.38	—	0.015
A2	1.78	2.41	0.070	0.095
b	0.36	0.48	.0140	.0190
c	0.15	0.25	0.006	0.010
D	12.45	13.08	0.490	0.515
E	10.16	11.18	0.400	0.440
E1	7.24	7.62	0.285	0.300
E2	4.70 BSC		0.185 BSC	
e	1.27 BSC		0.050 BSC	
L	0.50	0.76	0.020	0.030

Figure 9-2. CSOIC-20 (Flat Leads) Package Dimensions

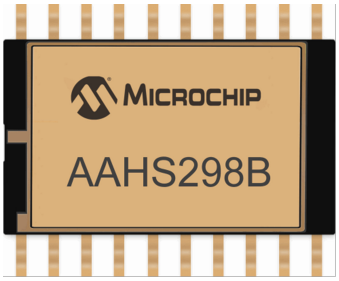


Dim.	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	2.03	2.67	0.080	0.105
A2	1.78	2.41	0.070	0.095
b	0.36	0.48	.0140	.0190
c	0.15	0.25	0.006	0.010
D	12.45	13.08	0.490	0.515
E	21.00	24.00	0.827	0.945
E1	7.24	7.62	0.285	0.300
E2	4.70 BSC		0.185 BSC	
e	1.27 BSC		0.050 BSC	

Notes:

1. Controlling dimensions are in mm. Inch equivalents are shown for general information
2. Package mass is 0.83g typical for products with formed leads
3. Lead material is Alloy 42 with NiAu plating (nickel under-plate followed by gold plating)
4. Lid material is Kovar with NiAu plating (nickel under-plate followed by gold plating) with AuSn solder seal
5. Lid is electrically isolated from the leads, and is bonded hermetically to the ceramic body using AuSn solder
6. Use the base of the package as the surface for conducting heat from the package

Figure 9-3. CSOIC-20 (Formed Leads) Package



10. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	06/2025	Document was converted to Microchip template and assigned literature number DS00006041.
2.1	9/2024	Added new section 4 with HBM ESD ratings.
2	04/2024	Added explanation in section 10.2 why the negative temperature coefficient of the driver outputs voltage drop means that directly paralleled driver outputs will not current share.
1.9	10/2023	Added package mass to packaging section.
1.8	05/2023	Updated weblinks from Microsemi to Microchip. Added empty package samples to ordering table. Added AuSn solder seal lid attach detail to package notes.
1.7	04/2021	Branding moved from Microsemi to Microchip, and some terminology changed. Added latch-up immunity, hot links to product pages and radiation test report to front page. Engineering sample disclaimer added. Added Heatsinking Recommendations section. Mild rewrite of Operation and Application section, adding 2.5V logic guidance, correcting resistor values in block diagram, and describing power switch behavior if enabled on power-up. Added Input Logic High Threshold Variation with Temperature characteristic curve. Added package picture to package section.
1.6	06/2017	This is the release before the change log started.

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ISBN: 979-8-3371-1501-6

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