Single Bus LVDS Transceiver

Features

- Bus LVDS Signaling (BLVDS)
- Designed for Double Termination Applications
- Balanced Output Impedance
- Light Bus Loading: 5pF typical
- Glitch-free power up/down (Driver Disabled)
- Operates from a 3.3V supply
- High Signaling Rate Capability: >100Mbps
- Driver:
  - ±250mV Differential Swing into a 27Ω load
  - Propagation Delay of 1.5ns typ.
  - Low Voltage TTL (LVTTL) Inputs are 5V Tolerant
- Receiver:
  - Accepts ±50mV (min.) Differential Swing with up to 2.0V ground potential difference
  - Propagation Delay of 3.3ns typical
  - Low Voltage TTL (LVTTL) Outputs
  - Open, Short, and Terminated Fail Safe
- Bus terminal ESD exceeds 10kV
- Industrial Temperature Operation (–40°C to +85°C)
- Packaging (Pb-free & Green available):
  - 8-lead SOIC (W)
  - 8-lead MSOP (U)

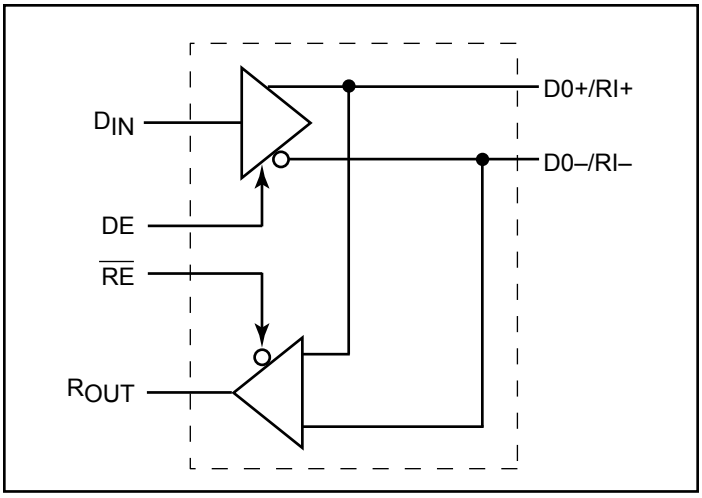
Description

The PI90LVB010 is a differential line driver and receiver (transceiver) that is similar to the IEEE1596.3 SCI and ANSI/TIA/EIA-644LVDS standards, the difference is that the driver output current is higher. This modification enables true half-duplex operation with more than one LVDS driver or with two line transmission resistors over a 50Ω differential transmission line. To minimize bus loading, the driver outputs and receiver inputs are internally connected. The logic interface provides maximum flexibility resulting from four separate lines that are provided: D_{IN}, DE, $\overline{RE}$, and R_{OUT}.

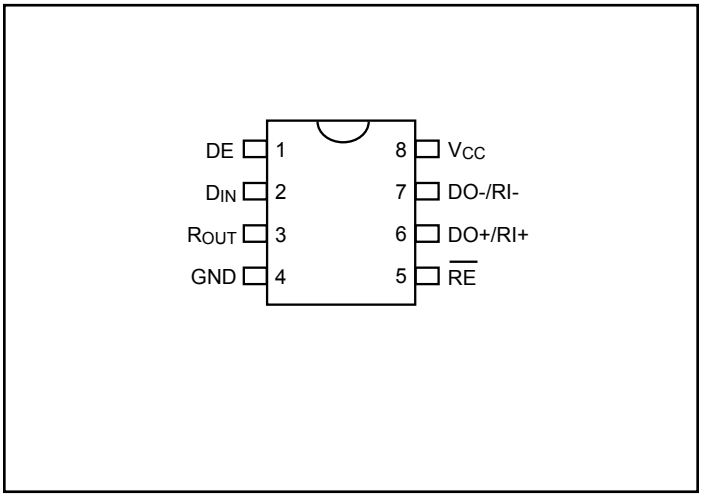
This device also feature flow-through which allows easy PCB routing for short stubs between the bus pins and the connector. The driver has 10mA drive capability, allowing it to drive heavily loaded backplanes, with impedance as low as 27Ω.

The driver translates between TTL levels (single-ended) to Low Voltage Differential Signaling levels. This allows for high-speed operation, while consuming minimal power with reduced EMI. In addition the differential signaling provides common mode noise rejection of ±1V.

Block Diagram



Pin Configuration



Absolute Maximum Ratings(1,2)

Supply Voltage (V_{CC}) 6.0V
Enable Input Voltage (DE, $\overline{RE}$).....–0.3V to (V_{CC} +0.3V)
Driver Input Voltage (DIN).....–0.3V to (V_{CC} +0.3V)
Receiver Output Voltage (R_{OUT}) .....–0.3V to (V_{CC} +0.3V)
Bus Pin Voltage (DO/RI±) ..... –0.3V to +3.9V
Driver Short Circuit ..... Continuous
ESD (HBM 1.5kΩ, 100pF)..... >10kV
Maximum Package Power Dissipation at 20°C
SOIC 1025mW
Derate SOIC Package ..... 8.2mW/°C
Storage Temperature Range .....–65°C to +150°C
Lead Temperature Range (Soldering, 4s) .....+260°C

Recommended Operating Conditions

	Min.	Max.	Units
Supply Voltage (V_{CC})	3.0	3.6	V
Receiver Input Voltage	0.0	2.9	V
Operating Free-Air Temperature	–40	+85	°C

Note:
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Functional Mode

Mode Select	DE	$\overline{RE}$
Driver Mode	H	H
Receiver Mode	L	L
3-State Mode	L	H
Loop Back Mode	H	L

Transmitter Mode

Inputs		Outputs	
DE	DI	DO+	DO-
H	L	L	H
H	H	H	L
H	2 > & > 0.8	X	X
L	X	Z	Z
H	Open	L	H

Receiver Mode

Inputs		Outputs
$\overline{RE}$	(RE+) - (RI-)	R_{OUT}
L	L (< -100mV)	L
L	H (> + 100mV)	H
L	100mV > & >-100mV	?
H	X	Z

Notes:
1. H = High, L = Low, Z = High Impedance, X = High or Low

Pin Description

Pin Name	Pin#	Inputs/ Outputs	Description
D_{IN}	2	I	TTL Driver Input
DO± RI±	6, 7	I/O	LVDS Driver Outputs/ LVDS Receiver Inputs
R_{OUT}	3	O	TTL Receiver Outputs
$\overline{RE}$	5	I	Receiver Enable TTL Input (Active Low)
DE	1	I	Driver Enable TTL Input (Active High)
GND	4	NA	Ground
V_{CC}	8	NA	Power Supply

DC Electrical Characteristics[2,3] (T_A = –40°C to +85°C, unless otherwise noted. V_{CC} = 3.3V ±0.3V)

Symbol	Parameter	Test Condition		Pin	Min.	Typ.	Max.	Units
V_{OD}	Output Differential Voltage	R_L = 27Ω, See figure 1		DO+/RI+ DO-/RI-	140	250	360	mV
ΔV_{OD}	V_{OD} Magnitude Change					3	30	
V_{OS}	Offset Voltage				1	1.25	1.65	V
ΔV_{OS}	Offset Magnitude Change					5	50	mV
I_{OSD}	Output Short Circuit Current	V_O = 0V, DE = V_{CC}				-12	-20	mA
V_{OH}	Voltage Output High	V_{ID} = +100mV	I_{OH} = -400	R_{OUT}	2.8	3		V
		Inputs Open			2.8	3		
		Inputs Shorted			2.8	3		
		Inputs Terminated, R_L = 27Ω			2.8	3		
V_{OL}	Voltage Output Low	I_{OL} = 2.0mA, V_{ID} = -100mV				0.1	0.4	
I_{OS}	Output Short Circuit Curretn	V_{OUT} = 0V, V_{ID} = 100V			-5	-35	-85	mA
V_{TH}	Input Threshold High	DE = 0V		DO+/RI+ DO-/RI-			100	mV
V_{TL}	Input Threshold Low				-100			
I_{IN}	Input Current	DE = 0V, V_{IN} = 2.4V or 0V			-20	±1	20	µA
		V_{CC} = 0V, V_{IN} = 2.4V or 0V			-20	±1	20	
V_{IH}	Minimum Input High Voltage			IN, DE, RE	2.0		V_{CC}	V
V_{IL}	Minimum Input Low Voltage				GND		0.8	
I_{IH}	Input High Current	V_{IN} = V_{CC} or 2.4V				±1	10	µA
I_{IL}	Input Low Current	V_{IN} = GND or 0.4V				±1	10	
V_{CL}	Input Diode Clamp Voltage	I_{CLAMP} = -18mA			-1.5	-0.8		V
I_{CCD}	Power Supply Current	DE = $\overline{RE}$ = V_{CC}, R_L = 27Ω		V_{CC}		13	20	mA
I_{CCR}		DE = $\overline{RE}$ = 0V				5	8	
I_{CCZ}		DE = 0V, $\overline{RE}$ = V_{CC}				3	7.5	
I_{CC}		DE = V_{CC}, $\overline{RE}$ - 0V, R_L = 27Ω				16	22	
C_{OUTPUT}	Bus Pin Capacitance			DO+/RI+ DO-/RI-		5		pF

Notes:

1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.
2. All currents into device pins are positive, all currents out of device pins are negative. All voltages are referenced to ground except: V_{OD}, V_{ID}, V_{TH}, and V_{TL}, unless otherwise specified.
3. All typicals are given for V_{CC} = +3.3V or 5.0V and T_A = +25°C unless otherwise stated.
4. ESD Rating: HBM (15kΩ, 100pF) > 2.0kV EAT (0Ω, 200pF) >300V.
5. C_L includes probe and jig capacitance.
6. Generator waveforms for all tests unless otherwise specified: f = 1MHz, ZO = 50Ω, t_r, $t_f \leq$ 6.0ns (0% - 100%) on control pins and ≤ 1.0ns for R_I inputs.
7. The PI90LVB010 is a current mode device and only functions with datasheet specification when a resistive load is appplied between the driver outputs.
8. For receiver disable delays, the switch is set to V_{CC} for t_{PZL}, and t_{PLZ} and to GND for t_{PZH} and t_{PHZ}.

AC Electrical Characteristics (T_A = –40°C to +85°C, V_{CC} = 3.3V ±0.3V)

Symbol	Paramter	Test Conditions	Min.	Typ.	Max.	Units
Differential Driver Timing Requirement						
t_{PHLD}	Differenital Propagation Delay High to Low	R_L = 27Ω Figures 2 & 3 C_L = 10pF	0.7	1.5	2.7	ns
t_{PLHD}	Differential Propagation Delay Low to High		0.7	1.5	2.7	
t_{SKD}	Differential Skew | t_{PHLD} - t_{PLHD} |			0.2	1.0	
t_{TLH}	Transition Time Low to High			0.3	0.9	
t_{THL}	Transition Time High to Low			0.3	0.9	
t_{PHZ}	Disable Time High to Z	R_L = 27Ω Figures 4 & 5 C_L = 10pF	0.5	2.6	3.3	
t_{PLZ}	Disable Time Low to Z		0.5	2.6	3.3	
t_{PZH}	Enable Time Z to High		0.5	2.6	3.3	
t_{PZL}	Enable Time Z to Low		0.5	2.6	3.3	
Differential Receicer Timing Requirements						
t_{PHLD}	Differential Propagation Delay High to Low	Figures 6 & 7 C_L = 10pF	1.3	2.1	3.2	ns
t_{PLHD}	Differenital Propagation Delay Low to High		1.3	2.1	3.2	
t_{SKD}	Differential Skew | t_{PHLD} - t_{PLHD} |			0.5	2.0	
t_R	Rise Time			0.8	1.4	
t_F	Fall Time			1.8	1.4	
t_{PHZ}	Disable Time High to Z	R_L = 500Ω Figures 8 & 9 C_L = 10pF(8)	1.5	4.0	6.0	
t_{PLZ}	Disable Time Low to Z		5.0	4.0	7.0	
t_{PZH}	Enable Time Z to High		0.5	2.5	7.0	
t_{PZL}	Enable Time Z to Low		0.5	2.5	6.0	

Test Circuits and Timing Waveforms

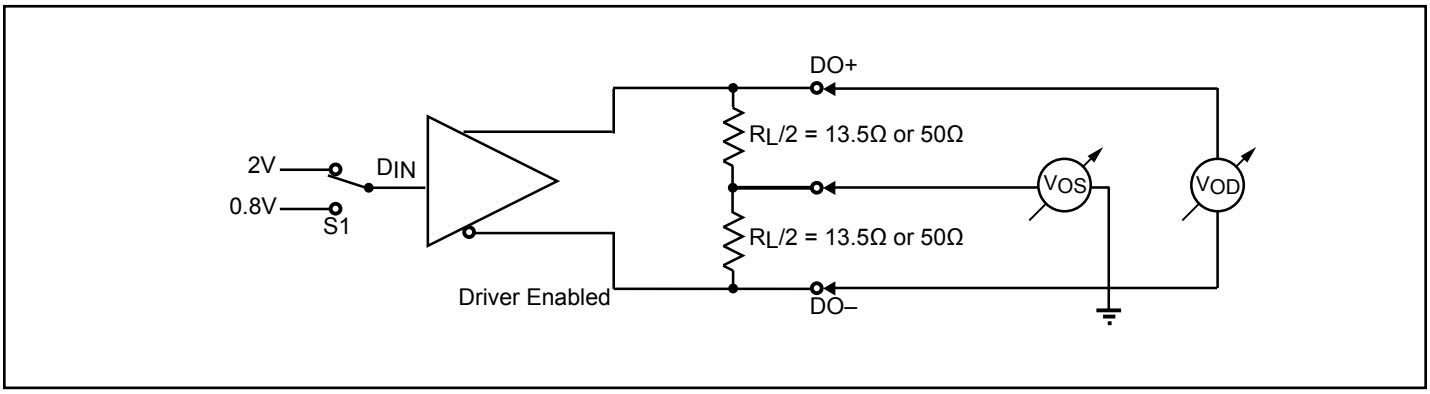


Figure 1. Differential Driver DC Test Circuit

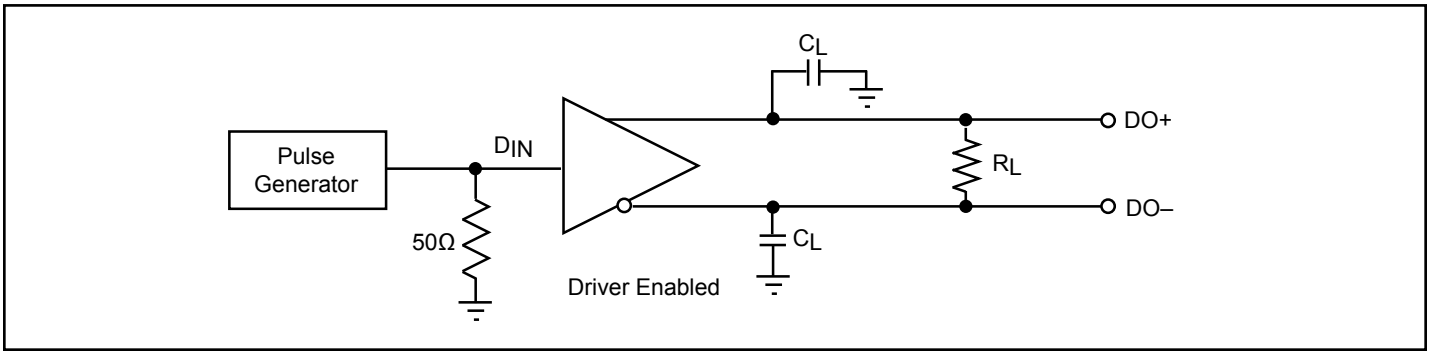


Figure 2. Differential Driver Propagation Delay and Transition Time Test Circuit

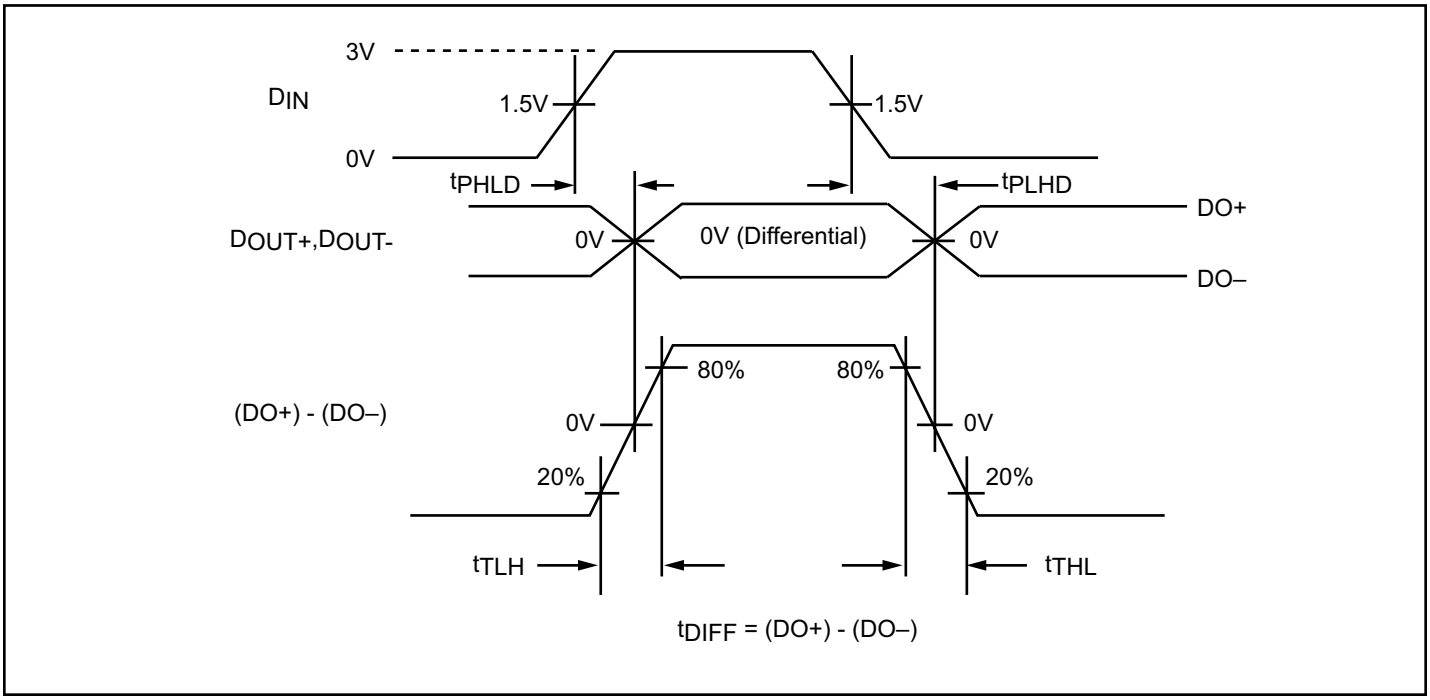


Figure 3. Driver Propagation Delay and Transition Time Waveforms

Test Circuits and Timing Waveforms (continued)

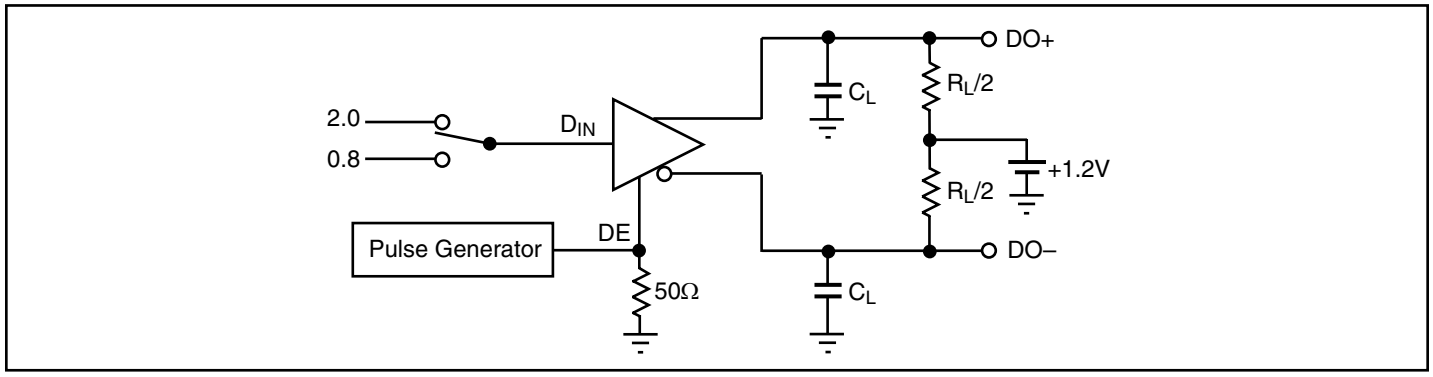


Figure 4. Driver Three-State Delay Test Circuit

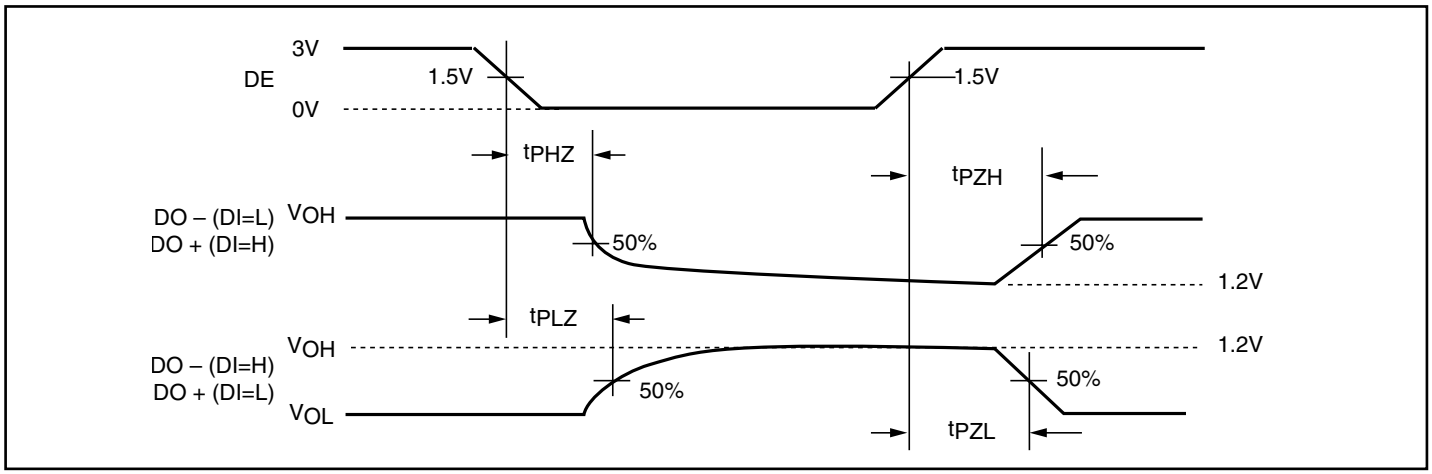


Figure 5. Driver Three-State Delay Waveforms

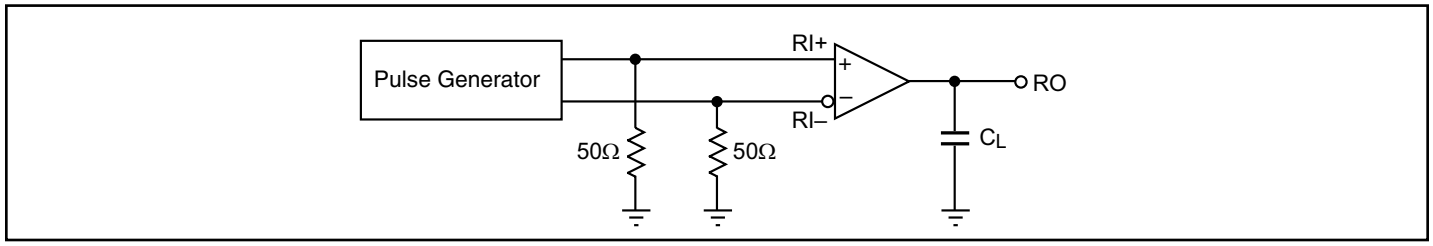


Figure 6. Receiver Propagation Delay and Transistion Time Test Circuit

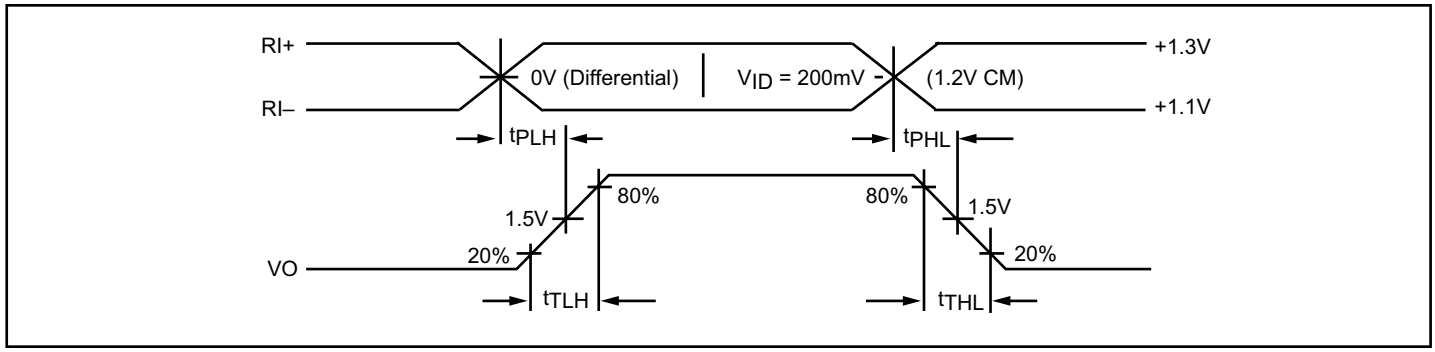


Figure 7. Receiver Propagation Delay and Transistion Time Waveforms

Test Circuits and Timing Waveforms (continued)

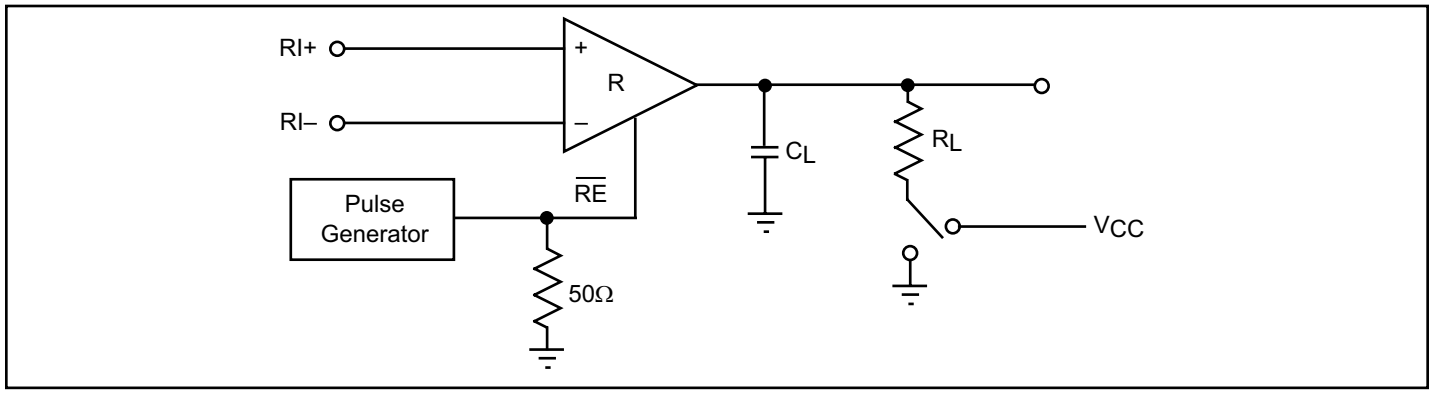


Figure 8. Receiver Three-State Delay Test Circuit

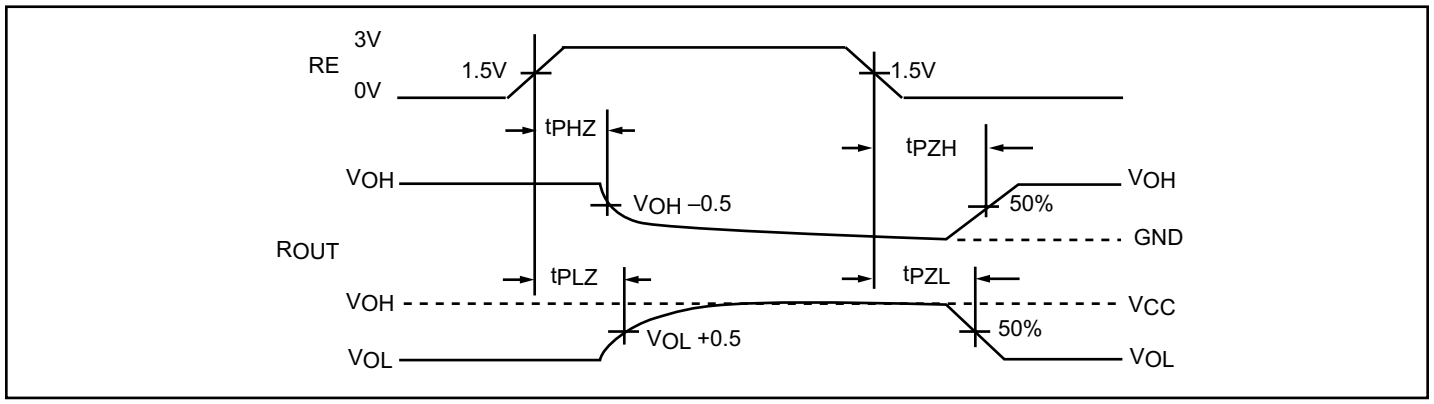


Figure 9. Receiver Three-State Delay Waveforms

Typical Bus Application Configurations

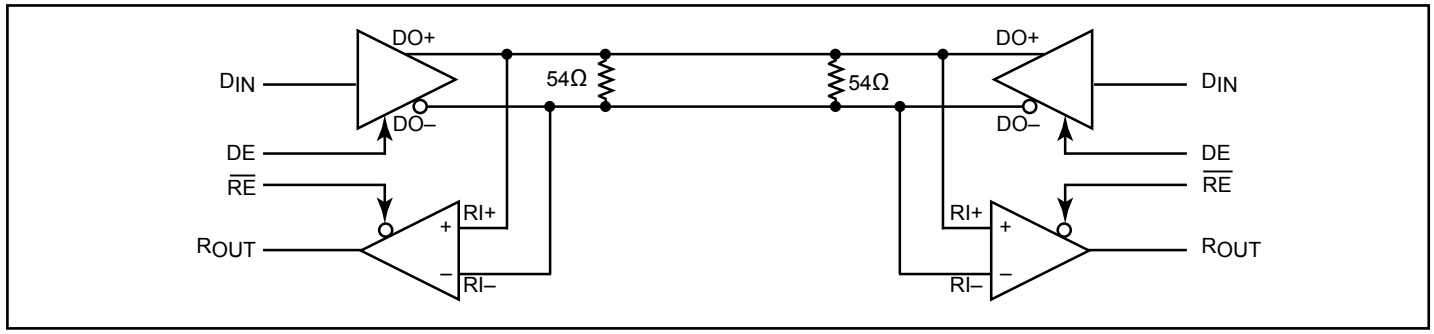


Figure 10. Bidirectional Half-Duplex Point-to-Point Applications

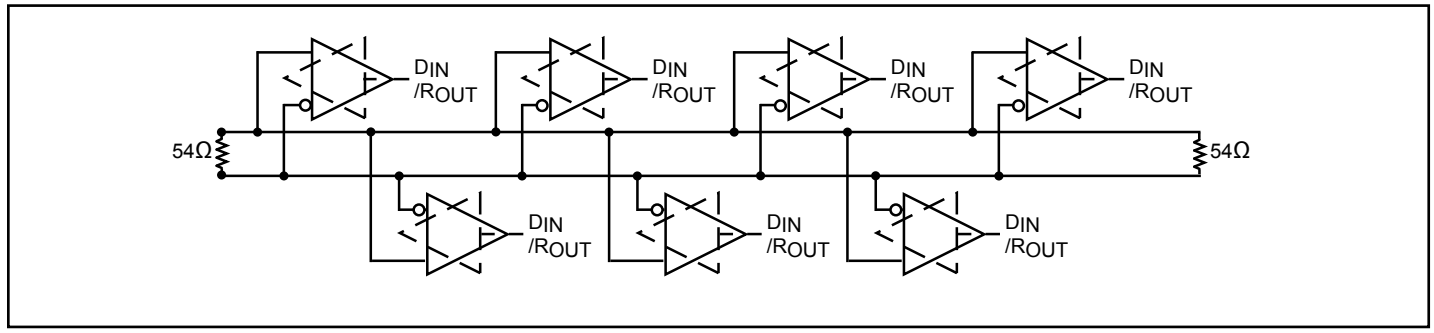
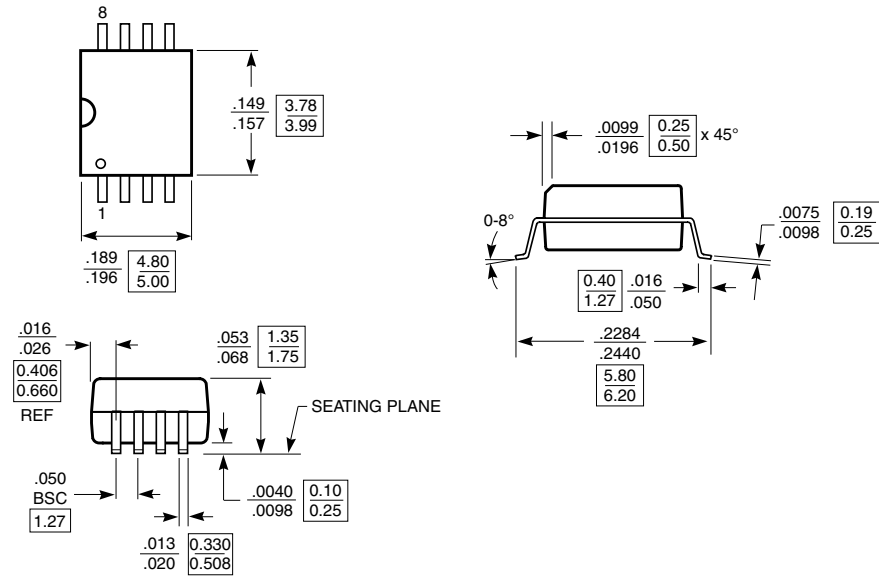
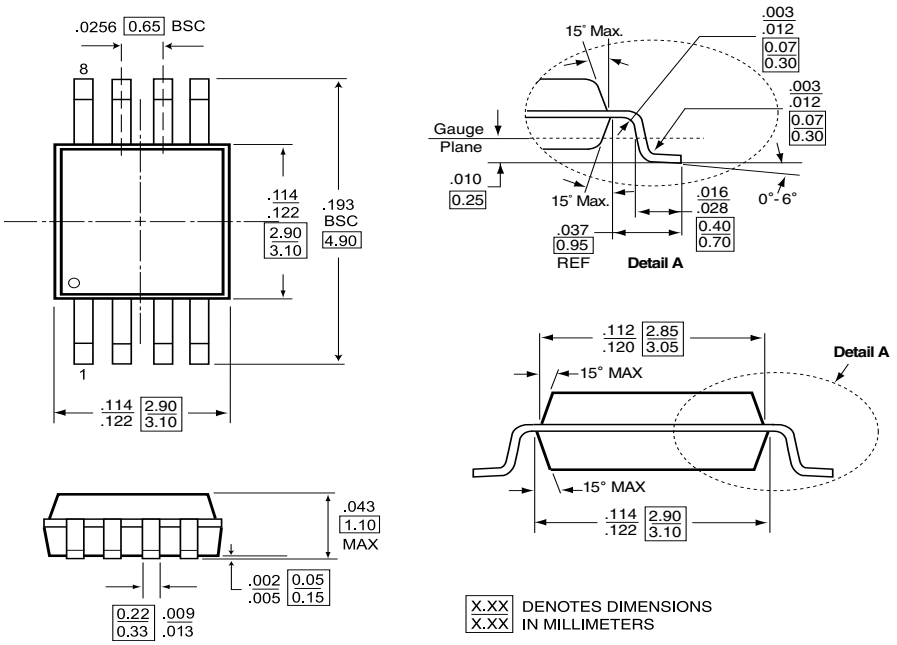


Figure 11. Multipoint Bus Applications

Packaging Mechanical: 8-Pin SOIC (W)



Packaging Mechanical: 8-Pin MSOP (U)



Ordering Information

Ordering Code	Package Code	Package Description
PI90LVB010WE	W	Pb-free & Green, 8-pin, SOIC
PI90LVB010UE	U	Pb-free & Green, 8-pin MSOP

Notes:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/