REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change in table I, I_{OZ} parameter. Also changes to footnotes 3 and 4. Editorial changes throughout.	89-05-18	M. A. Frye
B	Changes in accordance with NOR 5962-R227-92.	92-06-24	M. A. Frye
C	Update drawing to current requirements. Removed logic diagram. Editorial changes throughout. - gap	01-10-18	Raymond Monnin
D	Boilerplate update part of 5 year review. ksr	06-08-18	Raymond Monnin

THE ORIGINAL FRONT PAGE HAS BEEN REPLACED.

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REV STATUS				REV			D	D	D	D	D	D	D	D	D	D	D	D		
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

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DRAWING APPROVAL DATE
88-01-22

REVISION LEVEL
D

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, BIPOLAR, FIELD PROGRAMMABLE, LOGIC ARRAY (FPLA), MONOLITHIC SILICON

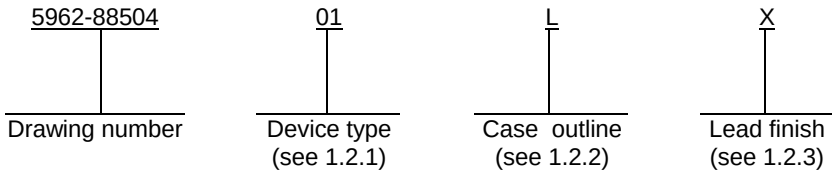
SIZE	CAGE CODE	
A	**67268**	**5962-88504**

SHEET 1 OF 12

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	PLS161	(12 x 48 x 8) programmable logic array
02	PLS173	(22 x 42 x 10) programmable logic array

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage (V_{CC}) ..... +7.0 V dc
Input voltage (V_I):
  Device 01 ..... +5.5 V dc
  Device 02 ..... +10 V dc
Storage temperature range ..... -65°C to +150°C
Maximum power dissipation 1/ ..... 1.0 watt
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}):
  Case L ..... See MIL-STD-1835
Junction temperature (T_J) ..... +200°C
Output sink current ..... +100 mA

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) ..... +4.5 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH}) ..... +2.0 V dc
Maximum low level input voltage (V_{IL}) ..... +0.8 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C

1/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2.1 Government specification, standards, and handbooks. The following specification, standards and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract, using an altered item drawing.

3.10.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 4.3.1c and table II. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.10.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. All devices processed to an altered item drawing may be programmed either before or after burn-in at the manufacturer's discretion. The required electrical testing shall include, as a minimum, the final electrical tests for programmed devices as specified in table II herein.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirement of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:

(1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing in accordance with the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming. If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than four total device failures allowable.

Ten devices from the programmability sample shall be submitted to the requirements for group A, subgroups 9, 10, and 11. If more than two total devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than four total device failures allowable.

d. Subgroups 7 and 8 must verify input to output logic combinations.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Device types	Group A subgroups	Limits		Unit
						Min	Max	
Low level input voltage	V_{IL}	V_{CC} = 4.5 V		All	1, 2, 3		0.8	V
High level input voltage	V_{IH}	V_{CC} = 5.5 V		All	1, 2, 3	2		V
Input clamp voltage 2/	V_{IC}	V_{CC} = 4.5 V, I_I = -18 mA		All	1, 2, 3		-1.2	V
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_I = 0.45 V		All	1, 2, 3		-150	µA
High level input current	I_{IH}	V_{CC} = 5.5 V, V_I = 5.5 V		All	1, 2, 3		50	µA
Low level output voltage 4/	V_{OL}	V_{CC} = 4.5 V, V_{IH} = 2 V, VIL = 0.8 V	I_{OL} = 9.6 mA	01	1, 2, 3		0.5	V
			I_{OL} = 12 mA	02			0.5	
High level output voltage 3/, 9/	V_{OH}	V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2 V, I_{OH} = -2 mA		All	1, 2, 3	2.4		V
Output short circuit current 2/, 5/, 6/	I_{OS}	V_{CC} = 5.5 V, V_O = 0 V		All	1, 2, 3	-15	-85	mA
DC supply current 7/	I_{CC}	V_{CC} = 5.5 V		01	1, 2, 3		180	mA
				02	1, 2, 3		170	mA
3-state output current 8/ I/O pins only	I_{OZ}	V_{CC} = 5.5 V	V_{OUT} = 5.5 V	01	1, 2, 3		60	µA
			V_{OUT} = 0.45 V	01			-60	
			V_{OUT} =5.5 V	02			±110	
			V_{OUT} = 0.45 V	02			±210	
Functional tests		See 4.3.1d		All	7, 8			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Propagation delay output to input	t_{PD}	V_{CC} = 5.0 V ±10% R1 = 470Ω, R2 = 1 KΩ, See figures 2 and 3	01	9, 10, 11		70	ns
			02	9, 10, 11		40	ns
Propagation delay chip enable	t_{CE}		01	9, 10, 11		50	ns
Propagation delay 9/ output enable	t_{OE}		02	9, 10, 11		35	ns
Disable time chip disable	t_{CD}		01	9, 10, 11		50	ns
Disable time 9/ 10/ output disable	t_{OD}		02	9, 10, 11		35	ns

1/ All voltage values are with respect to ground.

2/ Test one at a time.

3/ For device 01: measured with V_{IL} applied to $\overline{CE}$. For device 02: measured with pins 1-5 = 0 V, pins 6-10 = 4.5 V, pin 11 = 10 V and pin 13 = 10 V.

4/ For device 01: measured with a programmed logic condition for which the output test is at a low logic level. For device 02: pins 1 - 5 = 0 V, pins 6 -10 = 4.5 V, pin 11 = 0 V, pin 13 = 10 V.

5/ For device 01: on unprogrammed device apply 10 V I_0-I_{11}. For device 02: same conditions as listed in note 3 above, except pin 11 = +10 V.

6/ Duration of short circuit should not exceed 1 second.

7/ For device 01: I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5 V and the outputs open. For device 02: I_{CC} is measured with I_0 and I_1 = 0 V and I_2-I_{11} and B_0-B_9 = 4.5 V. Part in virgin state.

8/ Leakage values are a combination of input and output leakage.

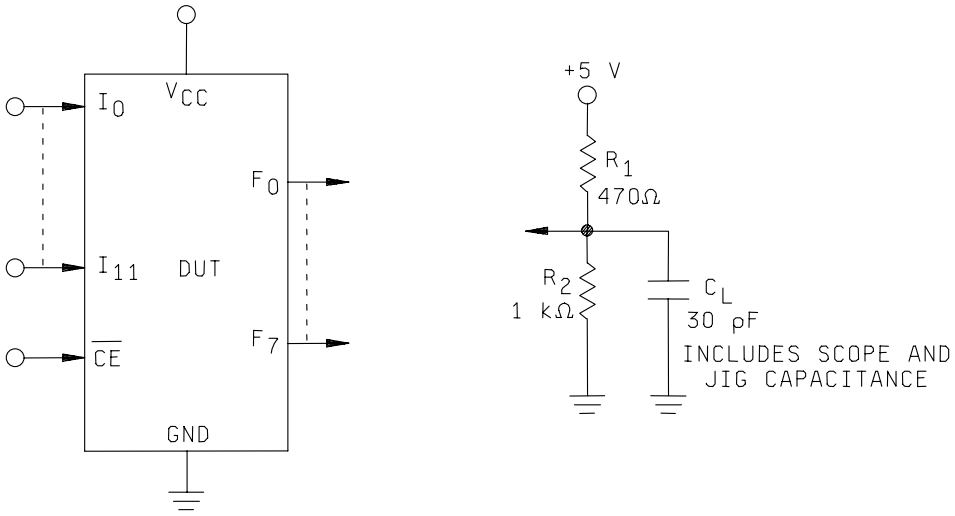
9/ Not testable on unprogrammed devices.

10/ Measured at $V_T = V_{OL}$ + 0.5 V.

Device types	01	02
Case outlines	L	L
Terminal number	Terminal symbol	Terminal symbol
1	FE	I0
2	I5	I1
3	I4	I2
4	I3	I3
5	I2	I4
6	I1	I5
7	I0	I6
8	F7	I7
9	F6	I8
10	F5	I9
11	F4	I10
12	GND	GND
13	F3	I11
14	F2	B0
15	F1	B1
16	F0	B2
17	$\overline{CE}$	B3
18	I11	B4
19	I10	B5
20	I9	B6
21	I8	B7
22	I7	B8
23	I6	B9
24	V_{CC}	V_{CC}

FIGURE 1. Terminal connections.

DEVICE TYPE 01



DEVICE TYPE 02

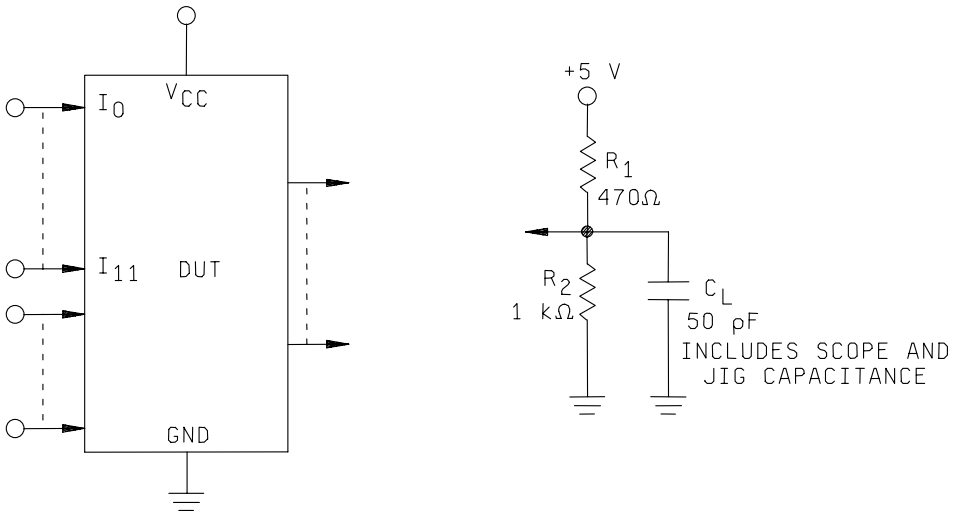
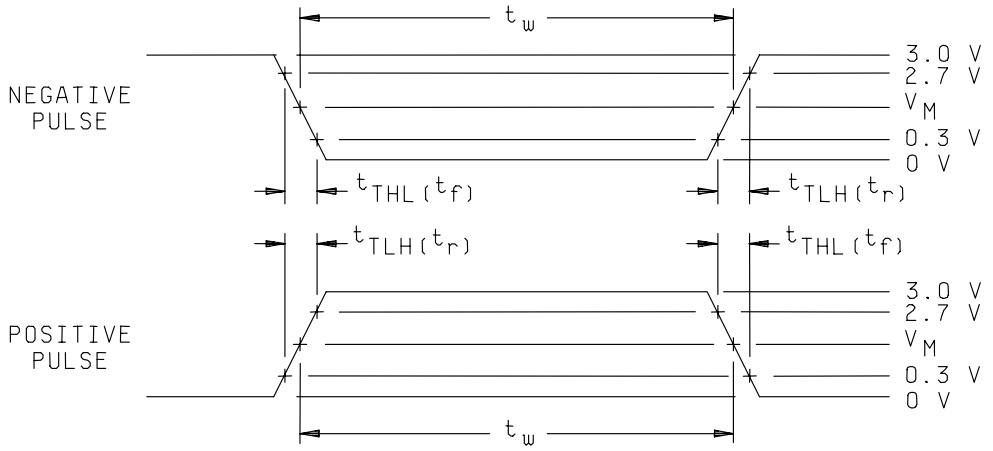


FIGURE 2. Test load circuits.

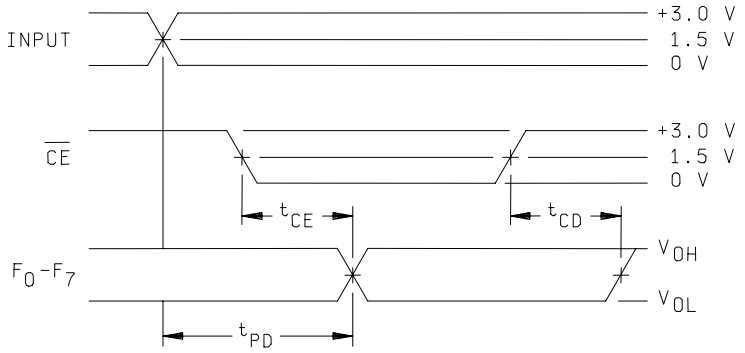
DEVICE TYPES 01 AND 02



Input pulse characteristics				
V_M	Rep. rate	Pulse width	t_{TLH}	t_{THL}
1.5 V	1 MHz	500 ns	≤ 5 ns	≤ 5 ns

FIGURE 3. Timing waveforms.

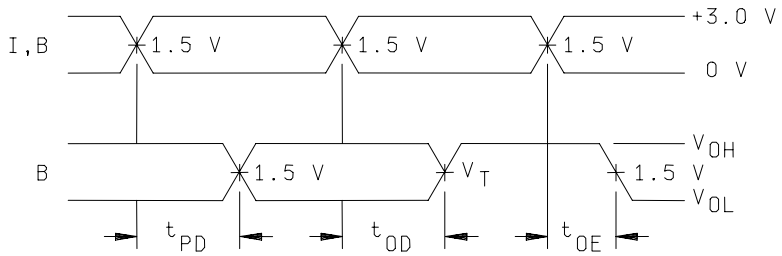
DEVICE TYPE 01



TIMING DEFINITIONS

T_{CE} Delay between beginning of Chip Enable low (with input valid) and when Data Output becomes valid.
T_{CD} Delay between when Chip Enable becomes high and Data Output is in off state (Hi-Z or high).
T_{PD} Delay between beginning of valid input (with Chip Enable low) and when Data Output becomes valid.

DEVICE TYPE 02



TIMING DEFINITIONS

T_{PD} Propagation delay between input and output.
T_{OD} Delay between input change and when output is off (Hi-Z or high).
T_{OE} Delay between input change and when output reflects specified output level.

FIGURE 3. Timing waveforms Continued.

TABLE II. Electrical test requirements. 1/, 2/, 3/

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004) for programmed devices	1*, 2, 3, 7*, 8 9
Final electrical test parameters (method 5004) for unprogrammed devices	1*, 2, 3, 7*, 8
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

1/ * PDA applies to subgroup 1 and 7.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional test shall also verify that no fuses are blown for unprogrammed devices or that the altered item drawing pattern exists for programmed devices (see table II).

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone 614-692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-08-18

Approved sources of supply for SMD 5962-88504 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8850401LA	3/	PLS161/BLX
5962-8850402LA	3/	ASPLS173C24/883C
5962-8850402LA	0C7V7	PLS173/BLA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor. 2945 Oakmead Village Court Santa Clara, CA 95051

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.