MOSFET – Power, Single N-Channel, PQFN8

80 V, 32 A

NTMFS006N08MC, NTMFS006N08MC-NC

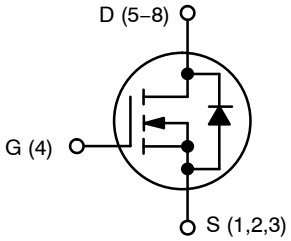
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
80 V	6.0 mΩ @ 10 V	32 A
80 V	17 mΩ @ 6 V	16 A

Features

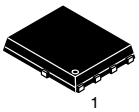
- Advanced Package (5 x 6mm) with Excellent Thermal Conduction
- Ultra Low $R_{DS(on)}$ to Improve System Efficiency
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Hot Swap Application
- Power Load Switch
- Battery Management and Protection

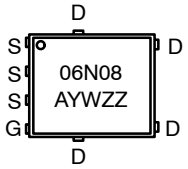


N–CHANNEL MOSFET



PQFN8
T1 SUFFIX
CASE 483AE

MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceabililty

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Symbol	Parameter			Value	Unit
V_{DSS}	Drain-to-Source Voltage			80	V
V_{GS}	Gate-to-Source Voltage			±20	V
I_D	Continuous Drain Current $R_{\theta JC}$ (Note 3)	Steady State	T_C = 25 °C	82	A
			T_C = 85 °C	59	
P_D	Power Dissipation $R_{\theta JC}$ (Note 3)		T_C = 25 °C	78	W
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3)	Steady State	T_A = 25 °C	14.7	A
			T_A = 85 °C	10.6	
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1, 3)		T_A = 25 °C	2.5	W
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 2, 3)		T_A = 25 °C	9.3	A
			T_A = 85 °C	6.7	
P_D	Power Dissipation $R_{\theta JA}$ (Notes 2, 3)		T_A = 25 °C	1.0	W
I_{DM}	Pulsed Drain Current	T_A = 25 °C, t_p = 10 μs		216	A
E_{AS}	Single Pulse Drain-to-Source Avalanche Energy (I_L = 32 A_{pk})			51	mJ
T_J, T_{stg}	Operating Junction and Storage Temperature Range			−55 to +175	°C
T_L	Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 in^2 pad, 2 oz Cu pad.
2. Surface-mounted on FR4 board using minimum pad size, 2 oz Cu pad.
3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

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THERMAL RESISTANCE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case-Steady State	1.61	°C/W
$R_{\theta JA}$	Junction-to-Ambient-Steady State (Note 4)	50	
$R_{\theta JA}$	Junction-to-Ambient-Steady State (Note 5)	125	

4. Surface-mounted on FR4 board using 1 in^2 pad, 2 oz Cu pad.
5. Surface-mounted on FR4 board using minimum pad size, 2 oz Cu pad.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA		80			V
$V_{(BR)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient	I_D = 250 μA. ref to 25 °C			96.6		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 64 V	T_J = 25 °C			1.0	μA
			T_J = 125 °C			100	
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 6)							
$V_{GS(TH)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA		2.0		4.0	V
$V_{GS(TH)}/T_J$	Threshold Temperature Coefficient	I_D = 200 μA. ref to 25 °C			−5		mV/°C
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 10 V	I_D = 32 A		4.9	6.0	mΩ
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 6 V	I_D = 16 A		10.2	17	mΩ
R_G	Gate Resistance	T_A = 25 °C			0.3		Ω
CHARGES AND CAPACITANCES							
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 40 V, f = 1 MHz			2300		pF
C_{OSS}	Output Capacitance				710		
C_{RSS}	Reverse Transfer Capacitance				31		
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 10 V, V_{DS} = 40 V; I_D = 32 A			30		nC
$Q_{G(TH)}$	Threshold Gate Charge				3.3		
Q_{GS}	Gate-to-Source Charge				10		
Q_{GD}	Gate-to-Drain Charge				6.0		
SWITCHING CHARACTERISTICS (Note 7)							
$t_{d(ON)}$	Turn-On Delay Time	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 32 A, R_G = 2.5 Ω			13		ns
t_r	Rise Time				4		
$t_{d(OFF)}$	Turn-Off Delay Time				18		
t_f	Fall Time				4		
DRAIN−SOURCE DIODE CHARACTERISTICS							
V_{SD}	Forward Diode Voltage	V_{GS} = 0 V, I_S = 32 A	T_J = 25 °C		0.84	1.2	V
			T_J = 125 °C		0.78		
t_{RR}	Reverse Recovery Time	V_{GS} = 0 V, dIS/dt = 100 A/μs, I_S = 32 A			49.58		ns
Q_{RR}	Reverse Recovery Charge				51.4		nC

6. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
7. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

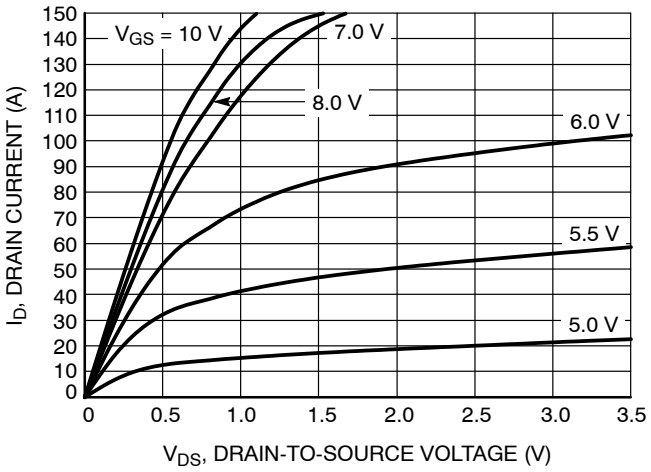


Figure 1. On-Region Characteristics

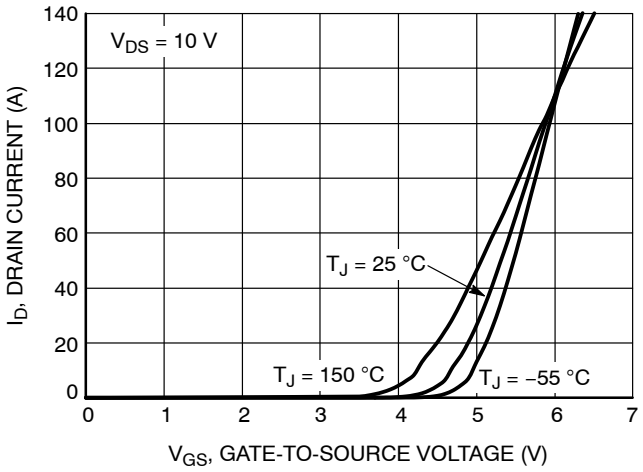


Figure 2. Transfer Characteristics

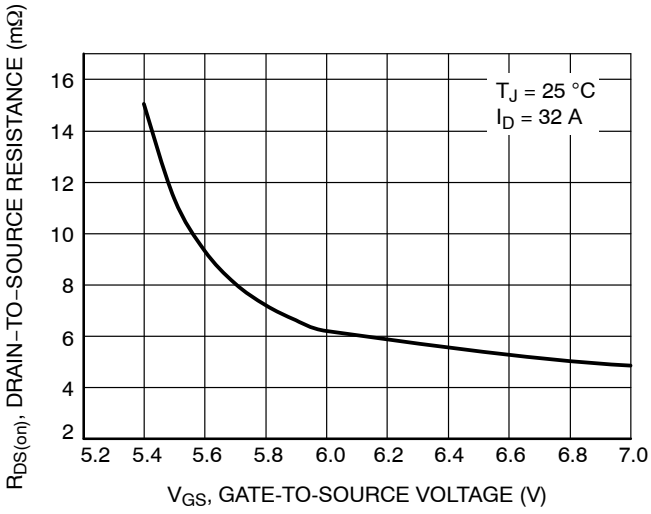


Figure 3. On-Resistance vs. Gate-to-Source Voltage

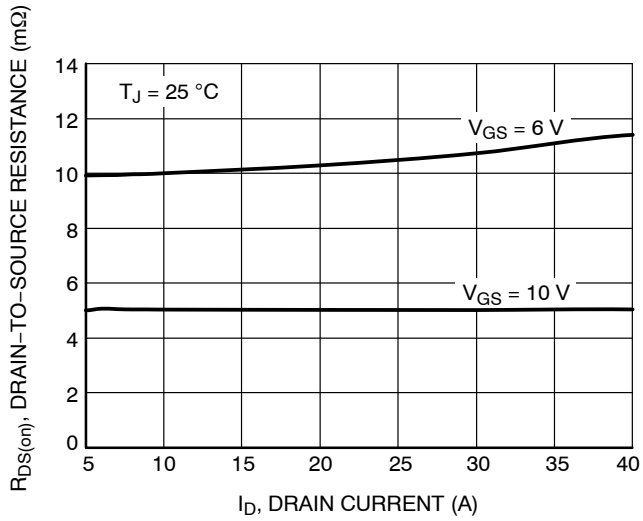


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

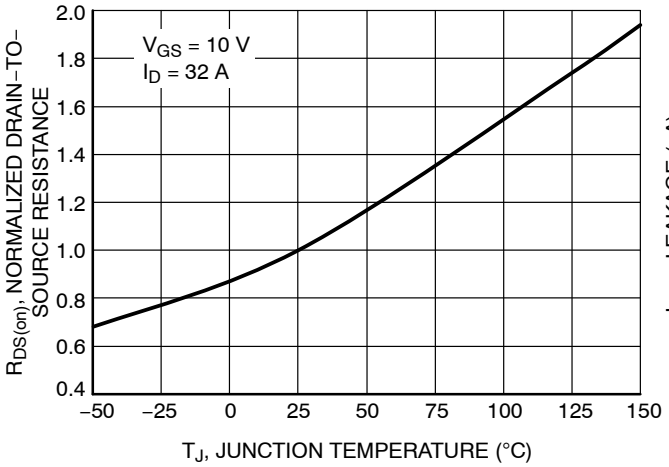


Figure 5. On-Resistance Variation with Temperature

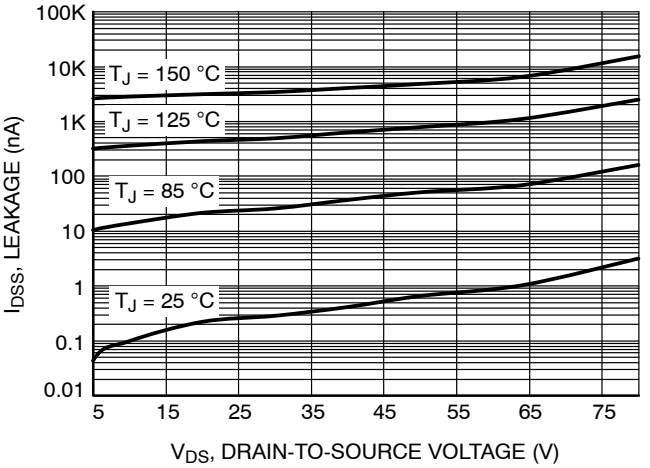


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

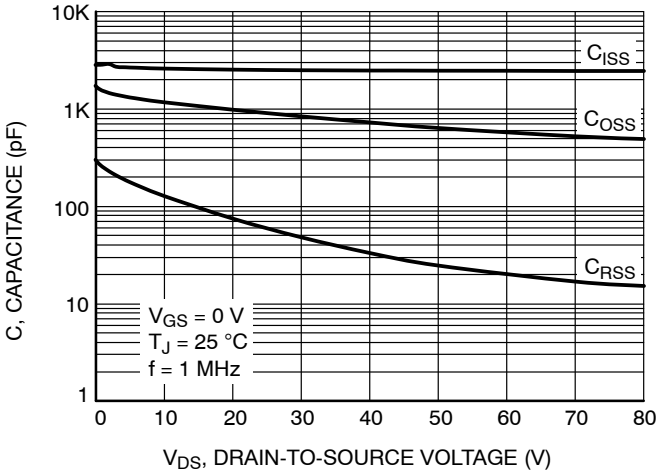


Figure 7. Capacitance Variation

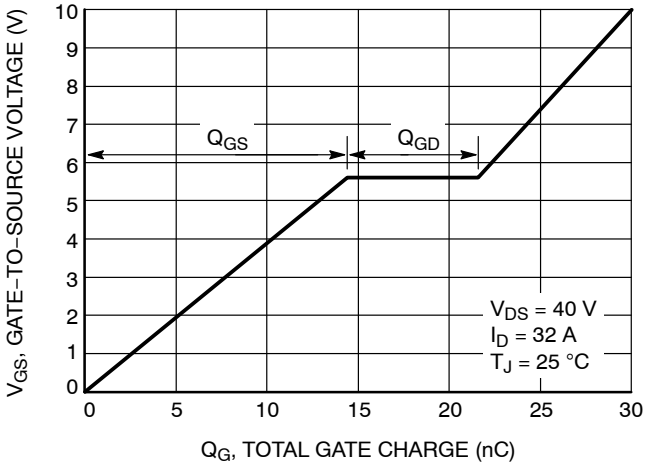


Figure 8. Gate-to-Source Voltage vs. Total Charge

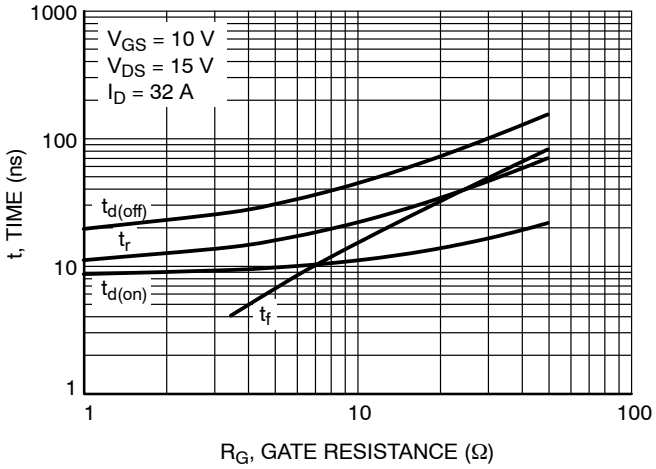


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

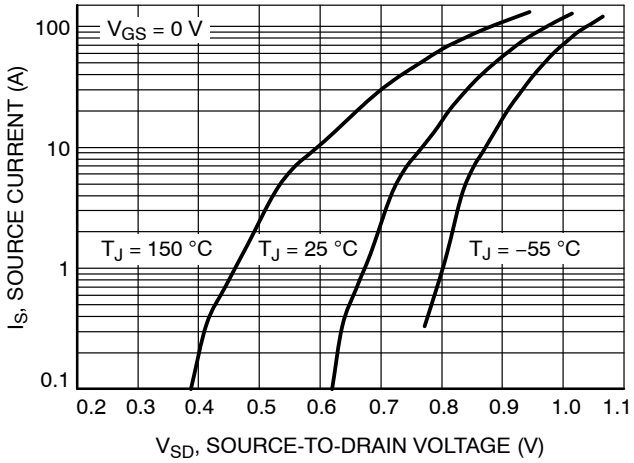


Figure 10. Diode Forward Voltage vs. Current

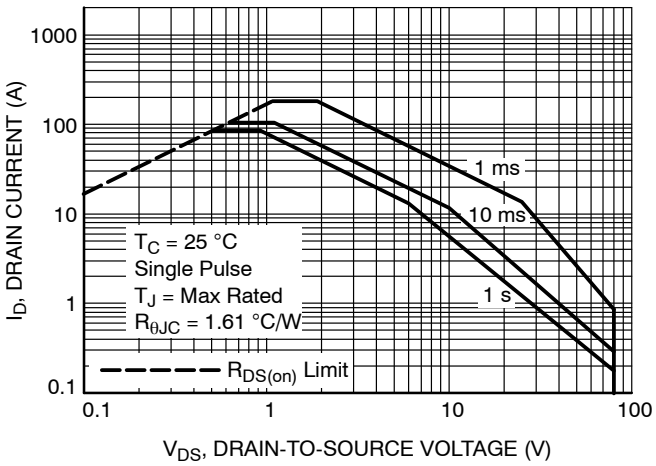


Figure 11. Safe Operating Area

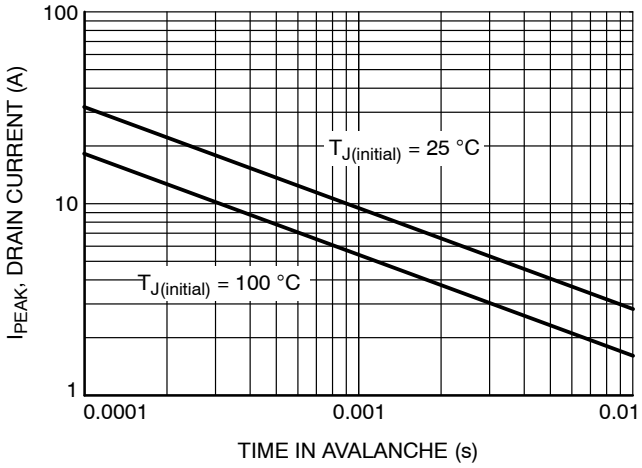


Figure 12. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

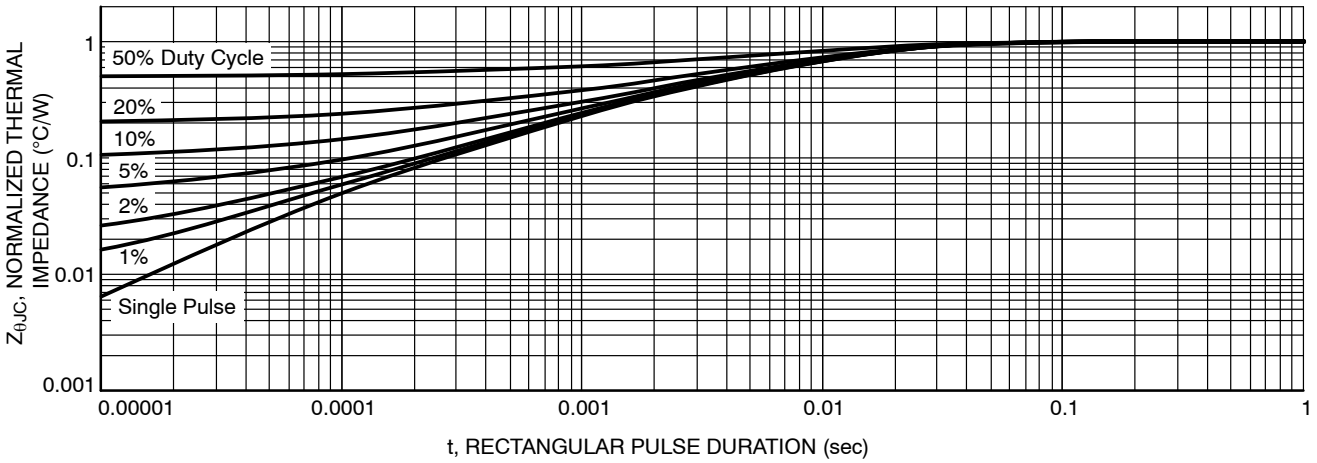


Figure 13. Transient Thermal Response

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTMFS006N08MC	06N08	PQFN8 (Pb-Free)	3000 / Tape & Reel
NTMFS006N08MC-NC	06N08	PQFN8 (Pb-Free)	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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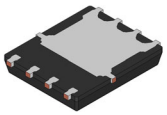
REVISION HISTORY

Revision	Description of Changes	Date
2	Adding NTMFS006N08MC-NC OPN + Rebranded to **onsemi**	2/4/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

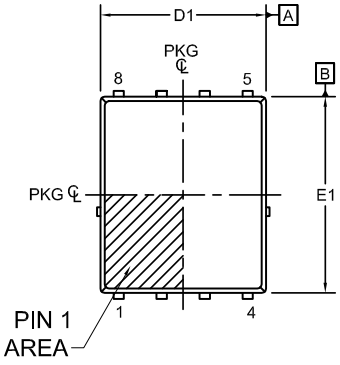
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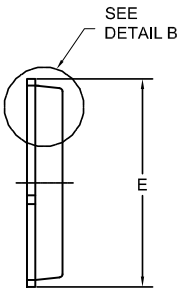


PQFN8 5X6, 1.27P
CASE 483AE
ISSUE C

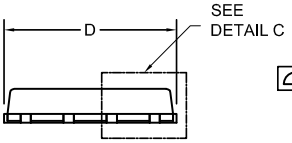
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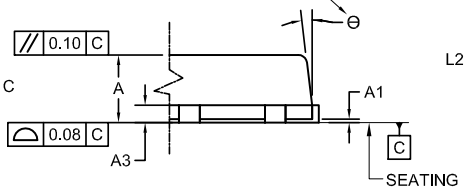
TOP VIEW



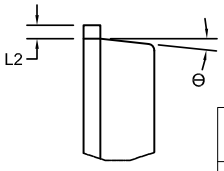
OPTIONAL DRAFT
ANGLE MAY APPEAR
ON FOUR SIDES
OF THE PACKAGE



SIDE VIEW



DETAIL C
SCALE: 2:1

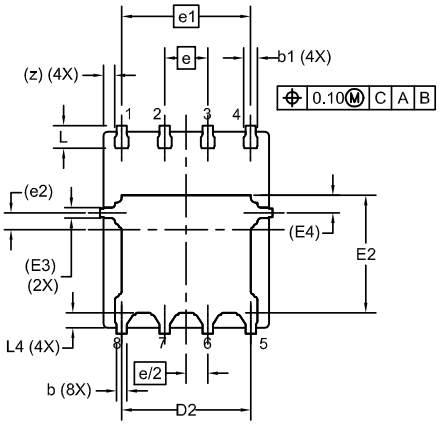


DETAIL B
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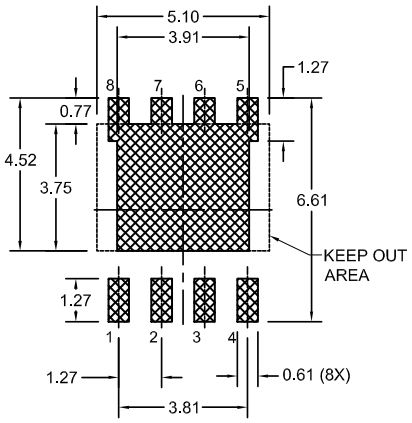
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
Θ	0°	-	12°



BOTTOM VIEW



LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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