A6274-1
A6284, A6284-1

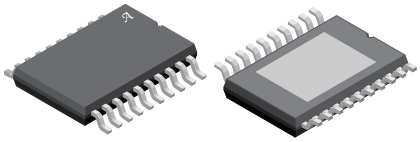
Linear Current Regulator and Controller for Automotive LED Arrays

FEATURES AND BENEFITS

- Six LED current sinks rated up to 60 mA (A6274) or 120 mA (A6284)
- Total LED drive current—up to 360 mA or 720 mA
- Wide input voltage range of 5 to 42 V for start/stop, cold-crank, and load-dump requirements
- Low-dropout voltage—drives two series WLEDs from 7 V input
- Gate driver for external ballast P-MOSFET
- LEDs combined in two groups with separate ENx and ISETx
- LED current level set by external reference resistors
- Internal or external PWM dimming
- Controlled output drivers slew during PWM for lower EMI
- Fault detection features: LED string open, LED pin short-to-ground, single LED short, VOUT short-to-ground, VIN overvoltage, and thermal protection
- Input supply and temperature-based derating
- Automotive K-temperature range (–40°C to 150°C)

PACKAGES:

20-Pin eTSSOP (LP) with Exposed Thermal Pad
AEC-Q100 qualified



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DESCRIPTION

The A6274 and A6284 are programmable linear current regulator ICs for driving automotive LED arrays. The LED current is programmed by external resistors. These devices sink up to 60 mA (A6274) or 120 mA (A6284), from each of six LED pins, to drive strings of high-brightness LEDs. LED pins can be paralleled to drive even higher current LED strings. Current settings are typically accurate to 2%, while typical matching between LED strings is 0.8%.

LED light output can be adjusted by PWM dimming. The ICs provide an internal PWM dimming circuit that is programmed by external resistors for PWM frequency and duty cycle. It can also accept an external PWM signal. Multiple ICs can be configured in parallel for larger lighting systems. An internal FULL (V_{DR} > 3.6 V) option is provided to override the PWM-dimming ratio for full LED current.

LED current derating with temperature and programmable VIN levels allows operation over a wide range of operating conditions.

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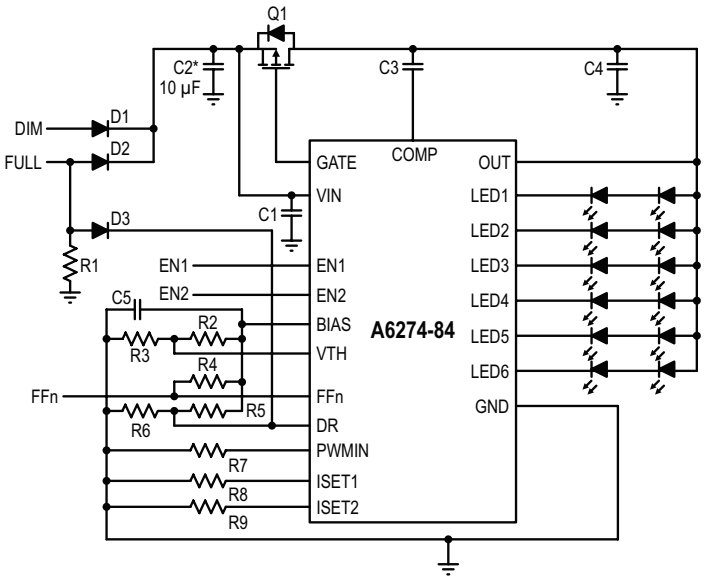
APPLICATIONS

- Automotive rear combination light
- DRL/position
- General automotive lighting



* C2 should be placed as close to the input connector as possible.
Good filter layout practices should be adhered to.

Figure 1: Typical Application Diagram for "-1" Latching Version

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DESCRIPTION (continued)

A GATE pin is provided to drive an external P-channel MOSFET, which serves as an active ballast resistor to reduce the heat dissipation within the IC package. It also serves as an input disconnect switch in the event of an LED string short-to-ground fault.

The A6284 provides a non-latching option while the A6274-1 and A6284-1 provide a latching option.

SPECIFICATIONS

SELECTION GUIDE

Part Number	$I_{LED(MAX)}$	FAULT Response (see Table 2 for details)	Package	Packing [1]
A6284KLPTR-T	120 mA per channel	Unlatched MODE0	20-pin eTSSOP with thermal pad	4,000 pieces per 13-in. reel
A6274KLPTR-T-1	60 mA per channel	Latched MODE1		
A6284KLPTR-T-1	120 mA per channel	Latched MODE1		

[1] Contact Allegro™ for additional packing options.

ABSOLUTE MAXIMUM RATINGS [2]

Characteristic	Symbol	Notes	Rating	Unit
VIN, OUT, DR, EN1, EN2, COMP, FFn	V_{IN}, V_{OUT}, V_{COMP}, V_{DR}, V_{EN1}, V_{EN2}, V_{FFn}		−0.3 to 45	V
GATE	V_{GATE}		Max of (–0.3 or V_{IN} – 9) to 45	V
LED1 to LED6	V_{LEDx}		−0.5 to 45	V
All Other Pins			−0.3 to 6.5	V
Junction Temperature	T_J		−40 to 150	°C
Transient Junction Temperature	T_{Jt}	Overtemperature event not exceeding 10 seconds, lifetime duration not exceeding 10 hours, determined by design characterization.	175	°C
Storage Temperature Range	T_{stg}		−55 to 150	°C

[2] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions [3]	Value	Unit
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	Estimated, on 4-layer PCB based on JEDEC standard	29	°C/W

[3] Additional thermal information available on the Allegro website.

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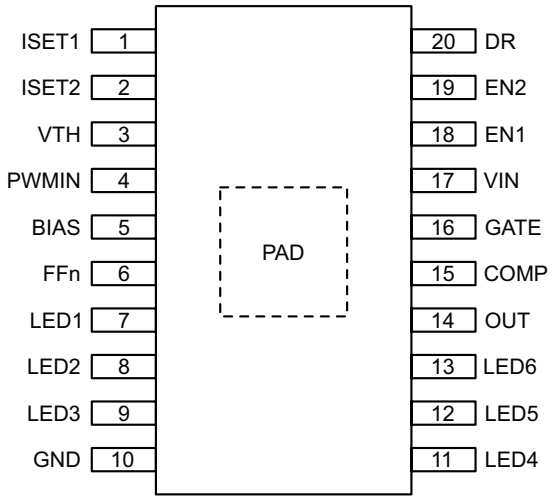
PINOUT DIAGRAM AND TERMINAL LIST TABLE



Package LP, 20-Pin eTSSOP Pinout Diagram

Terminal List Table

Number	Symbol	Function
1	ISET1	Sets LEDx sink current for LED1-3. Connect resistor to GND to set current, up to 60 mA (A6274) or 120 mA (A6284) per channel.
2	ISET2	Sets LEDx sink current for LED4-6. Connect resistor to GND to set current, up to 60 mA (A6274) or 120 mA (A6284) per channel. Connect ISET2 to BIAS if only one resistor setting is required for LED1-6.
3	VTH	Sets input voltage threshold for current foldback and V_{OUT} threshold for open-LED fault (D, E, F, and G) disable threshold.
4	PWMIN	PWM frequency setting. Internal PWM frequency set when connected to GND through a resistor and uses external PWM when a logic signal is applied to this pin.
5	BIAS	Output of internal bias regulator. Connect a 1 µF decoupling capacitor near to IC pin. BIAS pin can deliver up to 7 mA to an external load.
6	FFn	Active-low fault flag. This pin can be used as an input pin while using “-1” latching version. If pulled low, IC will turn all LEDs off for one-out-all-out functionality across multiple chips in the system.
7, 8, 9	LED1-3	Three LED current sinks. Connect the cathode of each LED string to these pins.
10	GND	Ground pin.
11, 12, 13	LED4-6	Three LED current sinks. Connect the cathode of each LED string to these pins.
14	OUT	Connect to drain of series-pass MOSFET.
15	COMP	Connect a 470 nF capacitor across COMP pin and drain node of external PMOS. If PMOS is not used, connect this pin to VIN.
16	GATE	Gate drive for series-pass MOSFET. If PMOS is not used, connect this pin to VIN.
17	VIN	Input voltage to IC. Connect to source of series-pass P-channel MOSFET. Connect a decoupling capacitor close to this pin.
18	EN1	Active-high-enable input for LED1-3.
19	EN2	Active-high-enable input for LED4-6.
20	DR	Voltage on this pin sets dimming duty cycle when $0 < V_{DR} < 3.6$ V. IC operates with 100% duty cycle in internal and external PWM mode when $V_{DR} > V_{DRDC}$(max)
–	PAD	Thermal pad. Solder to ground plane for better thermal performance.

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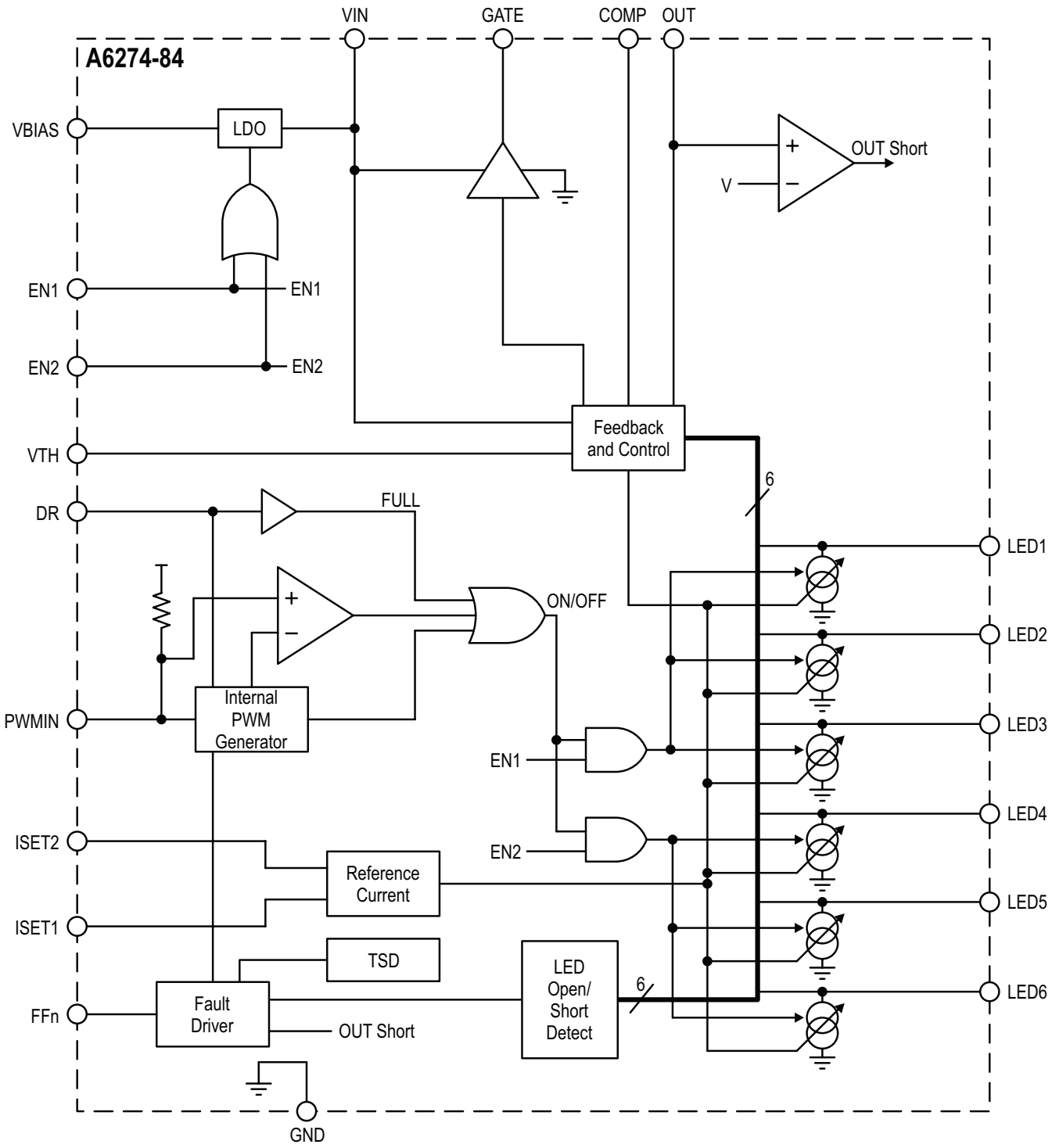

Functional Block Diagram

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ELECTRICAL CHARACTERISTICS: Valid at V_{IN} = 14 V, V_{ENx} = 3.3 V; • indicates specifications across the full operating temperature range with T_J = –40°C to 150°C; other specifications are at T_J = 25°C, unless noted otherwise. Refer to Figure 1 for typical application circuit.

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
INPUT SPECIFICATIONS							
Operating Input Voltage Range	V_{IN}		•	5	–	42	V
Input Quiescent Current [1]	I_Q	V_{ENx} = high, FULL mode		–	–	6	mA
Input Sleep Supply Current [1]	I_{QSLEEP}	$V_{EN1} = V_{EN2}$ = 0 V; $V_{DR} = V_{BIAS}$	•	–	–	6	µA
INTERNAL BIAS CIRCUIT							
BIAS Pin Voltage	V_{BIAS}	I_{BIAS} = 0 to 7 mA, 5.6 V ≤ V_{IN} ≤ 18 V	•	4.75	5	5.25	V
BIAS Pin Dropout	$V_{BIASDROP}$	Minimum voltage drop across VIN and BIAS pins. I_{BIAS} < 7 mA, V_{IN} = 5 V		–	0.3	–	V
V_{BIAS} Undervoltage Release Threshold	$V_{BIASSTART}$	V_{IN} rising	•	–	–	4.6	V
V_{BIAS} Undervoltage Lockout Stop Threshold	$V_{BIASSTOP}$	V_{IN} falling	•	–	–	4.2	V
P-CHANNEL MOSFET DRIVER SPECIFICATION							
GATE Sink Current [1]	$I_{GATE(SINK)}$	Due to on-chip current limit, 10 V < V_{IN} < 18 V		4	–	–	mA
		Due to on-chip current limit, V_{IN} = 5 V		2	–	–	mA
GATE Maximum Voltage (w.r.t. V_{IN})	$V_{GATE(MAX)}$	$V_{IN} – V_{GATE}$, V_{LEDx} = 0.3 V		8	10	12	V
GATE Minimum Voltage (w.r.t. V_{IN})	$V_{GATE(MIN)}$	$V_{IN} – V_{GATE}$, V_{LEDx} = 1 V		–	130	360	mV
PMOS Detect Threshold	$V_{GATE(PMOS)}$	Voltage measured ($V_{IN} – V_{GATE}$) at end of startup to detect PMOS connected		–	600	–	mV
LEDx CURRENT DRIVER SPECIFICATION							
LEDx Regulation Voltage [2a]	V_{LEDreg}	A6274; not in derating	•	–	0.4	0.7	V
		A6284; not in derating	•	–	0.55	0.85	V
LEDx Accuracy [3]	Err_{LEDx}	Measured at $I_{LED(MAX)}$, LEDx mismatch < 0.5 V, 5 V < V_{IN} < 18 V, T_J = 0°C to 150°C		–	2	3.5	%
LEDx Matching [4]	ΔI_{LEDx}	ISET2 connected to BIAS; compared to average I_{LEDx}, measured at $I_{LED(MAX)}$, LEDx mismatch < 1 V, 5 V < V_{IN} < 18 V	•	–	0.8	3	%
Maximum LEDx Current	$I_{LED(MAX)}$	A6274	•	–	60	–	mA
		A6284	•	–	120	–	mA
Minimum LEDx Current	$I_{LED(MIN)}$	A6274		–	6	–	mA
		A6284		–	12	–	mA
Maximum LED Current, ISETx Pin Short-to-Ground [2]	$I_{LED(ISETshrt)}$	A6274		–	66	–	mA
		A6284		–	129	–	mA
LED Current Ramp Time	t_{RAMP}	I_{LEDx} 10% to 90% and 90% to 10%		–	8	–	µs
ISETx to ILEDx Gain	g_{ILED}	A6274		–	248	–	A/A
		A6284		–	492	–	A/A
ISETx Voltage Level	V_{ISET}	0.015 mA ≤ I_{ISETx} ≤ 0.3 mA		–	1.2	–	V

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Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
PROTECTION							
V_{IN} Required to Derate I_{LED} by 10%	$V_{INth(L)}$	V_{VTH} = 1.84 V		19	20	21	V
V_{IN} Derating Range ($V_{INth(L)}$ to $V_{INth(H)}$)	V_{INthd}	I_{LED} drops from 90% to 50% level		–	6.4	–	V
MOSFET Drain Short Protection Threshold	$V_{OUT(SC)}$	Measure across OUT and GND pins		–	1	–	V
MOSFET Drain Short Protection Blank Delay During Startup	$t_{d(OUT,scblnk_strt)}$	Protection disabled from enable instance		–	12	–	ms
MOSFET Drain Short Protection Blank Delay During Steady-State	$t_{d(OUT,scblnk_stdy)}$	Protection blank time		–	1	–	µs
String Short Detect Voltage	$V_{SC(STRING)}$	While LED sinks are in regulation; sensed from VLEDx to VLEDreg, 5 V < V_{IN} < 18 V		1.8	–	2.6	V
LEDx Not-In-Use Voltage	$V_{LEDx(NULL)}$	Detect during t_{LEDdet} time period		0.18	0.26	0.34	V
LEDx Pin Source Current	I_{LEDsrc}	Source current for Not-In-Use Detection		65	–	95	µA
LED Connected Detect Time	t_{LEDdet}	ENx = high and V_{GATE} ≤ (V_{IN} – 3.3) at startup		–	5	–	ms
LEDx Short-to-Ground Detect Voltage	$V_{LED(SC)}$			–	–	0.16	V
Open-LED Disable Voltage	V_{OLED_dis}	Measured at OUT pin, V_{VTH} = 2 V		–	10	–	V
Input Overvoltage Threshold	V_{VINOV}	V_{EN1} = V_{EN2} = high		–	43	–	V
Thermal Monitor Activation Temperature [2]	T_{JM}	T_J where I_{LED} drops to 90% level		–	T_{JF} – 21	–	°C
Thermal Monitor Low-Current Temperature [2]	T_{JL}	T_J where I_{LED} drops to 35% level		–	T_{JF} – 7	–	°C
Overtemperature Shutdown [2]	T_{JF}	Temperature increasing		–	175	–	°C
Overtemperature Hysteresis [2]	$T_{J(HYS)}$	Recovery = T_{JF} – $T_{J(HYS)}$		–	30	–	°C
PWM DIMMING: INTERNAL AND EXTERNAL							
Internal-to-External PWM Mode Delay	$t_{d(PWM,INEX)}$			–	1	–	µs
External-to-Internal PWM Mode Delay	$t_{d(PWM,EXIN)}$	V_{PWMIN} < $V_{LOGIC(L)}$		–	20	–	ms
PWM DIMMING INTERNAL							
Maximum PWM-Dimming Frequency	$f_{PWM(MAX)}$	7.15 kΩ between PWMIN and GND		–	2050	–	Hz
Minimum PWM-Dimming Frequency	$f_{PWM(MIN)}$	71.5 kΩ between PWMIN and GND		195	215	235	Hz
PWM Duty Cycle	D_{PWM5} [2]	DR driven by resistor divider from BIAS, V_{BIAS} ÷ V_{DR} = 27.78, PWM = 205 Hz to 2 kHz	•	4.5	5.0	5.5	%
	D_{PWM90}	DR driven by resistor divider from BIAS, V_{BIAS} ÷ V_{DR} = 1.54, PWM = 205 Hz to 2 kHz		87	90	93	%
	$V_{DRDC(MAX)}$	Minimum required voltage on DR for 100% duty cycle		3.6	–	–	V
DR Pin Current [1]	$I_{DR(SRC)}$	V_{DR} = 2 V		–	–	1	µA

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Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
LOGIC SIGNAL SPECIFICATIONS							
FFn Output (Open Drain)	$V_{FFn(L)}$	I_{FFn} = 1 mA, fault asserted		–	–	0.4	V
FFn Output Leakage Current [1]	$I_{FFn(LKG)}$	V_{FFn} = 12 V, fault not asserted		–1	–	1	µA
PWMIN, ENx Low Voltage	$V_{LOGIC(L)}$		●	–	–	0.8	V
PWMIN, ENx High Voltage	$V_{LOGIC(H)}$		●	2	–	–	V
FFn Input Low Voltage	$V_{FFLOGIC(L)}$	MODE = 1; FFn pin acts as bidirectional pin when MODE = 1	●	–	–	0.8	V
FFn Input High Voltage	$V_{FFLOGIC(H)}$		●	2.1	–	–	V
PWMIN Input Hysteresis	$V_{LOGIC(HYS)}$			150	270	–	mV
ENx Input Hysteresis	$V_{LOGIC(HYS1)}$			40	–	–	mV
ENx Internal Pull-Down Resistance	$R_{PD(ENx)}$			–	200	–	kΩ
COMP SPECIFICATIONS							
COMP Source Current	$I_{COMP(SOURCE)}$			–	320	–	µA
COMP Sink Current [2]	$I_{COMP(SINK)}$			–	–320	–	µA
COMP Startup Sinking Current	$I_{COMP(START)}$	V_{LEDx} is < regulation voltage		–	2	–	mA

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), and positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[2a] Max limit ensured by design and characterization, not production tested.
[3] LED accuracy is defined for A6274 as $|[1 – (R_{ISETx} \times I_{LED(avg)} \div 298)]|$ and for A6284 as $|[1 – (R_{ISETx} \times I_{LED(avg)} \div 590)]|$, where $I_{LED(avg)}$ is the average of I_{LED1} through I_{LED6}, R_{ISETx} is in kΩ, and I_{LED} is in mA.
[4] LED current matching is defined as $[(I_{LEDx} – I_{LED(avg)}) \div I_{LED(avg)}]$, with $I_{LED(avg)}$ as defined in Footnote 3.

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FUNCTIONAL DESCRIPTION

Powering Up

The A6274/84 can be enabled either by ENx inputs or by input voltage as shown in Figure 3 and 4 respectively. In both cases, the IC starts when the internal bias circuit voltage, V_{BIAS}, rises above its starting level, $V_{BIASSTART}$. Any existing latched fault is cleared.

The IC shuts down when input voltage or both ENx inputs fall such that the internal bias circuit voltage, V_{BIAS}, drops below its stopping level, $V_{BIASSTOP}$.

EN1 is the active-high-enable input for LED1-3 while EN2 is the active-high-enable input for LED4-6. To drive all the LED strings with common EN input, connect EN1 and EN2 together. EN1 and EN2 pins are high-voltage tolerant and can be directly connected to a power supply.

Refer to Figure 3 for startup with ENx. Once ENx goes high, the BIAS regulator is allowed to start after a few microseconds internal delay (A to B), and the IC powers up when $V_{BIAS} > V_{BIASSTART}$ (at C). Once the IC powers up, it will check LEDx pin voltage to identify if any LEDx pin is used, unused, or shorted to ground.

After startup, for the time period of t_{LEDdet} (C to D), the IC detects unused LED sink pins by injecting current I_{LEDsrc} to LEDx pins and measures voltage on the LEDx pins. If the LEDx voltage is equal to $V_{LEDx(NULL)}$, the IC detects it as an unused channel and disables the corresponding LEDx channel. The internal current source, I_{LEDsrc}, is removed after t_{LEDdet} time period and disabled strings will be removed from the regulation loop. The unused pin, with the pull-down resistor, will be taken out of regulation at this point and will not contribute to the series-pass regulation loop or fault detection. The FFn pin remains high during the t_{LEDdet} period. The enabled strings will be continuously monitored, and can be treated as a fault after the t_{LEDdet} period.

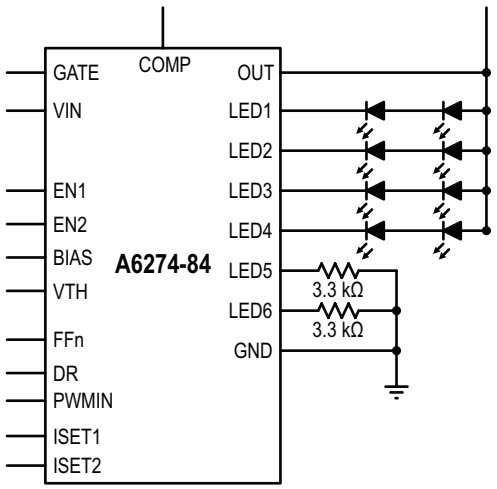

Figure 2: Channel-select setup using LED1-4; LED5-6 unused. LED5-6 connected through 3.3 kΩ resistor to GND.

All unused pins must be connected with a resistor connected from LEDx to ground, as shown in Figure 2. LEDx pins source I_{LEDsrd} current. Voltage on an LEDx pin, when connected through resistor, will be $V_{LEDx(NULL)}$.

FULL and DIM Mode

When the DR pin voltage is above $V_{DRDC(MAX)}$, the LEDs operate with 100% duty cycle (FULL mode). In FULL mode, the LEDs turn on with 100% duty cycle regardless of internal or external PWM mode. When the DR pin voltage is lower than $V_{DRDC(MAX)}$, the LEDs operate with PWM dimming (DIM mode). PWM frequency and duty cycle in DIM mode is controlled by the PWMIN and DR pins.

Table 1: LED Detection Voltage Thresholds

LED Pin Voltage Level	LED Pin	Action
$V_{LED(SC)}$ (<160 mV)	Indicates short-to-ground	FFn goes low after t_{LEDdet} time period.
$V_{LEDx(NULL)}$ (>180 mV, <340 mV)	Not used	Unused LEDx is removed from regulation loop. Related sink remains disabled and latched until it is re-enabled.
$V_{LEDx(NULL,max)}$ (>400 mV)	LED pin in use	None

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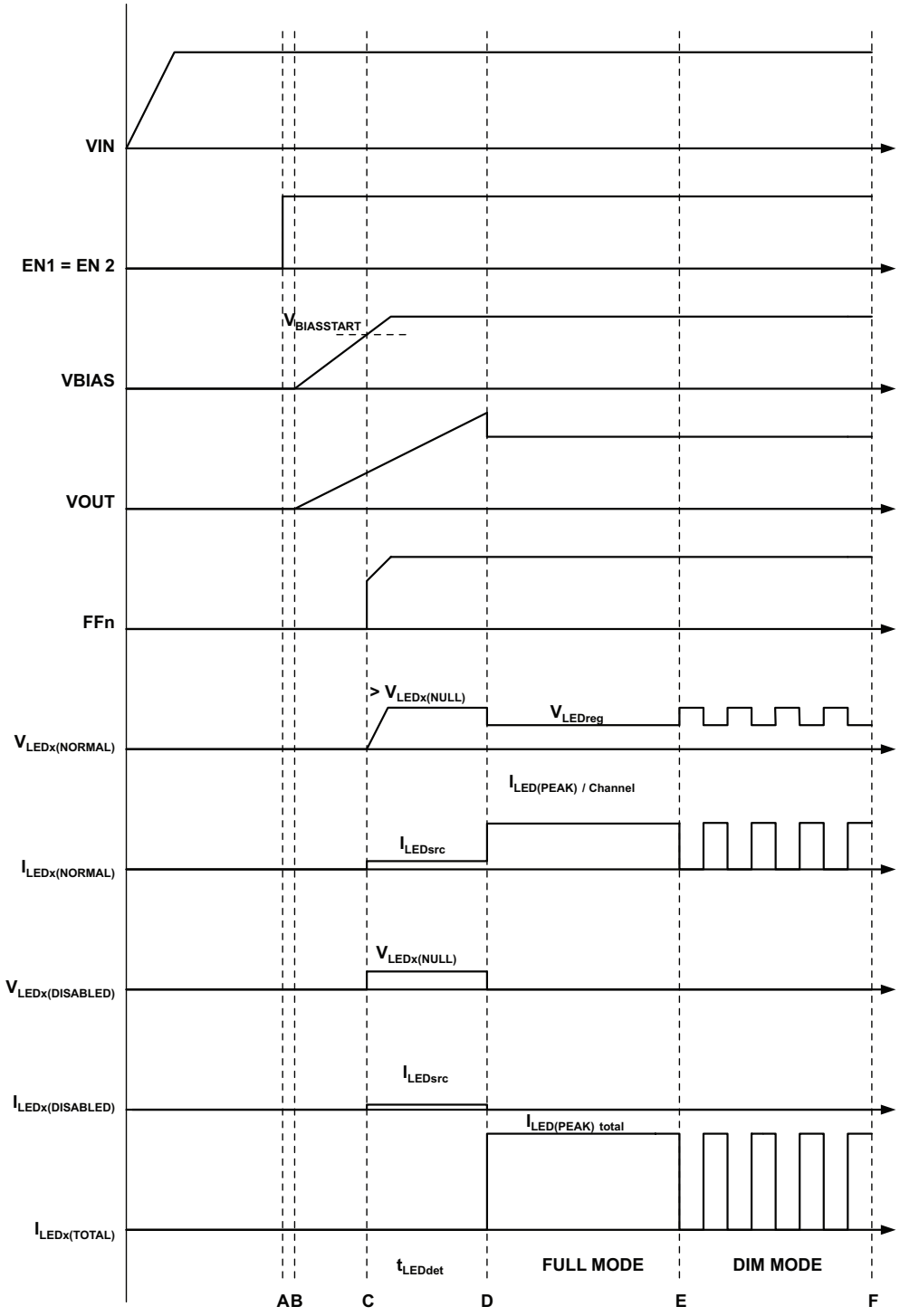

Figure 3: Typical Start Sequence with ENx

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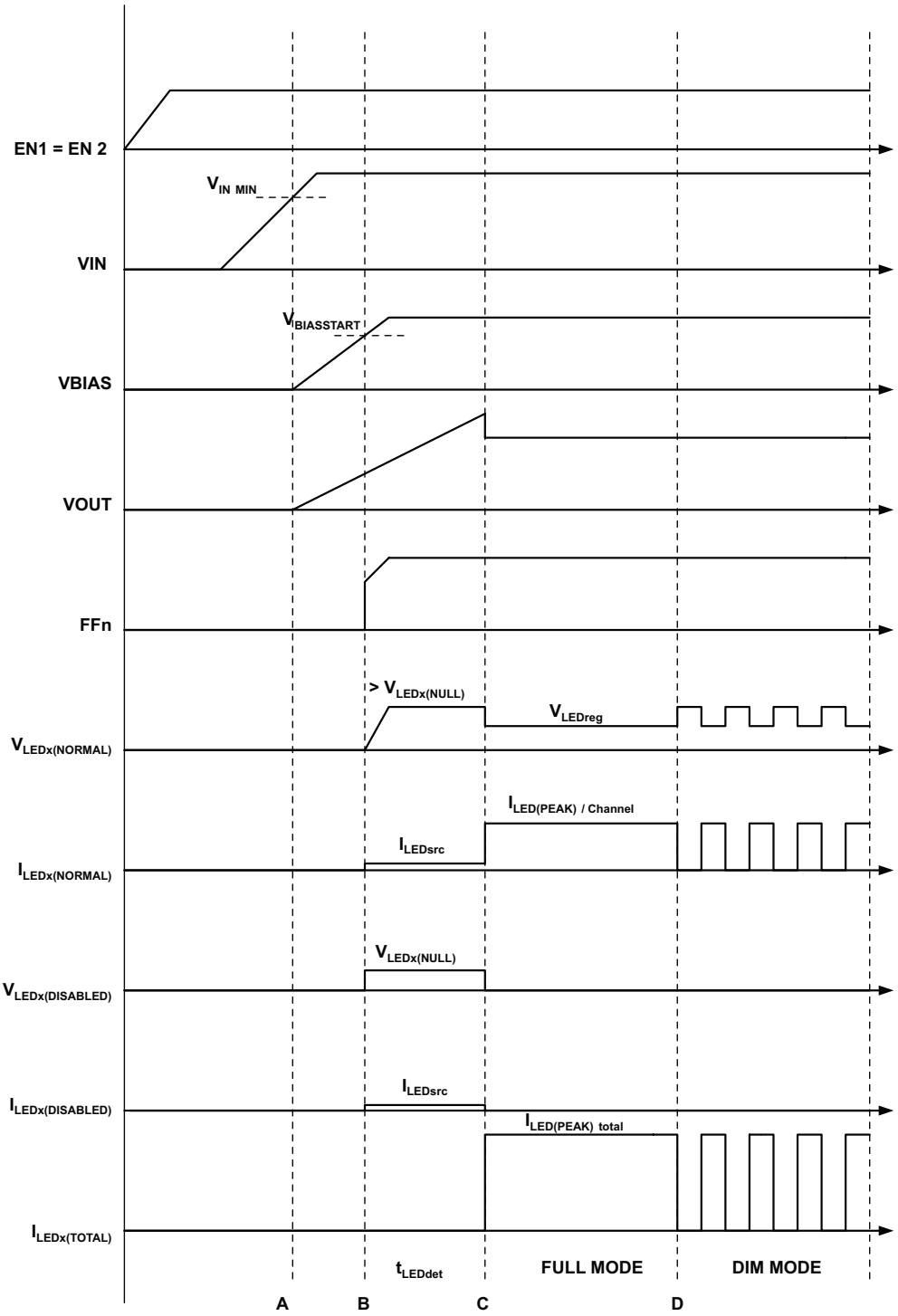

Figure 4: Typical Start Sequence with VIN

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PWM Dimming in DIM Mode

LED dimming during DIM mode can be controlled internally by the A6274/84, or externally. For external PWM mode, connect an external clock pulse on the PWMIN pin, which controls dimming, frequency, and duty cycle. The A6274/84 detects the logic level on the PWMIN pin. When logic voltage is applied on the PWMIN pin, the IC switches to external PWM mode where dimming, frequency, and duty cycle are directly controlled by signals on PWMIN pin.

In internal PWM mode, dimming frequency can be set using a resistor connected from PWMIN pin to GND as shown in Figure 1. It is not necessary to select the PWM mode before startup: the IC will transition from internal to external when PWMIN is raised above $V_{LOGIC(H)}$; and it will transition from external to internal when external PWMIN signal is removed for more than 20 ms. LEDx will not blink; they will be off during this period.

The recommended range for PWM frequency is 200 Hz to 2 kHz. Maximum PWM frequency is limited due to acceptable error at minimum PWM duty cycle. At higher PWM frequency and smaller duty cycles, error in LED current increases due to slow ramp-up and ramp-down in LED current. It is recommended to use a minimum on-time > 20 µs.

The equation for internal PWM frequency setting with the PWMIN pin resistor is given by:

$$f_{PWM} = (14165 \div R_{FPWM}) + 19$$

where f_{PWM} is in Hz and R_{FPWM} is in kΩ. For example, with a 29.4 kΩ resistor, f_{PWM} = 500 Hz.

R_{FPWM} must be greater than 5 kΩ for internal PWM; below this value, the PWMIN pin is detected at a logic-low level and operates in external PWM mode.

The voltage on the DR pin determines the operating duty cycle. For better accuracy, derive this voltage from BIAS using a voltage divider. The PWM duty cycle depends on the ratio of the DR and BIAS pin voltages. The duty cycle can be reduced, down to 5% (see Figure 5), as:

$$PWM\,(\%) = 139 \times V_{DR} \div V_{BIAS}$$

where V_{DR} and V_{BIAS} are in volts (V).

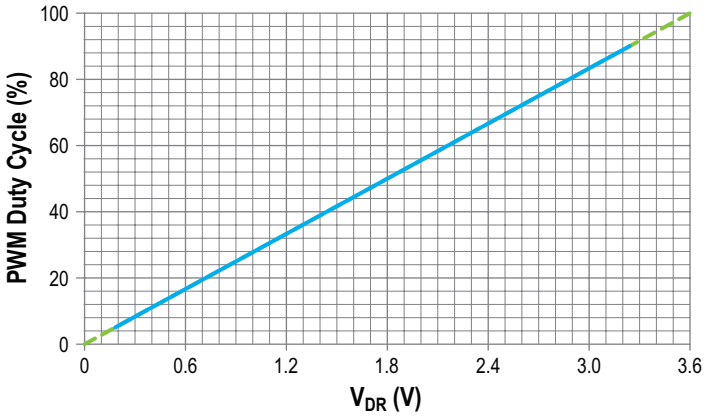

Figure 5: Relationship of Voltage on DR pin (VDR) and Dimming Duty Cycle
V_{DR} can be varied from 0 to 3.6 V

LED Current Setting

The peak LED current can be set at up to 60 or 120 mA per channel through the ISETx pin. ISET1 sets current through LED1-3 and ISET2 sets current through LED4-6.

By connecting ISET2 to BIAS, ISET1 current can be mirrored on all enabled LED channels (LED1-6). This will improve current matching between LED1-6 when all LED strings are identical.

Connect a resistor, R_{ISETx}, between ISETx pin and ground, to set peak LED current through each channel. The value of peak LED current through each LEDx sink is given by:

$$I_{LED(PEAK)} = 298 \div R_{ISETx}\,(k\Omega) \quad \text{for A6274}$$

$$I_{LED(PEAK)} = 590 \div R_{ISETx}\,(k\Omega) \quad \text{for A6284}$$

where I_{LED} is in mA and R_{ISETx} in kΩ. This sets the peak current through each LEDx, referred as the 100% Current. The average LEDx current can be reduced from the 100% Current value by dimming PWM duty ratio.

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Input Overvoltage Derating

This feature takes effect at higher V_{IN} levels, limiting power dissipation in the IC and the external MOSFET. At higher input voltages, output current drops corresponding with increasing V_{IN}. Output current is controlled with peak current (see Figure 6). The V_{IN} threshold can be set with an external resistor divider connected from BIAS to VTH. The LED current drops to 90% at the $V_{INth(L)}$ level and to 50% at $V_{INth(H)}$ level. LED current further drops to 40% and stays at this level for higher input voltages. Voltage on VTH pin sets the $V_{INth(L)}$ level, and the $V_{INth(H)}$ level is typically higher than $V_{INth(L)}$ by V_{INthd} (6.4 V).

The recommended range for $V_{INth(L)}$ is from 18 to 36 V.

$$V_{INth(L)} = 10 \times V_{VTH} + 1.6$$

where $V_{INth(L)}$ is the supply voltage level where LED current drops to the 90% level, and V_{VTH} is the voltage on VTH pin. Figure 7 shows relation between voltage on VTH pin and $V_{INth(L)}$.

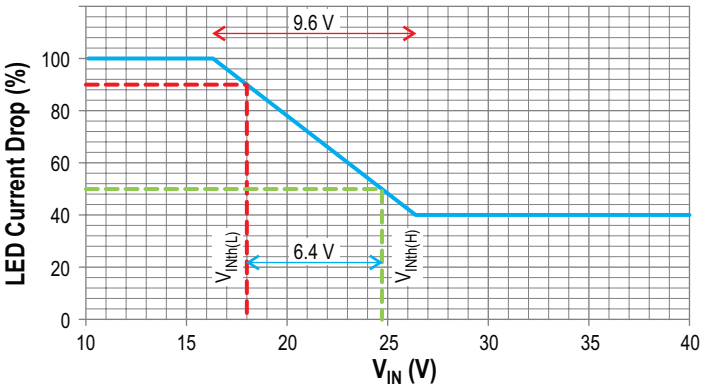

Figure 6: Input Voltage Derating
(V_{VTH} = 1.64 V)

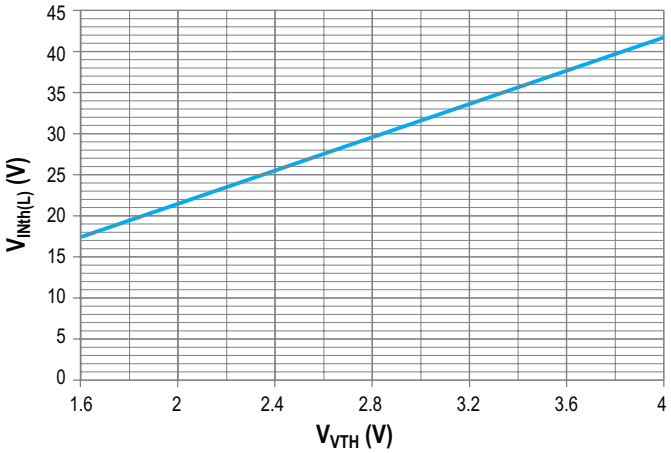

Figure 7: Relationship between $V_{INth(L)}$ and Voltage on the VTH Pin

Thermal Derating and Protection Shutdown

This feature takes effect at higher temperatures, limiting power dissipation in the IC and external MOSFETs. At higher temperatures, the LED current drops with increasing T_J, as shown in Figure 8. Thermal shutdown (TSD) completely disables the outputs under extreme overtemperature (>175°C) conditions, and FFn goes low. The IC restarts when the temperature drops by 30°C.

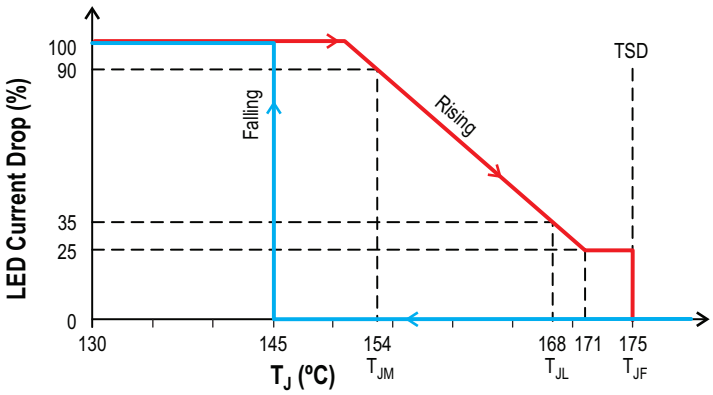

Figure 8: Output Current Foldback Based on Rising T_J
Output current changed by DC current control; when temperature exceeds 175°C (typ), the IC turns off due to TSD function, and turns on again at 145°C (30°C (typ)) hysteresis.

Operation of the Series-Pass Regulator

The A6274/84 consists of six regulated and matched current sinks, and a series-pass regulator controller to minimize power dissipation in the sinks. The series-pass regulator is controlled such that all LEDx pin voltage is above regulation. LEDx pin having maximum forward voltage drop will be regulated by series-pass regulator. This ensures optimum voltage supplied to common-anode node of LED strings to drive all strings at the desired current.

A capacitor connected across COMP to the drain of the external MOSFET provides a pole for control-loop stability. It is recommended to use NTB5605 or NTD2955 as external PMOS.

When the external PMOS is not used, connect the GATE and COMP pins to VIN. When the PMOS pre-regulator is not used, the LED string short faults B and C will be disabled.

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MOSFET Drain Short to GND Fault (FAULT A)

This fault is detected when the voltage at OUT pin drops below $V_{OUT(SC)}$. If the OUT-to-ground short circuit is caused by a weak shorting link, voltage on OUT pin may not drop below $V_{OUT(SC)}$. In that case, this fault will not be detected and high current will flow through the MOSFET.

During startup, the MOSFET drain short to GND is detected after $t_{d(OUT,scblnk_strt)}$ delay from part enabled (ENx pin pulled high and $V_{BIAS} > V_{BIASstart}$). During this period, the MOSFET may draw significant current. Current through the MOSFET is limited by $R_{ds(on)}$ of the MOSFET and external parasitic resistance from battery to MOSFET source.

During normal operation, the MOSFET drain short to GND fault is blanked for $t_{d(OUT,scblnk_stdy)}$ period.

Open-LED (FAULTs D, E, F, and G)

During normal operation, if the voltage on any enabled LED pin drops too low ($V_{LEDx} < V_{LED(SC)}$) and V_{OUT} is greater than V_{OLED_dis}, it may indicate either a short across LEDx and GND (Fault E), an open-LED (Fault F), a mid-LED-string short-to-ground (Fault D), or LED common-anode open (Fault G).

LEDs in faults D and E will only be reported on FF pin, but will not be protected, if MOSFET Q1 is not used.

Short LED Faults (FAULTs B and C)

Short LED faults are detected while LED sinks are in regulation and $V_{LEDx} - V_{LEDreg} > V_{SC}$ (STRING).

Open-LED Disable Threshold

At power-up (EN1 or EN2 raised to logic high), if the input voltage is below V_{OLED_dis}, faults D, E, F, and G will be disabled. Once V_{IN} is raised above V_{OLED_dis}, the faults are enabled and will remain enabled unless V_{BIAS} drops below $V_{BIASSTOP}$. The IC will continue to operate normally in cases where these faults exist. V_{OLED_dis} value is given by:

$$V_{OLED_dis} = 5 \times V_{VTH}$$

Voltage on VTH pin sets the input voltage derating threshold ($V_{INth(L)}$) as well as the open-LED disable level (V_{OLED_dis}). Select the V_{VTH} voltage suitable to avoid an open-LED fault due to insufficient input voltage.

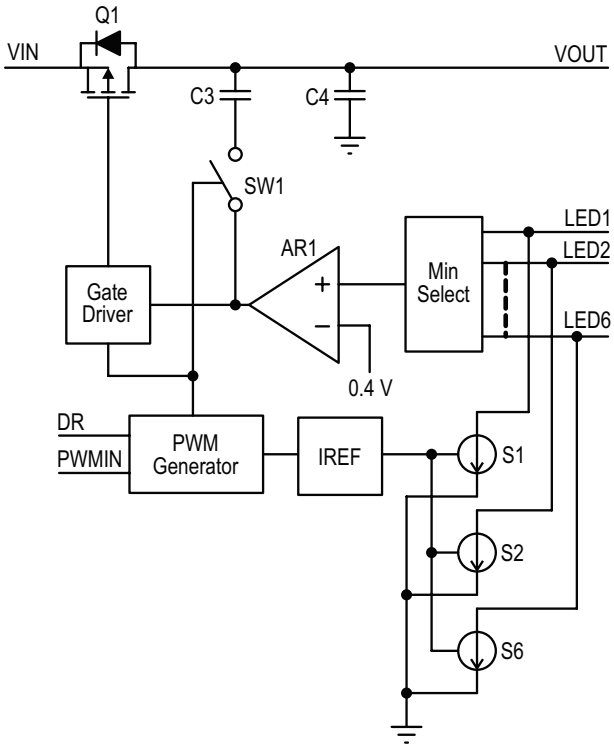
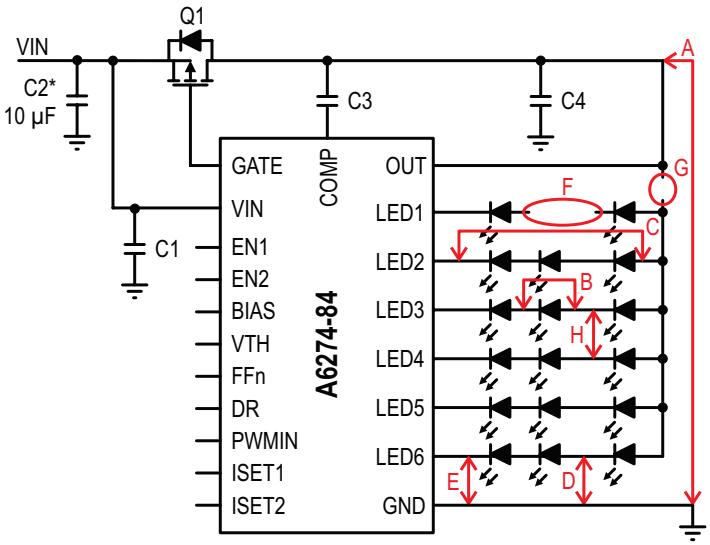


Figure 9: External MOSFET Regulator Loop



* C2 should be placed as close to the input connector as possible. Good filter layout practices should be adhered to.

Figure 10: Various Faults Handled by A6274/84

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Table 2: Fault Description

Fault		Detection Criterion	Auto-Restart		FFn	LED Sinks		Ballast MOSFET Q1		Operation	
		MODE State →	1	0	1 or 0	1	0	1	0	1	0
A	MOSFET drain shorted to ground	$V_{OUT} < V_{OUT(SC)}$. Fault detected after $t_{d(OUT,scblnk_strt)}$ blanking time from Q1 gate enabled. During normal operation, this blanking time is $t_{d(OUT,scblnk_stdy)}$.	No		Low	All Turn Off		Turn Off		IC shutdown and FFn pin goes low. This state remains latched until VIN or any ENx toggled.	
Group 1 Faults Based on Maximum LEDx Pin Voltage											
B	One LED short	While LED sinks are in regulation. Sensed from V_{LEDx} to V_{LEDreg}. $V_{LEDx} – V_{LEDreg} > V_{SC(STRING)}$	No	Yes	Low	All Turn Off	Operate Normally	Turn Off	Operate Normally	IC shutdown and FFn pin goes low. This state remains latched until VIN or any ENx toggled.	LEDx pin voltage on faulty string increases and IC detects the fault. IC responds only by pulling FFn pin low as long as fault present. Power dissipation in the faulty LED sink increases and may hit TSD. Current in LED still regulated to set level. FFn stays low as long as fault detected.
C	Short LED string	"	No	Yes	Low	"	"	"	"	IC shutdown and FFn pin goes low. This state remains latched until VIN or any ENx toggled. LED pins rated for 45 V to protect IC against this fault.	LEDx pin voltage on faulty string increases and IC detects the fault. IC responds only by pulling FFn pin low as long as fault present. Power dissipation in the faulty LED sink increases and may hit TSD. Current in LED still regulated to set level. FFn stays low as long as fault detected. LED pins rated for 45 V to protect IC against this fault.
Group 2 Faults Based on LEDx Pin Voltage $V_{LED(SC)}$											
D	Mid-LED-string short-to-ground	$V_{OUT} > V_{OLED_dis}$ and any enabled LEDx pin voltage < $V_{LED(SC)}$	No	Yes	Low	All Turn Off	Operate Normally	Turn Off	Operate Normally	IC shutdown and FFn pin goes low. This state remains latched until VIN or any ENx toggled.	LEDx pin voltage on faulty string drops and IC detects the fault. For a brief time, V_{OUT} increases due to open-loop operation. Q1 turns on harder as the LEDx pin voltage on faulty string drops below regulation. V_{OUT} rises close to V_{IN}. V_{OUT} drops to regulation level after removing the faulty string from regulation loop. The faulty string removed from Q1 regulation loop and sinks turned off. During output overshoot time, Fault B may also be detected by the IC but it does not affect the operation. Faulty string will be out of Q1 loop regulation until voltage on faulty string rises above regulation level or VIN or any ENx toggled. FFn pin stays low as other string shorted to ground.
E	LEDx pin short-to-ground	"	No	Yes	Low	"	"	"	"	"	"
F	LED string open	"	No	Yes	Low	"	"	"	"	"	"
G	LED common-anode open	"	No	Yes	Low	"	"	"	"	"	Voltage on all LED pins drop below regulation level. V_{OUT} rises close to V_{IN} and stays at this level as all LEDx pins removed from regulation. Sinks remain active and internal gate of sink driver rails high. When a string connected back, V_{OUT} controlled by this string. There will be a small LED current overshoot. FFn pin stays low if any string is open.

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Table 2: Fault Description (continued)

FAULT		Detection Criterion	Auto-Restart	FFn FAULT	LED Sinks	Ballast MOSFET	Operation
		MODE State →	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0
H	String-to-string short	This condition is not detected	Operate Normally	Normal	Operate Normally	Operate Normally	IC operates normally. LED currents in shorted string may not share same current
	Thermal Shutdown	Junction temperature exceeds T_{JF}	Yes	Low	All Turn Off	Turn Off	IC shutdown and FFn pin goes low. This state remains latched and re-enables when junction temperature drops below 145°C. This is a non-latching fault, but this fault leads to a Fault A condition if thermal shutdown is long enough to allow the OUT capacitor to fully discharge.
	Thermal Derating	Junction temperature exceeds T_{JM}	Operate Normally	Normal	LED current derated based on T_J	Operate Normally	LED current derated based on junction temperature
	V_{IN} Derating	Input voltage V_{IN} exceeds threshold set by voltage on VTH pin	Operate Normally	Normal	LED current derated based on V_{IN}	Operate Normally	LED current derated based on supply voltage and V_{VTH} setting.
	Undervoltage Protection	V_{BIAS} below $V_{BIASSTART}$	Yes	Low	All Turn Off	Turn Off	All faults cleared when this fault occurs. IC restarts when $V_{BIAS} > V_{BIASSTART}$
	V_{IN} Overvoltage	Input voltage V_{IN} exceeds V_{INOVth} level	Yes	Low	All Turn Off	Turn Off	This is a non-latching fault but this fault leads to a Fault A condition if the overvoltage is long enough to allow the OUT capacitor to fully discharge.

Notes:
- If the non-latching fault condition causes OUT voltage to drop below $V_{OUT(SC)}$, the IC will latch as described in Fault A.
- Once faulty condition is detected, FFn goes low after fault blanking time. Fault blanking time for Fault A is 1 µs; fault blanking time for Fault B and C is 3 µs; fault blanking time for Fault D, E, F, and G is 65 µs.
- For non-latching part, ignore FFn status when duty cycle is below 5%.
- For non-latching part, it is recommended to use a small capacitor of 4.7 nF from FFn to GND with a 10 kΩ FFn pull-up resistor during dimming mode.

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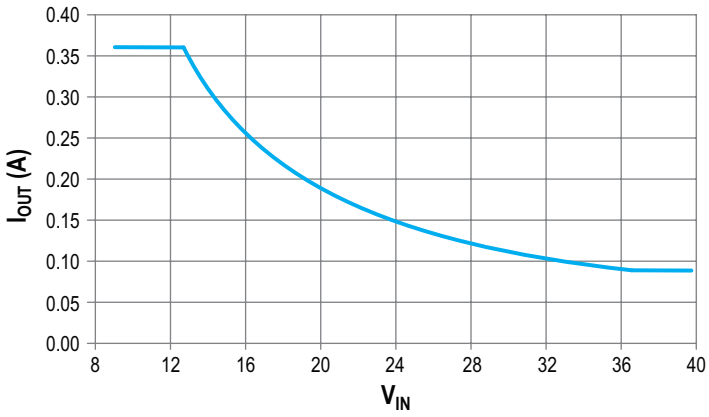
Power Derating Based on T_J

An external MOSFET dissipates excess voltage (V_{IN}, V_{LED}, V_{LEDreg}) and minimizes power loss in sinks. When an external MOSFET is not used, as shown in Figure 17, internal sinks drop this excess voltage, and power dissipation in sinks increases. The A6274/84 derates the LED current based on junction temperature to extend its operating range. A typical example (below) shows LED current derating and junction temperature of the IC (T_J) at different VIN conditions.

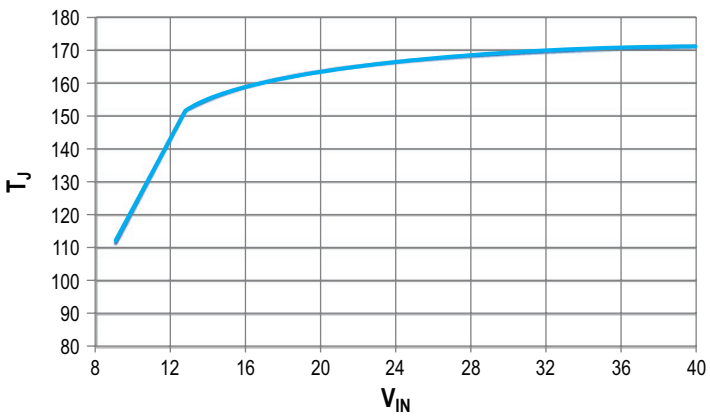
EXAMPLE 1

Table 3: LED Current Derating and Junction Temperature of the IC (T_J) at Different V_{IN} Conditions

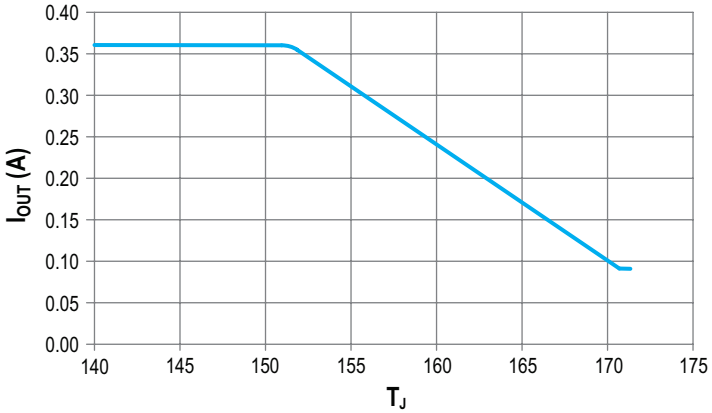
Symbol	Value	Units	Description
V_{LED}	7	V	Total LED string voltage at desired LED current
I_{OUT}	0.36	A	Total LED current
T_A	90	°C	Ambient temperature
$R_{\theta JA}$	30	°C/W	Junction-to-ambient thermal resistance for the IC
T_{JM}	154	°C	Junction temperature at which LED current drops to 90% level. Refer to Figure 8.
$V_{IN(MIN)}$	9	V	Minimum input voltage
$V_{IN(MAX)}$	40	V	Maximum input voltage



(a) Output combined LED current derating with supply voltage variation. LED current drop at higher V_{IN} due to excessive power dissipation.



(b) Junction temperature T_J of the IC with supply voltage variation



(c) Output combined LED current derating with junction temperature of the IC

Figure 11: Thermal Derating

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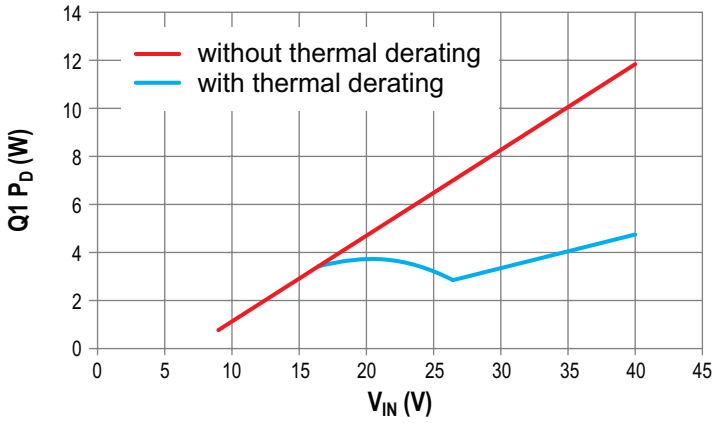
Power Derating Based on Input Supply Voltage V_{IN}

The A6274/84 derates LED current based on the supply voltage and reference voltage on the VTH pin. Power dissipation in the external transistor can be limited at higher input voltage. The example below shows the selection of V_{VTH} to limit MOSFET junction temperature below 140°C. Refer to Figure 1 for typical application.

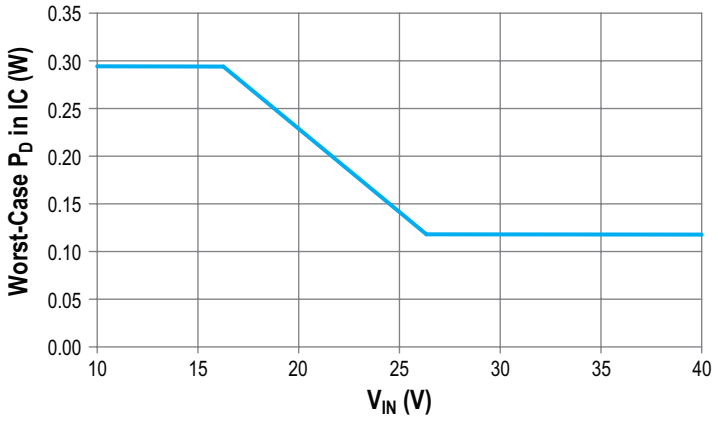
EXAMPLE 2

Table 4: LED Current Derating and Junction Temperature of the IC (T_J) at Different V_{IN} Conditions

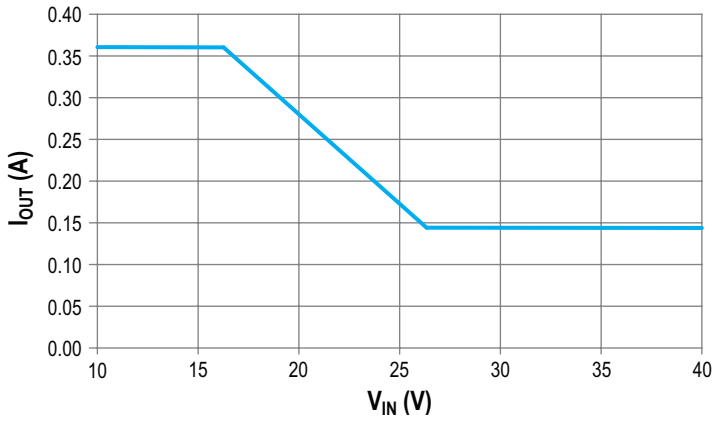
Symbol	Value	Units	Description
V_{LED}	7	V	Total LED string voltage at desired LED current
I_{OUT}	0.36	A	Total LED current
T_A	90	°C	Ambient temperature
$R_{\theta JA}$	10	°C/W	Junction-to-ambient thermal resistance for MOSFET
V_{LEDreg}	0.4	V	LEDx pin regulation voltage
$V_{IN(MIN)}$	9	V	Minimum input voltage
$V_{IN(MAX)}$	40	V	Maximum input voltage
V_{VTH}	1.64	V	External voltage applied to VTH pin
$V_{INth(L)}$	18	V	Input voltage at which LED current drops to 90% level; refer to Figure 7



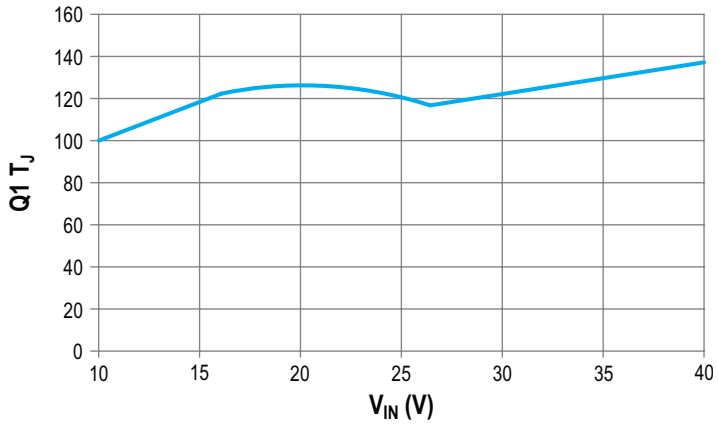
(a) Power Dissipation in MOSFET (RED – unlimited power dissipation, Blue – Power dissipation with V_{IN} derating)



(b) Worst-Case Power Dissipation in IC



(c) Output Current Derating



(d) MOSFET Junction Temperature

Figure 12: Input Voltage Derating

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APPLICATION CIRCUITS

External PWM

The PWMIN pin senses logic level input and switches to external PWM mode. PWM frequency and duty cycle are set by logic input on the PWMIN pin when the DR pin voltage is less than 3.6 V.

Figure 13a shows an application circuit to control dimming with an external logic level PWM signal in DIM mode and FULL mode controlled through DR pin. Duty cycle and frequency applied on PWMIN pin controls LED current during DIM mode. In FULL mode, LEDs always operate with 100% duty cycle.

Figure 13b shows an application circuit where external PWM controls LED dimming in FULL and DIM modes. Use Rz = 0 and open Dz for PWM signal level below 5 V. Rz-Dz should be used to limit PWMIN pin voltage when battery-referred PWM signal is applied.

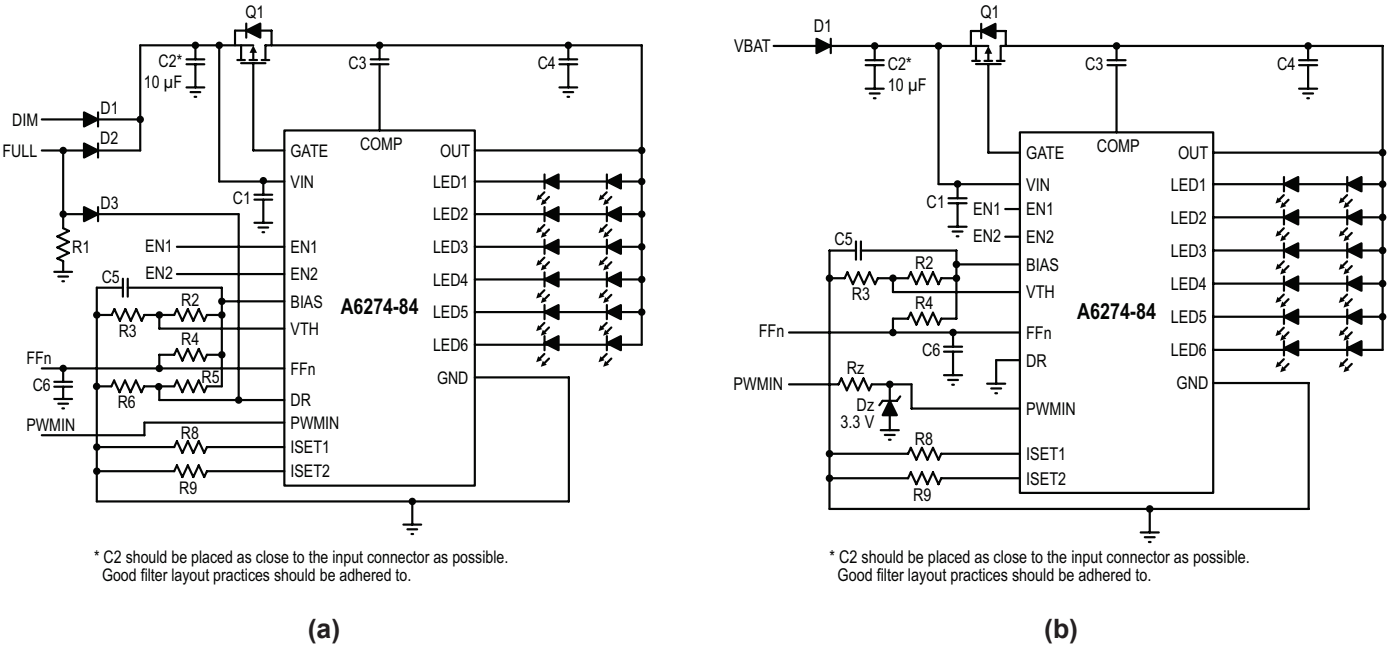

Figure 13: Dimming with External PWM

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Using One Reference Resistor for Setting Current in LED1-6

The A6274 and A6284 have two LED groups: LED1-3 and LED4-6. The peak LED current can be set separately using ISET1 and ISET2 respectively. If the same LED current is required for both groups, as shown in Figure 14, connect ISET2 to BIAS. This disables the ISET2 reference from the pin and internally uses the same reference as ISET1. Using a single resistor in setting current through all LEDs improves matching between the two LED groups.

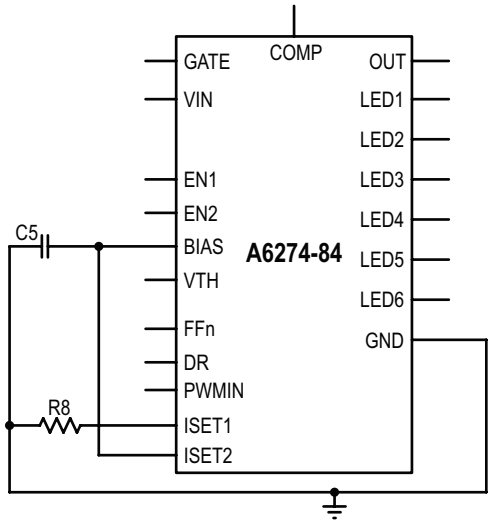

Figure 14: Using Common ISET Reference

MOSFET Protection by External Thermal Derating

The A6274/84 has a built-in thermal-derating function which works on the junction temperature of the IC. If the MOSFET is placed away from the IC, the junction temperature of the MOSFET and IC will be different, and thermal derating may not work effectively to protect the MOSFET.

An external circuit shown below can be placed close to the MOSFET to sense temperature and foldback LED current to limit power dissipation.

An NTC is placed close to Q1. The gain of the NTC and resistor ratios R11 to R8 set the derating slope. The NTC determines the thermal derating threshold. A typical application circuit for the thermal derating for the MOSFET is shown in Figure 15.

As temperature increases, NTC resistance drops. When voltage on Q2 base increases above ~1.6 V, Q2 turns on. Current through R11 is given by:

$$(VB - 0.4 - 1.2) \div R11$$

where VB is the voltage on the base of transistor Q2. This current reduces current sourced by the ISETx pins, and LED current drops proportionately.

Current through ISET1 pin is given by:

$$ISET1 = 1.2 \div R8 - (VB - 0.4 - 1.2) \div R11 \ .$$

Similarly, current through ISET2 pin is given by:

$$ISET2 = 1.2 \div R9 - (VB - 0.4 - 1.2) \div R12 \ .$$

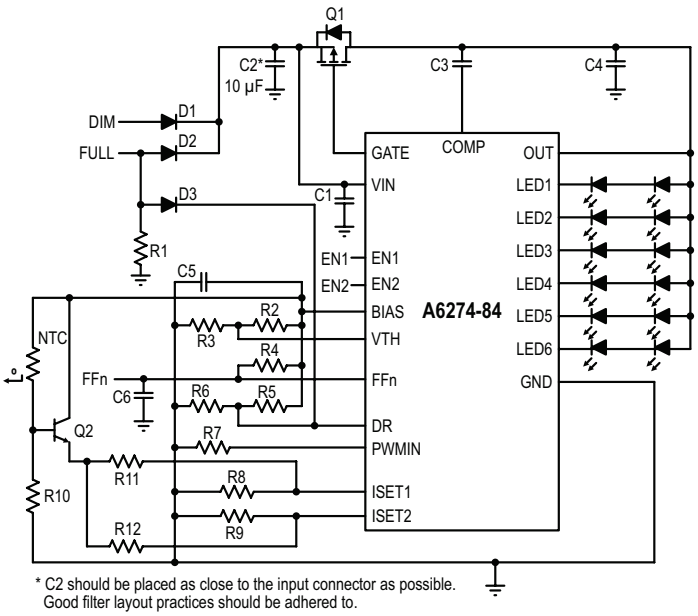

Figure 15: External Power Derating

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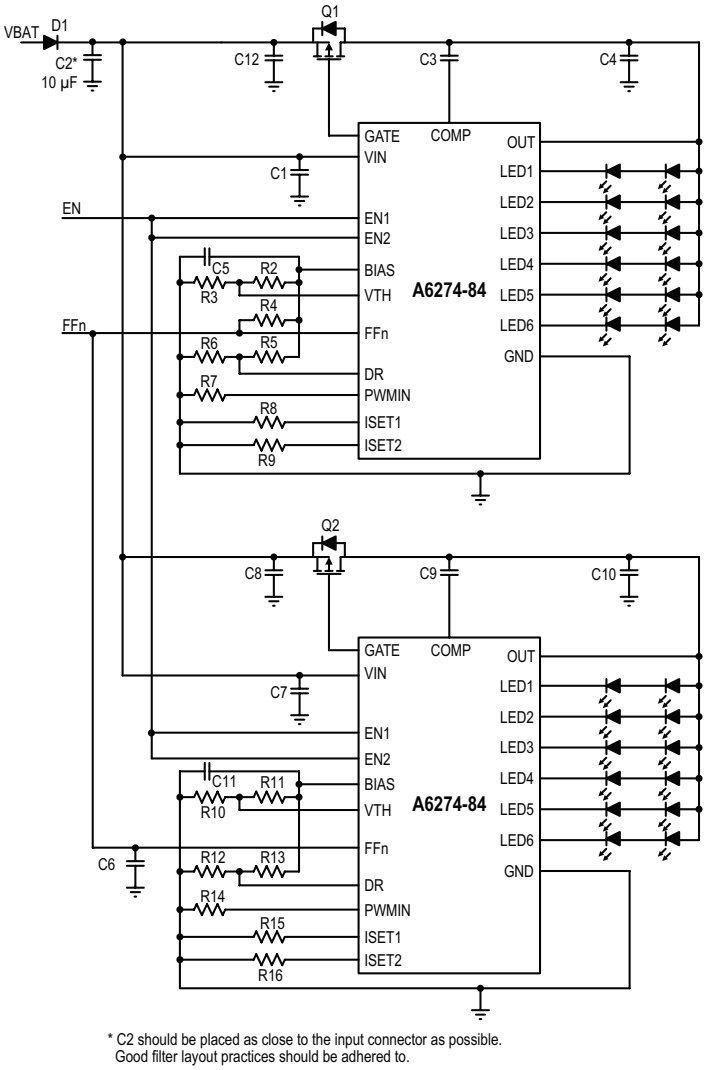
Connecting Multiple ICs and External PMOS in Parallel Configuration

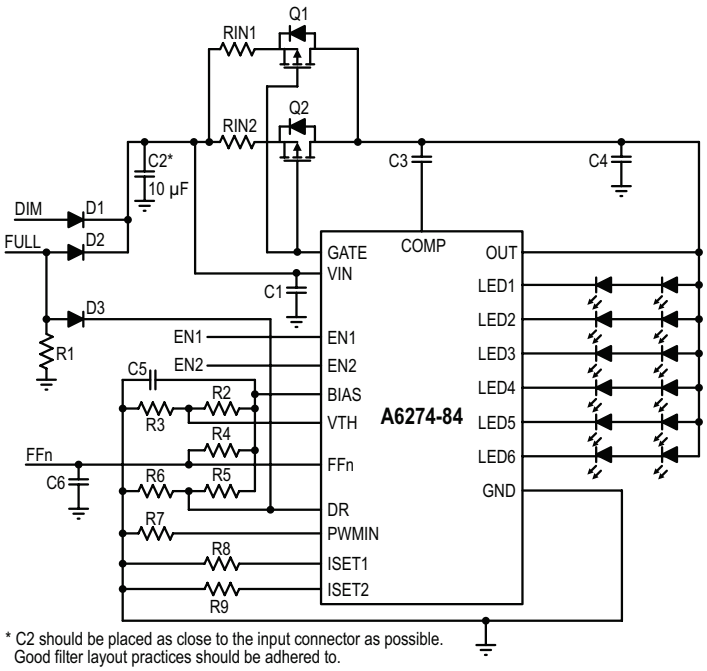
For larger lighting assemblies or to drive higher current, multiple ICs can be paralleled by connecting open-drain FFn pins of all the ICs together as shown in Figure 16a. Up to 20 ICs can be used in parallel configuration.

For better thermal performance of external PMOS, two PMOS can be paralleled as shown in Figure 16b.



* C2 should be placed as close to the input connector as possible.
Good filter layout practices should be adhered to.

Figure 16a: Parallel Connection for Multiple IC Operation



* C2 should be placed as close to the input connector as possible.
Good filter layout practices should be adhered to.

Figure 16b: Two External PMOS in Parallel Configuration

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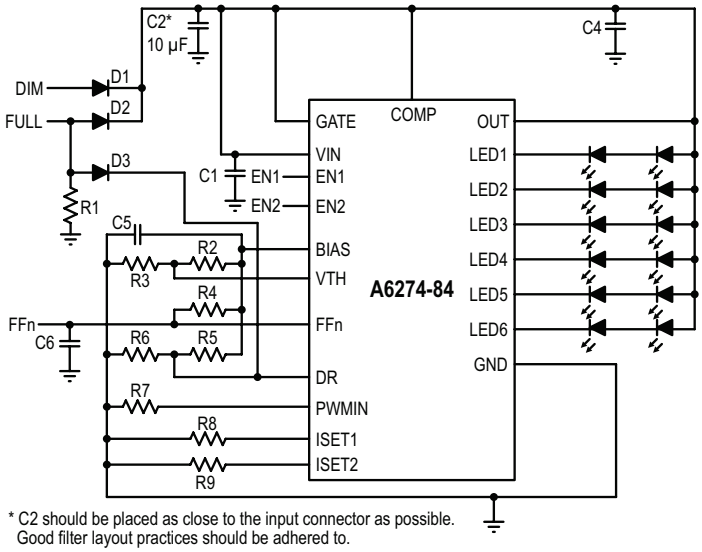
Operation without External P-Channel MOSFET

An external P-channel MOSFET should be used to minimize power dissipation in the IC; however, the A6274/84 can be used without an external MOSFET for low-power applications, as shown in Figure 17. The IC will detect but not be able to protect external components in case of A, D, and E faults. See Fault Table for more details.

Connect the GATE and COMP pins to VIN when an external PMOS is not connected. When the PMOS preregulator is not used, the LED string short faults B and C will be disabled.



* C2 should be placed as close to the input connector as possible. Good filter layout practices should be adhered to.

Figure 17: Operation without External P-Channel MOSFET
Connect COMP and GATE pins to VIN when external PMOS not used.

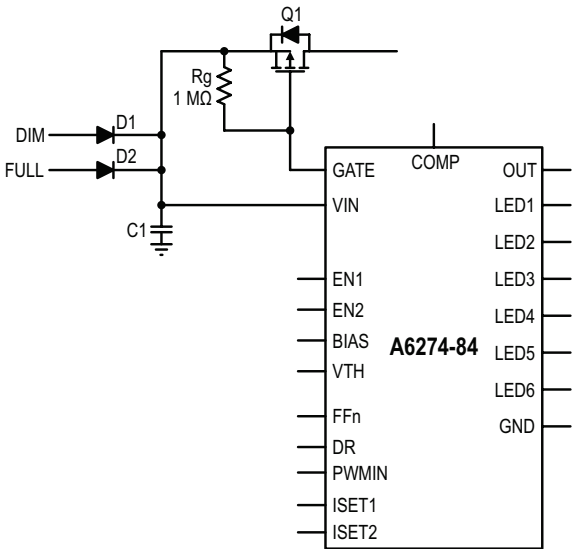


Figure 18: Floating Gate Protection
Add 1 MΩ resistor across MOSFET gate-source to prevent Q1 turn on in case of floating GATE pin.

Binning Resistor Arrangement

An external binning resistor can be connected in series with the ISETx pins as shown in Figure 19, to set appropriate current through various LED batches.

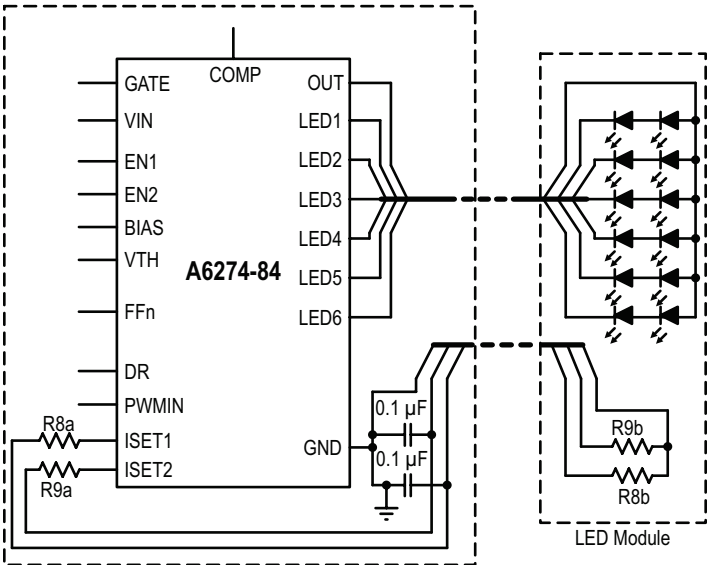


Figure 19: Application Circuit for Binning
Current-setting resistor can be placed on LED board for different bins of LEDs.

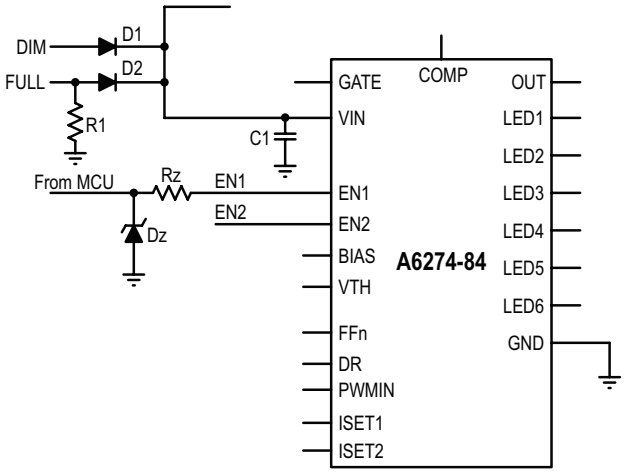


Figure 20: Application Circuit to Protect Microcontroller in Case of Accidental VIN Short to EN1
EN1 and VIN pins are close to each other. EN1 pin is rated for full supply voltage but external driving microcontroller may be damaged with VIN short. Adding a zener clamp will protect MCU.

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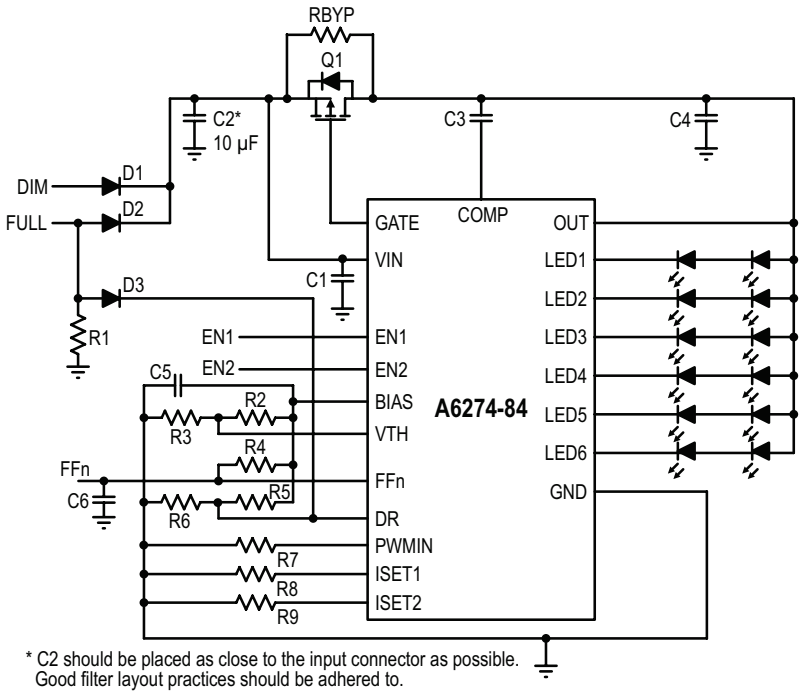

Figure 21 : Application circuit to prevent false latching state when $V_{OUT} < V_{OUT(SC)}$.

If any operating or fault condition causes OUT voltage to drop below $V_{OUT(SC)}$, the IC will detect this as a MOSFET drain short-to-ground fault. The IC will latch off as described in Fault-A in table 2. Adding a 1 MΩ bypass resistor across external MOSFET will keep $V_{OUT} > V_{OUT(SC)}$ level and prevent false latching. Adding this resistor will not affect normal MOSFET drain short-to-ground (Fault-A) detection.

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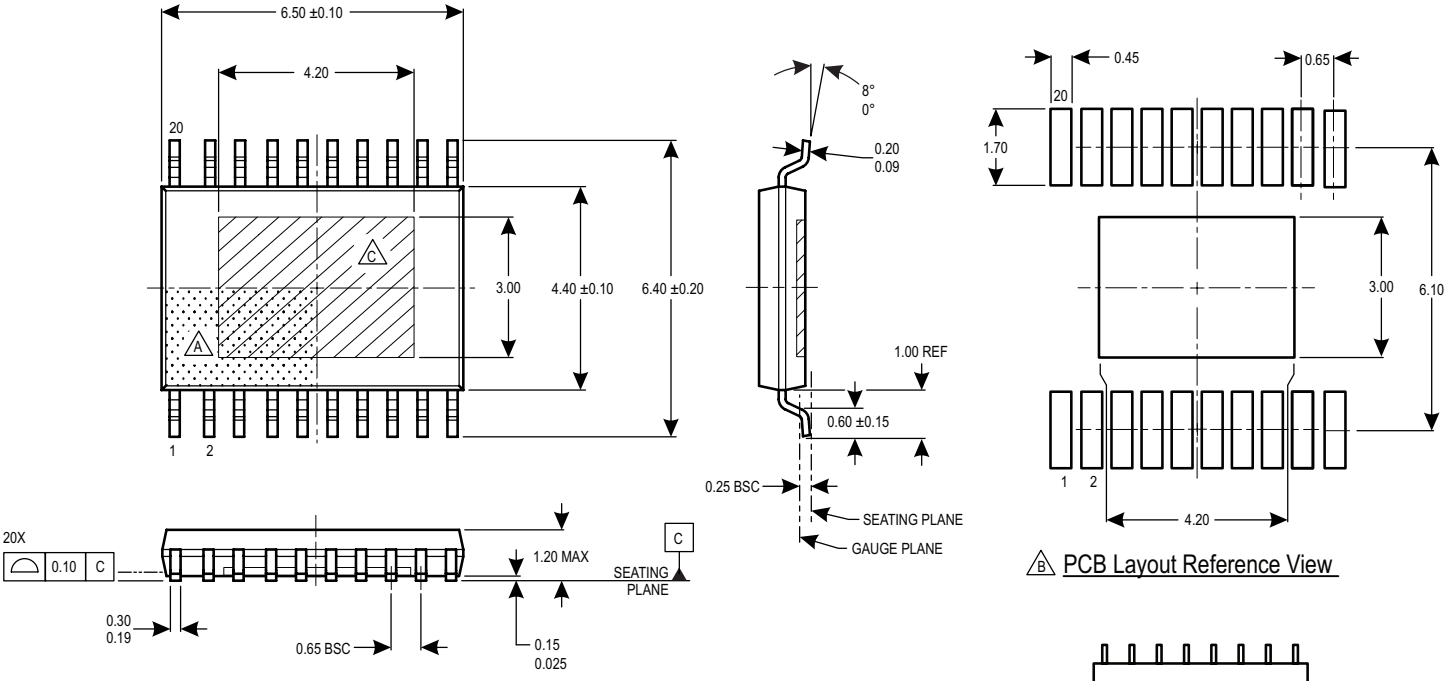
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-153ACT; Allegro DWG-0000379, Rev. 3)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 SOP65P640X110-21M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Exposed thermal pad (bottom surface)

D Branding scale and appearance at supplier discretion

Figure 22: Package LP, 20-Pin eTSSOP with Exposed Thermal Pad

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Revision Table

Number	Date	Description
–	July 8, 2016	Initial release
1	September 9, 2016	Added footnote to PWM Duty Cycle D_{PWM5} symbol (page 6).
2	January 3, 2017	Changed MOSFET Short Delay Disable Time at Startup typical value to 12 ms, and added MOSFET Drain Short Protection Blank Delay During Steady-State characteristic (pages 6, 13-14).
3	June 1, 2020	Updated Selection Guide, Figure 1, 10, 13, 15, 16, 17, 21 (added C2 capacitor and footnote), and other minor editorial updates
4	June 21, 2022	Updated package drawing (page 23)
5	June 4, 2026	Removed part number A6274KLPTR-T and made minor editorial modifications

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