FEMTOCLOCKS™ CRYSTAL-TO-3.3V LVPECL FREQUENCY SYNTHESIZER

ICS843003I-09

General Description

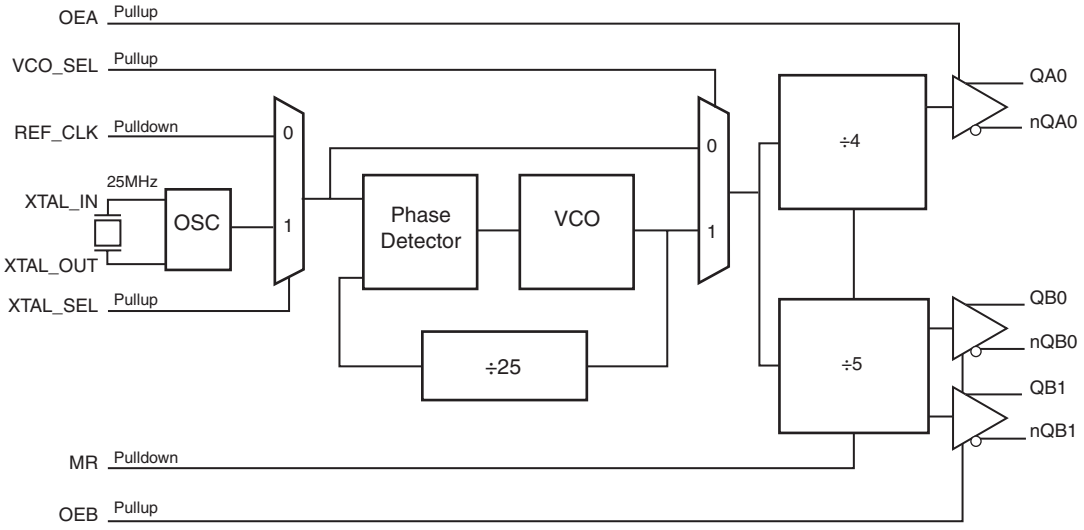
The ICS843003I-09 is a 3 differential output LVPECL Synthesizer designed to generate Ethernet reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from IDT. Using a 25MHz, 18pF parallel resonant crystal, the following frequencies can be generated: 156.25MHz and 125MHz. The 843003I-09 has two output banks, Bank A with one differential LVPECL output pair and Bank B with two differential LVPECL output pairs.

The ICS843003I-09 uses IDT's 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Ethernet jitter requirements. The ICS843003I-09 is packaged in a small 24-pin TSSOP, EPad package.

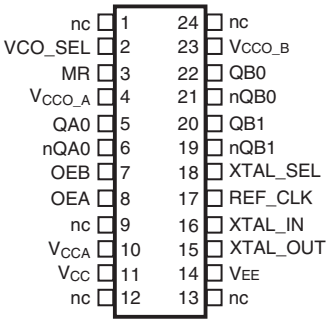
Features

- Three 3.3Vdifferential LVPECL output pairs on two banks:
  Bank A with one LVPECL output pair
  Bank B with two LVPECL output pairs
- Selectable crystal oscillator interface
  or LVCMOS/LVTTL single-ended reference clock input
- VCO range: 490MHz – 680MHz
- RMS phase jitter @ 156.25MHz (1.875MHz – 20MHz):
  0.53ps (typical)
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS843003I-09

24-Lead TSSOP, EPad
4.4mm x 7.8mm x 0.9mm
package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 9, 12, 13, 24	nc	Unused		No connect.
2	VCO_SEL	Input	Pullup	VCO select pin. When Low, the PLL is bypassed and the crystal reference or REF_CLK (depending on XTAL_SEL setting) are passed directly to the output dividers. Has an internal pullup resistor so the PLL is not bypassed by default. LVCMOS/LVTTL interface levels.
3	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs QX to go low and the inverted outputs nQX to go high. When logic LOW, the internal dividers and the outputs are enabled. MR has an internal pulldown resistor so the power-up default state of the outputs and dividers are enabled. LVCMOS/LVTTL interface levels.
4	V_{CCO_A}	Power		Output supply pin for Bank A outputs.
5, 6	QA0, nQA0	Output		Differential output pair. LVPECL interface levels.
7	OEB	Input	Pullup	Bank B output enable pin. Active High output enable. When logic HIGH, the 2 output pairs on Bank B are enabled. When logic LOW, the output pairs drive differential Low (QBx = Low, nQBx = High). OEB has an internal pullup resistor so the default power-up state of outputs are enabled. LVCMOS/LVTTL interface levels.
8	OEA	Input	Pullup	Bank A output enable pin. Active High output enable. When logic HIGH, the output pair on Bank A is enabled. When logic LOW, the output pair drives differential Low (QA0 = Low, nQA0 = High). OEA has an internal pullup resistor so the default power-up state of outputs are enabled. LVCMOS/LVTTL interface levels.
10	V_{CCA}	Power		Analog supply pin.
11	V_{CC}	Power		Core supply pin.
14	V_{EE}	Power		Negative supply pin.
15, 16	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
17	REF_CLK	Input	Pulldown	Single-ended reference clock input. LVCMOS/LVTTL interface levels.
18	XTAL_SEL	Input	Pullup	Crystal select pin. Selects between the single-ended REF_CLK or crystal interface. Has an internal pullup resistor so the crystal interface is selected by default. LVCMOS/LVTTL interface levels.
19, 20	nQB1, QB1	Output		Differential output pair. LVPECL interface levels.
21, 22	nQB0, QB0	Output		Differential output pair. LVPECL interface levels.
23	V_{CCO_B}	Power		Output supply pin for Bank B outputs.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Bank A Frequency Table

Input Crystal Frequency (MHz)	Feedback Divider	Bank A Output Divider	M/N Multiplication Factor	QA0/nQA0 Output Frequency (MHz)
25	25	4	6.25	156.25
24	25	4	6.25	150
20	25	4	6.25	125

Table 3B. Bank B Frequency Table

Input Crystal Frequency (MHz)	Feedback Divider	Bank B Output Divider	M/N Multiplication Factor	QB[0:1]/nQB[0:1] Output Frequency (MHz)
25	25	5	5	125

Table 3C. OEA Select Function Table

Input	Outputs	
OEA	QA0	nQA0
0	LOW	HIGH
1	Active	Active

Table 3D. OEB Select Function Table

Input	Outputs	
OEB	QB0, QB1	nQB0, nQB1
0	LOW	HIGH
1	Active	Active

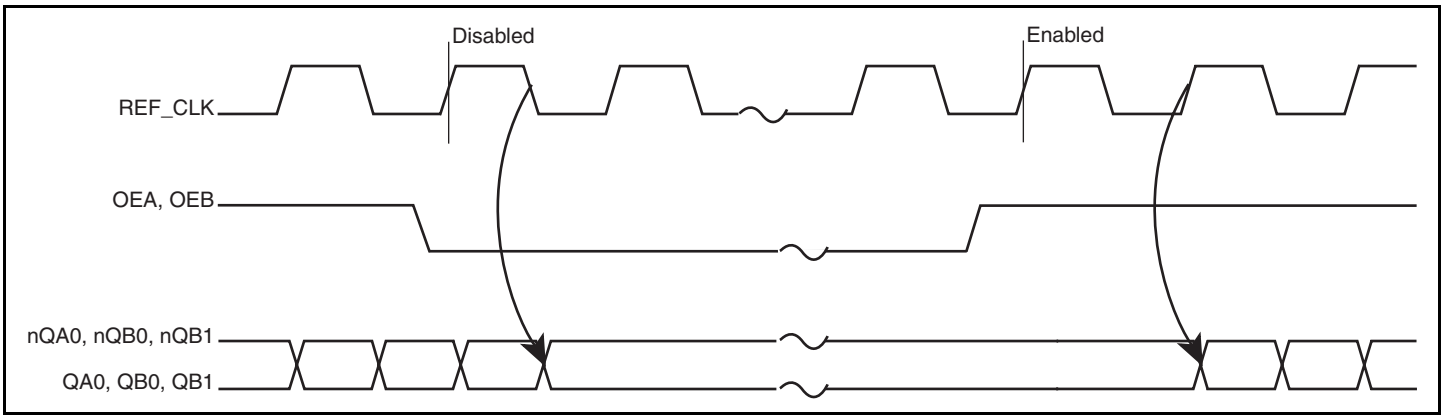


Figure 1. OE Timing Diagram

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	32.1°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCO\_A} = V_{CCO\_B} = 3.3V \pm 5\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.20	3.3	3.465	V
V_{CCO_A}, V_{CCO_B}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				150	mA
I_{CCA}	Analog Supply Current				20	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCO\_A} = V_{CCO\_B} = 3.3V \pm 5\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	MR, REF_CLK	$V_{CC} = V_{IN} = 3.465V$			150	µA
		OEA, OEB, VCO_SEL, XTAL_SEL	$V_{CC} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	MR, REF_CLK	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-5			µA
		OEA, OEB, VCO_SEL, XTAL_SEL	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA

Table 4C. LVPECL DC Characteristics, $V_{CC} = V_{CCO\_A} = V_{CCO\_B} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Current; NOTE 1		$V_{CCO\_A/B} - 1.4$		$V_{CCO\_A/B} - 0.9$	µA
V_{OL}	Output Low Current; NOTE 1		$V_{CCO\_A/B} - 2.0$		$V_{CCO\_A/B} - 1.7$	µA
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to $V_{CCO\_A, \_B} - 2V$.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		19.6		27.2	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

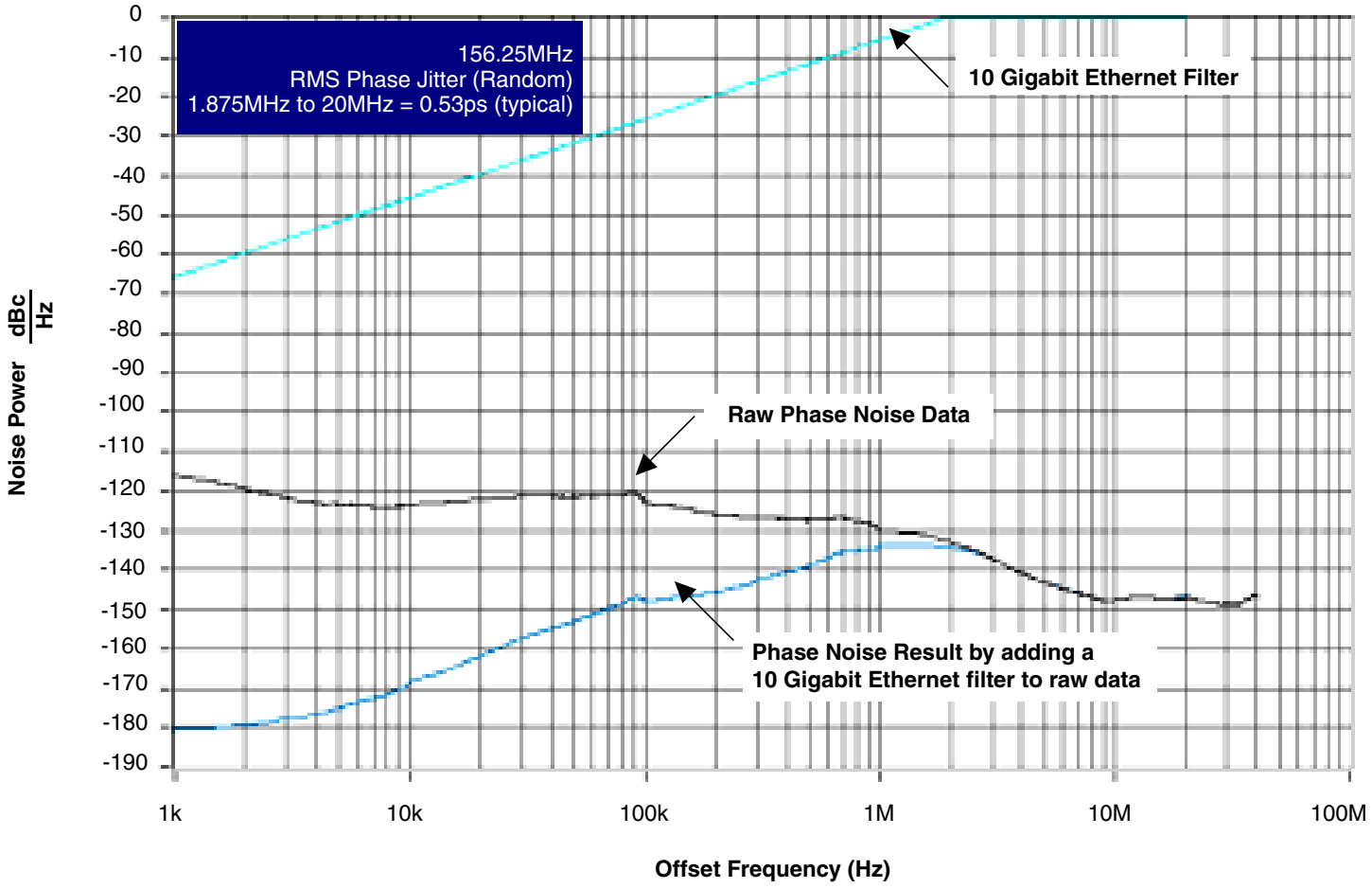
AC Electrical Characteristics

Table 6. AC Characteristics, $V_{CC} = V_{CCO\_A} = V_{CCO\_B} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

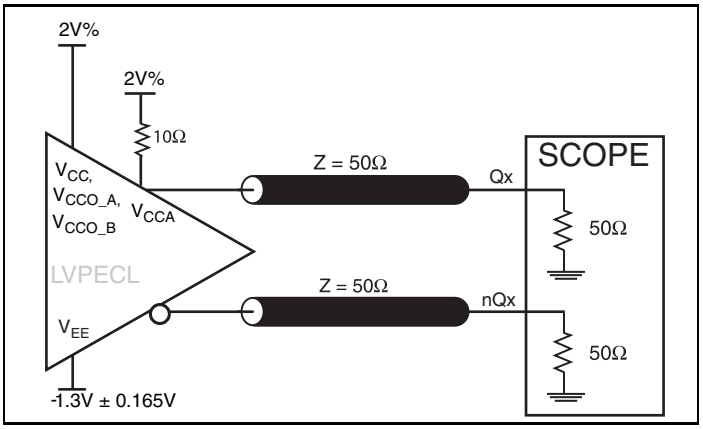
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Range	÷4	122.5		170	MHz
		÷5	98		136	MHz
*t*jit(Ø)	RMS Phase Jitter, (Random); NOTE 1	156.25MHz, (1.875MHz – 20MHz)		0.53		ps
		125MHz, (1.875MHz – 20MHz)		0.48		ps
*t*sk(b)	Bank Skew; NOTE 2				50	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		600	ps
odc	Output Duty Cycle		45		55	%

NOTE 1: Please refer to the Phase Noise Plots.
NOTE 2: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.

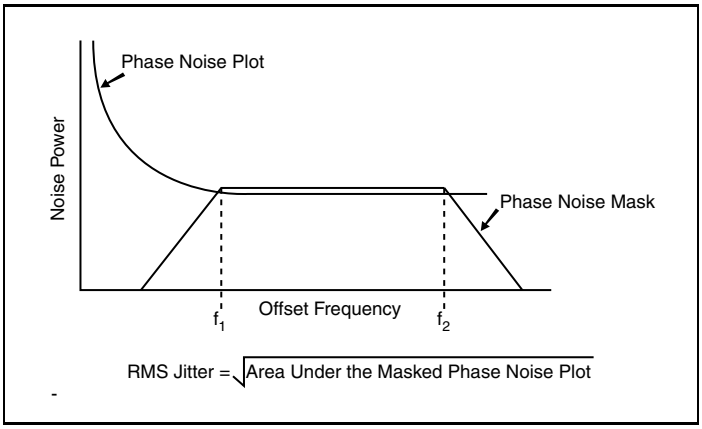
Typical Phase Noise at 156.25MHz



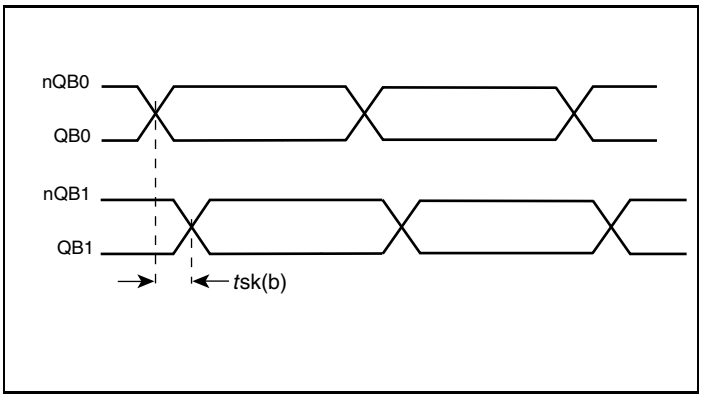
Parameter Measurement Information



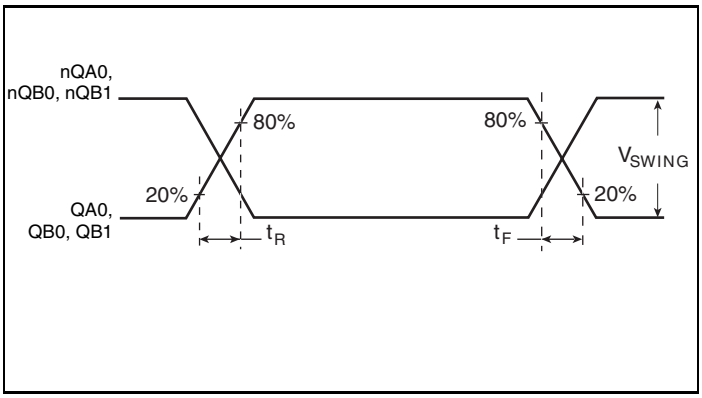
3.3V LVPECL Output Load AC Test Circuit



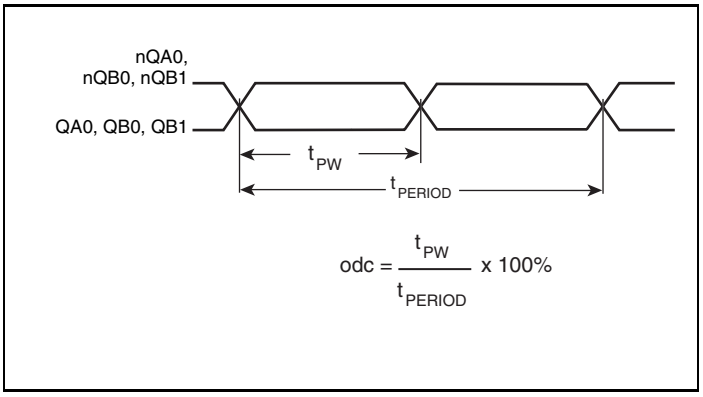
RMS Phase Jitter



Bank Skew



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS843003I-09 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, V_{CCO_B} and V_{CCO_B} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 2* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin.

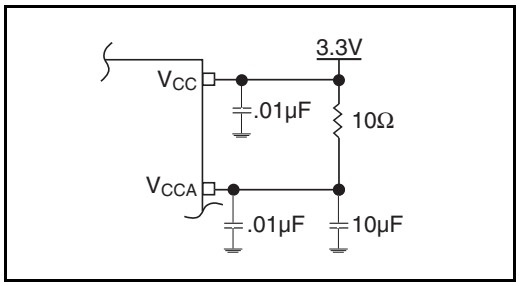


Figure 2. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Crystal Input Interface

The ICS843003I-09 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 3* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

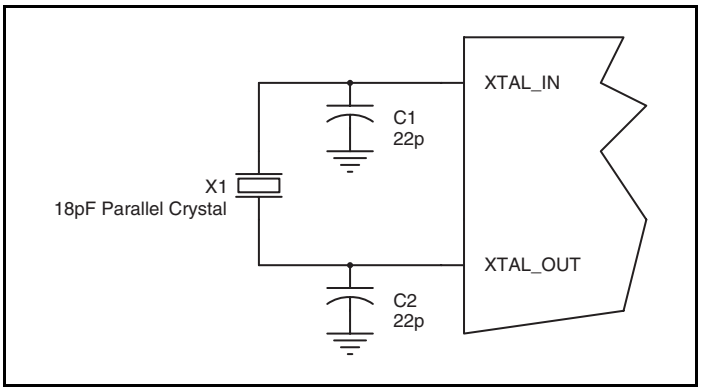


Figure 3. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 4.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

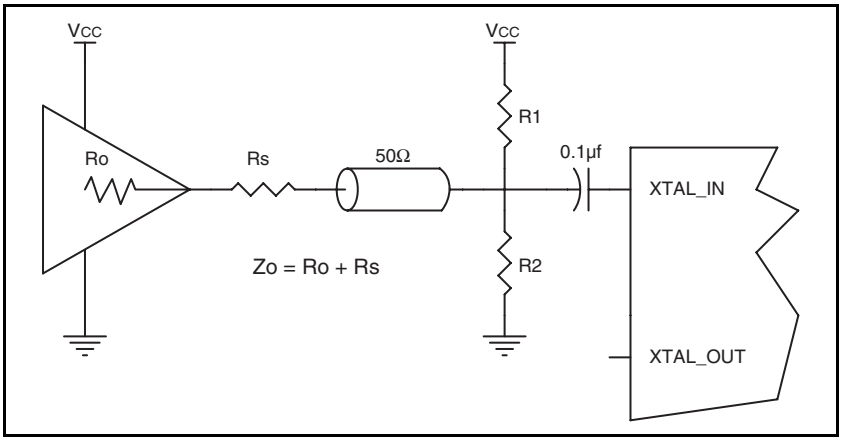


Figure 4. General Diagram for LVCMOS Driver to XTAL Input Interface

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

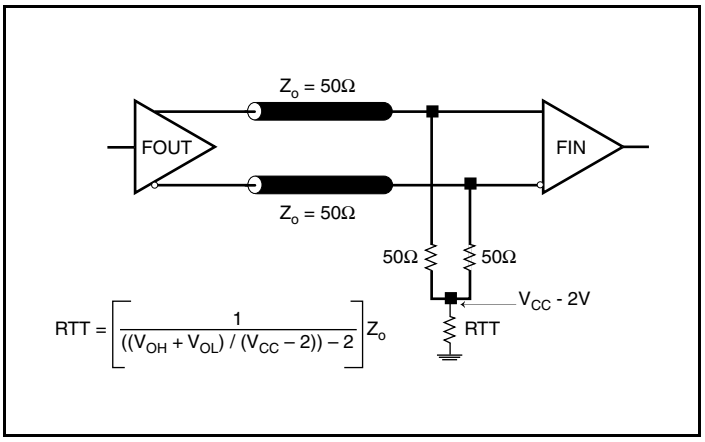


Figure 5A. 3.3V LVPECL Output Termination

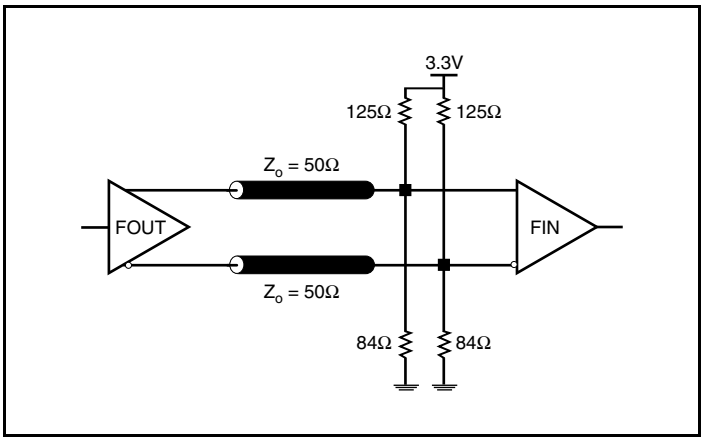


Figure 5B. 3.3V LVPECL Output Termination

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

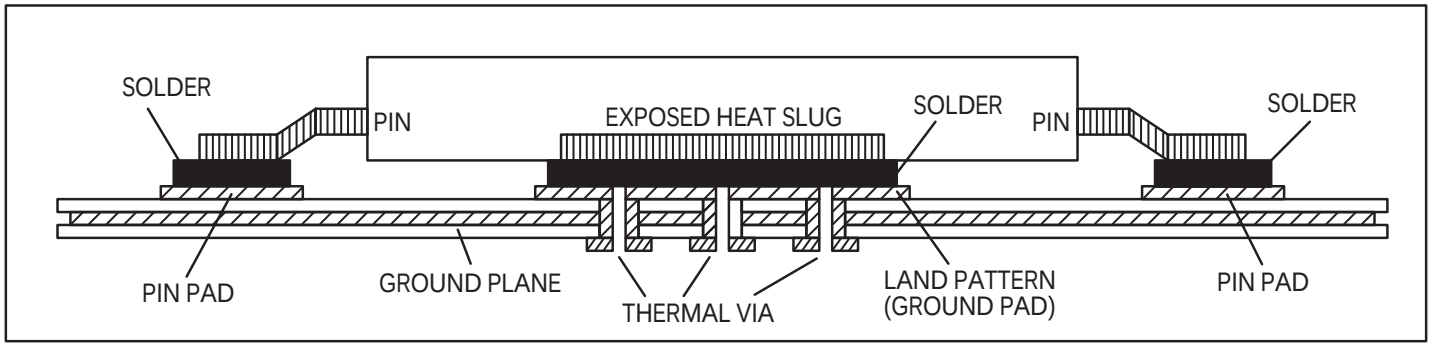


Figure 6. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS843003I-09.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS843003I-09 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 150mA = **519.75mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 3 * 30mW = **90mW**

Total Power$_{\_MAX}$ (3.3V, with all outputs switching) = 519.75mW + 90mW = **609.75mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 32.1°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.610W * 32.1°C/W = 104.6°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 7. Thermal Resistance θ_{JA} for 24 Lead TSSOP, EPad Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	32.1°C/W	25.5°C/W	24°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7.*

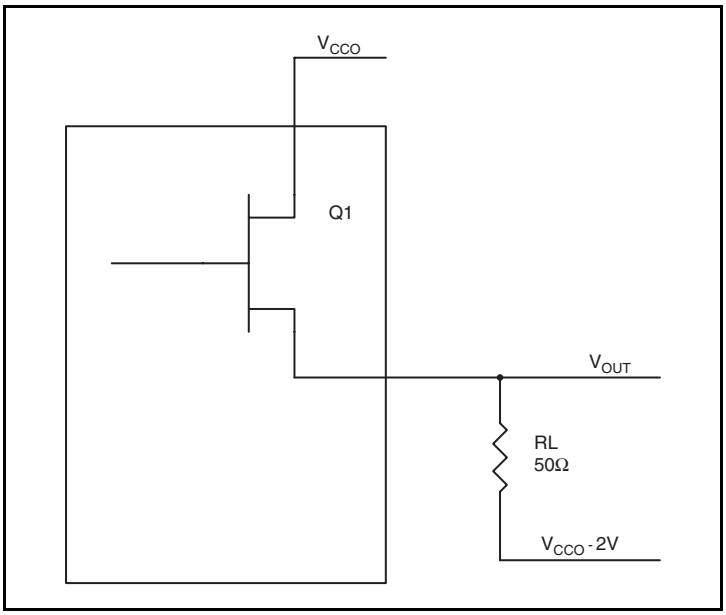


Figure 7. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} =$ **V_{CCO_MAX} – 0.9V**
  (V_{CCO_MAX} - V_{OH_MAX}) = **0.9V**
- For logic low, $V_{OUT} = V_{OL\_MAX} =$ **V_{COO_MAX} – 1.7V**
  (V_{CCO_MAX} - V_{OL_MAX}) = **1.7V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

Pd_H = $[(V_{OH\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50Ω] * 0.9V =$ **19.8mW**

Pd_L = $[(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50Ω] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 24 Lead TSSOP, EPad

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	32.1°C/W	25.5°C/W	24°C/W

Transistor Count

The transistor count for ICS843003I-09 is: 3822

Package Outline and Package Dimensions

Package Outline - G Suffix for 24 Lead TSSOP, EPad

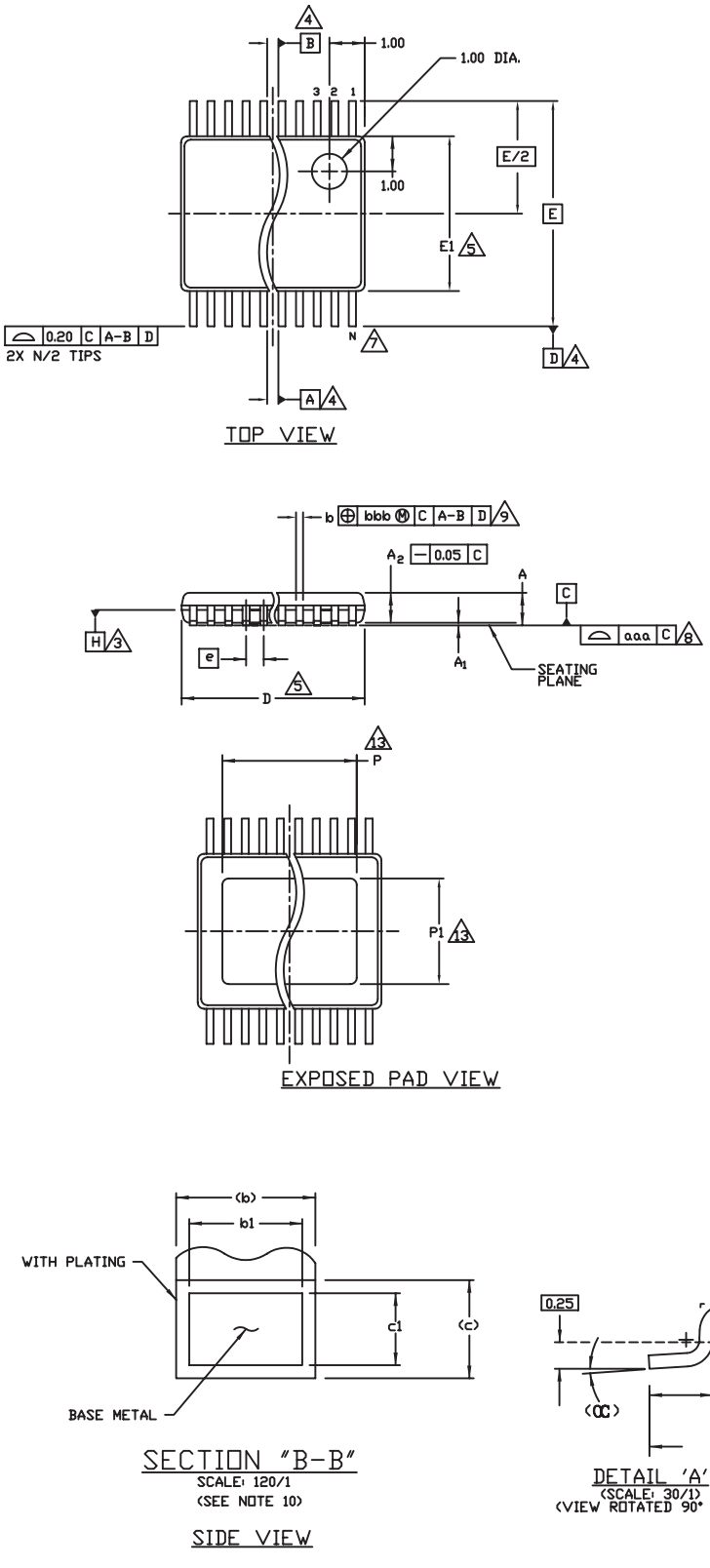


Table 9. Package Dimensions

All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		24	
A			1.10
A1	0.05		0.15
A2	0.85	0.90	0.95
b	0.19		0.30
b1	0.19	0.22	0.25
c	0.09		0.20
c1	0.09	0.127	0.16
D	7.70		7.90
E		6.40 Basic	
E1	4.30	4.40	4.50
e		0.65 Basic	
L	0.50	0.60	0.70
P	5.0		5.5
P1	3.0		3.2
α	0°		8°
ααα		0.076	
bbb		0.10	

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843003BGI-09	ICS843003BI09	24 Lead TSSOP, E-Pad	Tube	-40°C to 85°C
843003BGI-09T	ICS843003BI09	24 Lead TSSO, EPad	2500 Tape & Reel	-40°C to 85°C
843003BGI-09LF	ICS43003BI09L	“Lead-Free” 24 Lead TSSOP, EPad	Tube	-40°C to 85°C
843003BGI-09LFT	ICS43003BI09L	“Lead-Free” 24 Lead TSSOP, EPad	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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