



TPDxE05U06 1, 4, 6 Channel ESD Protection Device for Super-Speed (Up to 6 Gbps) Interface

1 Features

- IEC 61000-4-2 Level 4 ESD Protection
 - ± 12 -kV Contact Discharge
 - ± 15 -kV Air Gap Discharge
- IEC 61000-4-4 EFT Protection
 - 80 A (5/50 ns)
- IEC 61000-4-5 Surge Protection
 - 2.5 A (8/20 μ s)
- IO Capacitance 0.42 pF to 0.5 pF (Typical)
- DC Breakdown Voltage 6.5 V (Minimum)
- Ultra low Leakage Current 10 nA (Maximum)
- Low ESD Clamping Voltage
- Industrial Temperature Range: -40°C to $+125^{\circ}\text{C}$
- Easy Straight-Through Routing Packages

2 Applications

- HDMI 1.4b
- HDMI 2.0
- USB 3.0
- MHL
- LVDS Interfaces
- DisplayPort
- PCI-Express[®]
- eSata Interfaces
- V-by-One[®] HS

3 Description

The TPDxE05U06 is a family of unidirectional Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diodes with ultra-low capacitance. Each device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 international standard. The TPDxE05U06s ultra-low loading capacitance makes it ideal for protecting any high-speed signal pins.

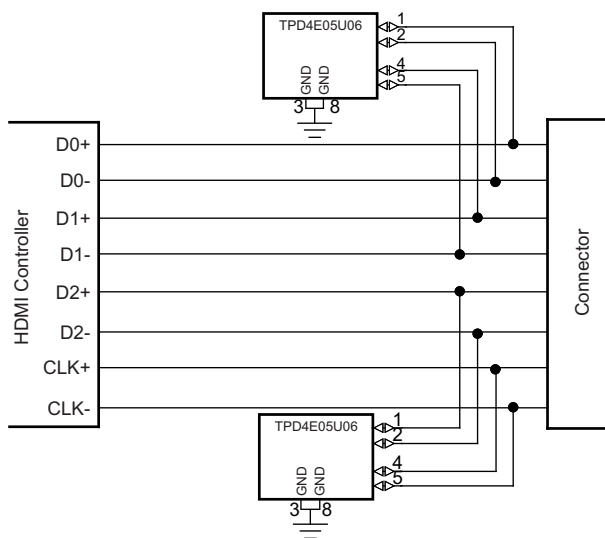
Typical applications for TPDxE05U06 includes high speed signal lines in HDMI 1.4b, HDMI 2.0, USB 3.0, MHL, LVDS, DisplayPort, PCI-Express[®], eSata, and V-by-One[®] HS.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD1E05U06	X1SON (2)	0.60 mm $\times$ 1.00 mm
TPD4E05U06	USON (10)	2.50 mm $\times$ 1.00 mm
TPD6E05U06	USON (14)	3.50 mm $\times$ 1.35 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



TPD4E05U06 Functional Block Diagram

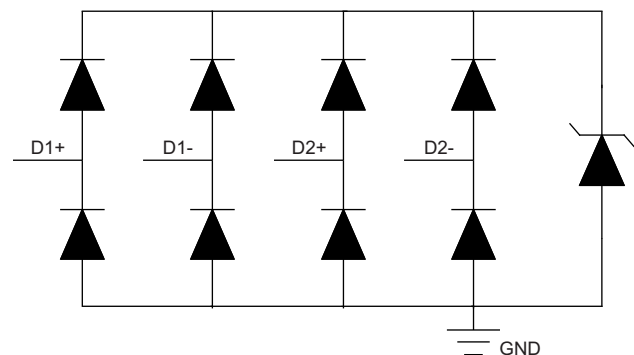


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (November 2016) to Revision L	Page
• Updated DPY pinout image.	4
• Updated title from TPD4E05U06 to TPD6E05U06 in Figure 13	10

Changes from Revision J (March 2016) to Revision K	Page
• Changed min value of V_{BR} from "6 V" to "6.5 V" in the Electrical Characteristics table	7

Changes from Revision I (June 2015) to Revision J	Page
• Replaced all instances of X2SON with X1SON.....	1
• Update the <i>Pin Functions</i> table	4
• Added Power Supply Recommendations section.....	16

Changes from Revision H (May 2015) to Revision I	Page
• Added Trademarks	1
• Corrected TPD6E05U06 Pin 13 name	5
• Corrected TLP definition	7

Changes from Revision G (July 2014) to Revision H	Page
• Added Additional Application.....	1
• Updated with HDMI 2.0 Eye Diagrams.....	13

Changes from Revision F (November 2013) to Revision G
Page

• Added 61000-4-4 EFT compliance.....	1
• Added Handling Ratings table.....	6
• Added Thermal Information table.	6
• Added Detailed Description section.	10
• Added Application and Implementation section.	12
• Added Layout section.	16

Changes from Original (December 2012) to Revision A
Page

• Added TPS2EUSB30A part to document.....	1
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Changes from Revision A (December 2012) to Revision B
Page

• Added Insertion Loss Graphic.....	9
• Added Eye Diagrams.....	13

Changes from Revision B (January 2013) to Revision C
Page

• Changed IO Capacitance range.....	1
• Changed test conditions and typ values for V_{clamp}	7
• Added typ R_{DYN} values for DQA and RVZ packages.....	7
• Added C_L values for DQA and RVZ packages.....	7
• Changed CURRENT vs VOLTAGE graphic.....	8
• Changed Insertion Loss graphic.....	9
• Changed HDMI Eye Diagrams.....	13

Changes from Revision C (March 2013) to Revision D
Page

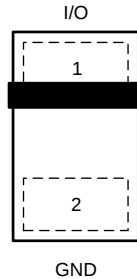
• Updated Title.....	1
• Removed Ordering Information table.....	4

Changes from Revision D (August 2013) to Revision E
Page

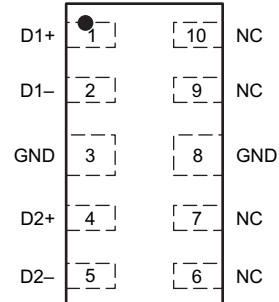
• Updated document formatting.....	1
• Added additional application.....	1

5 Pin Configuration and Functions

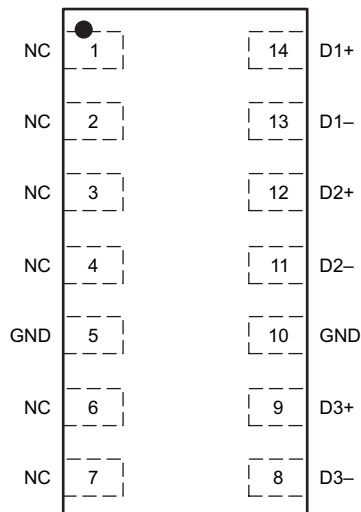
DPY Package
2-Pin X1SON
Top View



DQA Package
10-Pin USON
Top View



RVZ Package
14-Pin USON
Top View



Pin Functions TPD1E05U06 DPY

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	2	Ground	Ground; Connect to ground
I/O	1	I/O	ESD protected channel ⁽¹⁾

(1) Place as close to the connector as possible.

Pin Functions TPD4E05U06 DQA

PIN		TYPE	DESCRIPTION
NAME	NO.		
D1+	1	I/O	ESD protected channel ⁽¹⁾
D1–	2	I/O	ESD protected channel ⁽¹⁾
D2+	4	I/O	ESD protected channel ⁽¹⁾
D2–	5	I/O	ESD protected channel ⁽¹⁾

(1) Place as close to the connector as possible.

Pin Functions TPD4E05U06 DQA (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	3	Ground	Ground; Connect to ground
GND	8		
NC	6	—	Not connected; Used for optional straight-through routing. Can be left floating or grounded
NC	7		
NC	9		
NC	10		

Pin Functions TPD6E05U06 RVZ

PIN		TYPE	DESCRIPTION
NAME	NO.		
D1+	14	I/O	ESD protected channel ⁽¹⁾
D1–	13	I/O	ESD protected channel ⁽¹⁾
D2+	12	I/O	ESD protected channel ⁽¹⁾
D2–	11	I/O	ESD protected channel ⁽¹⁾
D3+	9	I/O	ESD protected channel ⁽¹⁾
D3–	8	I/O	ESD protected channel ⁽¹⁾
GND	5	Ground	Ground; Connect to ground
GND	10		
NC	1	—	Not connected; Used for optional straight-through routing. Can be left floating or grounded
NC	2		
NC	3		
NC	4		
NC	6		
NC	7		

(1) Place as close to the connector as possible.

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾⁽²⁾⁽³⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Electrical fast transient	IEC 61000-4-4 (5/50 ns)		80	A
Peak pulse	IEC 61000-4-5 Current (tp – 8/20 μ s) ⁽⁴⁾		2.5	A
	IEC 61000-4-5 Power (tp – 8/20 μ s) ⁽⁴⁾		40	W
T _A	Operating temperature	–40	125	°C
T _{stg}	Storage temperature	–65	155	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Absolute maximum ratings apply over recommended junction temperature range.
- (3) Voltages are with respect to GND unless otherwise noted.
- (4) Measured at 25°C.

6.2 ESD Ratings—JEDEC Specification

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±4000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±1500 V may actually have higher performance.

6.3 ESD Ratings—IEC Specification

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	IEC 61000-4-2 contact discharge	±12000
		IEC 61000-4-2 air-gap discharge	±15000

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{IO}	Input pin voltage	0	5.5	V
T _A	Operating free-air temperature	–40	125	°C

6.5 Thermal Information

THERMAL METRIC ⁽¹⁾		TPD1E05U06	TPD4E05U06	TPD6E05U06	UNIT
		DPY (X1SON)	DQA (USON)	RVZ (USON)	
		2 PINS	10 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	697.3	327	197.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	471	189.5	119.1	°C/W
R _{θJB}	Junction-to-board thermal resistance	575.9	257.7	92.6	°C/W
ψ _{JT}	Junction-to-top characterization parameter	175.7	60.9	22	°C/W
ψ _{JB}	Junction-to-board characterization parameter	575.1	257	91.6	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{RWM}	Reverse stand-off voltage	I _{IO} < 10 μA				5.5	V
V _{BR}	Break-down voltage	I _{IO} = 1 mA		6.5		8.5	V
V _{clamp}	Clamp voltage	I = 1 A, TLP, I/O to ground ⁽¹⁾			10		V
		I = 5 A, TLP, I/O to ground ⁽¹⁾			14		
		I = 1 A, TLP, ground to I/O ⁽¹⁾			3		
		I = 5 A, TLP, ground to I/O ⁽¹⁾			7		
I _{LEAK}	Leakage current	V _{IO} = 2.5 V			0.01	10	nA
R _{DYN}	DPY package dynamic resistance	I/O to GND ⁽²⁾			0.8		Ω
		GND to I/O ⁽²⁾			0.8		
	DQA package dynamic resistance	I/O to GND ⁽²⁾			0.8		Ω
		GND to I/O ⁽²⁾			0.8		
	RVZ package dynamic resistance	I/O to GND ⁽²⁾			0.8		Ω
		GND to I/O ⁽²⁾			0.8		
Capacitance							
C _L	Line capacitance ⁽³⁾	V _{IO} = 2.5 V, f = 1 MHz, I/O to GND	TPD1E05U06 DPY package		0.42		pF
			TPD4E05U06 DQA package		0.5		
			TPD6E05U06 RVZ package		0.47		
ΔC _{IO-TO-GND}	Variation of channel input capacitance	GND Pin = 0 V, F = 1 GHz, V _{BIAS} = 2.5 V, channel_x pin to GND – channel_y pin to GND			0.05	0.07	pF
C _{CROSS}	Channel to channel input capacitance	GND Pin = 0 V, F = 1 GHz, V _{BIAS} = 2.5 V, between channel pins			0.01	0.06	pF

(1) Transmission Line Pulse (TLP) with 100 ns width, 200 ps rise time.

(2) Extraction of R_{DYN} using least squares fit of TLP characteristics between $I = 10 \text{ A}$ and $I = 20 \text{ A}$.

(3) Capacitance data is taken at 25°C.

6.7 Typical Characteristics

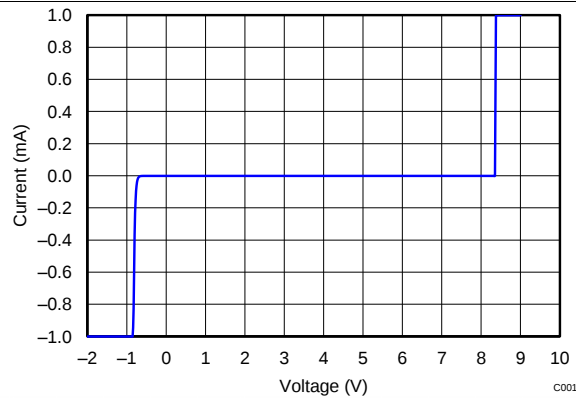


Figure 1. DC Voltage Sweep I-V Curve

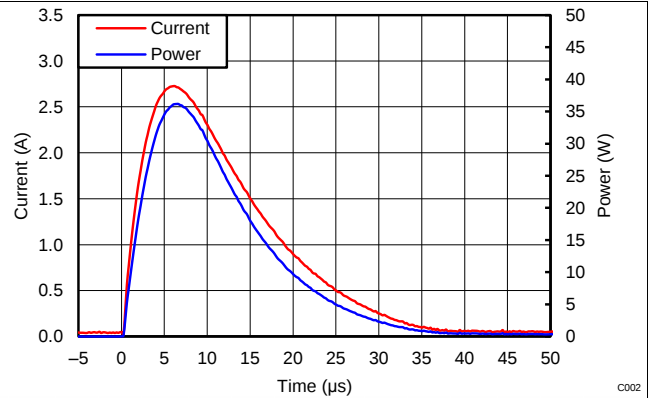


Figure 2. Surge Curve ($t_p = 8/20 \mu s$), Pin IO to GND

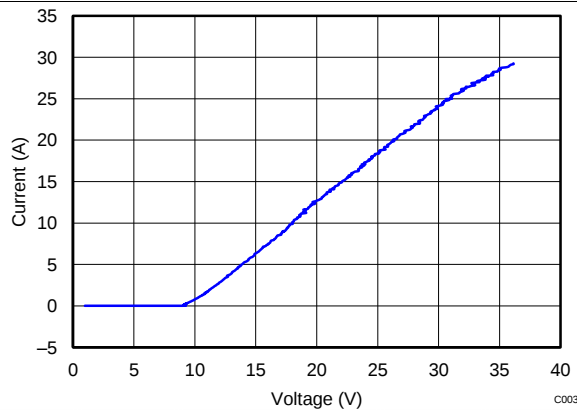


Figure 3. Positive TLP Plot IO to GND

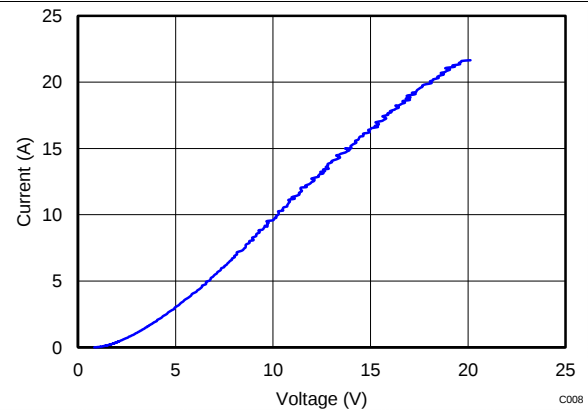


Figure 4. Negative TLP Plot IO to GND

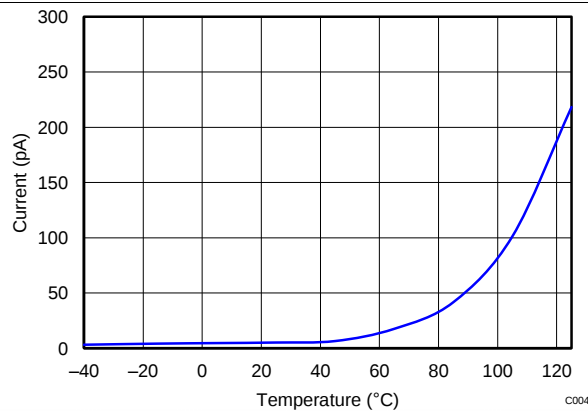


Figure 5. Leakage vs Temperature

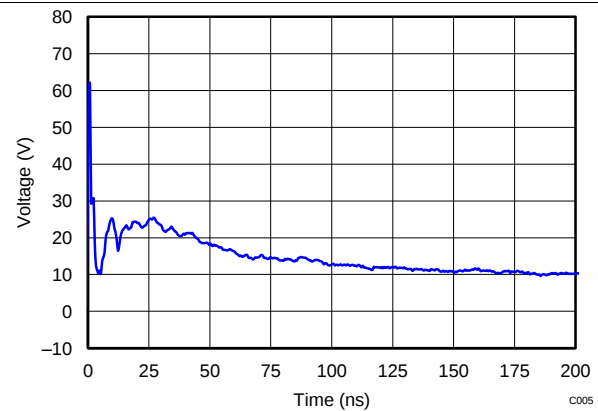


Figure 6. 8-kV IEC Waveform

Typical Characteristics (continued)

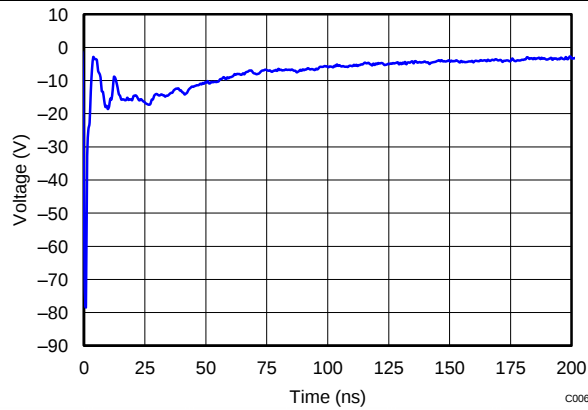


Figure 7. -8-kV IEC Waveform

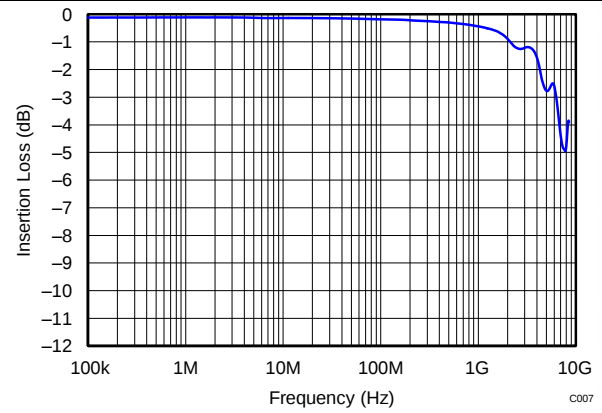


Figure 8. TPD1E05U06 Insertion Loss

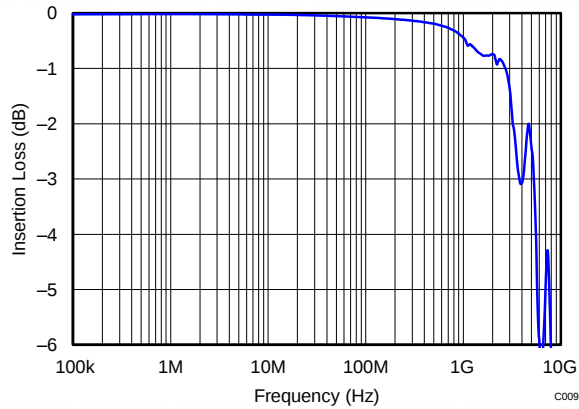


Figure 9. TPD4E05U06 Insertion Loss

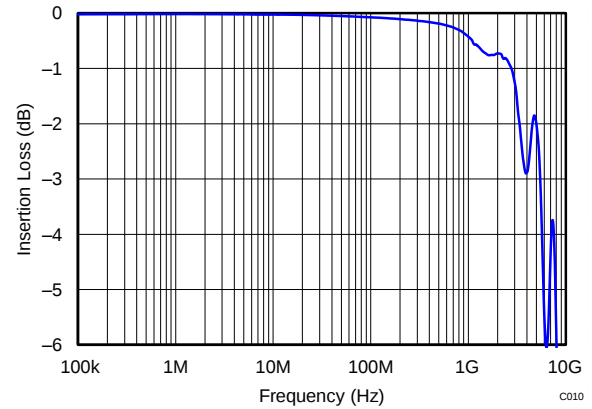


Figure 10. TPD6E05U06 Insertion Loss

7 Detailed Description

7.1 Overview

The TPDxE05U06 is a family of unidirectional Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diodes with ultra-low capacitance. Each device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 international standard. The TPDxE05U06s ultra-low loading capacitance makes it ideal for protecting any high-speed signal pins.

7.2 Functional Block Diagram

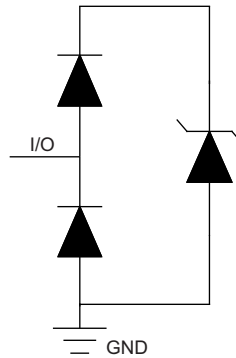


Figure 11. TPD1E05U06 Block Diagram

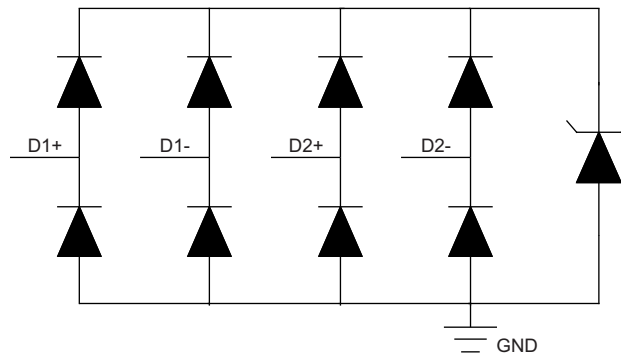


Figure 12. TPD4E05U06 Block Diagram

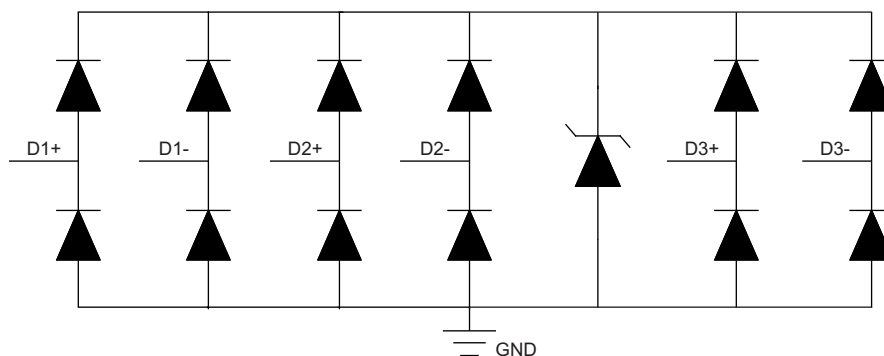


Figure 13. TPD6E05U06 Block Diagram

7.3 Feature Description

The TPDxE05U06 is a family of unidirectional Transient Voltage Suppressor (TVS) Electrostatic Discharge (ESD) protection diodes with ultra-low capacitance. Each device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 international standard. The TPDxE05U06s ultra-low loading capacitance makes it ideal for protecting any high-speed signal pins.

7.3.1 ± 15 -kV IEC61000-4-2 Level 4 ESD Protection

The I/O pins can withstand ESD events up to ± 12 -kV contact and ± 15 -kV air. An ESD-surge clamp diverts the current to ground.

7.3.2 IEC61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50- Ω impedance). An ESD-surge clamp diverts the current to ground. This has been validated on the TPD4E05U06 only.

7.3.3 IEC61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 2.5 A and 40 W (8/20 μ s waveform). An ESD-surge clamp diverts this current to ground.

7.3.4 I/O Capacitance

The capacitance between each I/O pin to ground is 0.42 pF (TPD1E05U06), 0.5 pF (TPD4E05U06) or 0.47 pF (TPD6E05U06). These devices support data rates up to 6 Gbps.

7.3.5 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is a minimum of 6 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of 5 V.

7.3.6 Ultra-Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (max) with a bias of 2.5 V.

7.3.7 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 10 V ($I_{PP} = 1$ A).

7.3.8 Industrial Temperature Range

This device features an industrial operating range of -40°C to $+125^{\circ}\text{C}$.

7.3.9 Easy Flow-Through Routing

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

7.4 Device Functional Modes

The TPDxE05U06 is a passive integrated circuit that triggers when voltages are above VBR or below the lower diodes V_f (-0.6 V). During ESD events, voltages as high as ± 15 kV (air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of TPDxE05U06 (usually within 10s of nano-seconds) the device reverts to passive.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPDxE05U06 is a diode type TVS which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP} , to a safe level for the protected IC.

8.2 Typical Applications

8.2.1 HDMI 2.0 Application

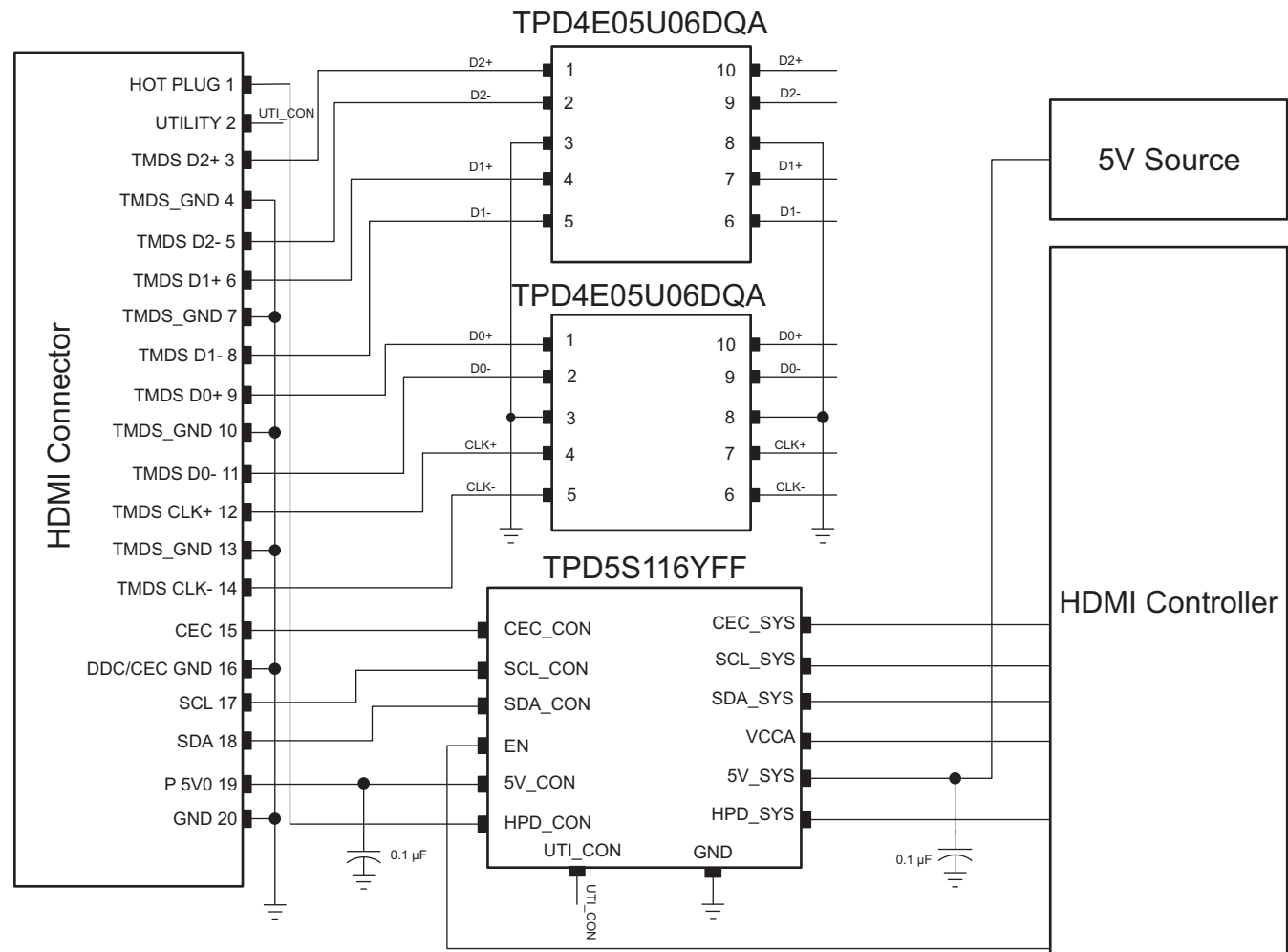


Figure 14. HDMI 2.0 Schematic

Typical Applications (continued)

8.2.1.1 Design Requirements

For this design example, the two TPD4E05U06 devices, and a TPD5S116 are being used in an HDMI 2.0 application. This provides a complete port protection scheme.

Given the HDMI 2.0 application, the parameters listed in [Table 1](#) are known.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on pins 1, 2, 4, or 5	0 V to 5 V
Operating frequency	3 GHz

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Signal Range on Pin 1, 2, 4, or 5

The TPD4E05U06 has 4 identical protection channels for signal lines. The symmetry of the device provides flexibility when selecting which of the 4 I/O channels is going to protect which signal lines. Any I/O supports a signal range of 0 to 5.5 V.

8.2.1.3 Application Curves

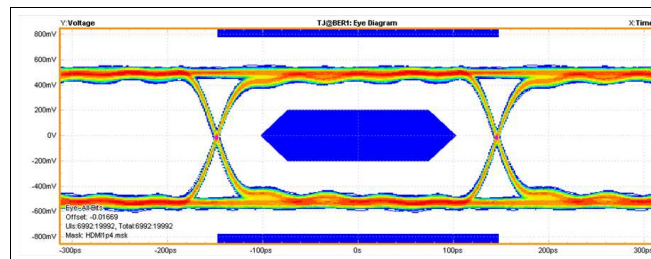


Figure 15. 3.4-Gbps HDMI 1.4 TP1 Eye Diagram Unpopulated EVM

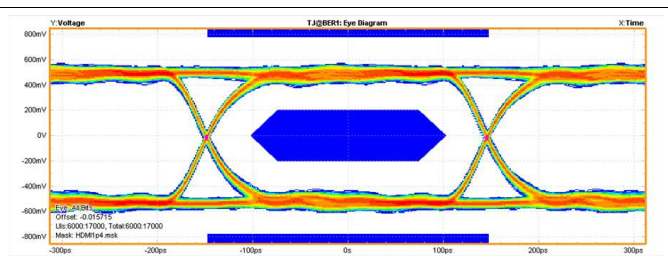


Figure 16. 3.4-Gbps HDMI 1.4 TP1 Eye Diagram TPD1E05U06

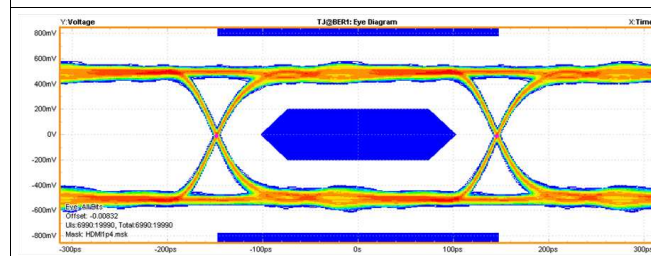


Figure 17. 3.4-Gbps HDMI 1.4 TP1 Eye Diagram TPD4E05U06

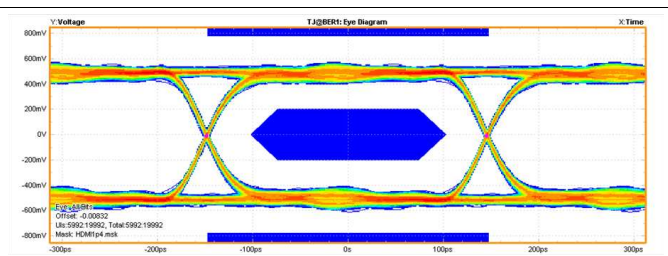


Figure 18. 3.4-Gbps HDMI 1.4 TP1 Eye Diagram TPD6E05U06

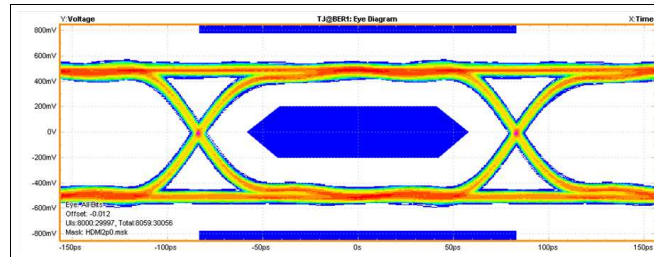


Figure 19. 6-Gbps HDMI 2.0 (TP1) Eye Diagram Unpopulated EVM

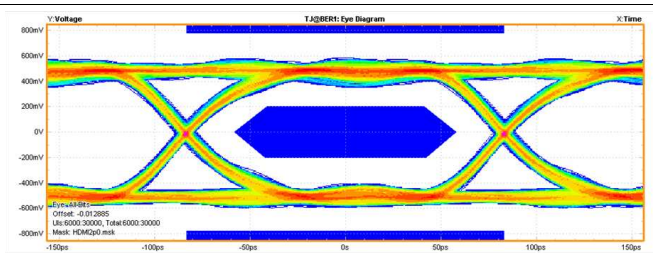


Figure 20. 6-Gbps HDMI 2.0 (TP1) Eye Diagram TPD1E05U06

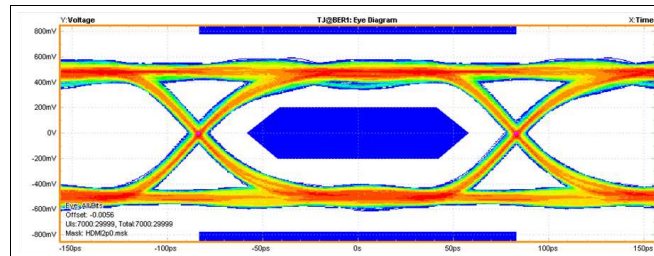


Figure 21. 6-Gbps HDMI 2.0 (TP1) Eye Diagram TPD4E05U06

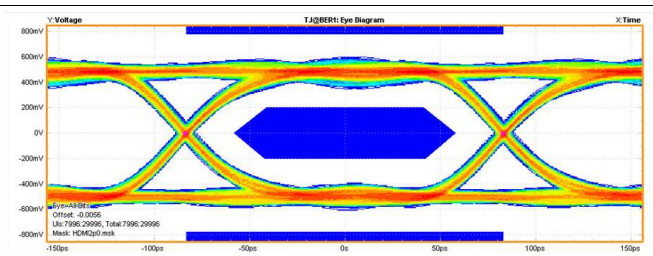


Figure 22. 6-Gbps HDMI 2.0 (TP1) Eye Diagram TPD6E05U06

8.2.2 HDMI 2.0 Application

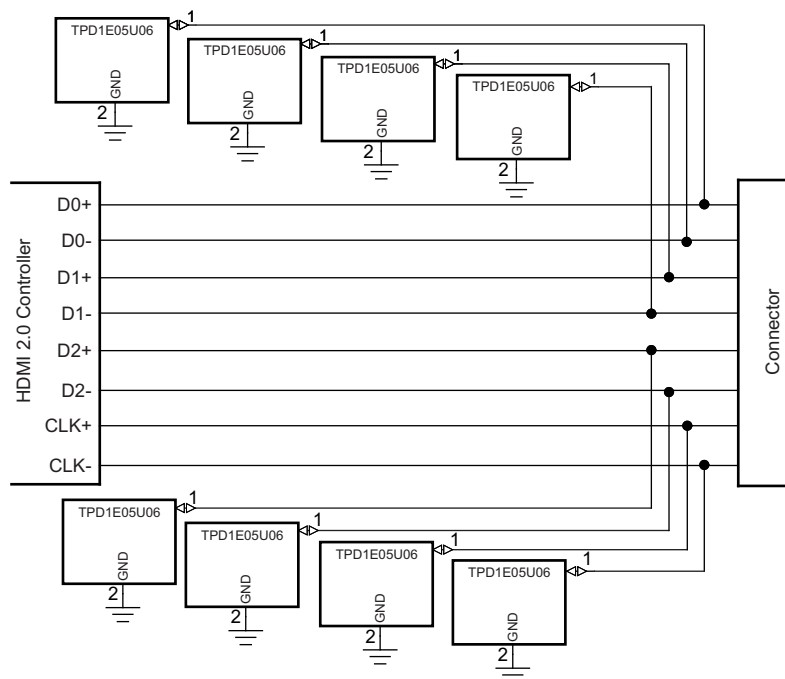


Figure 23. HDMI 2.0 Schematic

8.2.2.1 Design Requirements

For this design example, the TPD1E05U06 and the TPD5S116 are used to protect the data pairs and control lines of the HDMI 2.0 connection. This provides full HDMI 2.0 port protection.

Given the HDMI 2.0 application, the following parameters in [Table 2](#) are known.

Table 2. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on data lines	0 V to 5 V
Operating frequency	3 GHz

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Signal Range

The TPD1E05U06 has 1 protection channel for signal lines, supporting a signal range of 0 V to 5.5 V.

8.2.2.2.2 Operating Frequency

The TPD1E05U06 has 0.42 pF of capacitance, which supports HDMI 2.0 data rates.

8.2.2.3 Application Curves

Refer to the [Application Curves](#) section.

9 Power Supply Recommendations

This device is a passive ESD protection device and there is no need to power it. Care must be taken to make sure that the maximum voltage specifications for each line are not violated.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
 - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
 - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
 - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

10.2.1 TPD4E05U06 Layout Example

This application is typical of an HDMI 1.4 layout.

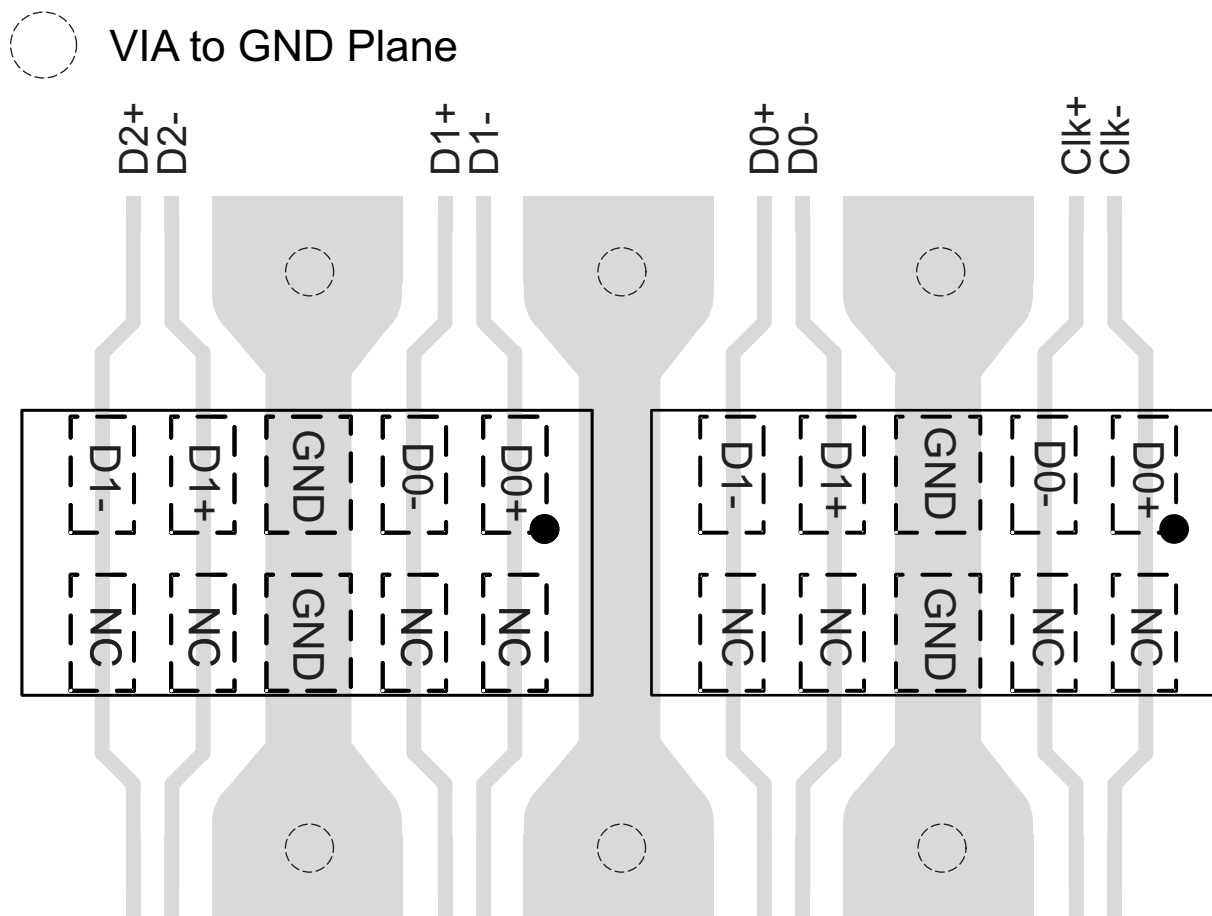


Figure 24. TPD4E05U06 Layout

Layout Example (continued)

10.2.2 TPD1E05U06 Layout Example

This application is typical of an HDMI 2.0 layout.

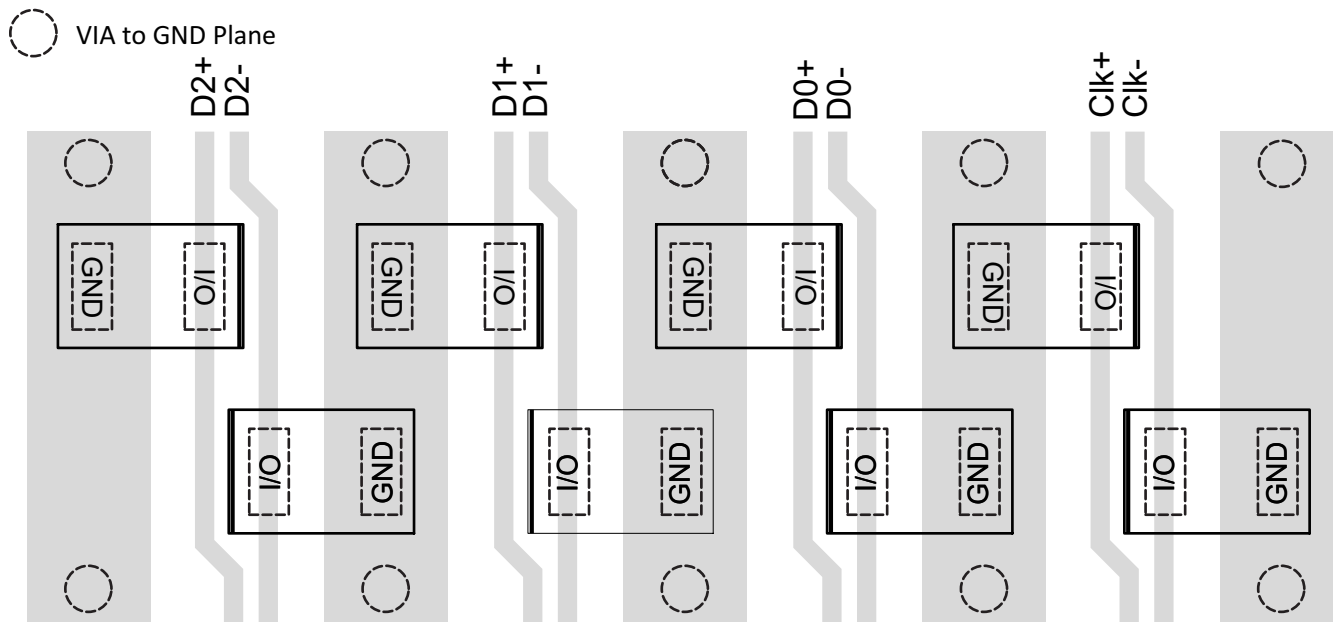


Figure 25. TPD1E05U06 Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- [Reading and Understanding an ESD Protection Datasheet](#)
- [ESD Layout Guide](#)
- [TPD6E05U06RVZ EVM User's Guide](#)
- [Picking ESD Diodes for Ultra High-Speed Data Lines](#)
- [ESD PROTECTION DIODES EVM](#)
- [TPD1E05U06DPY EVM User's Guide](#)
- [TPD4E05U06DQA EVM User's Guide](#)

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPD1E05U06	Click here	Click here	Click here	Click here	Click here
TPD4E05U06	Click here	Click here	Click here	Click here	Click here
TPD6E05U06	Click here	Click here	Click here	Click here	Click here

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on [ti.com](#). In the upper right-hand corner, click the *Alert me* button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
PCI-Express is a registered trademark of PCI-SIG .
V-by-One is a registered trademark of Thine Electronics, Inc.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD1E05U06DPYR	ACTIVE	X1SON	DPY	2	10000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(BK, C1, C6) C2	Samples
TPD1E05U06DPYT	ACTIVE	X1SON	DPY	2	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(BK, C1, C6) C2	Samples
TPD4E05U06DQAR	ACTIVE	USON	DQA	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(BLG, BRG) BRY	Samples
TPD6E05U06RVZR	ACTIVE	USON	RVZ	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(BV, BVY)	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

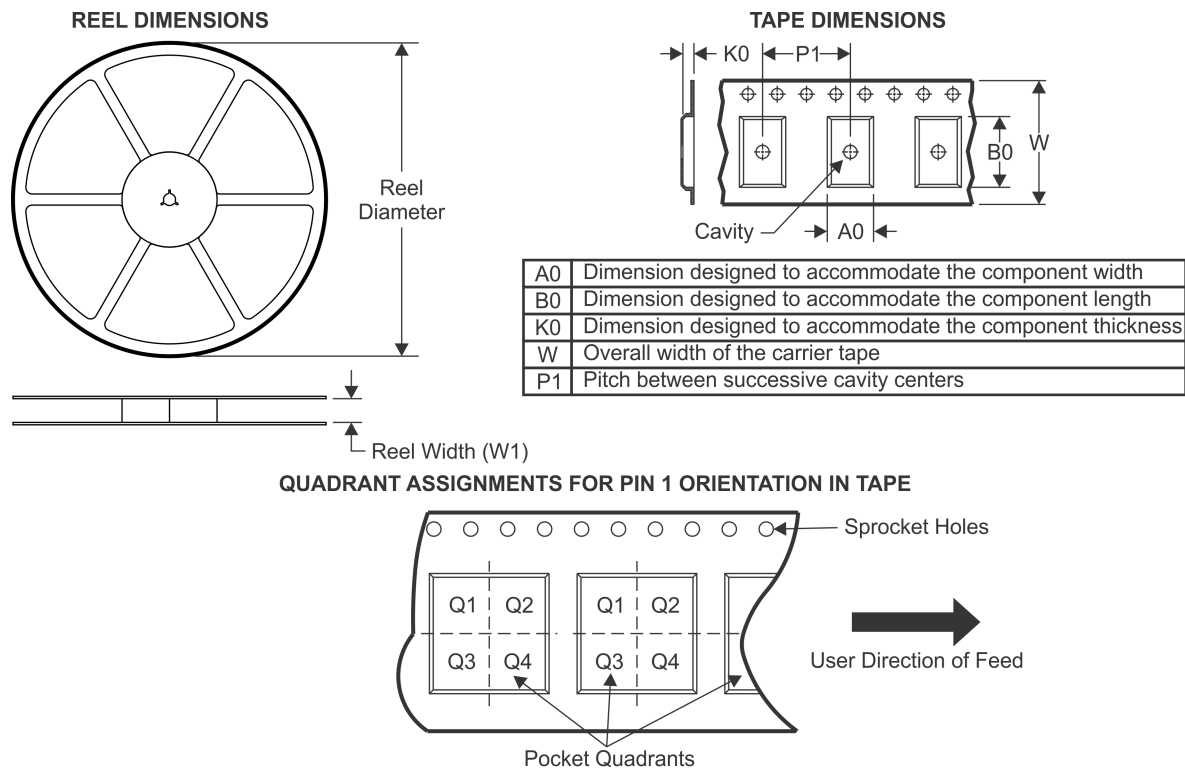
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPD1E05U06, TPD4E05U06 :

- Automotive: [TPD1E05U06-Q1](#), [TPD4E05U06-Q1](#)

NOTE: Qualified Version Definitions:

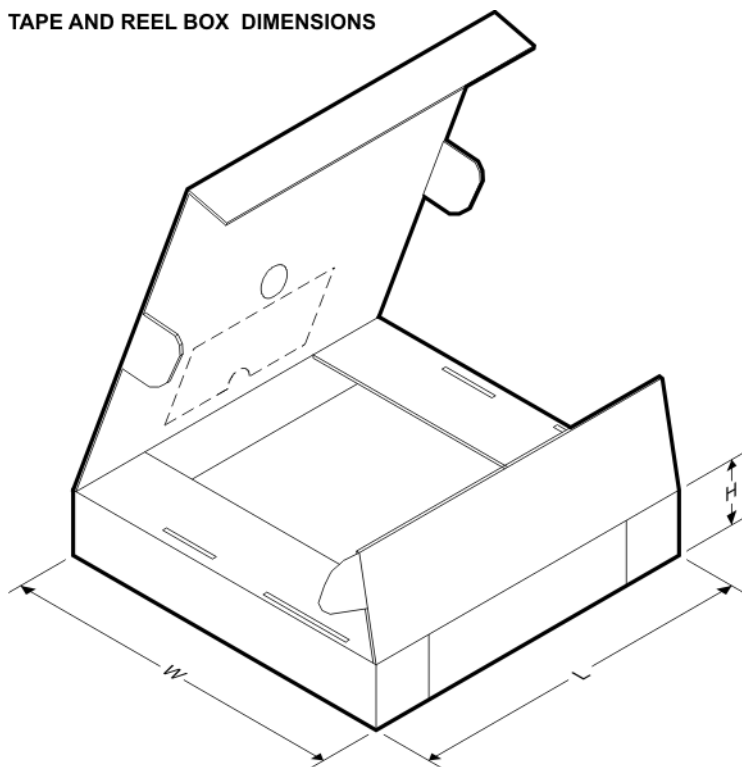
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD1E05U06DPYR	X1SON	DPY	2	10000	180.0	9.5	0.66	1.15	0.66	2.0	8.0	Q1
TPD1E05U06DPYR	X1SON	DPY	2	10000	180.0	8.4	0.07	1.1	0.47	2.0	8.0	Q1
TPD1E05U06DPYT	X1SON	DPY	2	250	180.0	8.4	0.07	1.1	0.47	2.0	8.0	Q1
TPD1E05U06DPYT	X1SON	DPY	2	250	180.0	9.5	0.66	1.15	0.66	2.0	8.0	Q1
TPD4E05U06DQAR	USON	DQA	10	3000	180.0	9.5	1.23	2.7	0.7	4.0	8.0	Q1
TPD4E05U06DQAR	USON	DQA	10	3000	180.0	9.5	1.18	2.68	0.72	4.0	8.0	Q1
TPD4E05U06DQAR	USON	DQA	10	3000	180.0	8.4	1.23	2.7	0.6	4.0	8.0	Q1
TPD6E05U06RVZR	USON	RVZ	14	3000	180.0	13.2	1.65	3.8	0.7	4.0	12.0	Q1
TPD6E05U06RVZR	USON	RVZ	14	3000	178.0	13.5	1.6	3.75	0.7	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

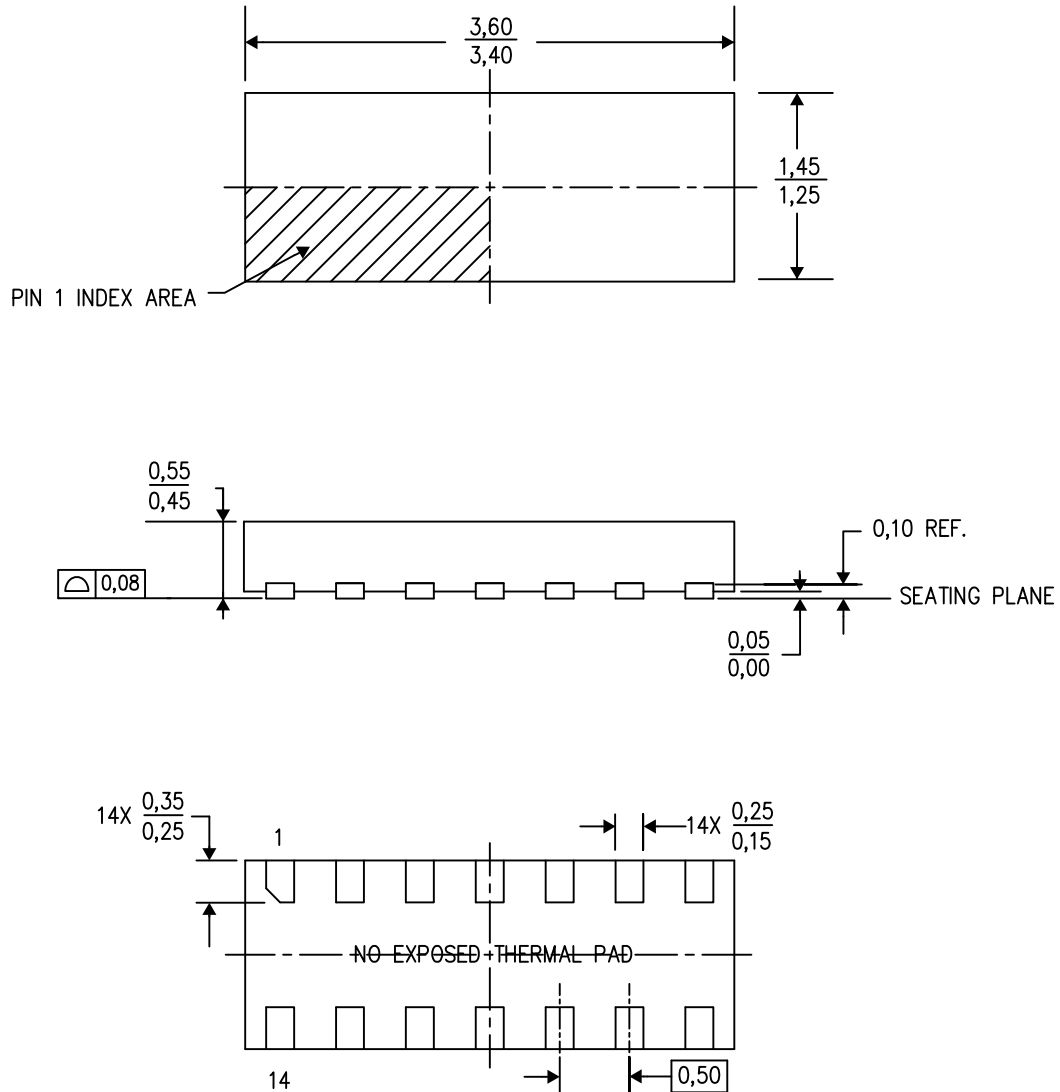


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD1E05U06DPYR	X1SON	DPY	2	10000	184.0	184.0	19.0
TPD1E05U06DPYR	X1SON	DPY	2	10000	203.2	196.8	33.3
TPD1E05U06DPYT	X1SON	DPY	2	250	203.2	196.8	33.3
TPD1E05U06DPYT	X1SON	DPY	2	250	184.0	184.0	19.0
TPD4E05U06DQAR	USON	DQA	10	3000	184.0	184.0	19.0
TPD4E05U06DQAR	USON	DQA	10	3000	189.0	185.0	36.0
TPD4E05U06DQAR	USON	DQA	10	3000	203.2	196.8	33.3
TPD6E05U06RVZR	USON	RVZ	14	3000	184.0	184.0	19.0
TPD6E05U06RVZR	USON	RVZ	14	3000	189.0	185.0	36.0

RVZ (R-PUSON-N14)

PLASTIC SMALL OUTLINE NO-LEAD



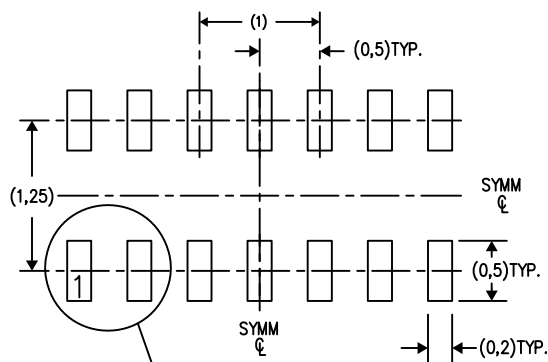
4218112/B 04/14

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.

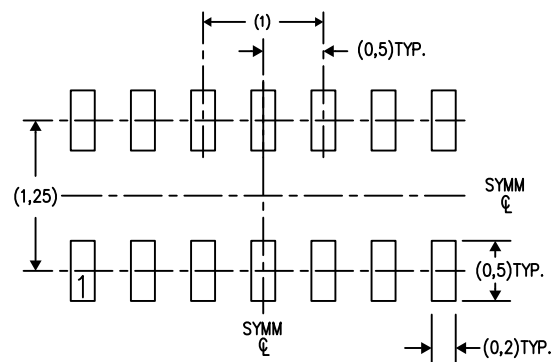
RVZ (R-PUSON-N14)

PLASTIC SMALL OUTLINE NO-LEAD

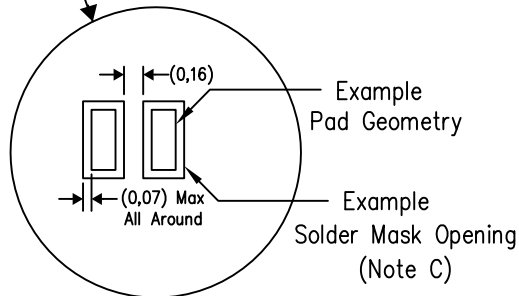
Example Board Layout



Example Stencil Design
Stencil thickness of 0,1 mm recommended.
(Note D)



Example
Non Solder Mask
Defined Pad

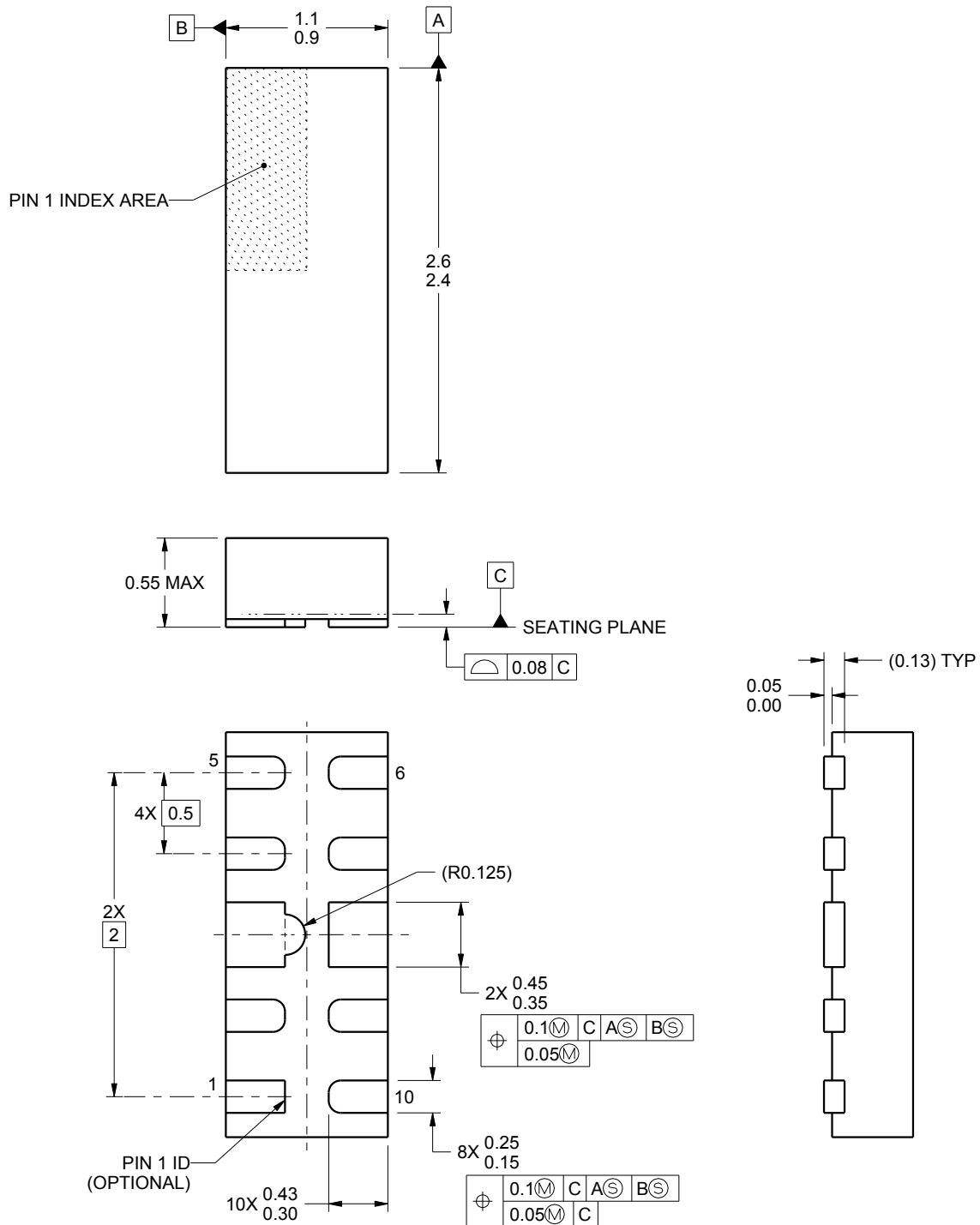
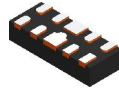


Example
Pad Geometry

Example
Solder Mask Opening
(Note C)

4221500/A 04/14

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.



4220328/A 12/2015

NOTES:

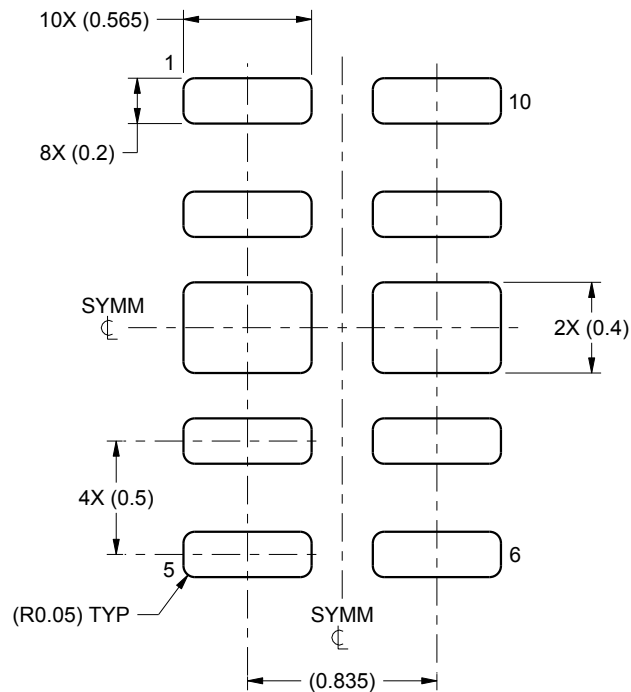
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

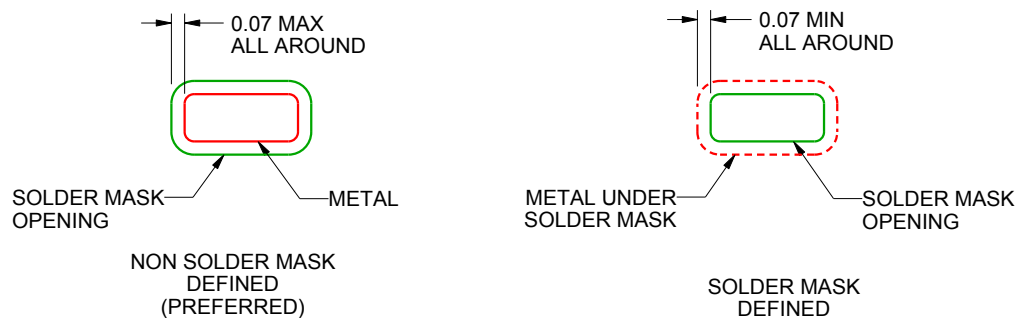
DQA0010A

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS

4220328/A 12/2015

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

DQA0010A

USON - 0.55 mm max height

Technical drawing of a 2x6 array of rectangular features on a plate. The drawing shows a top-down view with dimensions and symmetry indicators. The array is 10 units wide and 8 units high. The features are 10 units wide and 2 units high. The drawing includes dimensions for the overall size, individual feature size, and spacing. Symmetry is indicated by dashed lines and the word 'SYMM'. A note '(R0.05) TYP' points to the rounded corners of the features. A note 'METAL TYP' points to the material of the plate.

Dimensions:

- Overall width: 10X (0.565)
- Overall height: 8X (0.2)
- Feature width: 10
- Feature height: 2X (0.36)
- Spacing between features: 4X (0.5)
- Spacing between rows: 5
- Radius of corner: (R0.05) TYP
- Material: METAL TYP
- Symmetry: SYMM (indicated by dashed lines and the word 'SYMM')
- Feature count: 6
- Feature spacing: (0.835)

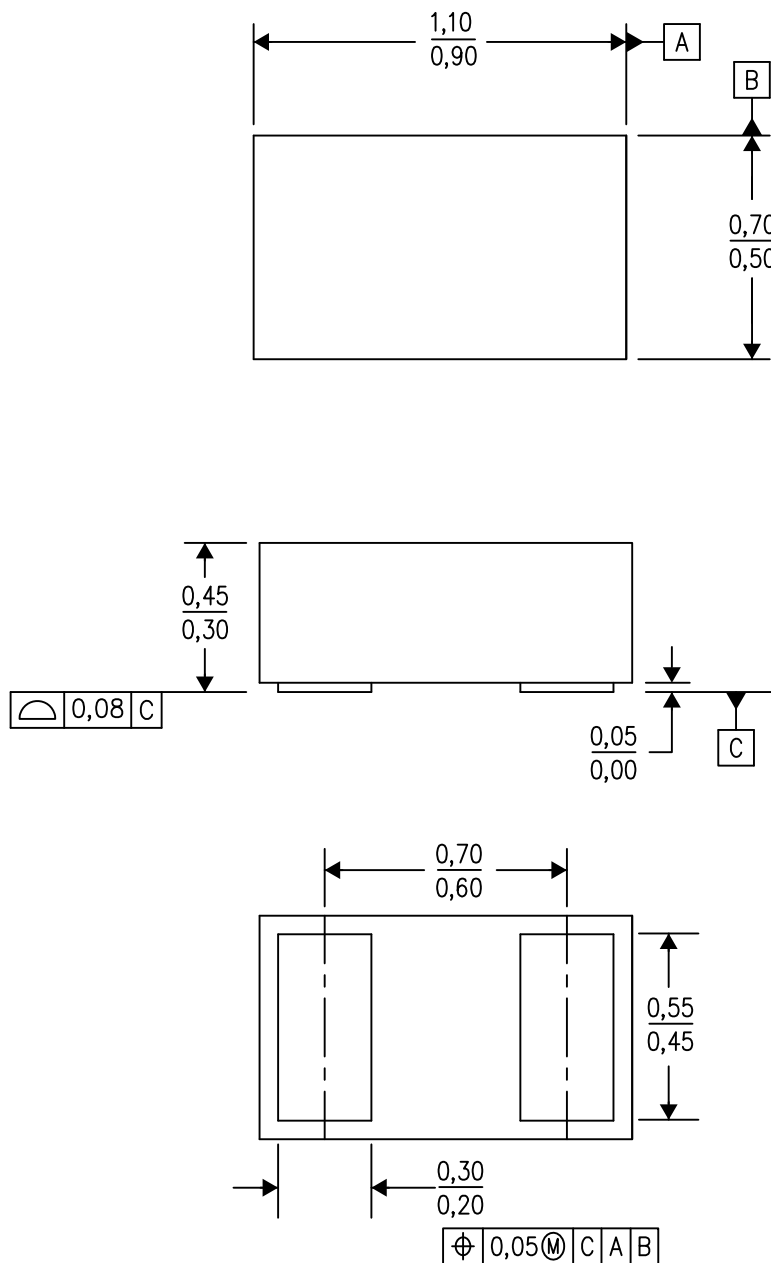
EXPOSED PADS 3 & 8:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DPY (R-PX1SON-N2)

PLASTIC SMALL OUTLINE NO-LEAD



4211012/D 08/14

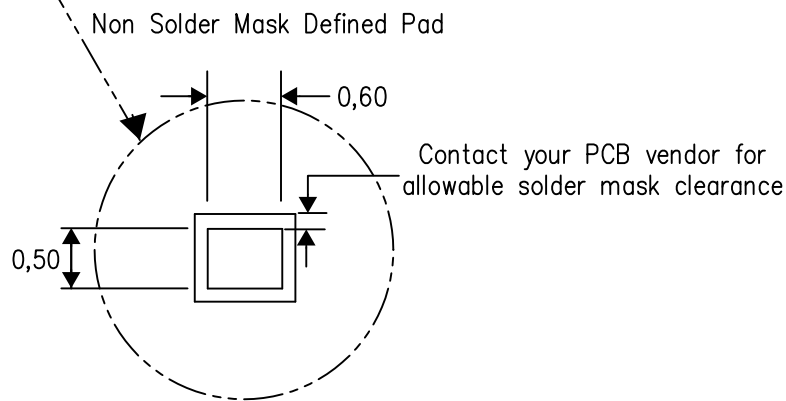
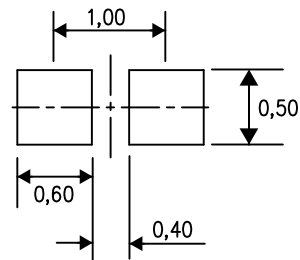
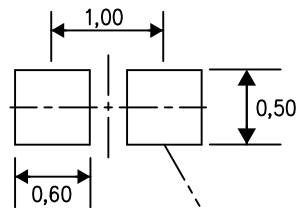
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.

DPY (R-PX1SON-N2)

PLASTIC SMALL OUTLINE NO-LEAD

Example Board Layout

Example Stencil Design
(Note E)



4215270/B 08/15

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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