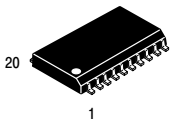
3.3 V ECL 1:5 Clock Distribution Chip

MC100LVEL14



SOIC-20 WB
DW SUFFIX
CASE 751D-05

Description

The MC100LVEL14 is a low skew 1:5 clock distribution chip designed explicitly for low skew clock distribution applications. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. The LVEL14 is functionally and pin compatible with the EL14 but is designed to operate in ECL or PECL mode for a voltage supply range of –3.0 V to –3.8 V (or 3.0 V to 3.8 V).

The LVEL14 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pulldown resistor) the SEL pin will select the differential clock input.

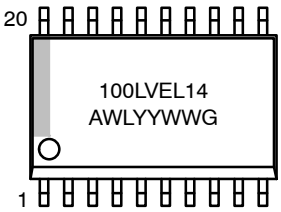
The common enable ($\overline{EN}$) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

Features

- 50 ps Output-to-Output Skew
- Synchronous Enable/Disable
- Multiplexed Clock Input
- ESD Protection: Human Body Model > 2 kV
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range:
  V_{CC} = 3.0 V to 3.8 V with V_{EE} = 0 V
- NECL Mode Operating Range:
  V_{CC} = 0 V with V_{EE} = –3.0 V to –3.8 V
- Internal Input Pulldown Resistors on CLK
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity: Level 3 (Pb-Free)
- Flammability Rating: UL 94 V-0 @ 0.125 in,
  Oxygen Index: 28 to 34
- Transistor Count = 303 Devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
MC100LVEL14DWR2G	SOIC-20 WB (Pb-Free)	1000 Tape & Reel

DISCONTINUED (Note 1)

MC100LVEL14DWG	SOIC-20 WB (Pb-Free)	38 Units / Tube

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

1. **DISCONTINUED:** This device is not available. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

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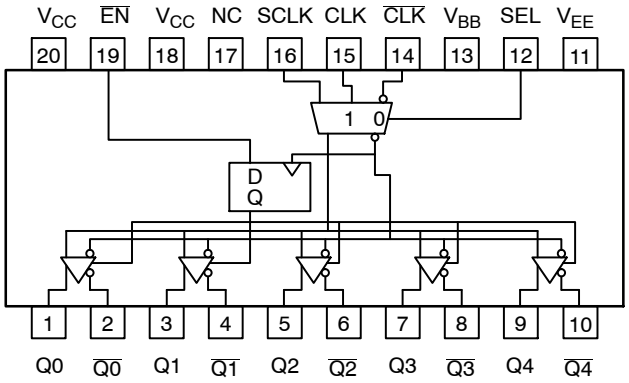

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. Pinout (Top View) **and Logic Diagram**

Table 1. PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{CLK}$	ECL Diff Clock Inputs
SCLK	ECL Scan Clock Input
$\overline{EN}$	ECL Sync Enable
SEL	ECL Clock Select Input
Q_{0-4}, $\overline{Q_{0-4}}$	ECL Diff Clock Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

Table 2. FUNCTION TABLE

CLK	SCLK	SEL	$\overline{EN}$	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

* On next negative transition of CLK or SCLK
X = Don't Care

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		−8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 to 0 −6 to 0	V
I_{out}	Output Current	Continuous Surge		50 100	mA
I_{BB}	V_{BB} Sink/Source			±0.5	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-20 WB SOIC-20 WB	90 60	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-20 WB	30 to 35	°C/W
T_{sol}	Wave Solder	< 2 to 3 sec @ 260 °C		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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Table 4. LVPECL DC CHARACTERISTICS (V_{CC} = 3.3 V; V_{EE} = 0 V (Note 2))

Symbol	Characteristic	−40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		32	40		32	40		34	42	mA
V_{OH}	Output HIGH Voltage (Note 3)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 3)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 7) V_{PP} < 500 mV V_{PP} ≥ 500 mV	 1.3 1.5		 2.9 2.9	 1.2 1.4		 2.9 2.9	 1.2 1.4		 2.9 2.9	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Others $\overline{CLK}$	 0.5 −300			 0.5 −300			 0.5 −300			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

2. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
3. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2.0 V.
4. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1.0 V.

Table 5. LVNECL DC CHARACTERISTICS (V_{CC} = 0.0 V; V_{EE} = −3.3 V (Note 5))

Symbol	Characteristic	−40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		32	40		32	40		34	42	mA
V_{OH}	Output HIGH Voltage (Note 6)	−1085	−1005	−880	−1025	−955	−880	−1025	−955	−880	mV
V_{OL}	Output LOW Voltage (Note 6)	−1830	−1695	−1555	−1810	−1705	−1620	−1810	−1705	−1620	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	−1165		−880	−1165		−880	−1165		−880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	−1810		−1475	−1810		−1475	−1810		−1475	mV
V_{BB}	Output Voltage Reference	−1.38		−1.26	−1.38		−1.26	−1.38		−1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 7) V_{PP} < 500 mV V_{PP} ≥ 500 mV	 −2.0 −1.8		 −0.4 −0.4	 −2.1 −1.9		 −0.4 −0.4	 −2.1 −1.9		 −0.4 −0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Others $\overline{CLK}$	 0.5 −300			 0.5 −300			 0.5 −300			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

5. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
6. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2.0 V.
7. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1.0 V.

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Table 5. AC CHARACTERISTICS (V_{CC} = 3.3 V; V_{EE} = 0.0 V or V_{CC} = 0.0 V; V_{EE} = −3.3 V (Note 8)

Symbol	Characteristic	−40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency (Figure 2)		> 1			> 1			> 1		GHz
t_{PLH} t_{PHL}	Prop CLK to Q (Diff) Delay CLK to Q (SE) SCLK to Q	520 470 470		720 770 770	580 530 530	680 680 680	780 830 830	630 580 580		830 880 880	ps
t_{SKEW}	Part-to-Part Skew Within-Device Skew (Note 9)			200 50			200 50			200 50	ps
t_{JITTER}	Random Clock Jitter (RMS) @ 1 GHz (Figure 2)		0.2	< 1		0.2	< 1		0.2	< 1	ps
t_S	Setup Time $\overline{EN}$	0	−95		0	−110		0	−125		ps
t_H	Hold Time $\overline{EN}$	250	150		250	160		250	175		ps
V_{PP}	Input Swing CLK (Note 10)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20%−80%)	230		500	230		500	230		500	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

8. V_{EE} can vary ±0.3 V.
9. Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.
10. V_{PP}(min) is minimum input swing for which AC parameters guaranteed.

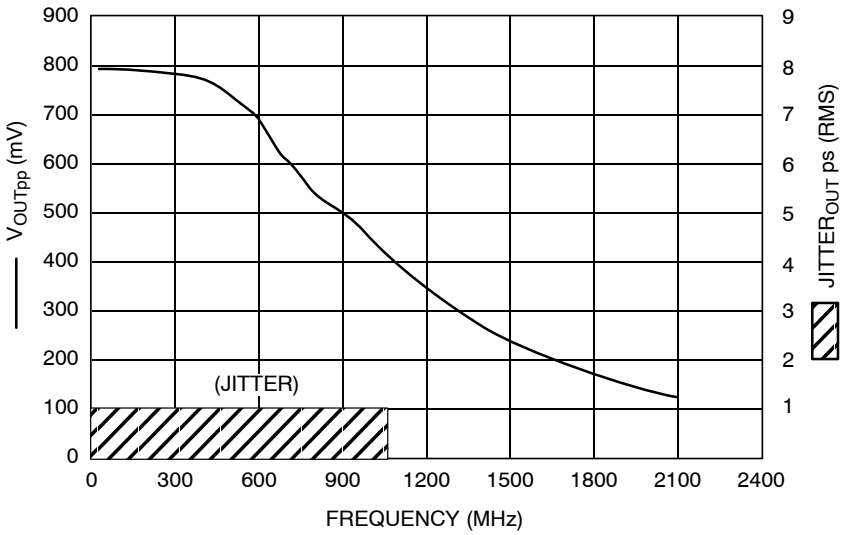

Figure 2. F_{max}/Jitter

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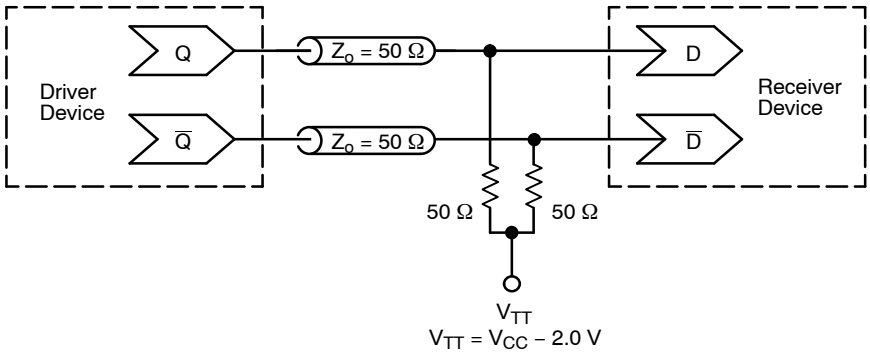

Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices)

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Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

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REVISION HISTORY

Revision	Description of Changes	Date
12	MC100LVEL14DWG OPN Marked as Discontinued.	1/16/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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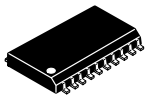

SOIC−20 WB
CASE 751D−05
ISSUE H

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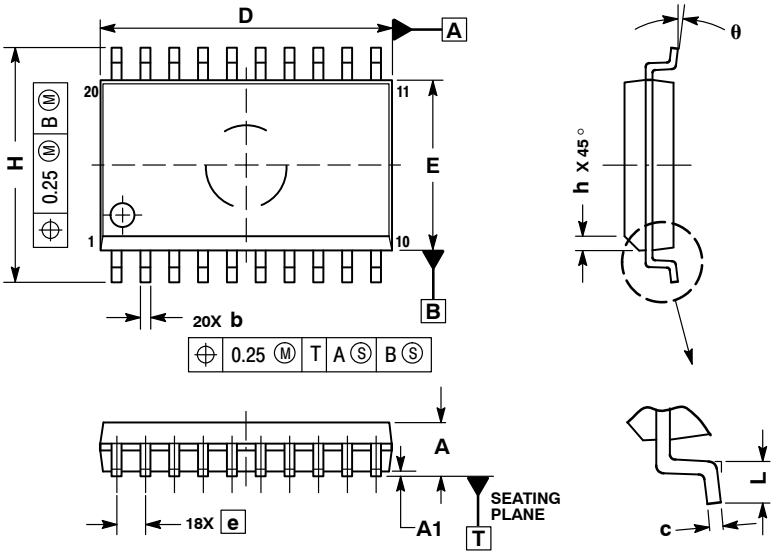
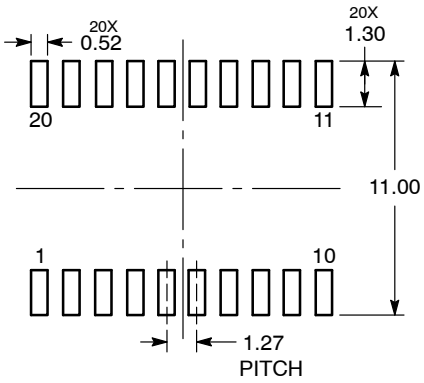
SCALE 1:1



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

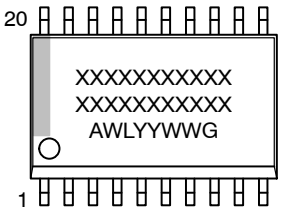
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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