R-IN32M3 Series

LSI for Industrial Ethernet

R18DS0008EJ0501

Jan. 12, 2021

1. Overview

1.1 Introduction

Ethernet communication continues to spread rapidly in the field of industrial automation as manufacturers seek to improve the capability, efficiency, and flexibility of their organizations. Modern Industrial Ethernet applications require high-speed real-time response, low power consumption, and high performance. These requirements are not necessarily met by traditional methods such as hard-wired Ethernet processors or dedicated high-speed CPUs.

Renesas R-IN32M3 series of large-scale integrated circuits (LSI) are specifically tailored to meet the demands of Industrial Ethernet applications. Key features include:

- High-speed, real-time, deterministic, low-latency, low-jitter response for real-time applications
- Low power consumption
- Integrated Arm® Cortex®-M3 core for flexibility
- Integrated Real-Time OS Accelerator with support for µITRON version 4.0
- Integrated Gigabit Ethernet MAC (R-IN32M3-CL only)
- Integrated 10/100Mbps EtherPHY (R-IN32M3-EC only)
- Dedicated, DMA controller and buffer for the network processor
- High performance with low CPU usage by offloading functions to Real-Time OS Accelerator
- Multiple timers, serial interfaces, general purpose I/O (GPIO), external memory interfaces

1.2 Product Lineup

Renesas R-IN32M3 series includes the following two devices:

Table1.1 R-IN32M3 Product Lineup

Product name	Feature
R-IN32M3-EC	R-IN32M3 with built-in EtherCAT® Slave Controller
R-IN32M3-CL	R-IN32M3 with built-in CC-Link IE Field (intelligent device station)

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1.3 Overview

Table 1.2 Overview of R-IN32M3 (1/2)

Item \ Product	R-IN32M3
CPU cores	Arm Cortex-M3 32-bit RISC CPU + Real-Time OS Accelerator (Hardware Real-Time OS, HW-RTOS)
Operating frequency	100 MHz
Instruction set	Thumb®-2 instruction Armv7-M architecture
Instruction RAM	768 Kbytes (RAM with ECC)
Data RAM	512 Kbytes (RAM with ECC)
Buffer RAM	64 Kbytes (RAM with ECC)
Internal system bus	- 32-bit system bus at 100 MHz - 128-bit communication bus at 100 MHz
DMA	- 4 channels + 1 channel (for real-time port) - Supports software and various interrupt-triggered DMA
Boot options	- Serial flash ROM boot - External memory boot - External MPU boot
External memory support	- 16-bit or 32-bit bus interface - Page ROM / ROM / SRAM interface - Synchronous burst memory interface - Four chip selects for external SRAM - 256-Mbyte (max) external memory space - Programmable wait function
External MCU Interface	- 16-bit or 32-bit bus interface - General-purpose interface for static memory - Address space:2 Mbytes (instruction RAM, data RAM, register area)
Serial flash ROM memory controller	- Support serial interface compatible with SPI of the companies - Support direct boot from serial memory device - Support Fast Read, Fast Read Dual Output, Fast Read Dual I/O mode - Direct layout in memory space
Interrupt	- 29 external interrupt pins
Internal peripheral circuit	
I/O Ports	CMOS I/O: 96 pins (max.)
System timers (three systems)	- Internal timer of Hardware RTOS
	- Internal timer of CPU
	- 4-channel timer array - 32-bit counter & 32-bit data register - Counter by external signal
Watchdog timer	- 1 channel - Software-triggered start mode - Selectable operations in response to errors: - Generation of a non-maskable interrupt (NMI) - Generation of a reset

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Table 1.2 Overview of R-IN32M3 (2/2)

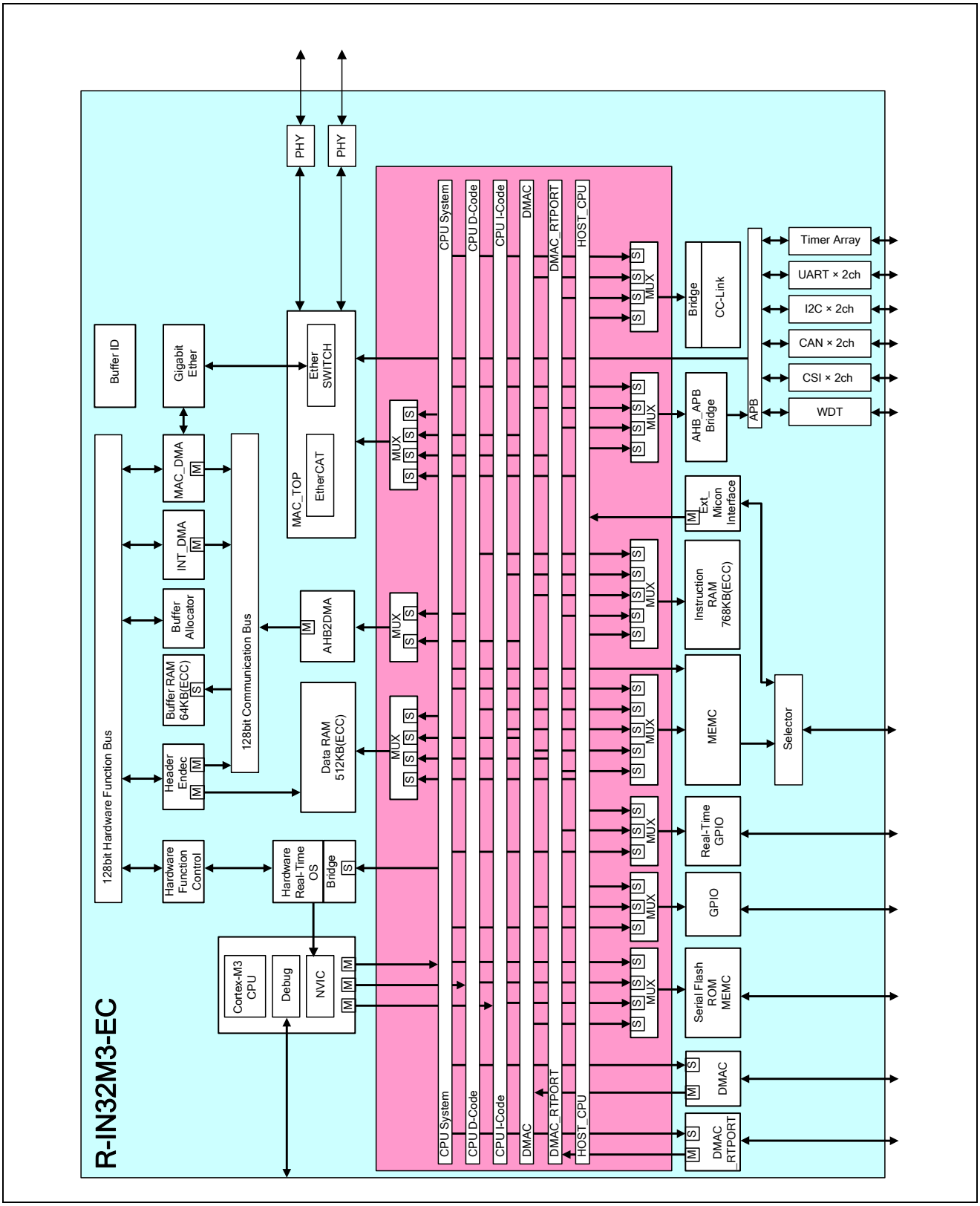
Item \ Product	R-IN32M3
Internal Peripherals (cont.)	
Asynchronous serial interface	- 2 channels - Full duplex - FIFOs: 10 bits x 16 receive and 8 bits x 16 transmit - Support output of receive errors and status - Character length: 7 or 8 bits - Parity bit options: Odd, even, 0, none - Transmit stop bits: 1 or 2 bits
I2C serial interface	- 2 channels - Operating modes: Normal or high-speed - Transfer modes: Single-transfer mode or continuous-transfer mode - Transmission data length: 8 bits
CAN controller	- 2 channels - Conforming to ISO11898 - Support to transfer and receive normal frame and expand frame - Transmission speed: 1 Mbps (max)
Clock synchronous serial interface	- 2 channels - Synchronized serial data transmission by three-wire system - Selectable master mode or slave mode - Built-in baud-rate generator - Transmission data length: 7 bits to 16 bits
CC-Link	- Intelligent device station Notes3 - Remote device station
10/100/1000Mbps Ether MAC Notes1	- 1 channel - Built-in 2-port switch - GMII / MII interface
10/100Mbps EtherPHY Notes2, 4	- 2 ports - Support for 10BaseT and 100BaseTX/FX
CC-Link IE Notes1	CC-Link IE field (Intelligent device station)
EtherCAT Notes2	EtherCAT slave controller
On-chip debug function	- Select serial wire or JTAG - Support full trace (Built-in ETM)
Internal PLL	Generates various clocks from 25-MHz input clock
Power supply voltage	I/O: VDD33 = 3.3±0.3 V Internal circuit: VDD10 = 1.0±0.1 V Power supply for internal PHY Note 2: VDD15 = 1.5±0.15 V (internal regulator available)

Notes 1. Only applied to R-IN32M3-CL.
2. Only applied to R-IN32M3-EC.
3. Please contact our sales representative for details.
4. EtherCAT P is not supported. <R>

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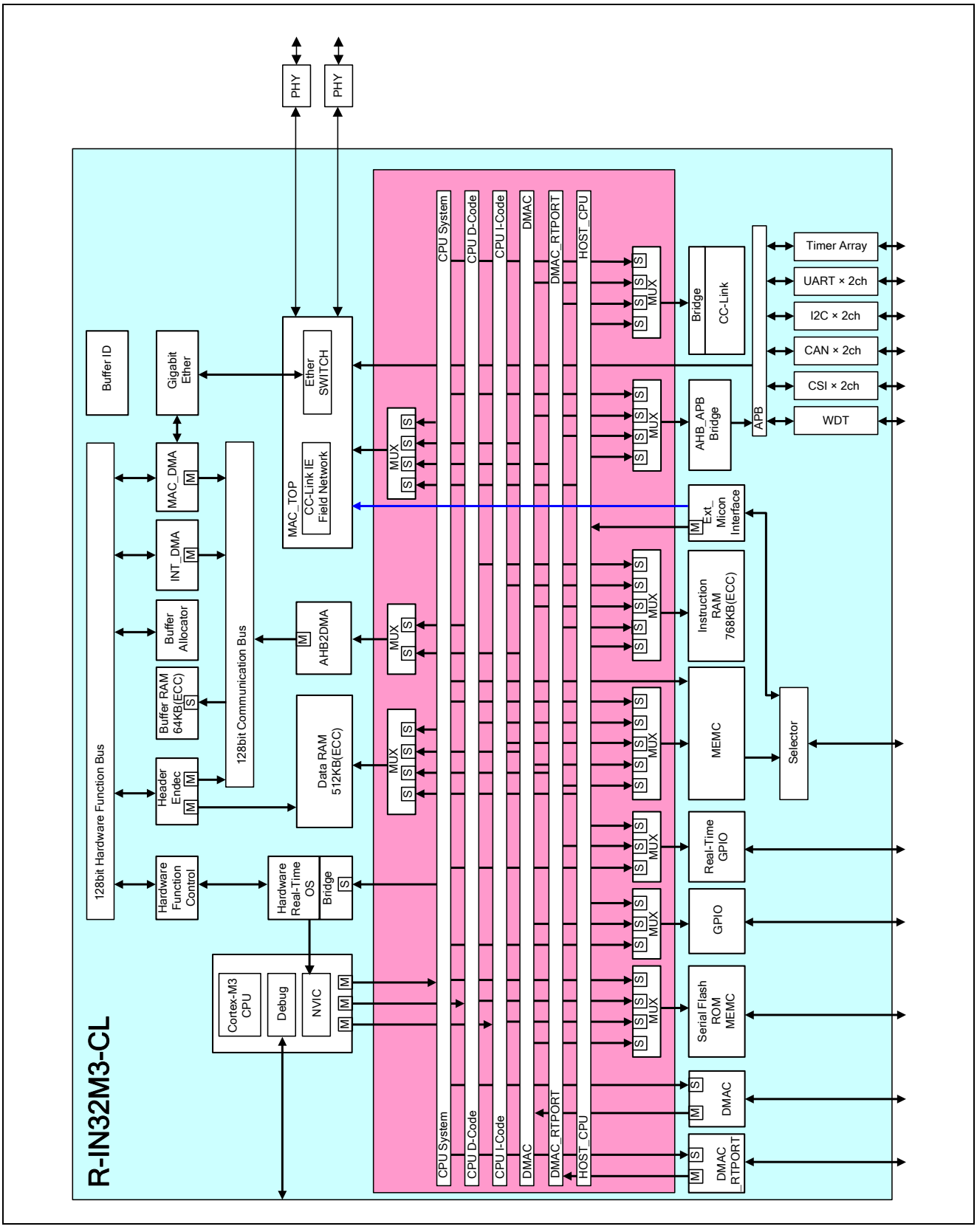
1.4 Internal Block Diagram

1.4.1 R-IN32M3-EC Block Diagram



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1.4.2 R-IN32M3-CL Block Diagram



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1.5 Memory Maps

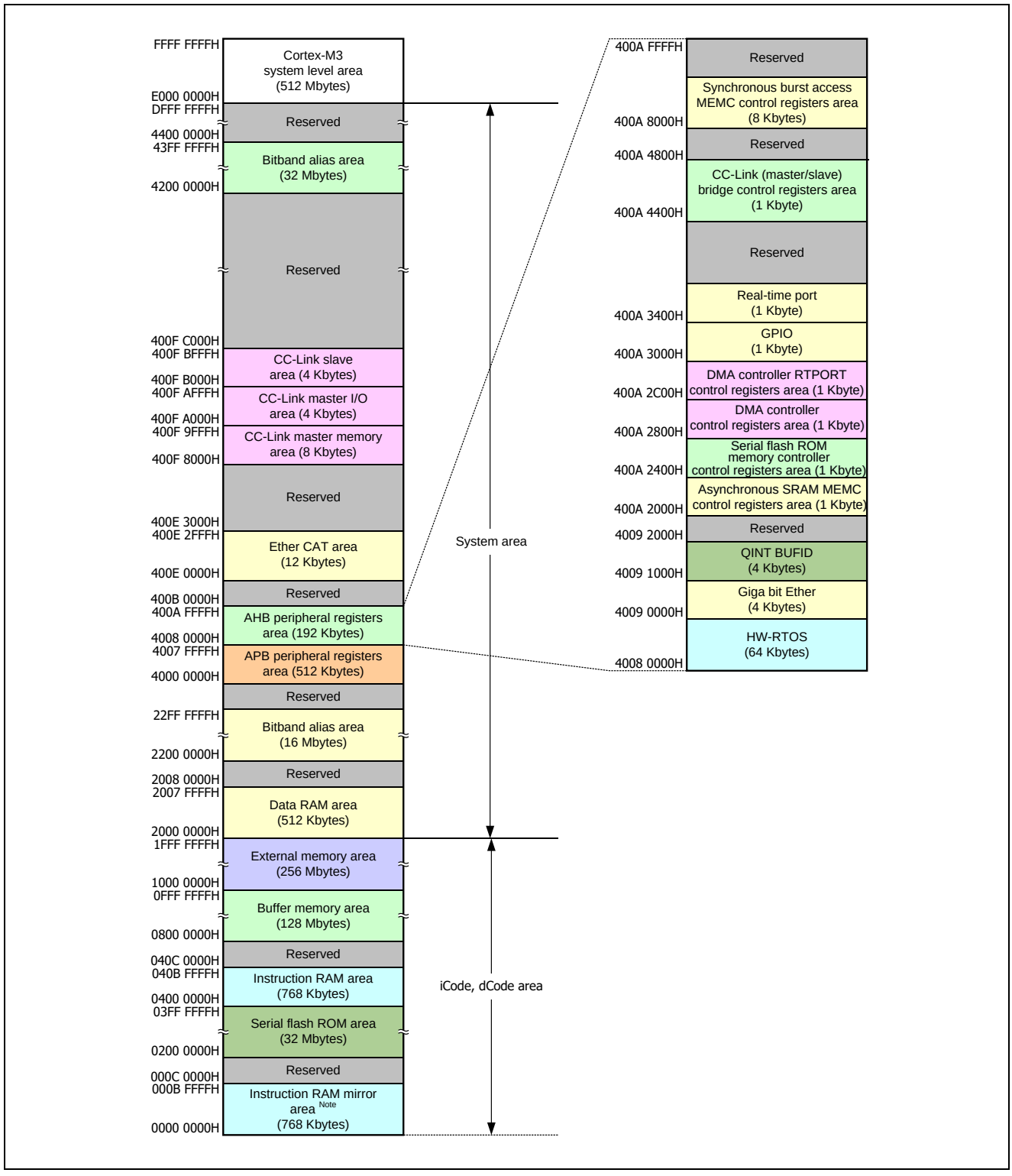


Figure 1.1 Memory Map (ALL) (R-IN32M3-EC)

Note: The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode. For details, see section 5.3, Memory MAP in Each Boot Mode, in the R-IN32M3 Series User's Manual: Peripheral Modules.

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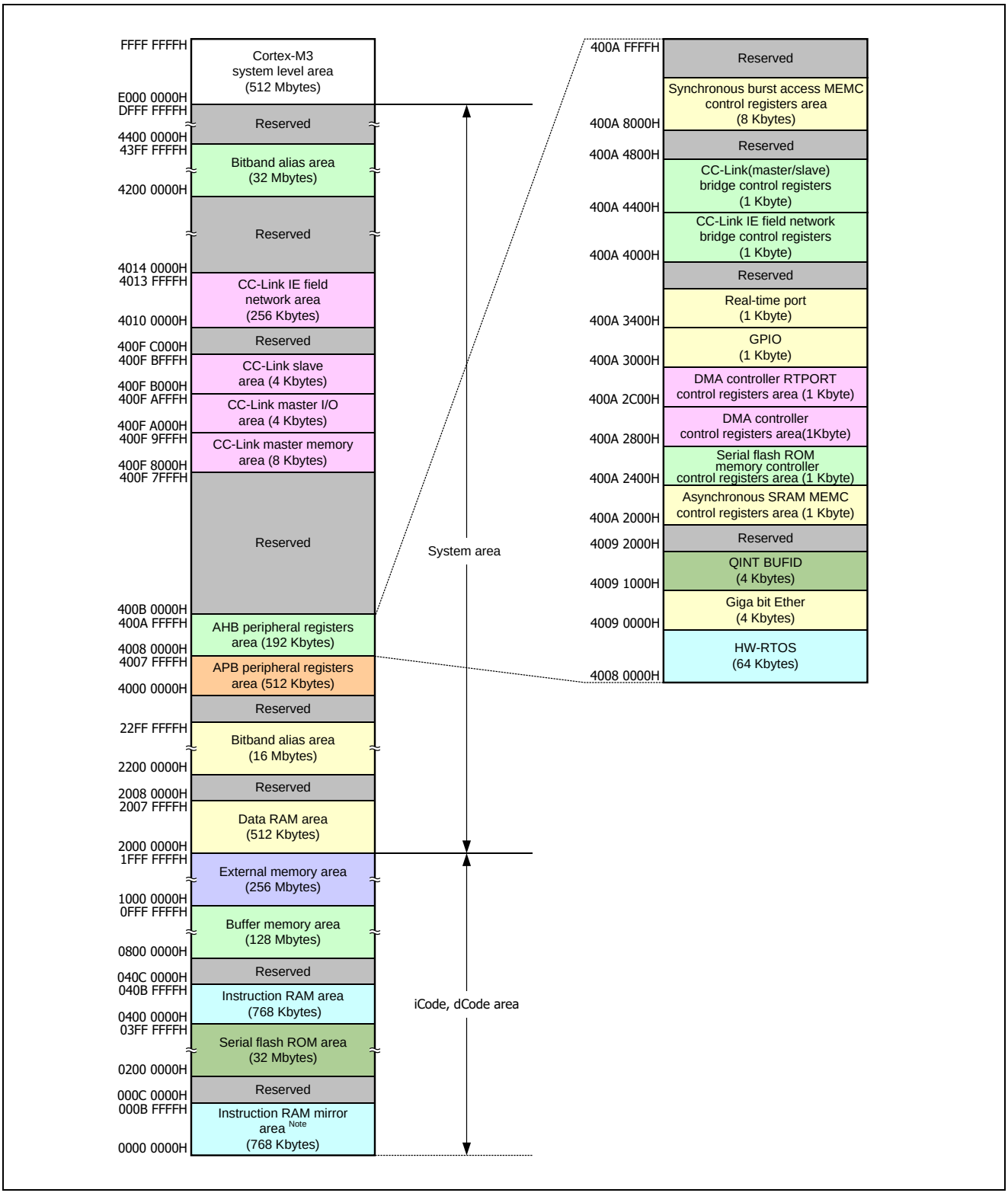


Figure 1.2 Memory Map (ALL) (R-IN32M3-CL)

Note: The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode. For details, see section 5.3, Memory MAP in Each Boot Mode, in the R-IN32M3 Series User's Manual: Peripheral Modules.

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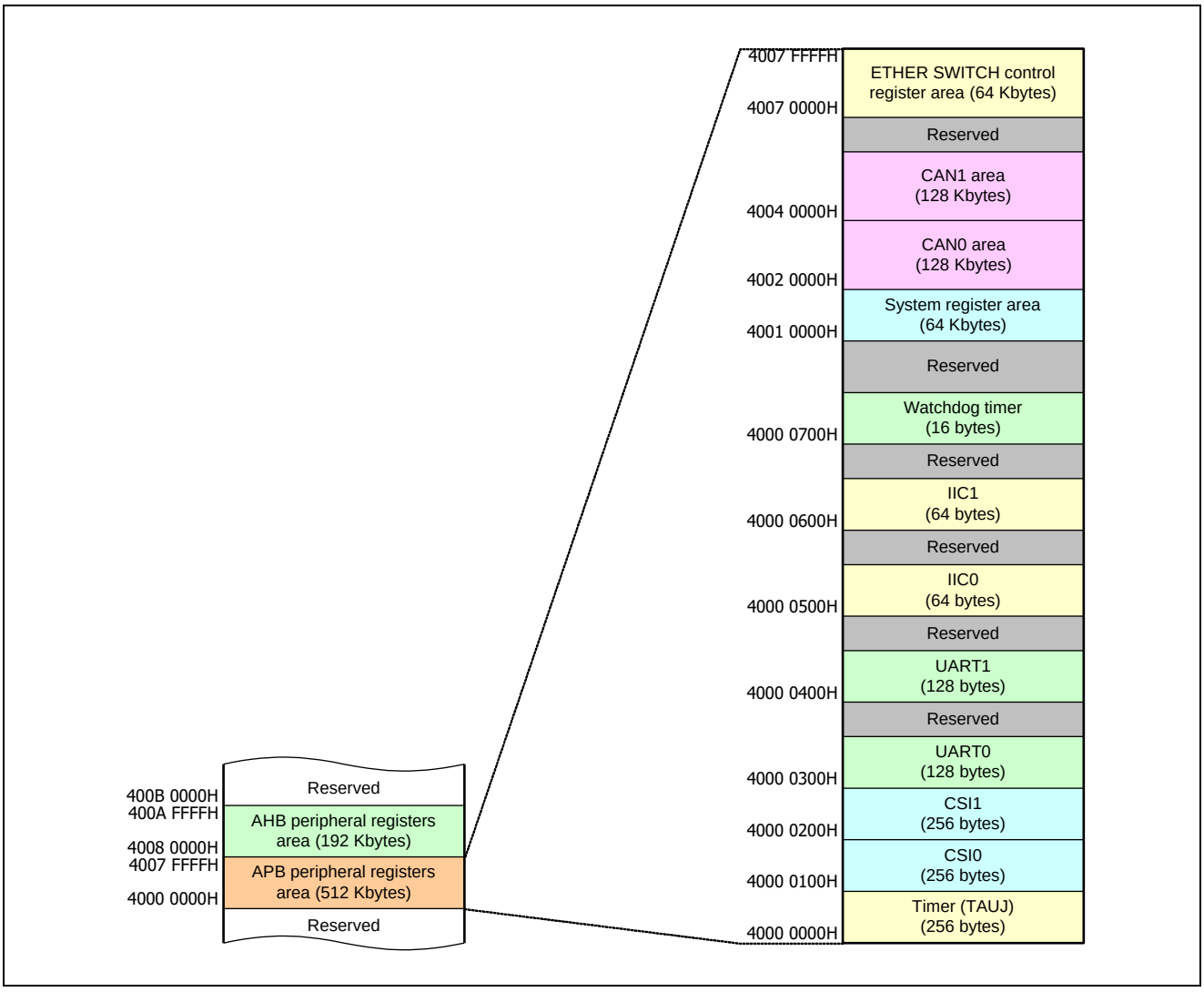


Figure 1.3 Memory Map (APB Peripheral Registers Area; Common to R-IN32M3-EC/CL)

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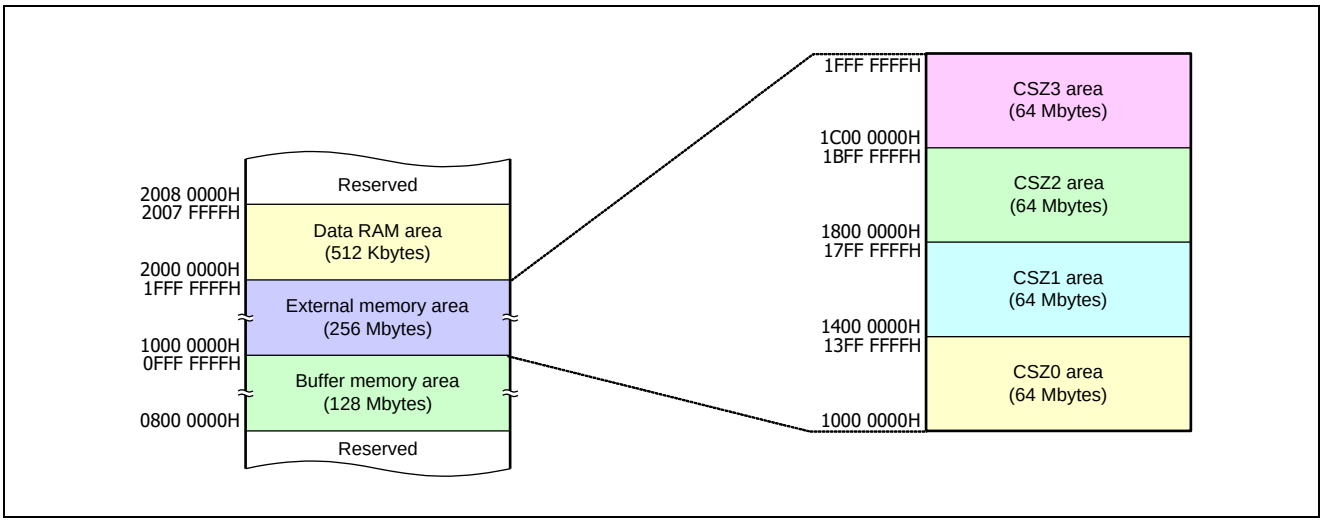


Figure 1.4 Memory Map (External Memory Area; Common to R-IN32M3-EC/CL)

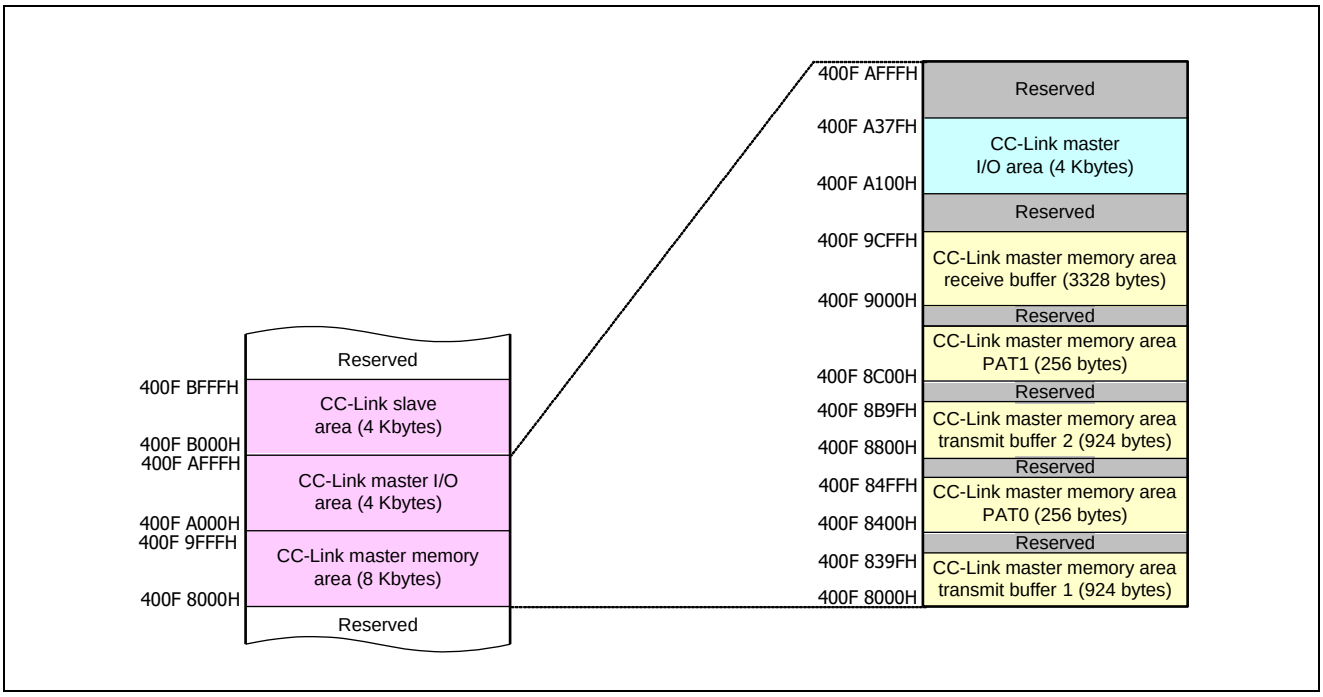


Figure 1.5 Memory Map (CC-Link Master Area; Common to R-IN32M3-EC/CL)

Cautions 1. CC-Link master shows the function block of intelligent device station.

2. CC-Link slave shows the function block of the remote device station.

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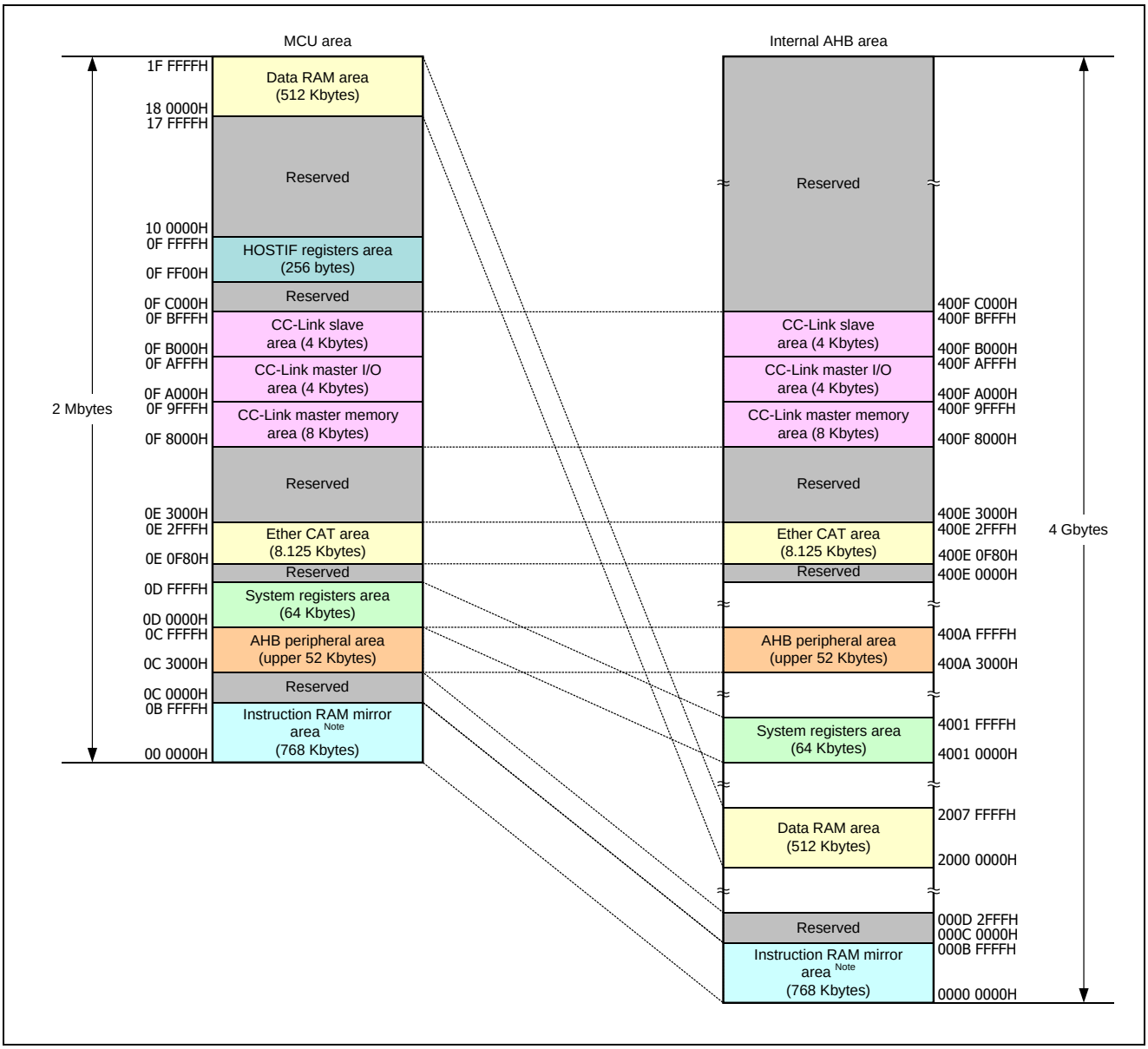


Figure 1.6 External MCU Interface Area (R-IN32M3-EC)

Note: The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode, as shown in the table below. For details, see section 5.3, Memory MAP in Each Boot Mode, and section 4, Bus Architecture, in the R-IN32M3 Series User's Manual: Peripheral Modules.

BOOT1	BOOT0	Boot Mode	Access Destination Area	Remarks
0	0	External memory boot	—	External MCU interface is disabled
0	1	External serial flash ROM boot	Reserved	Access disabled
1	0	External MCU boot	Instruction RAM area	—
1	1	Instruction RAM boot	Instruction RAM area	Enabled only for debugging

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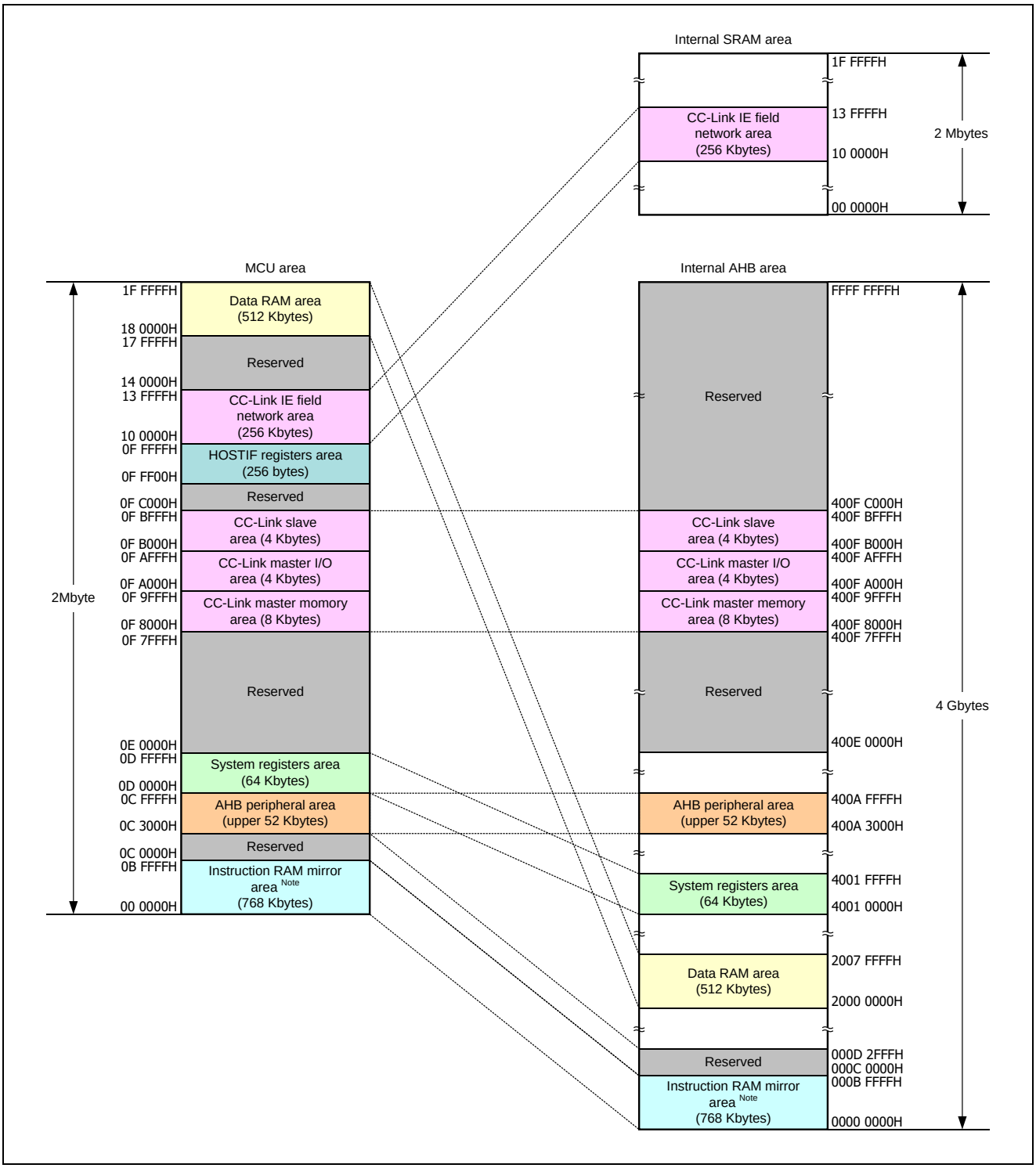


Figure 1.7 External MCU Interface Area (R-IN32M3-CL)

Note: The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode, as shown in the table below. For details, see section 5.3, Memory MAP in Each Boot Mode, and section 4, Bus Architecture, in the R-IN32M3 Series User's Manual: Peripheral Modules.

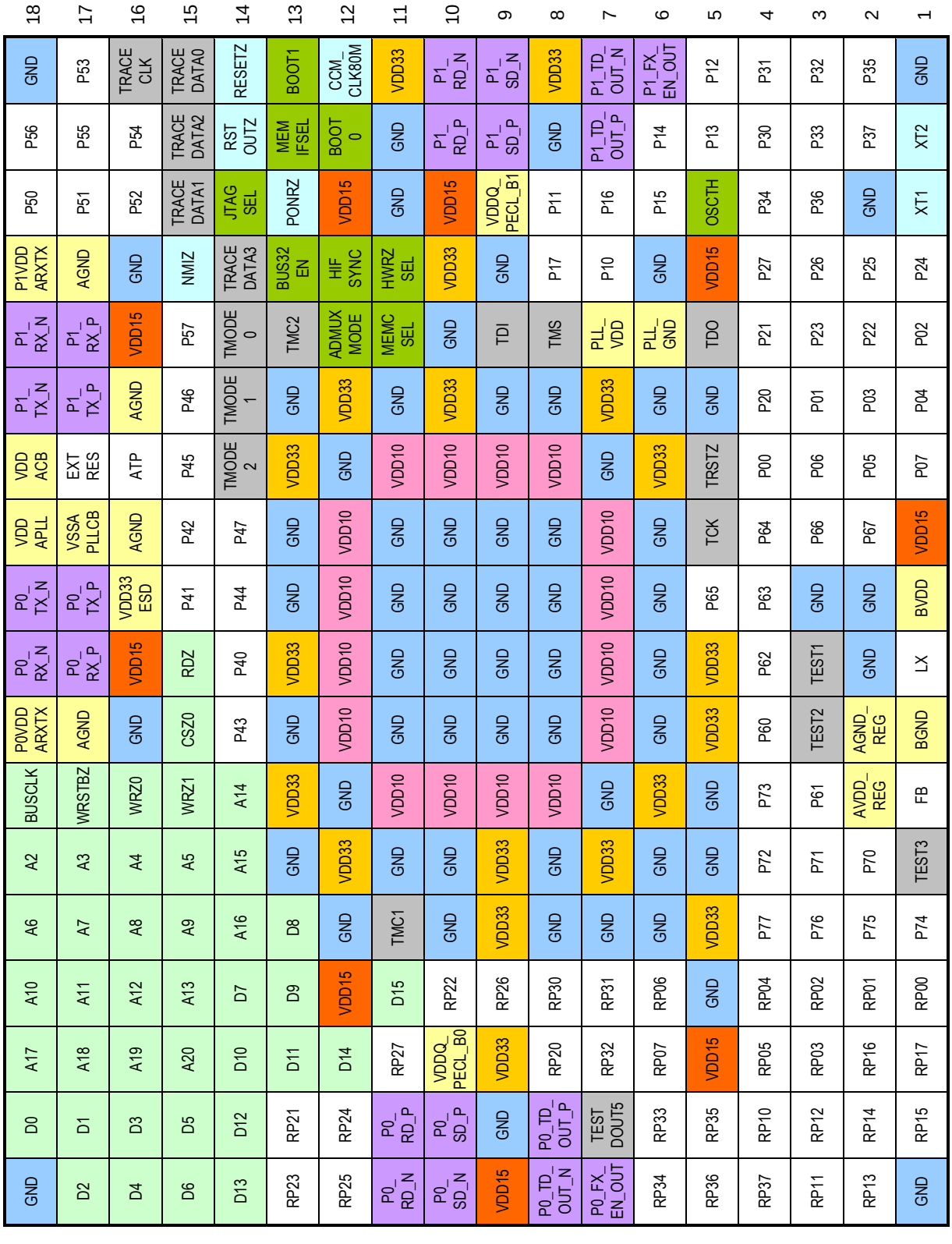
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BOOT1	BOOT0	Boot Mode	Access Destination Area	Remarks
0	0	External memory boot	—	External MCU interface is disabled
0	1	External serial flash ROM boot	Reserved	Access disabled
1	0	External MCU boot	Instruction RAM area	—
1	1	Instruction RAM boot	Instruction RAM area	Enabled only for debugging

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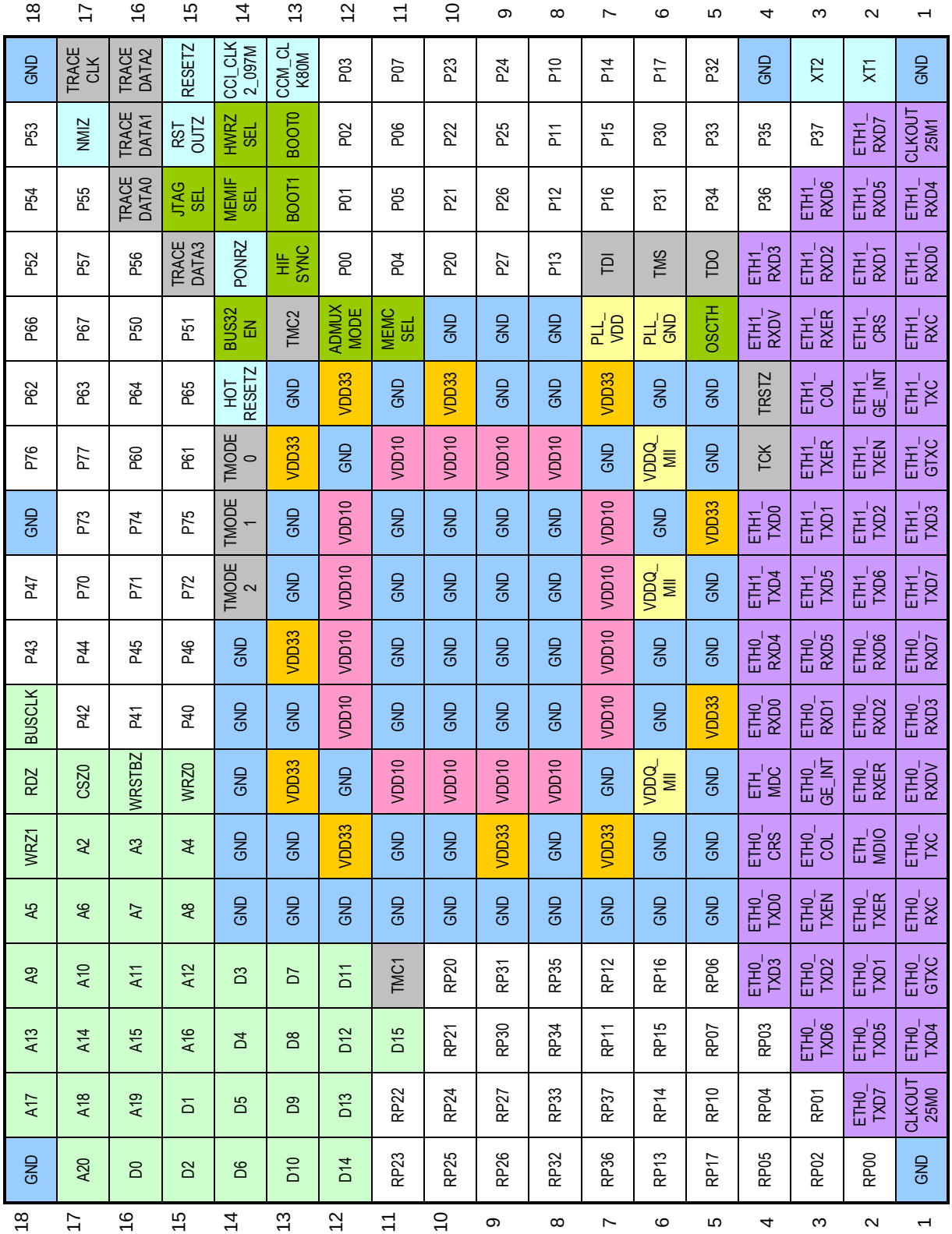
2. Pin Information

2.1 Pin Placement (R-IN32M3-EC Top View)



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2.2 Pin Placement (R-IN32M3-CL Top View)



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2.3 Pin Functions

The meanings of the symbols and abbreviations used in this document are given below.

Table 2.1 Meanings of the Items in the List of Pins

Item	Meaning
Pin name	Name of the pin shown in the following sections. 2.1, Pin Placement (R-IN32M3-EC Top View), 2.2, Pin Placement (R-IN32M3-CL Top View).
I/O	I/O direction of the given pin
Function	Summary of the given pin function
Active	Active level of the given pin
Level during reset	Indicates the pin state while RSTOUTZ = Low. For details on the reset specifications, refer to the R-IN32M3 Series User's Manual (Peripheral Modules).

Table 2.2 Meanings of the Symbols and Abbreviations in the List of Pins

Target	Symbol and Abbreviation	Meaning
Pin name	- (hyphen)	Indicates that the pin is a dedicated pin and is not multiplexed with a port-pin function.
I/O	- (hyphen)	Indicates that the pin is a pin such as a power supply or ground pin and so does not have an I/O direction.
Active	- (hyphen)	Indicates that there is no active level (clock signals, data bus, and address bus).
	High	The active level is high.
	Low	The active level is low.
Level during reset	- (hyphen)	Indicates an input-dedicated pin that has no initial level or state following a reset.
	High	The pin state during a reset is high.
	Low	The pin state during a reset is low.
	Hi-Z (High)	The pin state during a reset is hi-Z (High) with the internal pull-up resistor pulling it to the high level.
	Hi-Z (Low)	The pin state during a reset is hi-Z (Low) with the internal pull-up resistor pulling it to the low level.

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2.3.1 Ethernet Pins

(1) PHY Interface Pins (R-IN32M3-CL only)

Caution: Only applied to R-IN32M3-CL.

Pin Name	I/O	Function	Active	Level during Reset
ETH0_TXC	I	Ethernet 0 10-M/100-M transmit clock (2.5 MHz/25 MHz)	-	-
ETH0_GTXC Note	O	Ethernet 0 1-G transmit clock (125 MHz)	-	High
ETH0_TXEN Note	O	Ethernet 0 transmit enable output	High	Low
ETH0_TXER Note	O	Ethernet 0 transmit error output	High	Low
ETH0_TXD0-ETH0_TXD7 Note	O	Ethernet 0 transmit data output	-	Low
ETH0_GE_INT	I	Ethernet 0 PHY interrupt	High/Low	-
ETH0_RXC	I	Ethernet 0 receive clock	-	-
ETH0_RXDV	I	Ethernet 0 receive enable input	High	-
ETH0_RXER	I	Ethernet 0 receive error input	High	-
ETH0_RXD0-ETH0_RXD7	I	Ethernet 0 receive data input	-	-
ETH0_CRS	I	Ethernet 0 carrier sense input	High	-
ETH0_COL	I	Ethernet 0 collision input	High	-
ETH1_TXC	I	Ethernet 1 10-M/100-M transmit clock (2.5 MHz/25 MHz)	-	-
ETH1_GTXC Note	O	Ethernet 1 1-G transmit clock (125 MHz)	-	High
ETH1_TXEN Note	O	Ethernet 1 transmit enable output	High	Low
ETH1_TXER Note	O	Ethernet 1 transmit error output	High	Low
ETH1_TXD0-ETH1_TXD7 Note	O	Ethernet 1 transmit data output	-	Low
ETH1_GE_INT	I	Ethernet 1 PHY interrupt input	High/Low	-
ETH1_RXC	I	Ethernet 1 receive clock	-	-
ETH1_RXDV	I	Ethernet 1 receive enable input	High	-
ETH1_RXER	I	Ethernet 1 receive error input	High	-
ETH1_RXD0-ETH1_RXD7	I	Ethernet 1 receive data input	-	-
ETH1_CRS	I	Ethernet 1 carrier sense input	High	-
ETH1_COL	I	Ethernet 1 collision input	High	-
ETH_MDC	O	Ethernet management interface clock	-	Low
ETH_MDIO	I/O	Ethernet management interface data input/output	-	Hi-Z

Note: The driving ability can be switched by the setting of the ETHDRCTRL register.
For details, see the R-IN32M3 Series User's Manual (Peripheral Modules).

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(2) Media Interface Pins (R-IN32M3-EC only)

Caution: Only applied to R-IN32M3-EC.

Pin Name	I/O	Function	Active	Level during Reset
P0_RX_P	I	PHY0 receive data input (+)	-	-
P0_RX_N	I	PHY0 receive data input (-)	-	-
P1_RX_P	I	PHY1 receive data input (+)	-	-
P1_RX_N	I	PHY1 receive data input (-)	-	-
P0_TX_P	O	PHY0 transmit data output (+)	-	-
P0_TX_N	O	PHY0 transmit data output (-)	-	-
P1_TX_P	O	PHY1 transmit data output (+)	-	-
P1_TX_N	O	PHY1 transmit data output (-)	-	-
P0_SD_P	I	PHY0 100BASE-FX signal detect input (+)	High	-
P0_SD_N	I	PHY0 100BASE-FX signal detect input (-)	Low	-
P1_SD_P	I	PHY1 100BASE-FX signal detect input (+)	High	-
P1_SD_N	I	PHY1 100BASE-FX signal detect input (-)	Low	-
P0_RD_P	I	PHY0 100BASE-FX receive data input (+)	-	-
P0_RD_N	I	PHY0 100BASE-FX receive data input (-)	-	-
P1_RD_P	I	PHY1 100BASE-FX receive data input (+)	-	-
P1_RD_N	I	PHY1 100BASE-FX receive data input (-)	-	-
P0_TD_OUT_P	O	PHY0 100BASE-FX transmit data output (+)	-	-
P0_TD_OUT_N	O	PHY0 100BASE-FX transmit data output (-)	-	-
P1_TD_OUT_P	O	PHY1 100BASE-FX transmit data output (+)	-	-
P1_TD_OUT_N	O	PHY1 100BASE-FX transmit data output (-)	-	-
P0_FX_EN_OUT	O	PHY0 100BASE-FX FX enable indication output 1: 100BASE-FX mode	High	-
P1_FX_EN_OUT	O	PHY1 100BASE-FX FX enable indication output 1: 100BASE-FX mode	High	-

Remark: In MDI-X mode, the input and output attributes of TXP/TXN and RXP/RXN are reversed.

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(3) Other Pins

Pin Name	I/O	Function	Shared Port	Active	Level during Reset
PHYLINK0, PHYLINK1	I	PHY link input Note1 (for EtherSwitch)	P06-P07	High	Hi-Z (High)
P0LINKLEDZ	O	SIP_PHY0 link status LED output Note2	P06	Low	Hi-Z
P1LINKLEDZ	O	SIP_PHY1 link status LED output Note2	P07	Low	
ETHSWSECOUT	O	EtherSwitch event output par second	P24	High	Note 3
P0DUPLEXLEDZ	O	SIP_PHY0 half-duplex transfer status LED output Note2 0: Full-duplex 1: Half-duplex	P70	-	
P0SPEED100LEDZ	O	SIP_PHY0 100-BASE status LED output Note2	P72	Low	
P0SPEED10LEDZ	O	SIP_PHY0 10-BASE status LED output Note2	P73	Low	
P1DUPLEXLEDZ	O	SIP_PHY1 half-duplex status LED output Note2 0: Full-duplex 1: Half-duplex	P74	-	
P1SPEED100LEDZ	O	SIP_PHY1 100-BASE status LED output Note2	P76	Low	
P1SPEED10LEDZ	O	SIP_PHY1 10-BASE status LED output Note2	P77	Low	
P0ACTLEDZ	O	SIP_PHY0 RX status LED output Note2	RP02	Low	Hi-Z (High)
P1ACTLEDZ	O	SIP_PHY1 TX status LED output Note2	RP04	Low	

Notes 1. Only applies to R-IN32M3-CL.
2. Only applies to R-IN32M3-EC.
3. Hi-Z for R-IN32M3-EC and hi-Z (High) for R-IN32M3-CL.

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2.3.2 EtherCAT Slave Controller Pins (R-IN32M3-EC only)

Caution: Only applies to R-IN32M3-EC.

Pin Name	I/O	Function	Shared Port	Active	Level during Reset
CATLEDRUN	O	EtherCAT RUN LED output	P00	High	Hi-Z
CATIRQ	O	EtherCAT IRQ output	P01	High	
CATLEDSTER	O	EtherCAT dual-color state LED output	P02	High	
CATLEDERR	O	EtherCAT error LED output	P03	High	
CATLINKACT0, CATLINKACT1	O	EtherCAT link / activity LED output	P04-P05	High	
CATSYNC1	O	EtherCAT SYNC1 output	P10	High	Hi-Z (High)
CATSYNC0	O	EtherCAT SYNC0 output	P11	High	Hi-Z (Low)
CATLATCH1	I	EtherCAT LATCH1 input	P10	High	Hi-Z (High)
CATLATCH0	I	EtherCAT LATCH0 input	P11	High	Hi-Z (Low)
CATI2CCLK	O	EtherCAT EEPROM I2C clock output	P22	-	Hi-Z
CATI2CDATA	I/O	EtherCAT EEPROM I2C data input/output	P23	-	
CATRESTOUT	O	EtherCAT PHY RESETOUT	P56	-	Hi-Z (High)

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2.3.3 External Memory Interface Pins

Pin Name	I/O	Function	Shared Signal	Shared Port	Active	Level during Reset
BUSCLK	O	Bus clock output	-	-	-	Clock output
CSZ0	O	Chip select signal output	HCSZ	-	Low	Hi-Z (High)
CSZ1	O		HPGCSZ	P44		
CSZ2	O		-	P51		
CSZ3	O		-	P50		
A1 / MA0 Note4	O	Address output	HA1	P40	-	Hi-Z (High)
A2-A20 / MA1-MA19 Note4	O		HA2-HA20	-		Hi-Z (Low)
A21-A27 / MA20-MA26 Note4	O		-	RP21-RP27		
D0-D15 / MD0-MD15 / MA0-MA15 Note1, Note4	I/O	Data bus	HD0-HD15	-		
D16-D31 / MD16-MD31 / MA16-MA31 Note1, Note4	I/O		HD16-HD31	RP30-RP37 RP10-RP17	-	Hi-Z (High)
RDZ	O	Read strobe output	HRDZ	-	Low	Hi-Z (High)
WRSTBZ	O	Write strobe output	HWRSTBZ	-	Low	
WRZ0, WRZ1/ BENZ0, BENZ1	O	Valid byte lane strobe output	HWRZ0, HWRZ1/ HBENZ0, HBENZ1	-	Low	
WRZ2, WRZ3/ BENZ2, BENZ3	O		HWRZ2, HWRZ3/ HBENZ2, HBENZ3	RP06, RP07	Low	
WAITZ	I	Wait signal input	HWAITZ	P41	Low	Hi-Z (High)
WAITZ1-WAITZ3 Note2	I	Wait signal input	-	P45-P47	Low	
BCYSTZ / ADVZ Note3	O	Address valid output	HBCYSTZ	RP20	Low	Hi-Z (High)

Remark: Pins of the external memory interface other than BUSCLK are input pins while the internal reset signal (HRESETZ) is at its active level.

Notes 1. While the synchronous burst access memory controller is in use, these signals are multiplexed with the address signals if the ADMUXMODE pin is driven high.
ADMUXMODE = 0: MD0-MD31 (Separate address and data lines)
ADMUXMODE = 1: MD0-MD31/MA0-MA31 (Multiplexed address and data lines)

2. These pins are only available when the synchronous burst access memory controller is in use.

3. This pin functions as BCYSTZ when the asynchronous SRAM memory controller is in use and as ADVZ when the synchronous burst access memory controller is in use.

4. This pin functions as A1-A27 and D0-D31 functions when the asynchronous SRAM memory controller is in use and as MA0-MA26 and MD0-MD31 functions when the synchronous burst access memory controller is in use.

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2.3.4 External MCU Interface Pins

Pin Name	I/O	Function	Shared Pin	Shared Port	Active	Level during Reset
HBUSCLK	I	Bus clock input for host	INTPZ11	P43	-	Hi-Z (High)
HCSZ	I	Chip select signal input	CSZ0	-	Low	
HPGCSZ	I	PageRom mode chip select input	CSZ1	P44	Low	
HWAITZ	O	Wait signal output	WAITZ	P41	Low	
HA1	I	Address signal input	A1	P40	-	Hi-Z (High)
HA2-HA20	I		A2-A20	-		Hi-Z (Low)
HD0-HD15	I/O	Data bus	D0-D15	-	-	
HD16-HD31	I/O		D16-D31	RP30-RP37 RP10-RP17		Hi-Z (High)
HRDZ	I	Read strobe input	RDZ	-	Low	Hi-Z (High)
HWRSTBZ	I	Write strobe output	WRSTBZ	-	Low	
HWRZ0, HWRZ1/ HBENZ0, HBENZ1	I	Valid byte lane strobe input	WRZ0, WRZ1/ BENZ0, BENZ1	-	Low	
HWRZ2, HWRZ3/ HBENZ2, HBENZ3	I		WRZ2, WRZ3/ BENZ2, BENZ3	RP06, RP07		
HERROUTZ	O	Error interrupt output	SLEEPING	P42	Low	High
HBCYSTZ	I	Bus cycle input	BCYSTZ / ADVZ	RP20	Low	Hi-Z (High)

Caution: Input the low level to the HBUSCLK pin while asynchronous mode is in use.

Remark: The external MCU interface pins continue to operate during a reset.

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2.3.5 Port Pins and Real-time Port Pins

The port and pins are configured as 12 sets of 8-bit ports.
They are accessible in 32-bit units by grouping sets of 4 ports; i.e. ports 0 to 3, 4 to 7, and real-time ports 0 to3.

(1/4)

	Pin Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during Reset
P0	P00	INTPZ0	CATLEDRUN Note1	CCI_RUNLEDZ Note2	-	Note 3
	P01	INTPZ1	CATIRQ Note1	-	-	
	P02	INTPZ2	CATLEDSTER Note1	CCI_DLINKLEDZ Note2	-	
	P03	INTPZ3	CATLEDERR Note1	CCI_ERRLEDZ Note2	CCS_MON5	
	P04	INTPZ4	CATLINKACT0 Note1	CCI_LERR1LEDZ Note2	CCS_MON6	
	P05	INTPZ5	CATLINKACT1 Note1	CCI_LERR2LEDZ Note2	CCS_MON7	
	P06	PHYLINK0 Note2	P0LINKLEDZ Note1	CCI_SDLEDZ Note2	CCS_MON0	
	P07	PHYLINK1 Note2	P1LINKLEDZ Note1	CCI_RDLEDZ Note2	CCS_RESOUT	
P1	P10	CATLATCH1 Note1	CATSYNC1 Note1	-	CCS_REFSTB	Hi-Z (High)
	P11	CATLATCH0 Note1	CATSYNC0 Note1	-	CCS_MON4	Hi-Z (Low)
	P12	INTPZ6	-	CCI_NMIZ Note2	-	Hi-Z (High)
	P13	INTPZ7	-	CCI_WDTIZ Note2 / CCS_WDTZ / CCM_WDTENZ	-	
	P14	SMSCK	-	-	-	
	P15	SMSI	-	-	-	
	P16	SMSO	-	-	-	
	P17	SMCSZ	-	-	-	
P2	P20	RXD0	-	CCM_LINKERRZ	-	Note3
	P21	TXD0	-	CCM_ERRZ	-	
	P22	INTPZ8	CATI2CCLK Note1	CCS_IOTENSU	-	
	P23	INTPZ9	CATI2CDATA Note1	CCS_SENYU0	-	
	P24	INTPZ10	ETHSWSECOUT	CCS_SENYU1	-	
	P25	WDTOUTZ	–	CCS_ERRZ	-	
	P26	TIN1	TOUT1	CCM_RUNZ / CCS_RUNZ	-	
	P27	TIN0	TOUT0	-	-	

Notes 1. Only applies to R-IN32M3-EC.
2. Only applies to R-IN32M3-CL.
3. Hi-Z for R-IN32M3-EC and hi-Z (High) for R-IN32M3-CL

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	Port Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during Reset
P3	P30	RXD1	-	-	-	Hi-Z (High)
	P31	TXD1	-	-	-	
	P32	DMAREQZ1	-	-	CCS_MON1	
	P33	DMAACKZ1	CCI_WAITEDGEH Note2	-	CCS_MON2	
	P34	DMATCZ1	CCI_WRLENH Note2	-	CCS_MON3	
	P35	CSISCK1	INTPZ22	CCM_IRLZ	-	
	P36	CSISI1	INTPZ23	CCS_FUSEZ	-	
	P37	CSISO1	INTPZ24	CCM_MSTZ	-	
P4	P40	A1 / MA0	HA1	-	-	Hi-Z (High)
	P41	WAITZ	HWAITZ	-	-	
	P42	SLEEPING	HERROUTZ	CCM_SDGCZ	-	
	P43	INTPZ11	HBUSCLK	-	-	
	P44	CSZ1	HPGCSZ	-	-	
	P45	CSISCK0	WAITZ1	-	-	
	P46	CSISI0	WAITZ2	-	-	
	P47	CSISO0	WAITZ3	-	-	
P5	P50	CSZ3	-	CCM_LNKRUNZ / CCS_LNKRUNZ	-	
	P51	CSZ2	-	CCM_RDLEDZ / CCS_RDLEDZ	-	
	P52	TIN3	TOUT3	CCS_SDGATEON	-	Hi-Z (Low)
	P53	CRXD0	CCS_RD	CCM_RD	-	Hi-Z (High)
	P54	CTXD0	CCS_SD	CCM_SD	-	
	P55	CRXD1	-	-	-	
	P56	CTXD1	CATRESTOUT Notes1	CCI_PHYREZ1 Notes2	-	
	P57	TIN2	TOUT2	CCI_PHYREZ0 Notes2	-	

Notes 1. Only applies to R-IN32M3-EC.

2. Only applies to R-IN32M3-CL.

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	Port Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during reset
P6	P60	SCL0	–	–	–	Note3
	P61	SDA0	–	–	–	
	P62	RTDMAREQZ	–	CCM_MDIN0	–	
	P63	RTDMAACKZ	–	CCM_MDIN1	–	
	P64	RTDMATCZ	–	CCM_MDIN2	–	
	P65	DMAREQZ0	–	CCM_MDIN3	–	
	P66	DMAACKZ0	–	CCI_INTZ Note2	–	
	P67	DMATCZ0	–	–	–	
P7	P70	CSICS00	P0DUPLEXLEDZ Note1	CCS_STATION_NO_0 / CCM_SNIN0	–	
	P71	CSICS01	–	CCS_STATION_NO_1 / CCM_SNIN1	–	
	P72	CSICS10	P0SPEED100LEDZ Note1	CCS_STATION_NO_2 / CCM_SNIN2	–	
	P73	CSICS11	P0SPEED10LEDZ Note1	CCS_STATION_NO_3 / CCM_SNIN3	–	
	P74	INTPZ12	P1DUPLEXLEDZ Note1	CCS_STATION_NO_4 / CCM_SNIN4	–	
	P75	INTPZ13	–	CCS_STATION_NO_5 / CCM_SNIN5	–	
	P76	INTPZ14	P1SPEED100LEDZ Note1	CCS_STATION_NO_6 / CCM_SNIN6	–	
	P77	INTPZ15	P1SPEED10LEDZ Note1	CCS_STATION_NO_7 / CCM_SNIN7	–	

Notes 1. Only applies to R-IN32M3-EC.

2. Only applies to R-IN32M3-CL.

3. Hi-Z for R-IN32M3-EC and hi-Z (High) for R-IN32M3-CL

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RP0x to RP3x functions as real-time ports which can transfer data via a dedicated DMA controller. They are able to input and output data in 32-bit units in synchronization with the DMA transfer trigger.

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	Port Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during Reset
RP0	RP00	INTPZ16	SCL1	CCM_SDLEDZ / CCS_SDLEDZ	−	Hi-Z (High)
	RP01	INTPZ17	SDA1	CCM_SMSTZ	−	
	RP02	INTPZ18	P0ACTLEDZ Note	CCS_BS1	−	
	RP03	INTPZ19	−	CCS_BS2	−	
	RP04	INTPZ20	P1ACTLEDZ Note	CCS_BS4	−	
	RP05	INTPZ21	−	CCS_BS8	−	
	RP06	WRZ2/BENZ2	HWRZ2/HBENZ2	-	−	
	RP07	WRZ3/BENZ3	HWRZ3/HBENZ3	−	−	
RP1	RP10	D24/MD24/HD24	−	−	−	Hi-Z (High)
	RP11	D25/MD25/HD25	−	−	−	
	RP12	D26/MD26/HD26	−	−	−	
	RP13	D27/MD27/HD27	−	−	−	
	RP14	D28/MD28/HD28	−	−	−	
	RP15	D29/MD29/HD29	−	−	−	
	RP16	D30/MD30/HD30	−	−	−	
	RP17	D31/MD31/HD31	−	−	−	
RP2	RP20	BCYSTZ / ADVZ	HBCYSTZ	−	−	Hi-Z (High)
	RP21	A21/MA20	−	−	−	Hi-Z (Low)
	RP22	A22/MA21	−	−	−	
	RP23	A23/MA22	−	−	−	
	RP24	A24/MA23	INTPZ25	−	−	
	RP25	A25/MA24	INTPZ26	−	−	
	RP26	A26/MA25	INTPZ27	−	−	
	RP27	A27/MA26	INTPZ28	−	−	
RP3	RP30	D16/MD16/HD16	−	−	−	Hi-Z (High)
	RP31	D17/MD17/HD17	−	−	−	
	RP32	D18/MD18/HD18	−	−	−	
	RP33	D19/MD19/HD19	−	−	−	
	RP34	D20/MD20/HD20	−	−	−	
	RP35	D21/MD21/HD21	−	−	−	
	RP36	D22/MD22/HD22	−	−	−	
	RP37	D23/MD23/HD23	−	−	−	

Note: Only applies to R-IN32M3-EC.

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2.3.6 Serial Flash ROM Interface Pins

The serial flash ROM interface pins are pins of the serial flash ROM memory controller.
They support fast read, fast read dual output and fast read dual I/O modes.

Pin Name	I/O	Function	Shared Port	Active	Level during Reset
SMSCK	O	Serial clock output signal for serial flash ROM	P14	-	Hi-Z (High)
SMSI	I/O	Serial data I/O signal for serial flash ROM (connected to the SO pin of serial flash ROM)	P15	High	
SMSO	I/O	Serial data I/O signal for serial flash ROM (connected to the SI pin of serial flash ROM)	P16	High	
SMCSZ	O	Chip select output signal for serial flash ROM	P17	Low	

2.3.7 DMA Interface Pins

The DMA interface pins are interface pins of the DMA controllers for the internal AHB bus.
There are two DMA controllers: one with four internal channels but only two external interfaces, and one with one internal channel and one external interface.

Pin Name	I/O	Function	Shared Port	Active	Level during Reset
RTDMAREQZ	I	RTDMAC DMA transfer request input	P62	Low	Note
RTDMAACKZ	O	RTDMAC DMA acknowledge output	P63	Low	
RTDMATCZ	O	RTDMAC terminal count output	P64	Low	
DMAREQZ0	I	DMA transfer request input 0	P65	Low	
DMAACKZ0	O	DMA acknowledge output 0	P66	Low	
DMATCZ0	O	DMA terminal count output 0	P67	Low	
DMAREQZ1	I	DMA transfer request input 1	P32	Low	Hi-Z (High)
DMAACKZ1	O	DMA acknowledge output 1	P33	Low	
DMATCZ1	O	Terminal count output 1	P34	Low	

Caution: Each DMA interface is assigned to a specific DMA channel.

Note: Hi-Z for R-IN32M3-EC and hi-Z (High) for R-IN32M3-CL.

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2.3.8 External Interrupt Input Pins

The chip has one non-maskable interrupt and 29 maskable interrupt input pins.

Pin Name	I/O	Function	Shared Port	Active	Level during Reset
NMIZ	I	Non-maskable external interrupt input	-	Low	Hi-Z (High)
INTPZ0-INTPZ5	I	External interrupt input	P00-P05	Low	Note
INTPZ6, INTPZ7			P12, P13	Low	Hi-Z (High)
INTPZ8-INTPZ10			P22-P24	Low	Note
INTPZ11			P43	Low	Hi-Z (High)
INTPZ12-INTPZ15			P74-P77	Low	Note
INTPZ16-INTPZ21			RP00-RP05	Low	Hi-Z (High)
INTPZ22-INTPZ24			P35-P37		
INTPZ25-INTPZ28			RP24-RP27		Hi-Z (Low)

Note: Hi-Z for R-IN32M3-EC and hi-Z (High) for R-IN32M3-CL.

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2.3.9 Timer I/O Pins

Pin Name	I/O	Function	Shared Port	Active	Level during Reset
TIN0 / TOUT0	I/O	Timer TAUJ0 input/output	P27	-	Note
TIN1 / TOUT1	I/O	Timer TAUJ1 input/output	P26	-	
TIN2 / TOUT2	I/O	Timer TAUJ2 input/output	P57	-	Hi-Z (High)
TIN3 / TOUT3	I/O	Timer TAUJ3 input/output	P52	-	Hi-Z (Low)

Note: Hi-Z for R-IN32M3-EC and hi-Z (High) for R-IN32M3-CL.

2.3.10 Watchdog Timer Output Pin

Pin Name	I/O	Function	Shared Port	Active	Level during Reset
WDTOUTZ	O	Watchdog timer output	P25	Low	Note

Note: Hi-Z for R-IN32M3-EC and hi-Z (High) for R-IN32M3-CL.

2.3.11 Trace Pins

Pin Name	I/O	Function	Active	Level during Reset
TRACECLK	O	Trace port clock output	-	Clock output
TRACEDATA3- TRACEDATA0	O	Trace port data output	-	Low

2.3.12 CPU Power Control Pin

Pin Name	I/O	Function	Shared Port	Active	Level during Reset
SLEEPING	O	CPU SLEEP mode output	P42	High	Hi-Z (High)

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2.3.13 Serial Interface Pins

Pin Name	I/O	Function	Shared Port	Active	Level during Reset
TXD0	O	UART0 serial data output	P21	-	Note
RXD0	I	UART0 serial data input	P20	-	
TXD1	O	UART1 serial data output	P31	-	Hi-Z (High)
RXD1	I	UART1 serial data input	P30	-	
CSISCK0	I/O	CSI0 serial clock input/output	P45	-	
CSISI0	I	CSI0 serial data input	P46	-	
CSISO0	O	CSI0 serial data output	P47	-	
CSICS00, CSICS01	O	CSI0 chip select output 0,1	P70, P71	Low	Note
CSISCK1	I/O	CSI1 serial clock input/output	P35	-	Hi-Z (High)
CSISI1	I	CSI1 serial data input	P36	-	
CSISO1	O	CSI1 serial data output	P37	-	
CSICS10, CSICS11	O	CSI1 chip select output 0,1	P72, P73	Low	Note
SCL0	I/O	I2C0 serial clock input/output	P60	-	
SDA0	I/O	I2C0 serial data input/output	P61	-	
SCL1	I/O	I2C1 serial clock input/output	RP00	-	Hi-Z (High)
SDA1	I/O	I2C1 serial data input/output	RP01	-	
CRXD0	I	CAN0 receive data input (5V-tolerant buffer)	P53	-	
CTXD0	O	CAN0 transfer data output	P54	-	
CRXD1	I	CAN1 receive data input (5V-tolerant buffer)	P55	-	
CTXD1	O	CAN1 transfer data output	P56	-	

Note: Hi-Z for R-IN32M3-EC and hi-Z (High) for R-IN32M3-CL.

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2.3.14 CC-Link IE Field Pins (Intelligent Device Station) (R-IN32M3-CL only)

Pin Name	I/O	Function	Shared Port	Active	Level during Reset
CCI_RUNLEDZ	O	RUN status output	P00	Low	Hi-Z (High)
CCI_DLINKLEDZ	O	Cyclic communication status output	P02	Low	
CCI_ERRLEDZ	O	Field network error status output	P03	Low	
CCI_LERR1LEDZ	O	Link error status output 1	P04	Low	
CCI_LERR2LEDZ	O	Link error status output 2	P05	Low	
CCI_SDLEDZ	O	Transmission state output	P06	Low	
CCI_RDLEDZ	O	Port reception state output	P07	Low	
CCI_NMIZ	O	Output NMI interrupt to MCU	P12	Low	Hi-Z (High)
CCI_WDTIZ	I	Input from external watchdog timer	P13	Low	
CCI_WAITEDGEH Note	I/O	Wait synchronized edge setting 0: Fall edge mode 1: Rise edge mode	P33	-	
CCI_WRLENH Note	I/O	WRL signal enable setting 0: Write byte enable mode 1: Normal byte enable mode	P34	-	
CCI_PHYREZ1	O	PHY reset output 1	P56	Low	
CCI_PHYREZ0	O	PHY reset output 0	P57	Low	
CCI_INTZ	O	Output Interrupt to MCU	P66	Low	
CCI_CLK2_097M	I	2.097152-MHz clock (crystal oscillator)	-	-	-

Note: When user does boot with the external memory boot mode, external serial flash ROM boot mode, or instruction RAM boot mode, be sure not to input the low level to P33 (multiplexed with CCI_WAITEDGEH) and P34 (multiplexed with CCI_WRLENH) pins during a reset.
P33 and P34 pins should be left open circuit or the high level should be input to the pins during a reset. If you input the low level to P33 and P34 pins during a reset, you cannot access the CC-Link IE field from the CPU of the R-IN32M3.

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2.3.15 CC-Link Pins (Intelligent Device Station)

Pin Name	I/O	Function	Shared Port	Active	Level during Reset
CCM_LINKERRZ	O	Link error LED control output	P20	Low	Note
CCM_ERRZ	O	Not used	P21	Low	
CCM_RUNZ	O	Run LED control output	P26	Low	
CCM_MDIN0-CCM_MDIN3	I	Transfer rate setting input	P62-P65	-	
CCM_SNIN0-CCM_SNIN7	I	Station no. setting switch input	P70-P77	-	
CCM_LNKRUNZ	O	Link run LED control output	P50	Low	Hi-Z (High)
CCM_RDLEDZ	O	Receive data LED control output	P51	Low	
CCM_SDLEDZ	O	Transfer data LED control output	RP00	Low	
CCM_IRLZ	O	Interrupt signal output from communications circuit	P35	Low	
CCM_WDTENZ	I	Watchdog timer error input	P13	Low	
CCM_MSTZ	O	Not used	P37	Low	
CCM_SMSTZ	O	Not used	RP01	Low	
CCM_RD	I	Communications circuit data reception	P53	-	
CCM_SD	O	Communications circuit data transmission pin	P54	-	
CCM_SDGCZ	O	Communications circuit transmit data & gate control pin	P42	Low	
CCM_CLK80M	I	CC-Link clock input (80 MHz)	-	-	-

Note: Hi-Z for R-IN32M3-EC and hi-Z (High) for R-IN32M3-CL.

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2.3.16 CC-Link Pins (Remote Device Station)

Caution: To use a remote device station, it is necessary to connect a CCS_REFSTB pin (P10) to a port pin with the external interrupt function (INTPZ).

Pin Name	I/O	Function	Shared Port	Active	Level during Reset
CCS_MON1- CCS_MON3	O	Monitor signal output	P32-P34	-	Hi-Z (High)
CCS_MON4	O	Monitor signal output	P11	-	Hi-Z (Low)
CCS_MON0	O	Monitor signal output	P06	-	Note 1
CCS_MON5- CCS_MON7	O	Monitor signal output	P03-P05	-	
CCS_RESOUT	O	Reset output signal	P07	High	
CCS_IOTENSU	I	Initial setting pin	P22	-	
CCS_SENYU0	I	Initial setting pin	P23	-	
CCS_SENYU1	I	Initial setting pin	P24	-	
CCS_ERRZ	O	Operation check LED	P25	Low	
CCS_RUNZ	O	Operation check LED	P26	Low	
CCS_STATION_NO_0- CCS_STATION_NO_7	I	Station no. setting switch input	P70-P77	-	
CCS_LNKRUNZ	O	Link run LED control output	P50	Low	Hi-Z (High)
CCS_REFSTB	O	Interrupt signal	P10	High	
CCS_WDTZ	I	Watchdog timer input	P13	Low	
CCS_RDLEDZ	O	Receive data LED control output	P51	Low	
CCS_RD	I	Communications circuit data reception pin	P53	-	
CCS_SD	O	Communications circuit data transmission pin	P54	-	
CCS_SDLEDZ	O	Operation check LED	RP00	Low	
CCS_SDGATEON	O	Communication circuit transmit data & gate control pin	P52	High	Hi-Z (Low)
CCS_BS1	I	Baud rate setting switch input	RP02	-	Hi-Z (High)
CCS_BS2	I	Baud rate setting switch input	RP03	-	
CCS_BS4	I	Baud rate setting switch input	RP04	-	
CCS_BS8	I	Baud rate setting switch input	RP05	-	
CCS_FUSEZ	I	Fuse cutting input signal	P36	Low	
CCM_CLK80M[Note2]	I	CC-Link clock input port (80 MHz)	-	-	-

Notes 1. Hi-Z for R-IN32M3-EC and hi-Z (High) for R-IN32M3-CL.

2. This pin is shared with the pin for CC-Link intelligent device station.

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2.3.17 System Pins

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Pin Name	I/O	Function	Active	Level during Reset
XT1	I	Clock input pins OSCTH = 1: Oscillator is in use. XT1 and XT2 are respectively connected to GND and oscillator. OSCTH = 0: Resonator is in use. XT1 and XT2 are connected to resonator.	-	-
XT2	I/O		-	-
RESETZ	I	Reset input	Low	-
HOTRESETZ Note1	I	Hot reset input	Low	-
PONRZ	I	Internal RAM power-on reset input	Low	-
OSCTH	I	External clock input mode setting 0: Resonator using mode 1: External clock input mode	High	-
JTAGSEL	I	JTAG pin operating mode setting 0: Cortex-M3 JTAG mode 1: B-SCAN JTAG mode	-	-
RSTOUTZ	O	External reset output	Low	Low
CLKOUT25M0 Note1	O	PHY clock output	-	Oscillation source is passed through these pins
CLKOUT25M1 Note1	O	PHY clock output	-	
PLL_VDD	-	PLL power supply (1.0 V)	-	-
PLL_GND	-	PLL ground level (GND)	-	-
VDD33	-	I/O power supply (3.3 V)	-	-
VDD10	-	Internal power supply (1.0 V)	-	-
GND	-	Power supply ground level (GND)	-	-
VDDQ_MII Note1	-	Ethernet I/O power supply (3.3 V)	-	-

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Pin Name	I/O	Function	Active	Level during Reset
LX Note2	O	1.5-V output for on-chip regulator	-	-
EXTRES Note2	-	Reference resistor connecting pin for on-chip PHY	-	-
P0VDDARXTX Note2	-	Analog power supply for Rx/Tx pin (1.5 V) – port 0	-	-
P1VDDARXTX Note2	-	Analog power supply for Rx/Tx pin (1.5 V) – port 1	-	-
VDDACB Note2	-	Analog power supply for on-chip PHY (3.3 V)	-	-
AGND Note2	-	Analog ground level for on-chip PHY (GND)	-	-
VDD15 Note2	-	Power supply for on-chip PHY (1.5V)	-	-
VDDAPLL Note2	-	Analog core power supply for on-chip PHY (1.5V)	-	-
VSSAPLLCB Note2	-	Analog core ground level for on-chip PHY (GND)	-	-
VDD33ESD Note2	-	Analog test power supply for on-chip PHY (3.3 V)	-	-
AVDD_REG Note2	-	Analog power supply for on-chip regulator (3.3 V)	-	-
AGND_REG Note2	-	Analog ground level for on-chip regulator (GND)	-	-
BVDD Note2	-	Power supply for on-chip regulator (3.3 V)	-	-
BGND Note2	-	Ground level for on-chip regulator (GND)	-	-
FB Note2	I	Feedback input for on-chip regulator	-	-
VDDQ_PECL_B0 Note2	-	PECL buffer power supply (3.3 V)	-	-
VDDQ_PECL_B1 Note2	-	PECL buffer power supply (3.3 V)	-	-

Notes 1. Only applies to R-IN32M3-CL.

2. Only applies to R-IN32M3-EC.

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2.3.18 Test Pins

Pin Name	I/O	Function	Active	Level during Reset
TMODE0-TMODE2	I	Test mode select pin	-	-
TMS	I/O	Mode select signal	-	-
TDI	I	Serial data input	-	-
TDO	O	Serial data output	-	-
TRSTZ	I	Reset signal	Low	-
TCK	I	Clock signal (JTAG clock)	-	-
TMC1	I	Renesas test pins	-	-
TMC2	I		-	-
ATP Note	I			
TEST1 Note	I		-	-
TEST2 Note	I		-	-
TEST3 Note	I		-	-
TESTOUT5 Note	O		-	-

Note: Only applies to R-IN32M3-EC.

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2.3.19 Operating Mode Setting Pins

Pin Name	I/O	Function	Active	Level during Reset
BOOT1-BOOT0	I	Boot mode select 00: External memory boot 01: External serial flash ROM boot 10: External MCU boot 11: Instruction RAM boot (only available for debugging)	-	-
MEMIFSEL	I	External memory interface select 0: Slave memory interface 1: External MCU interface	-	-
BUS32EN	I	External memory interface bus width select 0: 16-bit bus 1: 32-bit bus	-	-
HIFSYNC	I	External MCU interface operation mode select 0: Asynchronous SRAM interface 1: Synchronous SRAM interface	-	-
HWRZSEL	I	External MCU interface HWRZ/HBENZ select 0: Used as HBENZ 1: Used as HWRZ	-	-
MEMCSEL	I	Internal memory controller select port 0: Asynchronous SRAM memory controller 1: Synchronous burst access memory controller	-	-
ADMUXMODE	I	Multiplexing of address and data lines 0: Separated address and data lines 1: Multiplexed address and data lines	-	-

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The combinations of available operating mode setting pins in this product are as follows.

Boot Mode	External Memory Boot				External MCU Boot				External Serial Flash ROM Boot							
External Memory Interface	Slave Memory Interface				External MCU Interface				Slave Memory Interface				External MCU Interface			
MEMC Type	Asynchronous		Synchronous		Asynchronous		Synchronous		Asynchronous		Synchronous		Asynchronous		Synchronous	
External Bus Width	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit
BOOT1-0	00	00	00	00	10	10	10	10	01	01	01	01	01	01	01	01
MEMIFSEL	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
MEMCSEL	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
BUS32EN	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
HIFSYNC	0	0	0	0	Note1	Note1	1	1	0	0	0	0	Note1	Note1	1	1
HWRZSEL	0	0	0	0	Note2	Note2	0	0	0	0	0	0	Note2	Note2	0	0
ADMUXMODE	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1

Caution: Any combination of operating mode setting pins other than the above is prohibited.

Notes 1. The mode of the external MCU interface is selectable by the level on the HIFSYNC pin.
HIFSYNC = 0: Asynchronous SRAM interface mode
HIFSYNC = 1: Synchronous SRAM interface mode
For details, see section 11, External MCU Interface, in the R-IN32M3 Series User's Manual (Peripheral Modules).
2. The external MCU interface HWRZ or HBENZ is selectable by the level on the HWRZSEL pin.
For details, see section 2.3.3, External Memory Interface Pins.

Remarks 1. The combination of operating-mode setting pins used to select booting for instruction RAM (BOOT1-0 = 11) is the same as that for booting from external memory (BOOT1-0 = 00).
2. Asynchronous: Asynchronous SRAM memory controller (MEMCSEL = 0)
Synchronous: Synchronous burst access memory controller (MEMCSEL = 1)

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2.4 Buffer Types and Recommended Connections for Unused Pins

2.4.1 Ethernet Pins

(1) PHY Interface Pins

Caution: Only applies to R-IN32M3-CL.

Pin Name	I/O	Interface	Recommended Connection when Not in Use
ETH0_TXC	I	Input buffer (3.3 V)	Connect to GND
ETH0_GTXC	O	BID_BUF (3.3 V_GMII_MII)_with_IOLH_Control	Open
ETH0_TXEN			
ETH0_TXER			
ETH0_TXD0- ETH0_TXD7			
ETH0_GE_INT	I	Input buffer (3.3 V)	Connect to GND
ETH0_RXC	I	BID_BUF (3.3 V_GMII_MII)_with_IOLH_Control	Connect to GND
ETH0_RXDV			
ETH0_RXER			
ETH0_RXD0- ETH0_RXD7			
ETH0_CRS	I	Input buffer (3.3 V)	Connect to GND
ETH0_COL			
ETH1_TXC			
ETH1_GTXC	O	BID_BUF (3.3 V_GMII_MII)_with_IOLH_Control	Open
ETH1_TXEN			
ETH1_TXER			
ETH1_TXD0- ETH1_TXD7			
ETH1_GE_INT	I	Input buffer (3.3 V)	Connect to GND
ETH1_RXC	I	BID_BUF (3.3 V_GMII_MII)_with_IOLH_Control	Connect to GND
ETH1_RXDV			
ETH1_RXER			
ETH1_RXD0- ETH1_RXD7			
ETH1_CRS	I	Input buffer (3.3 V)	Connect to GND
ETH1_COL			
ETH_MDC	O	Output buffer (3.3 V) 6 mA	Open
ETH_MDIO	I/O	I/O buffer (3.3 V) 6 mA	Connect to GND

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(2) Media Interface Pins

Caution: Only applies to R-IN32M3-EC.

Pin Name	I/O	Interface	Recommended Connection when Not in Use
P0_RX_P	I	Management data interface (analog)	Open
P0_RX_N	I		
P1_RX_P	I		
P1_RX_N	I		
P0_TX_P	O	Management data interface (analog)	Open
P0_TX_N	O		
P1_TX_P	O		
P1_TX_N	O		
P0_SD_P	I	3.3 -V PECL input buffer	Connect to GND
P0_SD_N	I		
P1_SD_P	I		
P1_SD_N	I		
P0_RD_P	I		
P0_RD_N	I		
P1_RD_P	I		
P1_RD_N	I		
P0_TD_OUT_P	O	3.3-V PECL output buffer	Open
P0_TD_OUT_N	O		
P1_TD_OUT_P	O		
P1_TD_OUT_N	O		
P0_FX_EN_OUT	O	Output buffer (3.3 V) 12 mA	Open
P1_FX_EN_OUT	O		

2.4.2 External Memory/ MCU Interface Pins

Pin Name	I/O	Interface	Recommended Connection when Not in Use
BUSCLK	O	Output buffer (3.3 V) 9 mA	Open
CSZ0 / HCSZ	I/O	I/O buffer (3.3 V) 6 mA 50kΩ pull-up	Open
A2-A20 / HA2-HA20	I/O	I/O buffer (3.3 V) 6 mA 50kΩ pull-down	Open
D0-D15 / HD0-HD15			
RDZ / HRDZ	I/O	I/O buffer (3.3 V) 6 mA 50kΩ pull-up	Open
WRSTBZ / HWRSTBZ			
WRZ0, WRZ1 / BENZ0, BENZ1 / HWRZ0, HWRZ1			

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2.4.3 System Pins

Pin Name	I/O	Interface	Recommended Connection when Not in Use
NMIZ	I	Input buffer (3.3 V) Schmitt in, 50kΩ pull-up	Connect to VDD33 (3.3 V)
XT1	I	Oscillator with EN	Connect to GND
XT2	I/O		-
RSTOUTZ	O	Output buffer (3.3 V) 6m A	Open
RESETZ	I	Input buffer (3.3 V) Schmitt in	-
PONRZ			
HOTRESETZ			Connect to VDD33 (3.3 V)
OSCTH	I	Input buffer (3.3 V) Schmitt in, 50kΩ pull-down	Set these pins according to the operating mode
JTAGSEL			

2.4.4 Test Pins

Pin Name	I/O	Interface	REQUIRED Connection when Not in Use
TMODE0-TMODE2	I	Input buffer (3.3 V) Schmitt in, 50kΩ pull-down	Connect to GND
TMS	I/O	I/O buffer (3.3 V) 6 mA 50kΩ pull-up	Open
TDI	I	Input buffer (3.3 V), 50kΩ pull-up	Open
TDO	O	3-state output buffer (3.3 V) 6 mA	Open
TRSTZ	I	Input buffer (3.3 V) Schmitt in, 50kΩ pull-up	Open
TCK	I	Input buffer (3.3 V), 50kΩ pull-down	Open
TMC1	I	(TMC1) input buffer (3.3 V) for TMC terminal	Connect to GND
TMC2	I	(TMC2) input buffer (3.3 V) for TMC terminal	Connect to GND
ATP Note	I	Input buffer (3.3 V)	Open
TEST1 Note	I	Input buffer (3.3 V)	Connect to GND
TEST2 Note	I	Input buffer (3.3 V)	
TEST3 Note	I	Input buffer (3.3 V)	
TESTDOUT5 Note	O	Output buffer (3.3 V)	Open

Note: Only applies to R-IN32M3-EC.

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2.4.5 Port Pins

(1/2)

Pin Name	I/O	Interface	Recommended Connection when Not in Use
P00-P07	I/O	[R-IN32M3-EC] I/O buffer (3.3 V) (6 mA) [R-IN32M3-CL] Programmable I/O buffer (3.3 V) Load drive select function (6 mA, 12 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or neither)	R-IN32M3-EC: Connect to GND R-IN32M3-CL: Open
P10	I/O	Programmable I/O buffer (3.3 V) Load drive select function (6 mA, 12 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or neither)	Open
P11-P17	I/O	Programmable I/O buffer (3.3 V) (6 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or neither)	Open
P20-21, P25-26	I/O	[R-IN32M3-EC] I/O buffer (3.3 V) (6 mA) [R-IN32M3-CL] Programmable I/O buffer (3.3 V) Load drive select function (6 mA, 12 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or neither)	R-IN32M3-EC: Connect to GND R-IN32M3-CL: Open
P22-24, 27	I/O	[R-IN32M3-EC] I/O buffer (3.3 V) (6 mA) [R-IN32M3-CL] Programmable I/O buffer (3.3 V) (6 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or neither)	
P30, P31	I/O	Programmable I/O buffer (3.3 V) Load drive select function (6 mA, 12 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or neither)	Open
P32-P36	I/O	Programmable I/O buffer (3.3 V) (6 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or neither)	
P37	I/O	Programmable I/O buffer (3.3 V) Load drive select function (6 mA, 12 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or neither)	

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(2/2)

Pin Name	I/O	Interface	Recommended Connection when Not in Use
P40-P47	I/O	Programmable I/O buffer (3.3 V) (6 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or neither)	Open
P50-P52	I/O	Programmable I/O buffer (3.3 V) Load drive select function (6 mA, 12 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or neither)	
P53-P56	I/O	5V-tolerant I/O buffer 4 mA 50kΩ pull-up	
P57	I/O	Programmable I/O buffer (3.3 V) (6 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or neither)	
P60, P65-P67	I/O	[R-IN32M3-EC] I/O buffer (3.3 V) (6 mA) [R-IN32M3-CL] Programmable I/O buffer (3.3 V) (6 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or neither)	R-IN32M3-EC: Connect to GND R-IN32M3-CL: Open
P61-P64	I/O	[R-IN32M3-EC] I/O buffer (3.3 V) (6 mA) [R-IN32M3-CL] Programmable I/O buffer (3.3 V) Load drive select function (6 mA, 12 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or neither)	
P70-P77	I/O	[R-IN32M3-EC] I/O buffer (3.3 V) (6 mA) [R-IN32M3-CL] Programmable I/O buffer (3.3 V) (6 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or neither)	R-IN32M3-EC: Connect to GND R-IN32M3-CL: Open
RP00-RP07 RP10-RP17 RP20-RP27 RP30-RP37	I/O	Programmable I/O buffer (3.3 V) Load drive select function (6 mA, 12 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or neither)	Open

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2.4.6 Operation Mode Setting Pins

Pin Name	I/O	Interface	Recommended Connection when Not in Use
BOOT0, BOOT1	I	Input buffer (3.3 V) Schmitt in	Set these pins according to the operating mode
MEMIFSEL			
BUS32EN			
HIFSYNC			
HWRZSEL			
MEMCSEL			
ADMUXMODE			

2.4.7 CC-Link IE Field (Intelligent Device Station) Pin (R-IN32M3-CL Only)

Pin Name	I/O	Interface	Recommended Connection when Not in Use
CCI_CLK2_097M	I	Input buffer (3.3 V)	2.097152-MHz clock input

Caution: This pin requires a clock input even when the CC-Link IE Field is not in use.

2.4.8 CC-Link Pins (Intelligent Device Station, Remote Device Station)

Pin Name	I/O	Interface	Recommended Connection when Not in Use
CCM_CLK80M	I	Input buffer (3.3 V)	Connect to GND

2.4.9 Trace Pins

Pin Name	I/O	Interface	Recommended Connection when Not in Use
TRACECLK	O	Output buffer (3.3 V) 6 mA	Open
TRACEDATA0-TRACEDATA3			

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3. Specifications

3.1 CPU (Cortex-M3)

An R-IN32M3 device incorporates a high-performance 32-bit processor (Arm Cortex-M3 core).
This chapter explains information specific to R-IN32M3 products.

3.1.1 CPU Core Information

The version of the Cortex-M3 core currently used in an R-IN32M3 is shown below.
More information about the architecture of the CPU can be obtained from:
http://infocenter.arm.com/help/topic/com.arm.doc.set.cortexm/index.html

Product Name	Revision
R-IN32M3 Series	Cortex-M3 r2p1

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3.1.2 CPU Core Configuration

The Cortex-M3 of an R-IN32M3 has the following configurations.

Category	Configuration Item	Setting	Remark
Interrupts	NUM_IRQ	128	The number of IRQ interrupts to be input: 1 to 240 (NMI interrupts are counted separately)
Interrupt priority	LVL_WIDTH	4	Priority bit number 3 to 8 (8 to 256 priority levels)
MPU	MPU_PRESENT	Yes	Presence of the memory protection unit
Debug level	DEBUG_LVL	3	Debug level 1 to 3
Trace level	TRACE_LVL	2	Trace level 0 to 2
SW/SWJ-DP selection	JTAG_PRESENT	SWJ-DP	SWJ-DP is selected when JTAG access circuit is built in.
Bit-band area	BB_PRESENT	Yes	Presence of bit-banding

Debug Level	1	2	3 (Settings in R-IN32M3)
Function outline	Minimum debug configuration	Full Debug configuration (Data matching is not available)	Full debug configuration (with data matching)
Debugging halt	Yes	Yes	Yes
Breakpoints	2 (Instruction)	6 (Instruction) 2 (Literal)	6 (Instruction) 2 (Literal)
DWT comparator number	1 (Data matching is not available)	4 (Data matching is not available)	4
Flash patch function	No	Yes	Yes

Trace Level	0	1	2 (Settings in R-IN32M3)
Function outline	No trace	Standard trace	Full trace
ITM and TPIU functions	No	Yes	Yes
DWT trigger and counter	No	Yes	Yes
ETM function	No	No	Yes

Caution: R-IN32M3 products do not support SLEEPDEEP mode. Do not set the SLEEPDEEP bit of the SCR register to 1.

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3.2 Gigabit Ethernet MAC

3.2.1 Features

- 1 port (by switching between two ports)
- 10BASE, 100BASE, 1000BASE MAC
- Supports 1000BASE-X Physical Coding Sublayer (PCS)
- Supports full-duplex and half-duplex communication modes
- Automatic pause packet transmission function
- Auto broadcast suspension in response to reception of a pause packet
- Supports MII/GMII interface

3.2.2 Switch Functions

Following switching features are provided in an R-IN32M3.

- Two-port interface
- Hardware switching, look-up and filtering
- QoS with frame prioritization
- Priority control based on VLAN Priority (IEEE802.1q), which enables priorities to be re-assigned
- Classification and assigning of priority based on Differentiated Services (DiffServ) Code Point Field of IP v.4 and Class of Service (CoS) in IP v.6
- Queue with four priority levels
- Multicasting and broadcasting
- VLAN frames
- Cut-through and hub features
- Device level ring (DLR)

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3.3 EtherCAT Slave Controller Function (R-IN32M3-EC only)

The EtherCAT Slave Controller (ESC) uses the EtherCAT Slave Controller IP Core made by Beckhoff Automation GmbH, Germany.
The ESC handles EtherCAT communications by serving as an interface between EtherCAT field bus and slave applications.

Table 3.1 Features of the EtherCAT Slave Controller

Feature		R-IN32M3-EC	ET1100
Ports		2	2-4
FMMUs		8	8
SyncManagers		8	8
RAM [Kbytes]		8	8
Distributed clocks		64 bits	64 bits
Ebus		Not available	Available (0-4)
Process data interfaces (PDIs)		-	-
	Digital I/O	Not available	Available
	SPI slave	Not available	Available
	Host CPU interface	On-chip bus (external MCU interface)	8 bits/16 bits, synchronous/asynchronous

Caution: The register area (0E_0000H-0E_0F7FH) cannot be accessed from the external MPU interface (host CPU interface).

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3.4 CC-Link IE Field (Intelligent Device Station) Function (R-IN32M3-CL only)

The CC-Link IE field intelligent device station has functionality equivalent to that of the dedicated CP220 communications LSI chips manufactured by Mitsubishi Electric Corporation.
The outline specifications of the CC-Link IE field are as follows. For detailed specifications on the CC-Link IE field network, visit the following CC-Link Partner Association website.

https://www.cc-link.org/en/cclink/cclinkie/index.html

Table 3.2 Outline Specifications of CC-Link IE Field

Item	Specification
Ethernet standards	IEEE802.3ab (1000BASE-T) compliant
Transfer rate	1Gbps
Topology	Line, star, ring
Maximum number of connected units	254 modules
Maximum station-to-station distance	100 m

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3.5 General DMA Controller

3.5.1 Features

- Number of channels: 4 independent channels
- Transfer data size
  - Independently selectable for source and destination
  - Size range: 8 to 512 bits
- Maximum number of transfer bytes: 2^{32}-1
- Channel priority control
  - Fixed priority mode
  - Round robin mode (The channel that last completed a transfer is shifted to the lowest priority position.)
- DMA transfer methods

  The data used for DMA transfer is set in an internal register by using the following two modes.
  - Register mode:

    DMA transfer is performed using the values set in the control registers of the DMA controller written by the CPU. This mode supports conventional general DMA transfer.
  - Link mode:

    DMA transfer is performed according to a descriptor located in data RAM and external memory. The responsiveness of this mode is inferior to register mode because access of the descriptor occurs at every DMA transfer.
- Skip function

  Continuous access size and skip space size can each be set for the areas that are accessed with DMA transfer. Following access of the set size, it is possible to skip to the next address to be accessed.
- Buffer data dump function

  Then DMA is forced to stop, the function can dump the data stored in the buffer. After the dump, the DMA transfer is continued.
- Suspension function

  The ongoing DMA transaction can be suspended.
- DMA transfers interval setting function

  The DMA transfer interval can be specified to adjust the bus occupancy rate.
- Transfer mode
  - Single transfer mode

    When a DMA transfer request is made, the right to use the bus is acquired and the bus is released each time a transfer is completed. After that, whenever a DMA transfer request is made, this operation is repeated until the numbers of transfers specified in the control register are completed.
  - Block transfer mode

    When a DMA transfer request is made, the right to use the bus is acquired and data transfer is repeated until the numbers of transfers specified in the control register are completed. In this case, the bus is not occupied.

Caution: Transfer 512-bit wide data requires the data to be aligned on a 512-bit boundary.

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3.6 DMA Controller for Real-time Port

3.6.1 Features

- Number of channels: 1
- Transfer data size
  - Independently selectable for source and destination
  - Size range: 8 to 128 bits
- Maximum number of transfer bytes: 23^2-1
- DMA transfer methods
  - Register mode:
    DMA transfer is performed according to the control register in the DMA controller that is set from the CPU. The conventionally used General DMA transfer is supported.
  - Link mode:
    DMA transfer is performed according to a descriptor located in data RAM and external memory. The responsiveness of this mode is inferior to register mode because the access of the descriptor occurs at every DMA transfer.
- SKIP function
  A continuous access size and skip space size can be set respectively for the area to be accessed for DMA transfer. After space of the set continuous access size has been accessed, the function can skip space of the set discrete access size before accessing the next address.
- Buffer data dump function
  When DMA is forced to stop, the function can dump the data stored in the buffer. After the dump, the DMA transfer is continued.
- Suspension function
  The ongoing DMA transaction can be suspended.
- DMA transfers interval setting function
  The DMA transfer interval can be specified to adjust the bus occupancy rate.
- Transfer mode
  - Single transfer mode
    When a DMA transfer request is made, the right to use the bus is acquired and the bus is released each time a transfer is completed. After that, whenever a DMA transfer request is made, this operation is repeated until the numbers of transfers specified in the control register are completed.
  - Block transfer mode
    When a DMA transfer request is made, the right to use the bus is acquired and data transfer is repeated until the numbers of transfers specified in the control register are completed. In this case, the bus is not occupied.

Caution: Transfer 128-bit wide data requires the data to be aligned on a 128-bit boundary.

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3.7 Window Watchdog Timer

3.7.1 Features

- Operation mode after reset selectable by using start-up option
- Software triggered start mode
- Error mode options
  - Generates an NMI request on error detection
  - Generates a reset on error detection
- Window watchdog function
- Overflow interval time
  - 25MHz operation: 163 µs to 5.36 s

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3.8 Timer Array Unit

3.8.1 Features

-1 unit with 4 channels is provided

-32-bit counter and 32-bit data registers per channel

-Independent channel operation

-Synchronous channel operation (master and slave operation)

-Generation of different types of output signals

-Counter can be triggered by an external signal

-Interrupt generation

Independent Channel Operation	Synchronous Channel Operation
Independent channel operation functions	Synchronous channel operation function
Interval timer function	PWM output function
External input interval timer function	
External event count function	
Independent channel signal measurement functions	
Overflow interrupt output function	
External input period count detection function	
External input pulse interval judgment function	
External input signal width judgment function	
Other independent channel function	
External input position detection function	

-Supplementary note

Timers support prescaler options: count clock selectable from among four types of internal clocks as well as from an external clock. Each timer may be configured to PCLK frequency divided by 2^0 to 2^{15}, and one clock may be configured to be further divided by 1 to 256.

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3.9 Asynchronous Serial Interface

3.9.1 Features

-Full-duplex communication via built-in receive and transmit FIFOs
- ➢Internal 10-bit × 16 receive data FIFO
- ➢Internal 8-bit × 16 transmit data FIFO

-2-pin configuration
- ➢Transmit data output pin
- ➢Receive data input pin

-Error detection functions
- ➢Rx parity error
- ➢Rx framing error
- ➢Tx data consistency error

-Tx FIFO overflow error
- ➢Rx FIFO overrun error
- ➢Rx timeout error
- ➢Rx BF receive error

-FIFO status information
- ➢Rx FIFO full/empty status
- ➢Tx FIFO empty/empty status
- ➢Rx FIFO fill level
- ➢Tx FIFO fill level

-Interrupt requests: 3
- ➢Transmission interrupt
- ➢Reception interrupt
- ➢Status interrupt

-Character length: 7 or 8 bits

-Parity options: odd, even, 0, none

-Transmission stop bits: 1 or 2 bits

-MSB-/LSB-first transfer selectable

-Transmit/receive data inverted input/output possible

-13 to 20 bits selectable for the BF (Break Field) in the LIN (Local Interconnect Network) communication format
- ➢Recognition of 11 bits or more possible for BF reception in LIN communication format
- ➢BF reception flag provided

-BF reception can be detected during data communication

-Bus monitor function to keep data consistency of the transmit data

-Supported Baud rate: 300 to 12,500,000bps

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Table 3.3 Baud Rate Generator Clocks Output (PCLK: 100 MHz)

Baud Rate (bps)	Prescaler Clock (PRSCLK) Divisor “URTJnPRS”	Baud Rate Clock (BRCLK) Divisor “URTJnBRS”	ERR (%)
300	6	2604	0.01
600	5	2604	0.01
1200	4	2604	0.01
2400	3	2604	0.01
4800	2	2604	0.01
9600	1	2604	0.01
19200	0	2604	0.01
31250	0	1600	0.01
38400	0	1302	0.01
76800	0	651	0.01
115200	0	434	0.01
153600	0	326	-0.15
312500	0	160	0.00
1000000	0	50	0.00
2000000	0	25	0.00
2500000	0	20	0.00
5000000	0	10	0.00
6250000	0	8	0.00
1000000	0	5	0.00
1250000	0	4	0.00

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3.10 Clocked Serial Interface

3.10.1 Features

- Three-wire serial synchronous data transfer
- Master mode and slave mode selectable
- Multiple slaves configuration plus RCB (Recessive Configuration for Broadcasting) thanks to two configurable chip select output signals
- Built-in baud rate generator
- Adjustable baud rate; in slave mode it is determined by the input clock
- Maximum transmission speed: (at 100 MHz PCLK operation)
  - in master mode: PCLK/4 (25 MHz)
  - in slave mode: PCLK/6 (16.6 MHz)
- Phase of clock and data selectable
- Data transfer with MSB or LSB first selectable
- Transfer data length selectable from 7 to 16 bits in 1-bit increments
- Extended data length (EDL) function for transferring more than 16 bits of data
- Three selectable transfer modes:
  - Transmission mode
  - Reception mode
  - Transmission and reception mode
- Error detection (data consistency check, parity, timeout, overflow, overrun)
- Full support of job concept
- 128 words I/O buffer memory
- Memory mode selectable (FIFO, dual buffer, Tx-only buffer, direct access)
- Four different interrupt request signals
  - communication interrupt
  - reception interrupt
  - error interrupt
  - job completion interrupt
- Loop back mode (LBM) function for self-test

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3.11 I2C Bus

3.11.1 Features

- Operating mode
  - Standard mode (serial clock frequency: 100 kHz max.)
  - Fast mode (serial clock frequency: 400 kHz max.)
- Transfer mode
  - Single transfer mode
  - Continuous transfer mode
- Pin configuration
  - Serial clock pin
  - Serial transmit/receive data pin
- Interrupt request signal
  - Data transmit/receive interrupt request signal
  - Status interrupt request signal
- Communication data length
  - 8 bits
- Multi master support
  - Multiple masters can control the bus simultaneously.
- Serial clock signal level width
  - Serial clock signal (SCLn) high- and low-level pulse width can be changed.
- Automatic detection
  - Start and stop conditions can be detected automatically

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3.12 CC-Link Function

The outline specifications of CC-Link are as follows.
Please refer to the following URL for the additional details of CC-Link.

https://www.cc-link.org/en/

Table 3.4 CC-Link Outline Specifications

Item	Specification
Version	Ver.1.10 and Ver.2.00
Supported stations	Intelligent device station and Remote device station
Maximum number of link points	Remote I/O: 8192 points each, Remote register: 2048 words
Total number of slave stations	64 units
Communication speed and maximum overall cable extension length	10 Mbps: 100 m 5 Mbps: 160 m 2.5 Mbps: 400 m 625 kbps: 900 m 156 kbps: 1200 m
Communication system	Broadcast polling system

Caution: To use a remote device station, it is necessary to connect CCS_REFSTB pin (P10) to a port pin with the external interrupt function (INTPZ).

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3.13 CAN Controller

3.13.1 Features

- Compliant with ISO-11898
- Standard frame and extended frame transmission/reception enabled
- Transfer rate: 1 Mbps max.
- 64 message buffers per channel
- Receive/transmit history list function (can be set individually for each message buffer)
- Automatic block transmission function
- Multi-buffer receive block function
- Mask setting of 8 patterns is possible for each channel, applicable for data and remote frames
- Data bit time, communication baud rate and sample point can be controlled
  - For example: 66.7%, 70.0%, 75.0%, 80.0%, 81.3%, 85.0%, 87.5%
  - Baud rates in the range of 10 kbps up to 1 Mbps can be configured
- Enhanced features:
  - Each message buffer can be configured to operate as a transmit or a receive message buffer
  - A transmission request can be aborted by clearing the Transmit-Request flag of the relevant message buffer. Supported by Transmission Abort Interrupt, on successful abortion.
  - Automatic block transmission operation mode (ABT)
  - Time stamp function in collaboration with timers capture channels
  - A centralized global data update bit monitor register makes it possible to check all data update bits from one location

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3.14 External MCU Interface

The external MCU interface is used to connect external MCUs. It functions both as an I/O port and an interface with external memory. The pin for the external MCU interface also functions for the external memory interface. The external MCU interface can be used when the high level is applied to the MEMIFSEL pin. After the power for the module is turned on, the level of the pin needs to be determined before the module is released from a reset state. This module does not support dynamic switching of levels.

3.14.1 Features

(1) External MCU interface

- Interface system
  - Asynchronous SRAM with wait control (for reading and writing)
  - Page ROM reading with wait control
- Synchronous relationship (set up with the HIFSYNC pin)
  - HBUSCLK synchronous mode (max. 50 MHz), asynchronous mode

Caution: Drive the HBUSCLK pin to low when asynchronous mode is to be used.

- Bus width (set up with the BUS32EN pin)
  - 32 bits / 16 bits

Remark: The module does not support 8-bit bus width.

- Transfer data size
  - 32 bits / 16 bits / 8 bits
- Buffers
  - Write buffer: Two stages (synchronous mode is selected) or one stage (asynchronous mode is selected)
  - Read buffer: Advance reading of up to 32 bytes is possible.
- Transfer type
  - Single transfer
  - Page read transfer
- Timing control function

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(2) AHB master port function

- AMBA Ver. 2.0 compliant
  - 32-bit AHB-Lite
  - Little endian fixed
- Address conversion
  - 4-Gbyte resource in the AHB memory area can be assigned as the area for the external MCU interface
- Bus sizing
  - External 16-bit => 32-bit
- Error response
  - Outputs an interrupt request HERROUTZ in response to reception of an error
  - Access information which involves the error source is stored in the register

(3) Status check function

- Check status of:
  - Internal reset (available in synchronous/asynchronous SRAM interface mode)
  - The HIFSYNC pin, the BUS32EN pin

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3.15 Asynchronous SRAM Memory Controller

The asynchronous SRAM memory controller is connectable to external paged ROM, ROM, and SRAM through a 16- or 32-bit bus. It is also connectable to peripheral devices compliant with the SRAM interface.
The pin functions for the asynchronous SRAM memory controller are multiplexed with those for the synchronous burst access memory controller and the external MCU interface, and the asynchronous controller can be used when the low level is applied to both the MEMCSEL and MEMIFSEL pins.
When both the BOOT0 and BOOT1 pins are at the low level, booting is from the memory connected to CSZ0.

3.15.1 Features

- Memory controller supporting page ROM, ROM, SRAM
- 32- or 16-bit data Bus
- Static memory control
  - SRAM and I/O connection
  - Page ROM connection (CSZ0 only)
  - Four chip select signals are available (CSZ0-CSZ3)

    CSZ0: page ROM / SRAM: 1000 0000H-13FF_FFFFH (64 Mbytes)
    CSZ1: SRAM only: 1400 0000H-17FF_FFFFH (64 Mbytes)
    CSZ2: SRAM only: 1800 0000H-1BFF_FFFFH (64 Mbytes)
    CSZ3: SRAM only: 1C00 0000H-1FFF_FFFFH (64 Mbytes)
- Programmable wait
  - Address setup wait
  - Data wait
  - Write recovery wait
  - Idle wait

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3.16 Synchronous Burst Access Memory Controller

The synchronous burst access memory controller can be used to connect external page ROM, ROM, SRAM, PSRAM, NOR-Flash, and peripheral devices with an interface similar to the SRAM interface via the 32/16-bit bus.
By setting the ADMUXMODE pin to high level, the address signals can be multiplexed to be output from data pins.
The synchronous burst access memory controller and asynchronous SRAM memory controller share external microcontroller interface pins. Using these pins for the synchronous burst access memory controller is selected when the MEMCSEL pin outputs a high level and the MEMIFSEL pin outputs a low level.
The CPU is booted from the memory connected to CSZ0 when the BOOT0 pin outputs a low level and the BOOT1 pin outputs a high level.

3.16.1 Features

- Memory controller supporting page ROM, ROM, SRAM (synchronous /asynchronous), PSRAM and NOR-Flash
- 32- or 16-bit data bus
- Address / data multiplex feature

Remark: Page access is possible only when performing asynchronous access in separate bus mode.

- Static memory control
  - External connection of SRAM (synchronous, asynchronous) and other peripheral devices with an interface similar to the SRAM interface
  - Four chip select signals are available (CSZ0-CSZ3)
    CSZ0: 1000 0000H-13FF_FFFFH (64 Mbytes)
    CSZ1: 1400 0000H-17FF_FFFFH (64 Mbytes)
    CSZ2: 1800 0000H-1BFF_FFFFH (64 Mbytes)
    CSZ3: 1C00 0000H-1FFF_FFFFH (64 Mbytes)

Remark: Chip select areas can be assigned to the area between addresses 1000_0000H – 1FFF_FFFFH by using the SMADSEL register (specified in 16-MB units).

- Programmable wait
- Memory access frequency (by dividing 100 MHz signal by 2 to 6)
- Up to four wait state signals available (WAITZ, WAITZ1 to WAITZ3)

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3.17 Instruction RAM

The instruction RAM is 768 Kbytes of memory that can be accessed from I-code AHB, D-code AHB, DMAC or an external MCU.

3.17.1 Features

- 128-bit (32-bit × 4) read buffer
- Latency: latency is 2 in read access in general but 1 in the case of hitting the read buffer.
  latency is 1 in write access.
- AHB bus width: 32 bits
- RAM data bus width: 128 bits (without ECC circuit)
- Transfer size: 16- or 32-bit transfer selectable
- Burst transfer: single burst transfer, burst transfer of the required length, burst transfer of the fixed length (INCR4/8/16, WRAP4/8/16)
- Little endian fixed
- ECC response: 1-bit error correction, 2-bit error detection

3.17.2 Read Buffer

- 128-bit (32bit × 4) read buffer
- Response to the AHB involves no waiting in the case of hitting the read buffer
- Clear the data in the read buffer when a 2-bit ECC error occurs.
- A 2-bit ECC error at the time of the read response generates an ECC error interrupt.

3.17.3 Write Interface

- When 16-bit write access arises, write to the RAM in 32-bit units through two consecutive rounds of access.
- When 8-bit write access arises, return an error response.

Caution: Write access by an external MCU in 16-bit units may occur. The specification assumes that such access to the RAM will always proceed two consecutive times (for the writing of data in 32-bit units).

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3.18 Data RAM

The internal data RAM is a 512-Kbyte RAM that can be accessed from the AHB and Header Endec (communication bus).

3.18.1 Features

- AHB latency: latency is 1 in read and write access (latency is 2 in read access following write access).
- Communication bus latency: latency is 1 in read and write access
- Arbitration of access when contention arises: Round robin
- AHB bus width: 32 bits
- Communication bus width: 128 bits
- RAM bus width: 128 bits (without ECC circuit)
- AHB transfer size: 8/16/ 32-bit selectable
- Communication bus transfer size: 8/16/32/128-bit selectable
- Burst transmission: single burst transfer, burst transfer of the required length, burst transfer of the fixed length (INCR4/8/16, WRAP4/8/16)
- Little endian fixed
- ECC response: 1-bit error correction, 2-bit error detection

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3.19 Buffer RAM

Buffer RAM is 64Kbyte of memory that can be accessed by the AHB and communication bus.

3.19.1 Features

- Communication-bus latency: latency is 1 in read and write access
- Arbitration of access when contention arises: Fixed priority (the communication bus is given priority)
- Communication bus width: 128 bits
- RAM bus width: 128 bits (without ECC circuit)
- Communication-bus transfer size: 8-, 16-, 32-, 128-bit transfer selectable
- ECC response: 1-bit error correction, 2-bit error detection

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3.20 Hardware Real-time OS

The Hardware Real-time OS supports 30 types of system-calls including event, semaphore and mailbox.

3.20.1 Outline of Features

-Task Scheduler

- Hardware ISR: 32 routines selectable from 128 interrupt sources
- Number of contexts elements: 64
- Number of semaphore identifiers: 128
- Number of event identifiers: 64
- Number of mailbox identifiers: 64
- Number of mailbox elements: 192
- Number of context priority levels: 16

-Hardware Function Manager

-Internal DMA

-Buffer allocator

-Header EnDec

Remark: The hardware real-time OS can be controlled by using the µITRON system calls provided by the sample driver. For how to use the driver, see the R-IN32M3 Series Programming Manual (OS).

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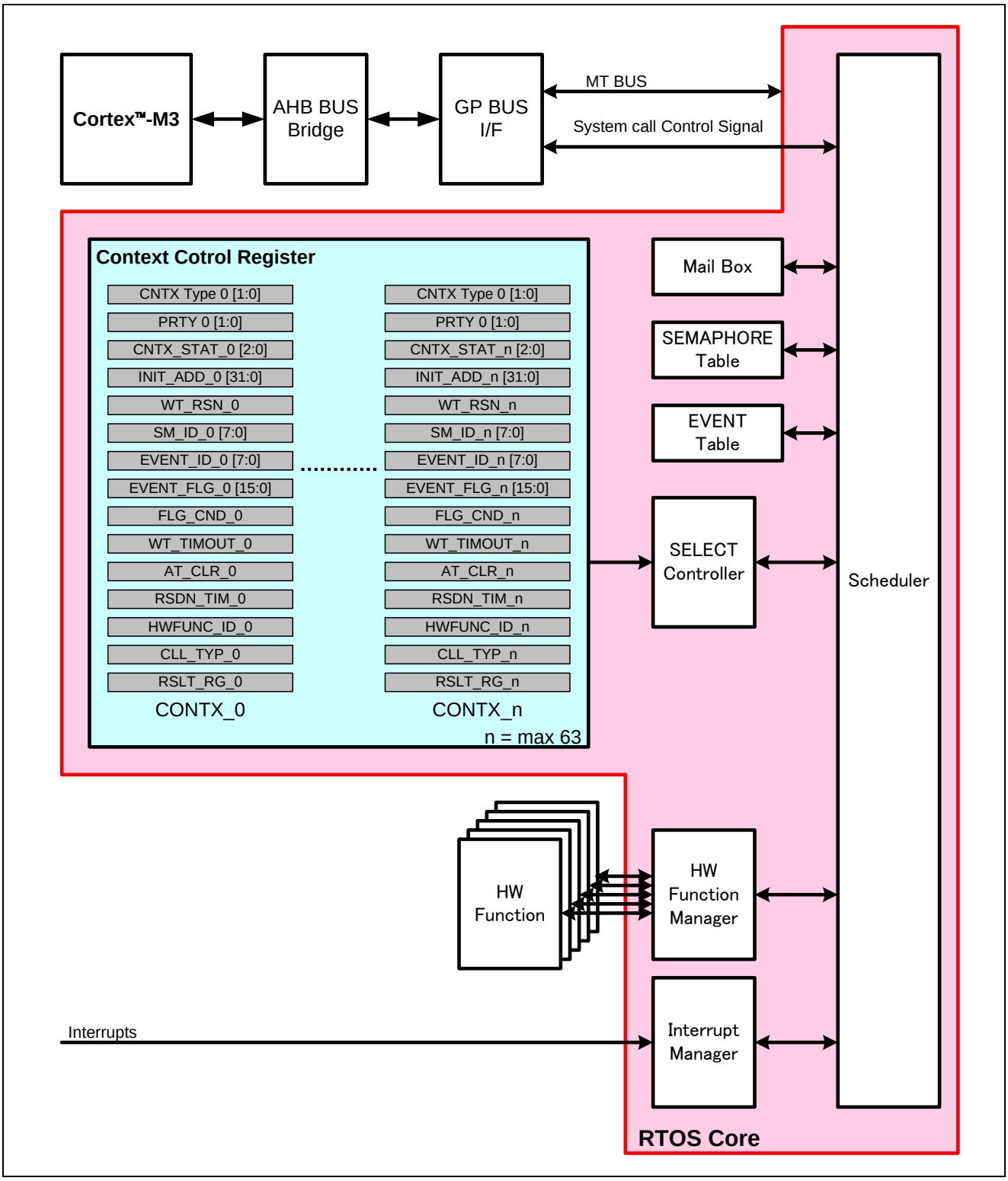


Figure 3.1 Structure of Hardware Real-time OS

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3.21 Port Functions

3.21.1 Features

- 96 I/O ports
- Shared with I/O ports of other peripheral circuits
- Ports can be designated as input or output on 1-bit basis

Cautions 1: Switching from a signal for a peripheral module that is multiplexed with a port pin to port mode might lead to a spike, depending on the state of the pin at the time.
The following general countermeasure for spikes should therefore be implemented in software.

- **Switch the pin function while the peripheral function is stopped.**
- **If the multiplexed pin function in use is an interrupt signal, clear the interrupt request flag and then remove masking of the interrupt.**
- **Only switch the mode after the output value is fixed.**

2: Do not externally apply an intermediate voltage to input buffers because these buffers do not implement through-current countermeasures.

3.21.2 Port Configuration

The R-IN32M3-EC incorporates eight 3-state I/O ports and four real-time control ports. Input or output mode can be specified for ports in 1-bit units. The basic structure of ports is the 8-bit unit, but ports P0x-P3x, P4x-P7x, and RP0x-RP3x (x = 0-7) can also be grouped to enable reading and writing in 32-bit units. The real-time port pins (RP00 to RP37) can be used for input and output in synchronization with interrupt signals.
Each port allows access in 8-, 16-, or 32-bit access depending on the setting of the corresponding register.

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4. Electrical Specifications

4.1 Terminology

Table 4.1 Terms Used in Absolute Maximum Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}	Indicates the voltage range within which damage or reduced reliability will not result when power is applied to a V_{DD} pin.
Input voltage	V_I	Indicates the voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V_O	Indicates the voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Output current	I_O	Indicates the absolute tolerance value for DC current to prevent damage or reduced reliability when a current flows out of or into an output pin.
Operating ambient temperature	T_A	Indicates the ambient temperature range for normal logic operations.
Storage temperature	T_{stg}	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current is being applied to the device.

Table 4.2 Terms Used in Recommended Operating Range Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}	Indicates the voltage range for normal logic operations that occur when V_{SS} = 0 V.
Input voltage, high	V_{IH}	Indicates the voltage, which is applied to the input pins of R-IN32M3, is the voltage indicates that the high level state for normal operation of the input buffer. -If a voltage that is equal to or greater than the “Min.” value is applied, the input voltage is guaranteed as a high level voltage.
Input voltage, low	V_{IL}	Indicates the voltage, which is applied to the input pins of R-IN32M3, is the voltage indicates that the low level state for normal operation of the input buffer. -If a voltage that is equal to or less than the “Max.” value is applied, the input voltage is guaranteed as a low level voltage.
Positive trigger voltage	V_P	Indicates the input level at which the output level is inverted when the input to R-IN32M3 is changed from the low-level side to the high-level side.
Negative trigger voltage	V_N	Indicates the input level at which the output level is inverted when the input to R-IN32M3 is changed from the high-level side to the low-level side.
Hysteresis Voltage	V_H	Indicates the differential between the positive trigger voltage and the negative trigger voltage.
Input rise time	t_{ried}, t_{ric}, t_{ris}	Indicates the limit value for the time period when an input voltage applied to R-IN32M3 rises from 10% to 90%. t_{ried}, t_{ric}, and t_{ris} each indicate the input rise time for the data clock and Schmitt buffer.
Input fall time	t_{fid}, t_{fic}, t_{fis}	Indicates the limit value for the time period when an input voltage applied to R-IN32M3 falls from 90% to 10%. t_{fid}, t_{fic}, and t_{fis} each indicate the input fall time for the data clock and Schmitt buffer.

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Table 4.3 Terms Used for DC Characteristics

Parameter	Symbol	Meaning
Off-state output current	I_{OZ}	Indicates the current that flows from the power supply pins when the rated power supply voltage is applied when a 3-state output has high impedance.
Output short circuit current	I_{OS}	Indicates the current that flows when the output pins are shorted (to GND pins) when output is at high level.
Input leakage current	I_{LI}	Indicates the current that flows via an input pin when a voltage is applied to that pin.
Output current, low	I_{OL}	Indicates the current that flows to the output pins when the rated low-level output voltage is being applied.
Output current, high	I_{OH}	Indicates the current that flows from the output pins when the rated high-level output voltage is being applied.
Output voltage, low	V_{OL}	Indicates the output voltage at low level and when the output pin is open.
Output voltage, high	V_{OH}	Indicates the output voltage at high level and when the output pin is open.

4.2 Absolute Maximum Ratings

Table4.4 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}	1.0V type	-0.5 to +1.4	V
		1.5 V type	-0.5 to +2.0	V
		3.3 V type	-0.5 to +4.6	V
I/O voltage	V_I /V_O	3.3 V buffer V_I /V_O < V_{DD} + 0.5V	-0.5 to +4.6	V
		5V-Tolerant buffer V_I /V_O < V_{DD} + 3.0V	-0.5 to +6.6	V
Output current (3.3 V buffer)	I_O	6 mA type	15	mA
		12 mA type	25	mA
Output current (5V-Tolerant buffer)	I_O	4 mA type	10.35	mA
Operating ambient temperature	T_A	-	-40 to +85	°C
Storage temperature	T_{stg}	-	-65 to +125	°C

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark: 3.3 V must be applied to the I/O pins only after applying the power supply voltage.

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4.3 Recommended Operating Conditions

Table 4.5 Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD}	1.0 V power supply	0.9	1.0	1.1	V
		1.5 V power supply	1.35	1.5	1.65	V
		3.3 V power supply	3.0	3.3	3.6	V
Negative trigger voltage	V_N	3.3 V buffer	0.6	-	1.8	V
		5 V tolerant buffer	0.8	-	1.1	V
Positive trigger voltage	V_P	3.3 V buffer	1.2	-	2.4	V
		5 V tolerant buffer	1.7	-	2.2	V
Hysteresis voltage	V_H	3.3 V buffer	0.3	-	1.5	V
		5 V tolerant buffer	0.9	-	1.1	V
Input voltage, low	V_{IL}	3.3 V buffer	-0.3	-	0.8	V
		5 V tolerant buffer	0	-	0.8	V
Input voltage, high	V_{IH}	3.3 V buffer	2.0	-	V_{DD} + 0.3	V
		5 V tolerant buffer	2.0	-	5.5	V
Input rise/fall time	t_{ried}	-	0	-	200	ns
	t_{fid}	-	0	-	200	ns
Input rise/fall time (clock)	t_{ric}	-	0	-	4	ns
	t_{fic}	-	0	-	4	ns
Input rise/fall time (Schmitt input)	t_{ris}	-	0	-	1	ms
	t_{fis}	-	0	-	1	ms
Operating ambient temperature	T_A	-	-40	-	85	°C

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4.4 DC Characteristics

Table 4.6 DC Characteristics (V_{DD} = 3.3 ± 0.3 V, T_A = –40 to +85° C) (1/2)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current (R-IN32M3-EC)	I_{DD}	V_I = V_{DD} or GND	With an internal regulator		-	-	-	-
				1.0V	-	270	880	mA
				3.3 V	-	210	220	mA
			Without an internal regulator		-	-	-	-
				1.0V		270	880	mA
				3.3 V		120	130	mA
				1.5V	-	150	170	mA
Supply current (R-IN32M3-CL)	I_{DD}	V_I = V_{DD} or GND	1.0V		-	280	890	mA
			3.3 V		-	45	50	mA
Off-state current	I_{OZ}	V_I = V_{DD} or GND	3.3 V output		-	-	±10	μA
			5V-tolerant buffer		-	-	±10	μA
Output short circuit current Note	I_{OS}	V_O = GND	-		-	-	-250	mA
Input leakage current (3.3 V buffer)	I_I	V_I = V_{DD} or GND	Normal input		-	-	±10	μA
		V_I = GND	With pull-up resistor (50kΩ)		-28.9	-65.7	-129.8	μA
		V_I = V_{DD}	With pull-down resistor (50kΩ)		10.2	43.4	83.9	μA
Input leakage current (5V-tolerant buffer)	I_I	V_I = GND	With pull-up resistor (50kΩ)		39.0	-	100.9	μA

Note: The output short circuit time is no more than one second and is only for one pin on the LSI.

Remark: In the notes for the table, the (+) and (–) signs indicate the current direction. Current flowing to the device is indicated by (+) and current flowing out is indicated by (–).

Table 4.7 DC Characteristics (V_{DD} = 3.3 ± 0.3 V, T_A = –40 to +85°C) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low (3.3 V buffer)	I_{OL}	V_{OL} = 0.4V	6 mA type	6.0	-	-	mA
			12 mA type	12.0	-	-	mA
Output current, low (5V-Tolerant buffer)	I_{OL}	V_{OL} = 0.4V	4 mA type	4.0	-	-	mA
Output current, high (3.3 V buffer)	I_{OH}	V_{OH} = 2.4V	6 mA type	-6.0	-	-	mA
			12 mA type	-12.0	-	-	mA
Output current, high (5V-Tolerant buffer)	I_{OH}	V_{OH} = 2.4V	4 mA type	-4.0	-	-	mA
Output voltage, low	V_{OL}	I_{OL} = 0 mA	3.3 V buffer	-	-	0.1	V
			5V-Tolerant buffer	-	-	0.1	V
Output voltage, high	V_{OH}	I_{OH} = 0 mA	3.3 V buffer	VDD – 0.1	-	-	V
			5V-Tolerant buffer	VDD – 0.1	-	-	V

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4.5 Pull-up/Pull-down Resistor Values

Table 4.8 Pull-up/Pull-down Resistor Values (V_{DD} = 3.3 ± 0.3 V, T_A = –40 to +85°C)

Parameter	Library Specification	MIN.	TYP.	MAX.	Unit
Pull-up resistor (3.3 V buffer)	50kΩ	27.7	50.2	103.9	kΩ
Pull-up resistor (5V-Tolerant buffer)	50kΩ	35.7	51.2	77.0	kΩ
Pull-down resistor (3.3 V buffer)	50kΩ	42.9	76.1	295.5	kΩ

4.6 Terminal Capacity Values

Table 4.9 Terminal Capacity Values

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Input Buffer	C_B	5.0	-	7.0	pF
Output Buffer		5.0	-	7.0	pF
I/O Buffer		5.0	-	7.0	pF

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4.7 Power-on/off sequence

The power circuit for the R-IN32M3 products consists of an internal power supply (VDD10: 1.0V), I/O power supply (VDD33: 3.3 V) and PHY power supply (VDD15: 1.5V). (PHY power only applies to R-IN32M3-EC.)

Supply power to the internal circuit then to the I/O circuit. Conversely, cut-off power to the I/O circuit then internal circuit. This is not a stipulated sequence for power supply (See Figure 4.1).

If power to the I/O circuit is supplied before power to the internal circuit is supplied, the mode of the I/O buffer will not be determined until the internal circuit starts up and thus the output values become unstable regardless of the mode of the buffer. Also, be sure to apply 3.3 V to the I/O pins after the power supply voltage has been decided.

Regardless of the power on/off sequence, the time difference between the startup of the first module and the levels of both modules having been stabilized should fall within 100 ms. Here, the time to be measured is when the voltage of each module is at 0.1 V_{DD} to 0.9 V_{DD}.

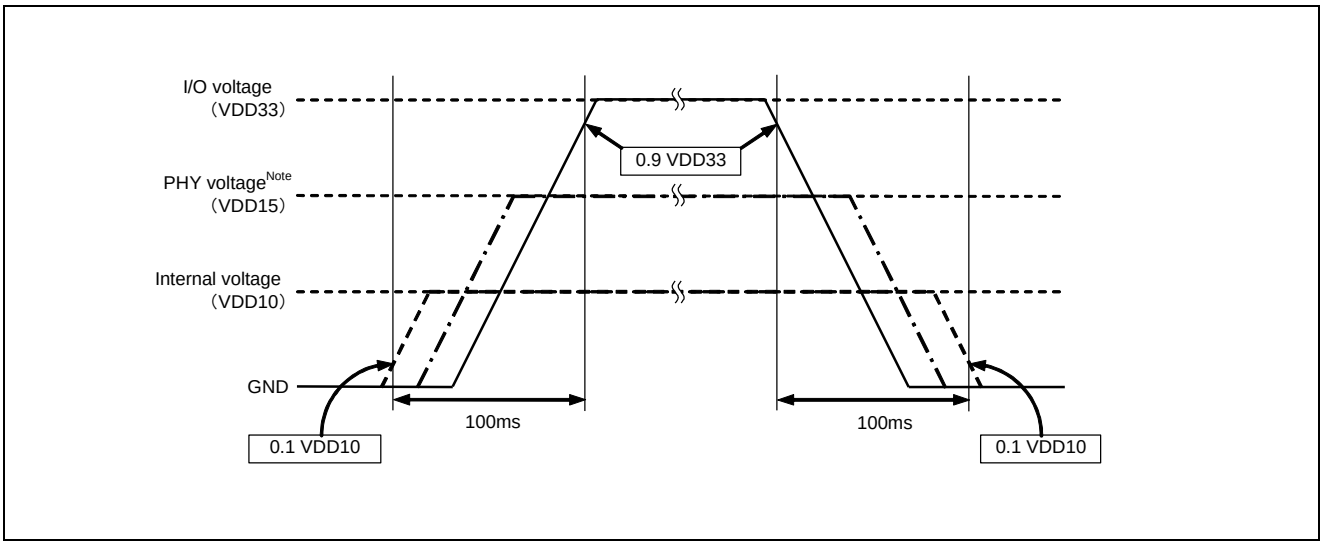


Figure 4.1 Recommended Sequence of Power-on/off

Note: The recommendation for time difference should also be applied to the PHY module only when a build-in regulator of an R-IN32M3-EC is not in use.

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4.8 AC Characteristics

4.8.1 Clock Pins

(1) Input clock

Parameter	Symbol	Conditions	MIN	MAX	Unit
XT1, XT2	t_{SYSCLK}	-	25 ± 50ppm		MHz
ETH0_TXC, ETH1_TXC Note	t_{TXC}	-	-	25	MHz
ETH0_RXC, ETH1_RXC Note	t_{RXC}	-	-	125	MHz
CCM_CLK80M	t_{CCLCLK}	-	80 ± 50ppm		MHz
CCI_CLK2_097M Note	$t_{CCLIECLK}$	-	2.097152 ± 100ppm		MHz
HBUSCLK	$t_{HBUSCLK}$	-	-	50	MHz
CSISCK0, CSISCK1	$t_{CSISSCK}$	Slave mode	-	16.6	MHz
TCK	t_{TCK}	-	-	50.	MHz

Note: This applies to R-IN32M3-CL only.

(2) Output clock

Parameter	Symbol	Conditions	MIN	MAX	Unit
BUSCLK output cycle	t_{BUSCLK}	C_L = 15pF	10	-	ns
BUSCLK high level width	t_{BCKH}		0.5 × t_{BUSCLK} – 2.0	0.5 × t_{BUSCLK} + 2.0	ns
BUSCLK low level width	t_{BCKL}		0.5 × t_{BUSCLK} – 2.0	0.5 × t_{BUSCLK} + 2.0	ns
BUSCLK rising time	t_{BCKR}		-	1.2	ns
BUSCLK falling time	t_{BCKF}		-	1.2	ns
CLKOUT25Mn Note1 output cycle	t_{CO25M}	C_L = 15pF	40	-	ns
CLKOUT25Mn Note1 high level width	t_{CO25MH}		0.5 × t_{BUSCLK} – 5.3	0.5 × t_{BUSCLK} + 5.3	ns
CLKOUT25Mn Note1 low level width	t_{CO25ML}		0.5 × t_{BUSCLK} – 5.3	0.5 × t_{BUSCLK} + 5.3	ns
CLKOUT25Mn Note1 rise time	t_{CO25MR}		-	3.4	ns
CLKOUT25Mn Note1 fall time	t_{CO25MF}		-	3.4	ns
ETHn_GTXC Note1 output frequency	t_{GTXC}	C_L = 13pF	-	125	MHz
CSISCKn output frequency	$t_{CSIMSCK}$	Master mode C_L = 15pF	-	25	MHz
SCLn output frequency	t_{SCL}	High speed mode C_L = 30pF	-	400	KHz
SMSCK output frequency	t_{SMSCK}	C_L = 15pF	-	50	MHz
CATI2CCLK Note2 output frequency	$t_{ECIICCLK}$	C_L = 30pF	-	148.8	kHz
TRACECLK output frequency	$t_{TRACECLK}$	C_L = 15pF	-	50	MHz

Notes 1. Only applies to R-IN32M3-CL.
2. Only applies to R-IN32M3-EC.

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Remark: n = 0 or1

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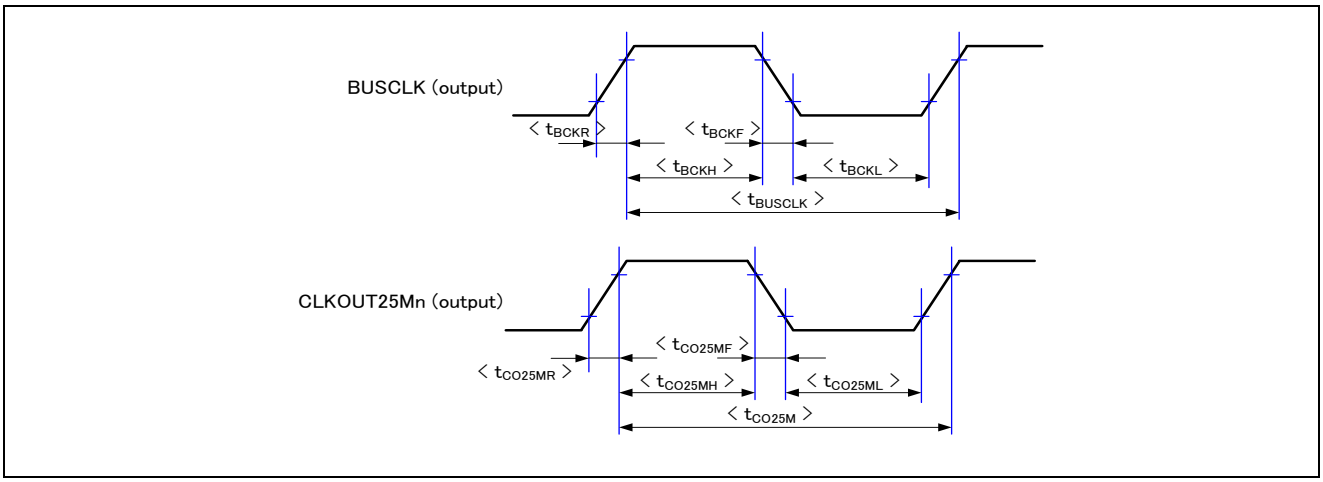


Figure 4.2 Output Clock Timing Diagram

Remarks 1: For the output timing of other clocks, see the sections of AC characteristics for the individual interfaces.

2: n = 0, 1

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4.8.2 Reset Pins

Parameter	Symbol	Conditions	MIN	MAX	Unit
RESETZ low level width	t_{WRSL}	-	Secure enough time for the external oscillator to be stabilized + 1 μsec.	-	ns
HOTRESETZ Note low level width	t_{WHRSL}	-		-	ns
PONRZ low level width	t_{WPRSL}	-		-	ns
PONRZ input timing (to RESETZ↑)	t_{SKPR}	-	0	-	ns

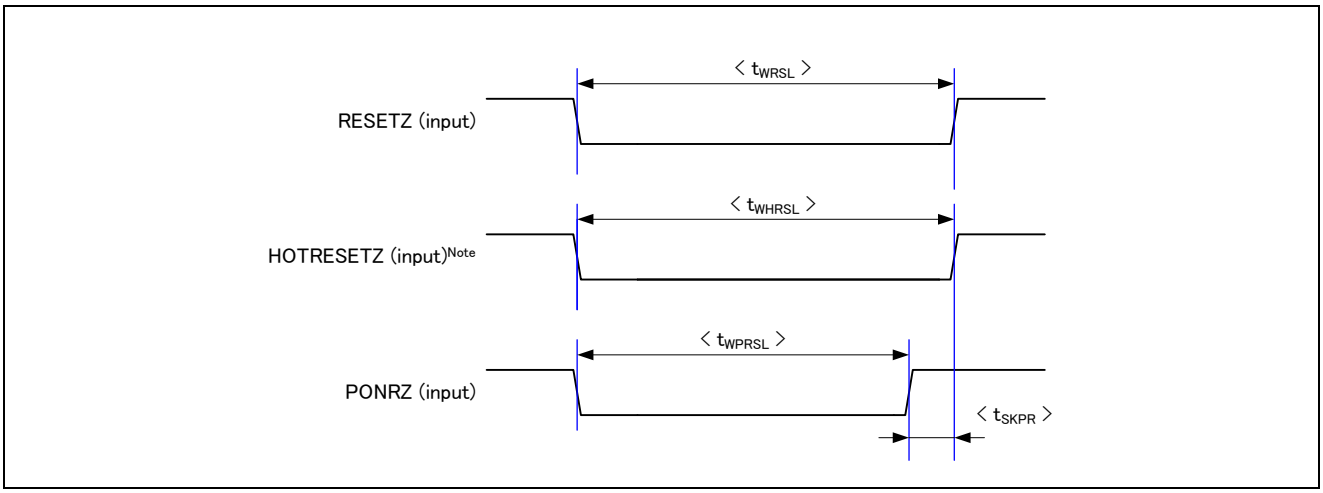


Figure 4.3 Reset Timing Diagram

Note: Only applies to R-IN32M3-CL.

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4.8.3 External Memory Interface Pins

(1) Calculating value for delay due to an external load

The values for transition delay of the external memory interface pins of the R-IN32M3 products do not consider external load on them because it depends on the user environment. Calculate the value for delay in consideration with the load under your environment and also with wiring delays on the printed board.

Drive capability	Delay value per pF (ns)	
	MIN.	MAX.
6 mA	0.026	0.067
12 mA	0.012	0.034

Example)

When an address pin (6- mA output buffer) has 30-pF load, the actual delay is as follows.

MIN.: 1.0 ns (The MIN delay value at the time of 0 pF) + (0.026×30) ns = 1.78ns
MAX.: 7.0 ns (The MAX delay value at the time of 0 pF) + (0.067×30) ns = 9.01ns

(2) Asynchronous SRAM MEMC access timing

Parameter	Symbol	MIN	MAX	Unit
Address, CSZ0-CSZ3 output delay time (from BUSCLK↑)	t_{DKA}	1.0 (1.78) Note	7.0 (9.01) Note	ns
RDZ output delay time (from BUSCLK↑)	t_{DKRD}	1.0 (1.78) Note	7.0 (9.01) Note	ns
WRZ0 – WRZ3 (BENZ0-BENZ3), WRSTBZ output delay time (from BUSCLK↑)	t_{DKWR}	1.0 (1.78) Note	7.0 (9.01) Note	ns
BCYSTZ output delay time (from BUSCLK↑)	t_{DKBSL}	1.0 (1.78) Note	7.0 (9.01) Note	ns
WAITZ input setup time (to BUSCLK↓)	t_{SKW}	4.0	-	ns
WAITZ input hold time (to BUSCLK↓)	t_{HKW}	0	-	ns
Date input setup time (from BUSCLK↑)	t_{SKID}	4.0	-	ns
Data input hold time (from BUSCLK↑)	t_{HKID}	0	-	ns
Date output delay time (from BUSCLK↑)	t_{DKOD}	1.0 (1.78) Note	7.0 (9.01) Note	ns
Data float delay time (from BUSCLK↑)	t_{HKOD}	1.0 (1.78) Note	7.0 (9.01) Note	ns

Note: Values in parenthesis are based on a 30pF capacitive load.

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(a) Read timing

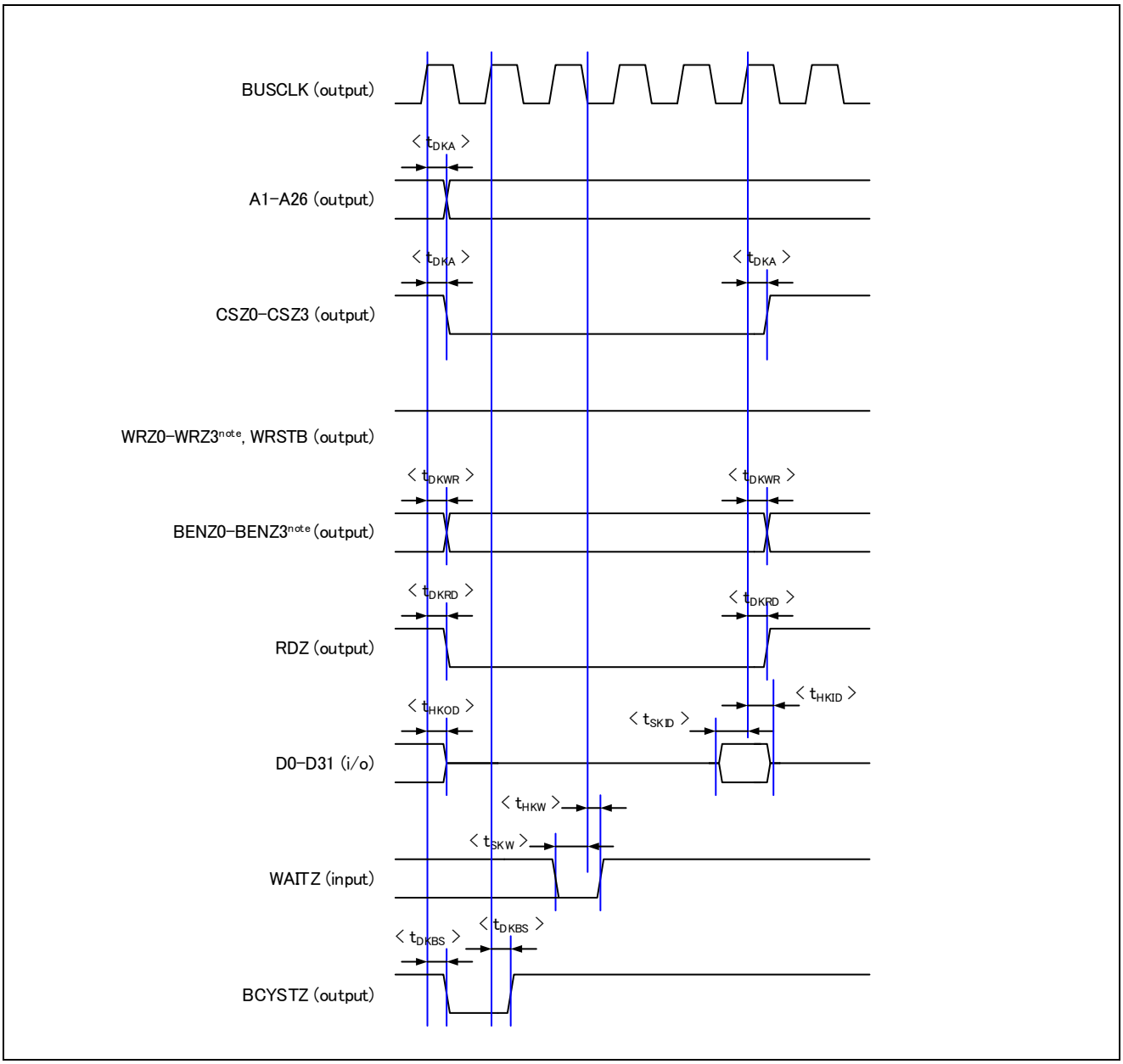


Figure 4.4 Memory Controller Read Timing Diagram (Asynchronous Memory)

Note: The WRZ0-WRZ3 pins function both as WRZ0-WRZ3 and BENZ0-BENZ3. These pins function as BENZ0-BENZ3 after a reset and can be switched with the write enable switch registers (WREN). For details, see section 9.3.5, Write Enable Switch Registers (WREN), in the R-IN32M3 Series User's Manual: Peripheral Modules.

Remark: Above timing shows the case for when "Idle Wait", "Write Recovery Wait", and "Address Wait" are set to 0, and "Data Wait" is set to 3.

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(b) Write timing

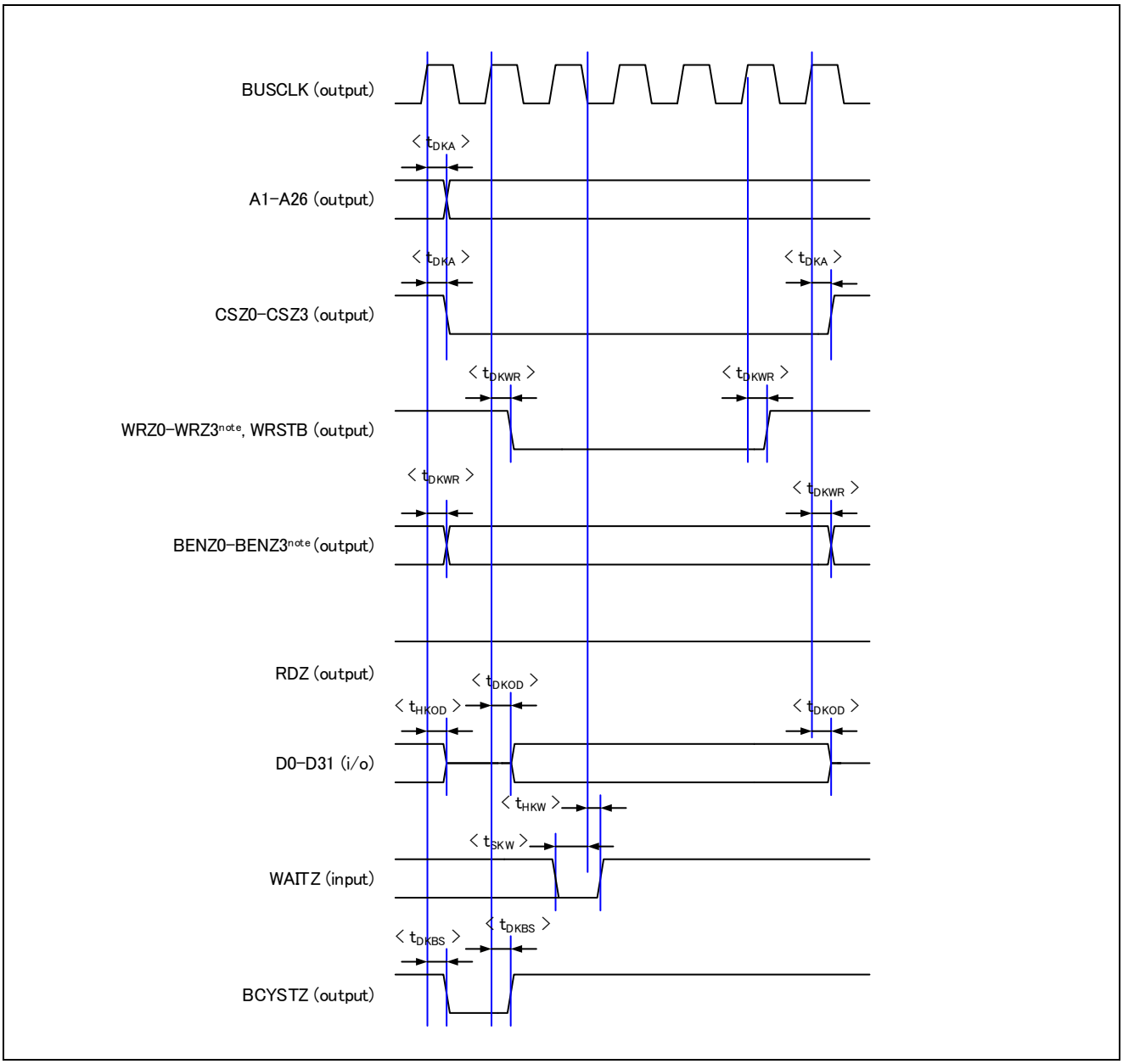


Figure 4.5 Memory Controller Read Timing Diagram (Asynchronous Memory)

Note: The WRZ0-WRZ3 pins function both as WRZ0-WRZ3 and BENZ0-BENZ3. These pins function as BENZ0-BENZ3 after a reset and can be switched with the write enable switch registers (WREN). For details, see section 9.3.5, Write Enable Switch Registers (WREN), in the R-IN32M3 Series User's Manual: Peripheral Modules.

Remark: Above timing shows the case for when "Idle Wait", "Write Recovery Wait", and "Address Wait" are set to 0, and "Data Wait" is set to 3.

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(3) Synchronous burst access MEMC access timing

Parameter	Symbol	MIN	MAX	Unit
BUSCLK output frequency	t_{BUSCLK}	-	50	MHz
Address, CSZ0-CSZ3 output delay time	t_{DKA}	1.0 (1.78) Note	7.8 (9.81) Note	ns
RDZ output delay time	t_{DKRD}	1.0 (1.78) Note	7.8 (9.81) Note	ns
WRZ0-WRZ3 (BENZ0-BENZ3), WRSTBZ output delay time	t_{DKWR}	1.0 (1.78) Note	7.8 (9.81) Note	ns
ADVZ output delay time	t_{DKBSL}	1.0 (1.78) Note	7.8 (9.81) Note	ns
WAITZ input setup time	t_{SKW}	5.3	-	ns
WAITZ input hold time	t_{HKW}	0	-	ns
Data input setup time	t_{SKID}	5.3	-	ns
Data input hold time	t_{HKID}	0	-	ns
Data output delay time	t_{DKOD}	1.0 (1.78) Note	7.8 (9.81) Note	ns
Data float delay time	t_{HKOD}	1.0 (1.78) Note	7.8 (9.81) Note	ns

Note: Values in parenthesis are based on a 30pF capacitive load.

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(a) Read timing

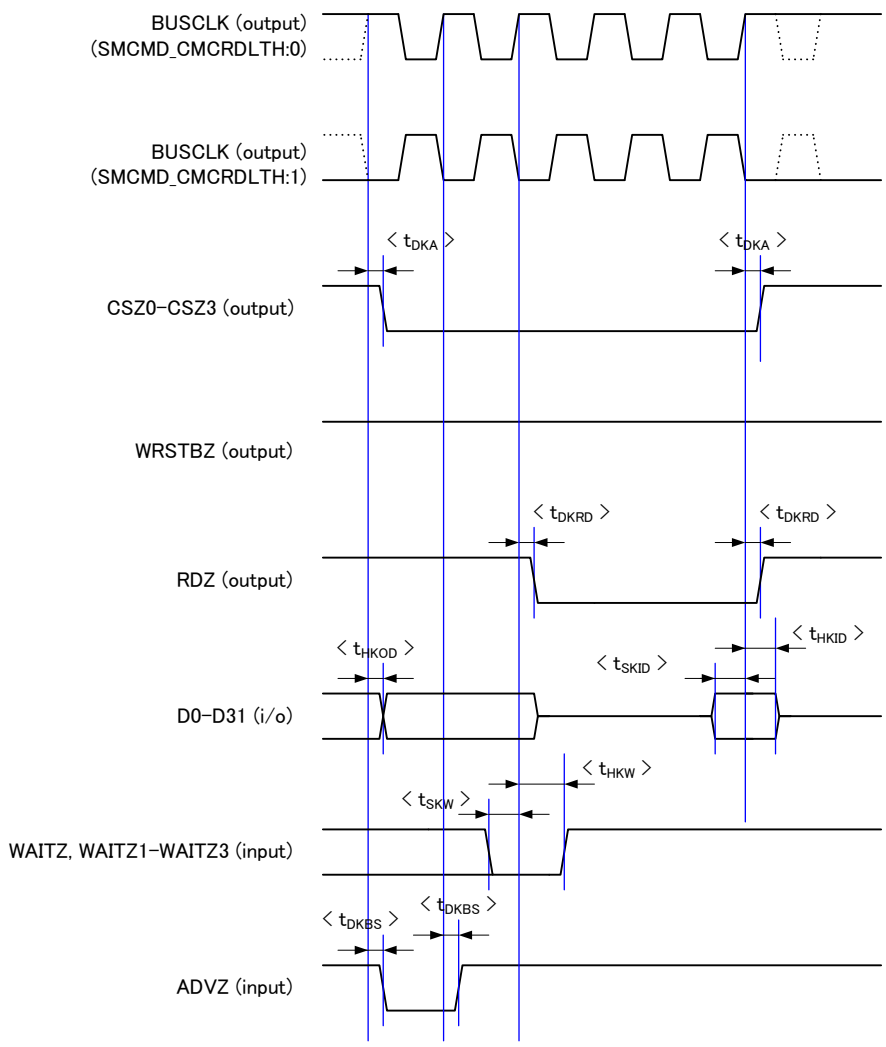


Figure 4.6 Memory Controller Read Timing Diagram (Synchronous Memory)

Remark: Above timing is for the case where “t_ceoe” is 2 and “t_rc” is 4.

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(b) Write timing

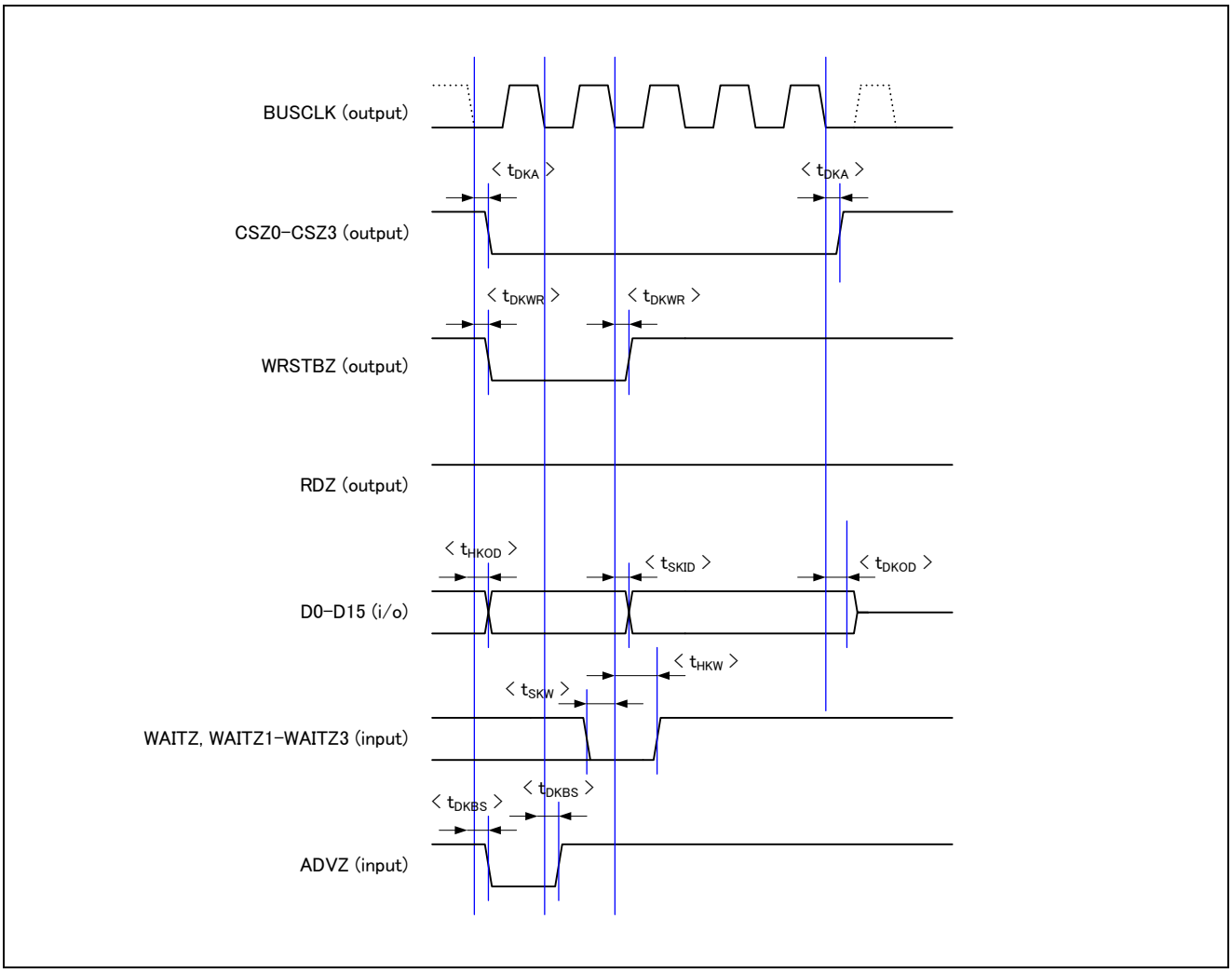


Figure 4.7 Memory Controller Write Timing Diagram (Synchronous Memory)

Remark: Above timing is for the case where “t_wp” is 2 and “t_wc” is 5.

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4.8.4 External MCU Interface Pins

The timing specification of external MCU interface pins are based on a 65pF (HD pins) and 35pF (HWAITZ pin) capacitive load.

(1) Synchronous Mode

(1/2)

No.	Parameter	Symbol	MIN	MAX	Unit
1	HBUSCLK high-level width	t_{HBHIGH}	$0.5t_{HBUSCLK}$ – 2.1	$0.5t_{HBUSCLK}$ + 2.1	ns
2	HBUSCLK low-level width	t_{HBLOW}	$0.5t_{HBUSCLK}$ – 2.1	$0.5t_{HBUSCLK}$ + 2.1	ns
3	HBUSCLK input cycle	$t_{HBUSCLK}$	20	-	ns
4	Address, HCSZ/HPGCSZ input setup time (to HBUSCLK↑)	t_{SKHA}	4.0	-	ns
5	HBENZ0-HBENZ3 (HWRZ0-HWRZ3), HWRSTBZ input setup time (to HBUSCLK↑)	t_{SKHWR}	4.0	-	ns
6	Address, HCSZ/HPGCSZ input hold time (from HBUSCLK↑)	t_{HKHA}	1.0	-	ns
7	HBENZ0-HBENZ3 (HWRZ0-HWRZ3), HWRSTBZ input hold time (from HBUSCLK↑)	t_{HKHWR}	1.0	-	ns
8	HWRZ0-HWRZ3, HWRSTBZ recovery time (high width)	t_{WHWR}	35.0	-	ns
9	Data input setup time (to HBUSCLK↑)	t_{SKIHD}	4.0	-	ns
10	Data input hold time (from HBUSCLK↑)	t_{HKIHD}	1.0	-	ns
11	HWAITZ output delay time (from HCSZ, HPGCSZ↓)	t_{DKHD}	2.0	-	ns
12	HWAITZ output delay time (from HWRSTBZ, HWRZ0-HWRZ3↓)	t_{DKHWT}	2.0	-	ns
13	HWAITZ enable data output delay time (from HBUSCLK↑)	t_{DKHWTV}	2.0	10.0	ns
14	HWAITZ enable data hold time (from HWRSTBZ, HWRZ0-HWRZ3↑)	t_{HKHWTV}	3.0	-	ns
15	HWAITZ output hold time (from HWRSTBZ, HWRZ0-HWRZ3↑)	t_{HKWTWR}	-	13.6	ns
16	Data, HWAITZ output hold time (from HCSZ/HPGCSZ↑)	t_{HKWTCS}	-	13.6	ns
17	Address, HCSZ/HPGCSZ input setup time (to HRDZ↓)	t_{SKHAHR}	4.3	-	ns
18	Data at the page access, Address input hold time (from HRDZ↑)	t_{HKHAHR}	4.3	-	ns
19	HRDZ recovery time (high width)	t_{WHRD}	35.0	-	ns
20	Data, HWAITZ output delay time (from HRDZ↓)	t_{DKHDHR}	2.0	-	ns
21	HWAITZ enable data output delay time (from HRDZ↓)	$t_{DKWTVHR}$	-	16.4	ns

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(2/2)

No.	Parameter	Symbol	MIN	MAX	Unit
22	Data settle time (from HWAITZ↑)	$t_{SKHDHWT}$	$t_{HBUSCLK}$ – 10	-	ns
23	Data, HWAITZ enable data output hold time (from HRDZ↑)	$t_{HKHWTHR}$	3.0	-	ns
24	Data, HWAITZ output hold time (from HRDZ↑)	t_{HKOHD}	-	13.6	ns
25	Data at the on-page access, HWAITZ output delay time (from the address)	t_{DKPON}	3.0	16.4	ns
26	Data at the off-page access, HWAITZ output delay time (from the address)	t_{DKPOFF}	3.0	16.4	ns
27	HWAITZ enable data output delay time (from HCSZ/HPGCSZ↓)	$t_{DKWTVCS}$	-	16.4	ns
28	HRDZ input setup time (to HBUSCLK↑)	t_{SKHRD}	4.0	-	ns
29	HRDZ input hold time (to HBUSCLK↑)	t_{HKHRD}	1.0	-	ns

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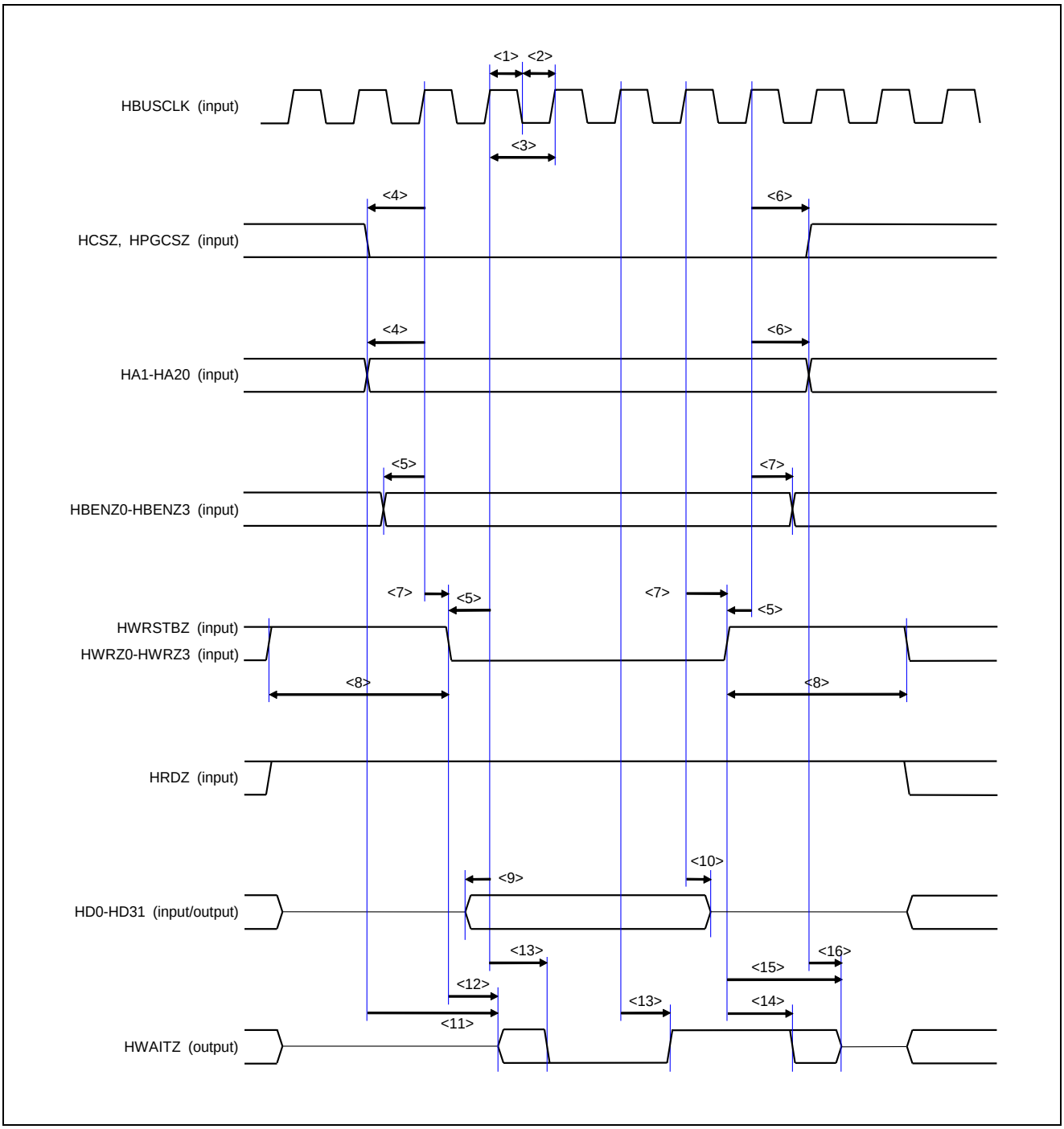


Figure 4.8 External MCU Write Timing (MEMCSEL = L, HIFSYNC = H)

Caution: Supply a stable signal to address/data/control system pins while being accessed.

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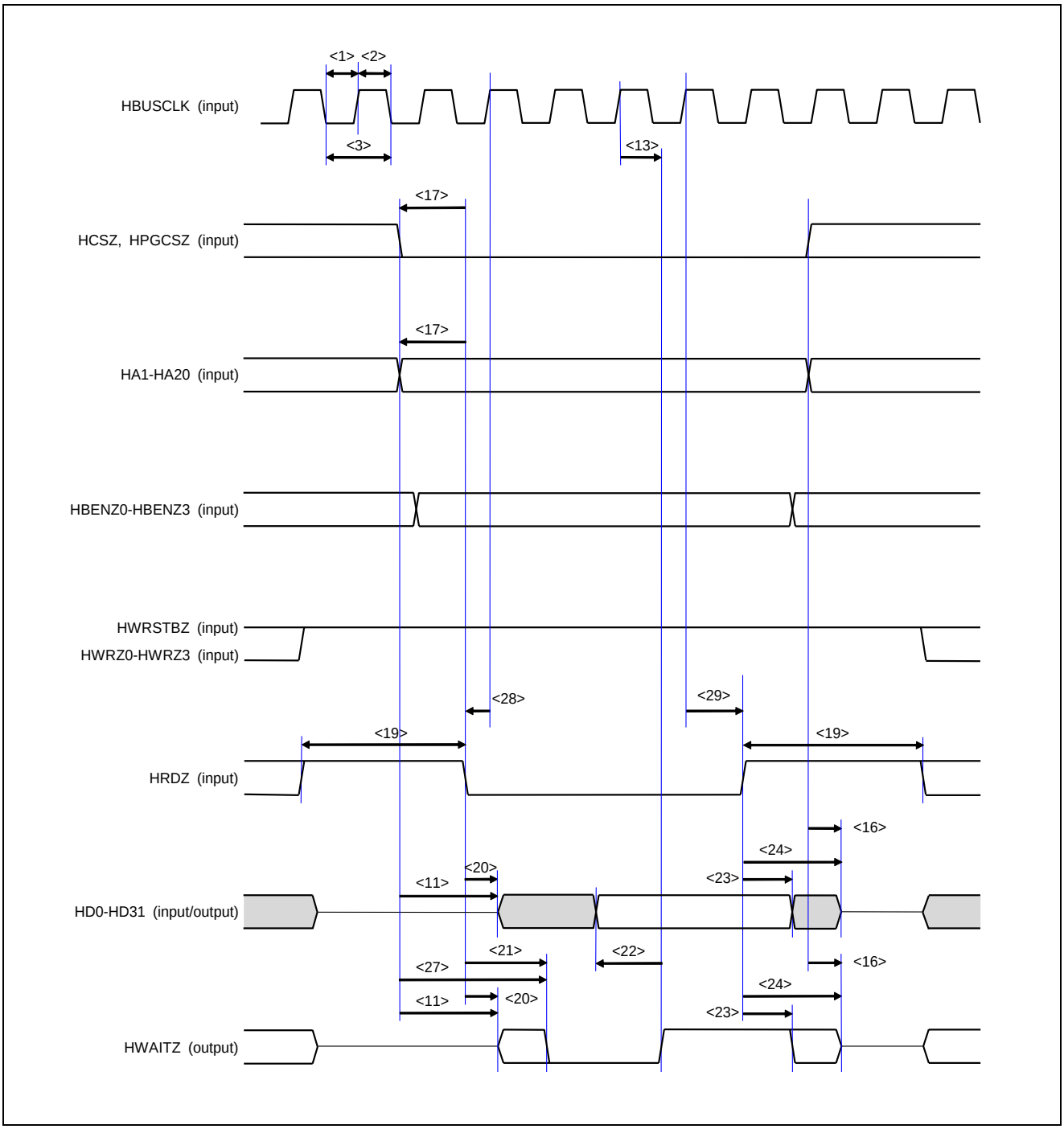


Figure 4.9 External MCU Read Timing (MEMCSEL = L, HIFSYNC = H)

Caution: Supply a stable signal to address/data/control system pins while being accessed.

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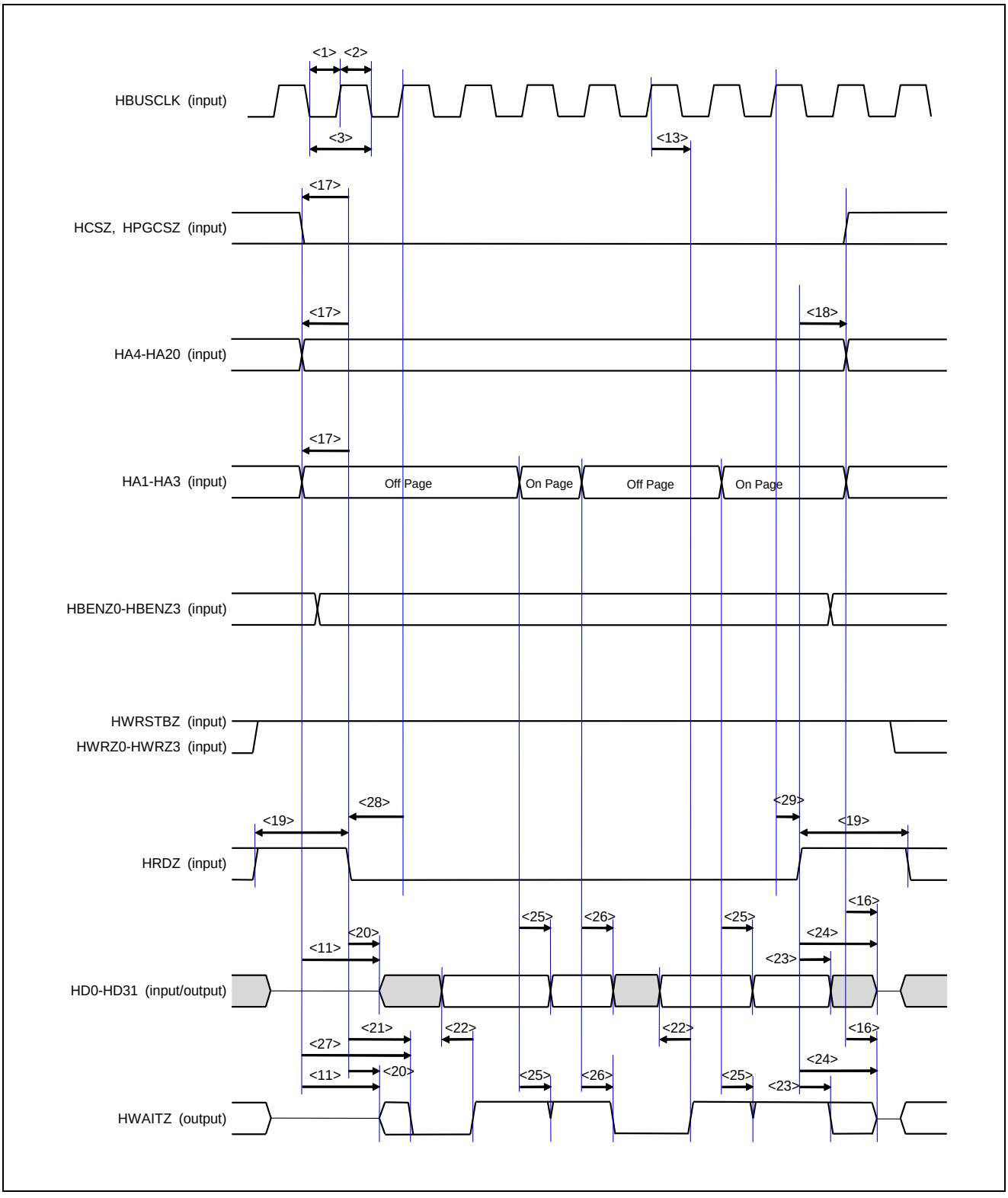


Figure 4.10 External MCU Page Read Timing (MEMCSEL = L, HIFSYNC = H)

Caution: Supply a stable signal to address/data/control system pins while being accessed.

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(2) Synchronous Mode (CC-Link IE Field)

No.	Parameter	Symbol	MIN	MAX	Unit
1	HBUSCLK high-level width	t_{HBHIGH}	$0.5t_{HBUSCLK}$-2.1	$0.5t_{HBUSCLK}$+2.1	ns
2	HBUSCLK low-level width	t_{HBLOW}	$0.5t_{HBUSCLK}$-2.1	$0.5t_{HBUSCLK}$+2.1	ns
3	HBUSCLK input cycle	$t_{HBUSCLK}$	20	-	ns
4	Address, HCSZ/HPGCSZ input setup time (to HBUSCLK↓)	t_{SKHCS}	5.0	-	ns
5	HBENZ0-HBENZ3 (HWRZ0-HWRZ3), HWRSTBZ input setup time (to HBUSCLK↓)	t_{SKHWR}	5.0	-	ns
6	Address, HCSZ/HPGCSZ, HBENZ0-HBENZ3, Data input hold time (from HRDZ, HWRSTBZ, HWRZ0-HWRZ3↑)	t_{HKHA}	0	-	ns
7	HWRZ0-HWRZ3, HWRSTBZ recovery time (high width)	t_{WHWR}	$t_{HBUSCLK}$ x 1	-	ns
8	Data input setup time (to HWRSTBZ, HWRZ0- HWRZ3↓)	t_{SKIHD}	0	-	ns
9	HWAITZ output delay time (from HCSZ, HPGCSZ↓)	t_{DKHD}	2.0	-	ns
10	HWAITZ output delay time (from HWRSTBZ, HWRZ0 – HWRZ3↓)	t_{DKHWT}	2.0	-	ns
11	HWAITZ enable data output delay time (from HBUSCLK↑) “HWAITZ output in synchronization with HBUSCLK↑”	t_{DKHWTV}	3.0	11.0	ns
	HWAITZ enable data output delay time (from HBUSCLK↓) “HWAITZ output in synchronization with HBUSCLK↓”	t_{DKHWTV}	3.0	11.0	ns
12	HWAITZ enable data output hold time (from HWRSTBZ, HWRZ0-HWRZ3↑)	t_{HKHWTV}	3.0	-	ns
13	HWAITZ output hold time (from HWRSTBZ, HWRZ0-HWRZ3↑)	t_{HKWTWR}	-	13.6	ns
14	Data, HWAITZ output hold time (from HCSZ, HPGCSZ↑)	t_{HKWTCS}	-	13.6	ns
15	HRDZ recovery time (high width)	t_{WHRD}	$t_{HBUSCLK}$ x 1	-	ns
16	Data, HWAITZ output delay time (from HRDZ↓)	t_{DKHDHR}	2.0	-	ns
17	HWAITZ enable data output delay time (from Latch timing of HRDZ, HWWRSTBZ, HWRZ0 – HWRZ3) “HWAITZ output in synchronization with HBUSCLK↑”	$t_{DKWTVHR}$	-	$t_{HBUSCLK}$/2 + 11.0	ns
	HWAITZ enable data output delay time (from Latch timing of HRDZ, HWWRSTBZ, HWRZ0 – HWRZ3) “HWAITZ output in synchronization with HBUSCLK↓”	$t_{DKWTVHR}$	-	$t_{HBUSCLK}$ + 11.0	ns
18	Data settle time (from HWAITZ↑) “HWAITZ output in synchronization with HBUSCLK↑”	$t_{SKHDHWT}$	-	10^{Note} - $t_{HBUSCLK}$ x n	ns
	Data settle time (from HWAITZ↑) “HWAITZ output in synchronization with HBUSCLK↓”	$t_{SKHDHWT}$	-	0^{Note} - $t_{HBUSCLK}$ x n	ns
19	Data, HWAITZ enable data output hold time (from HRDZ↑)	$t_{HKHWTHR}$	3.0	-	ns
20	Data, HWAITZ output delay time (from HRDZ↑)	t_{HKOHD}	-	13.6	ns
21	HRDZ input setup time (to HBUSCLK↓)	t_{SKHRD}	5.0	-	ns

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Remark: When setting the value other than 100_B to the CIEWAITDLY register, refer to the value of HWAITZ output in synchronization with HBUSCLK↑.

Note: This indicates the value when WAITDLY2-WAITDLY0 in the CIEWAITDLY register is 100_B.
n: 000_B = 4, 001_B = 3, 010_B = 2, 011_B = 1

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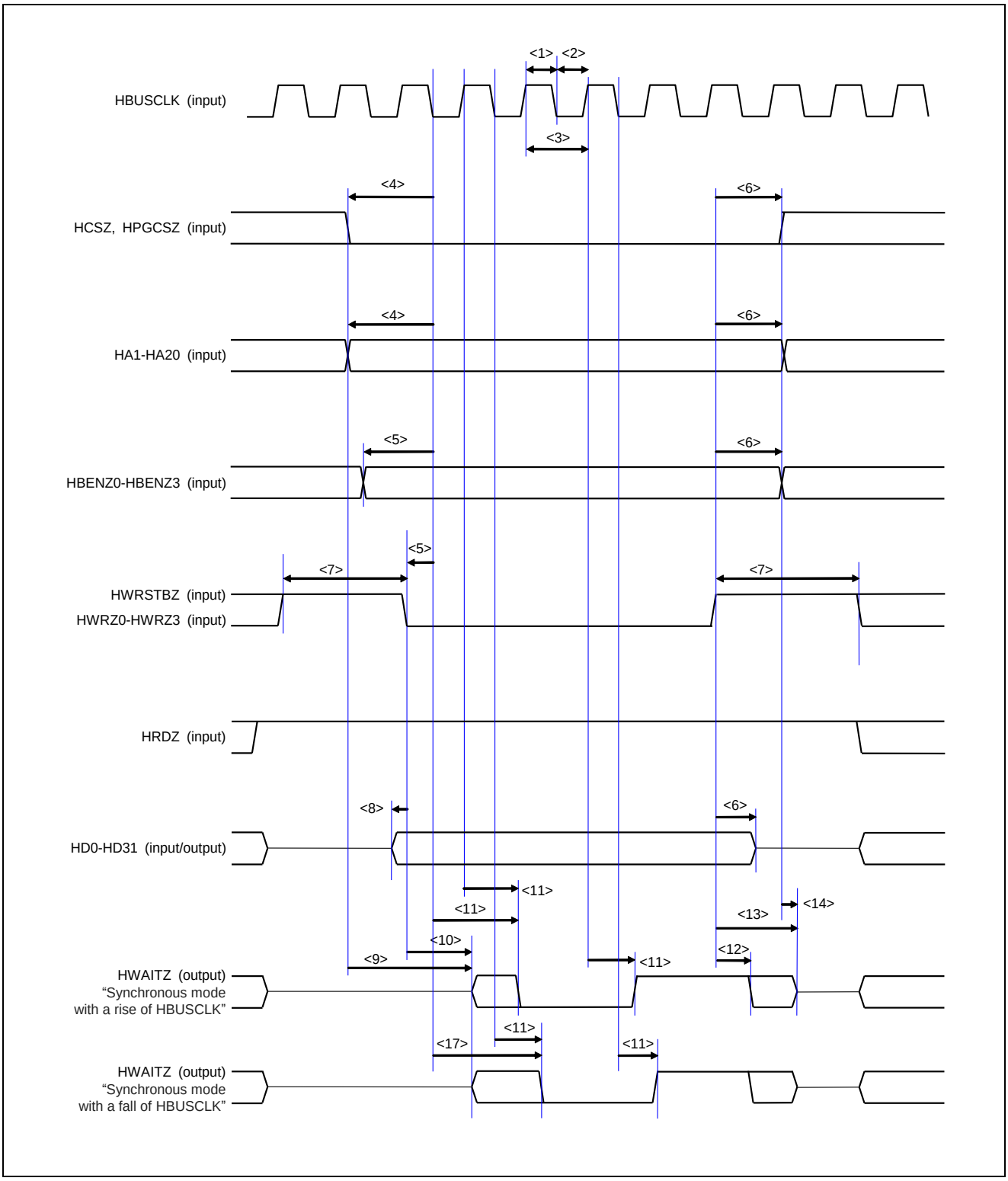


Figure 4.11 External MCU Write Timing (MEMCSEL = L, HIFSYNC = H)

Caution: Supply a stable signal to address/data/control system pins while being accessed.

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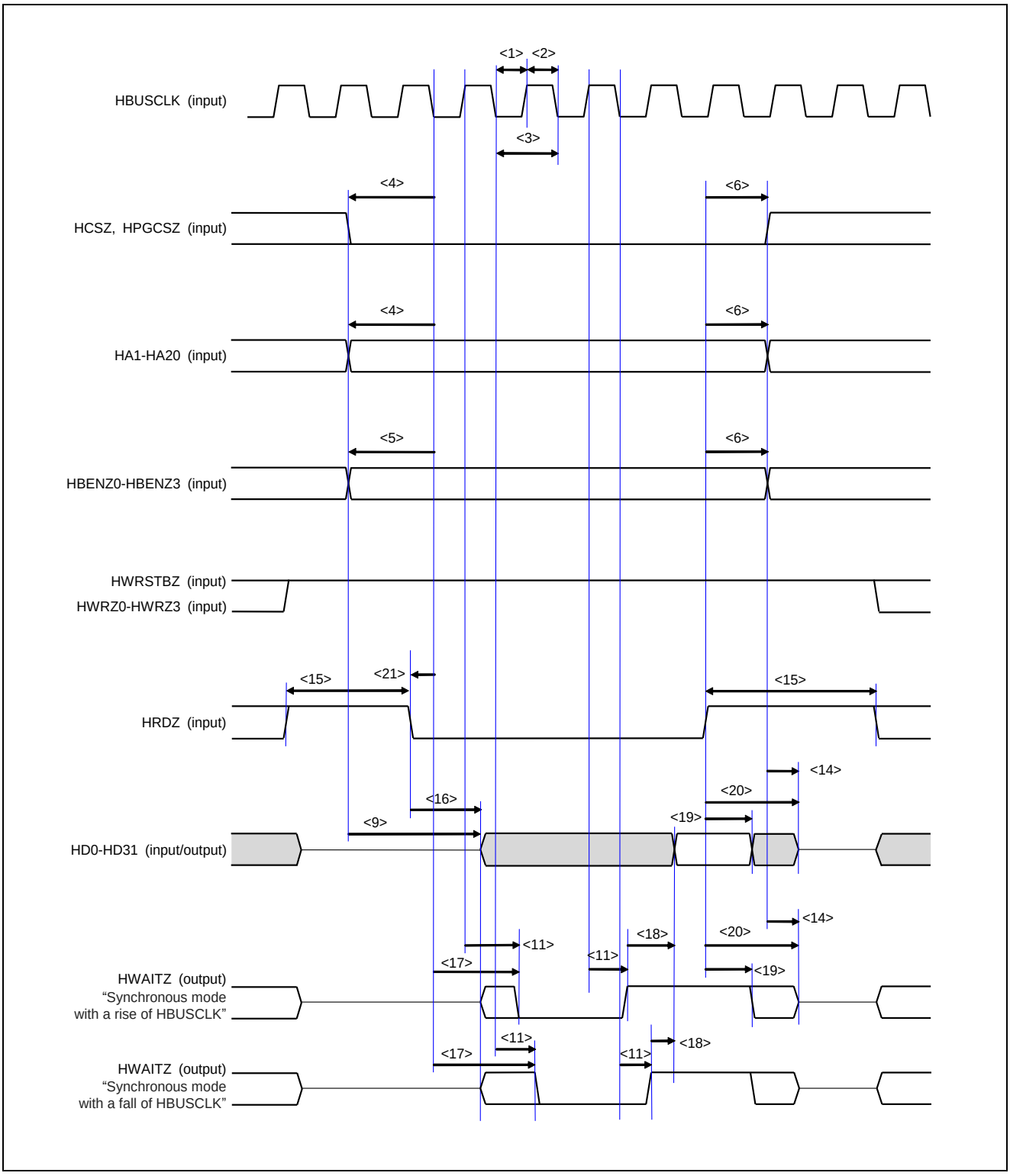


Figure 4.12 External MCU Read Timing (MEMCSEL = L, HIFSYNC = H)

Caution: Supply a stable signal to address/data/control system pins while being accessed.

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(3) Asynchronous Mode

No.	Parameter	Symbol	MIN	MAX	Unit
1	Address, HCSZ/HPGCSZ, HBENZ0-HBENZ3 input setup time (to HWRSTBZ, HWRZ0-HWRZ3↓)	t_{ADDWRS}	4.8[Note1] - 10 × n	-	ns
2	HWRZ0-HWRZ3, HWRSTBZ recovery time (high width)	t_{WRW}	35.0	-	ns
3	Data input setup time (to HWRSTBZ, HWRZ0-HWRZ3↓)	t_{WRS}	4.8[Note1] - 10 × n	-	ns
4	Data input hold time (from HWRSTBZ, HWRZ0-HWRZ3↑)	t_{WRH}	4.8	-	ns
5	HWAITZ output delay time (from HCSZ or HPGCSZ↓)	t_{CLZ}	2.0	-	ns
6	HWAITZ output delay time (from HWRSTBZ, HWRZ0-HWRZ3↓)	t_{WAITD}	2.0	-	ns
7	HWAITZ enable data output delay time (from HWRSTBZ, HWRZ0-HWRZ3↓)	$t_{WRWAITF}$	-	16.4	ns
8	HWAITZ enable data output hold time (from HWRSTBZ, HWRZ0-HWRZ3↑)	t_{WAITVH}	3.0	-	ns
9	HWAITZ output hold time (from HWRZ0-3, HWRSTBZ↑)	t_{WAITH}	-	13.6	ns
10	Data, HWAITZ output hold time (from HCSZ/HPGCSZ↑)	t_{CHZ}	-	13.6	ns
11	Address, HCSZ/HPGCSZ input setup time (to HRDZ↓)	t_{ADDRDS}	4.3[Note2] - 10 × n	-	ns
12	Data at the off-page access, Address input hold time (from HRDZ↑)	t_{ADDRDH}	4.3	-	ns
13	HRDZ recovery time (high width)	t_{RDW}	35.0	-	ns
14	Data, HWAITZ output delay time (from HRDZ↓)	t_{RDLZ}	2.0	-	ns
15	HWAITZ enable data output delay time (from HRDZ↓)	$t_{RDWAITF}$	-	16.4	ns
16	Data settle time (from HWAITZ↑)	t_{WAITR}	-	-7.5[Note3] +10 × n	ns
17	Data, HWAITZ enable data output hold time (from HRDZ↑)	t_{DATAOH}	3.0	-	ns
18	Data, HWAITZ output hold time (from HRDZ↑)	t_{RDHZ}	-	13.6	ns
19	Data at the on-page access, HWAITZ output delay time (from the address)	$t_{PAGEOND}$	3.0	16.4	ns
20	Data at the off-page access, HWAITZ output delay time (from the address)	$t_{PAGEOFD}$	3.0	16.4	ns
21	HWAITZ enable data output delay time (from HCSZ/HPGCSZ↓)	t_{WAITVD}	-	16.4	ns
22	Address input hold time when advance reading is enabled (from HRDZ↑)	$t_{ADDRDHP}$	4.3	-	ns

Notes 1. This indicates the value when WRSTD2-WRSTD0 in the HIFBTC register is 000_B.
n: Indicated by the value of WRSTD2-WRSTD0
2. This indicates the value when RDSTD1-RDSTD0 in the HIFBTC register is 00_B.
n: Indicated by the value of RDSTD1-RDSTD0
3. This indicates the value when RDDTS1-RDDTS0 in the HIFBTC register is 00_B.
n: Indicated by the value of RDDTS1-RDDTS0

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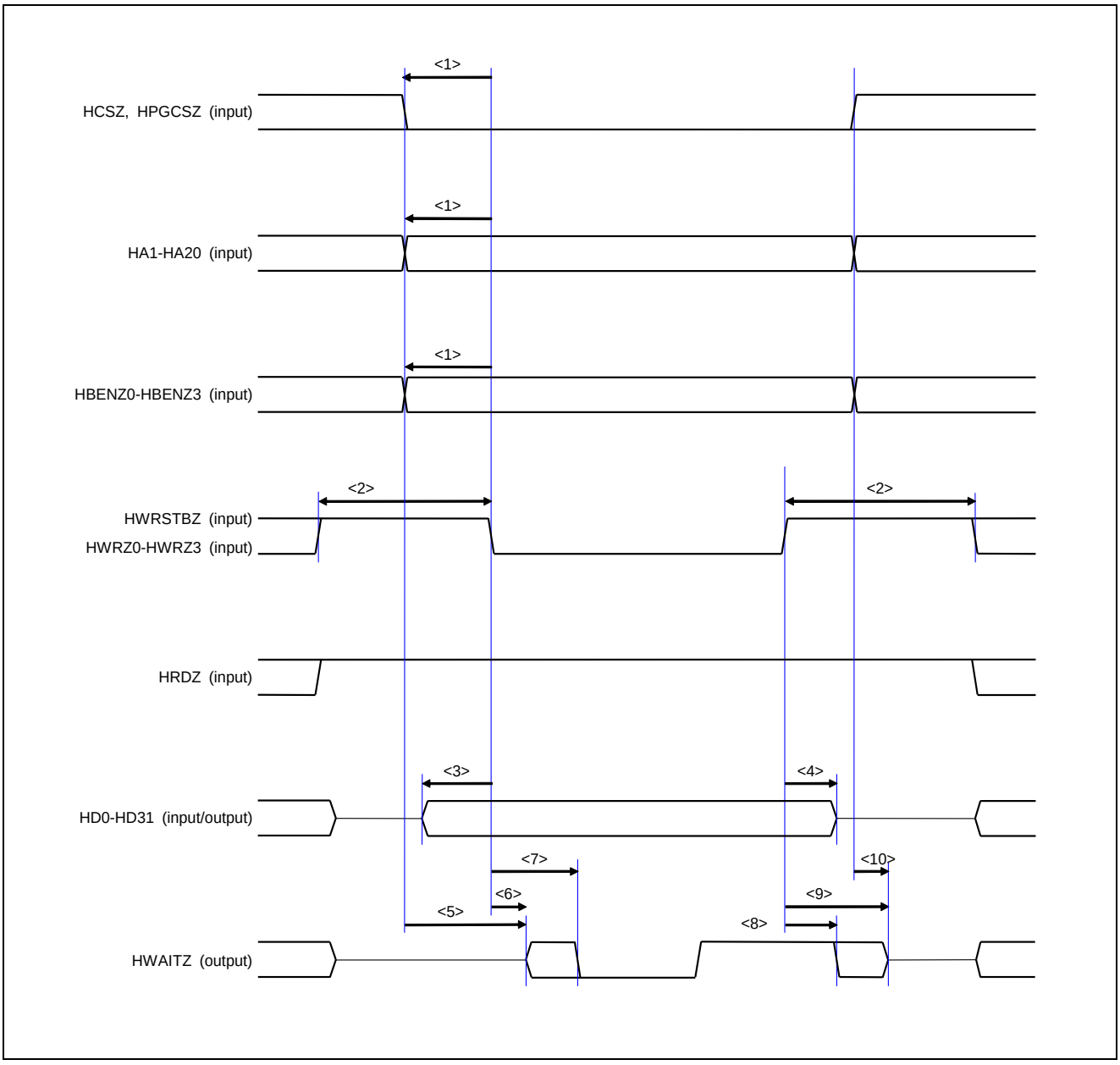


Figure 4.13 External MCU Write Timing (MEMCSEL = L, HIFSYNC = L)

Caution: Supply a stable signal to address/data/control system pins while being accessed.

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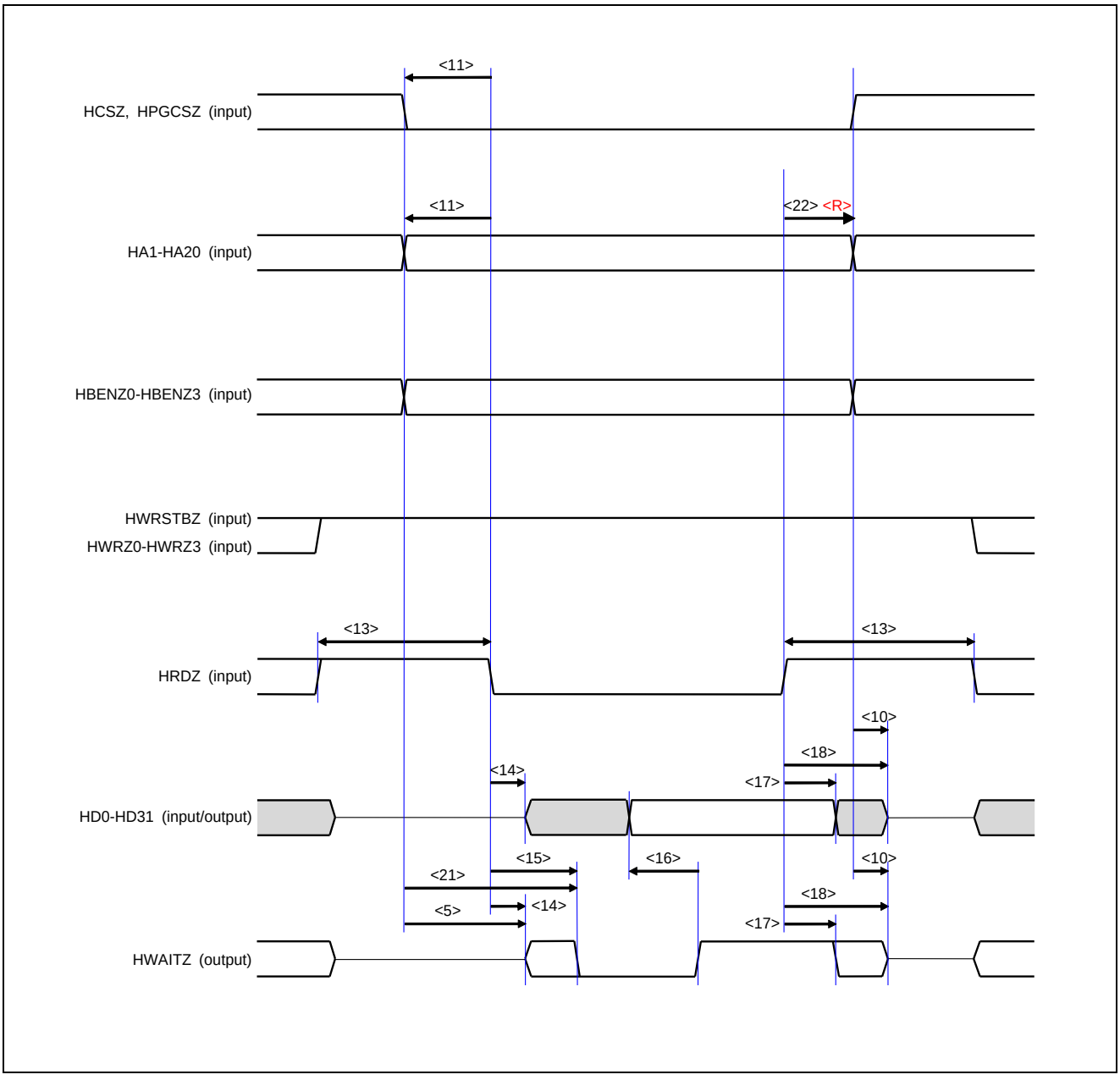


Figure 4.14 External MCU Read Timing (MEMCSEL = L, HIFSYNC = L)

Caution: Supply a stable signal to address/data/control system pins while being accessed.

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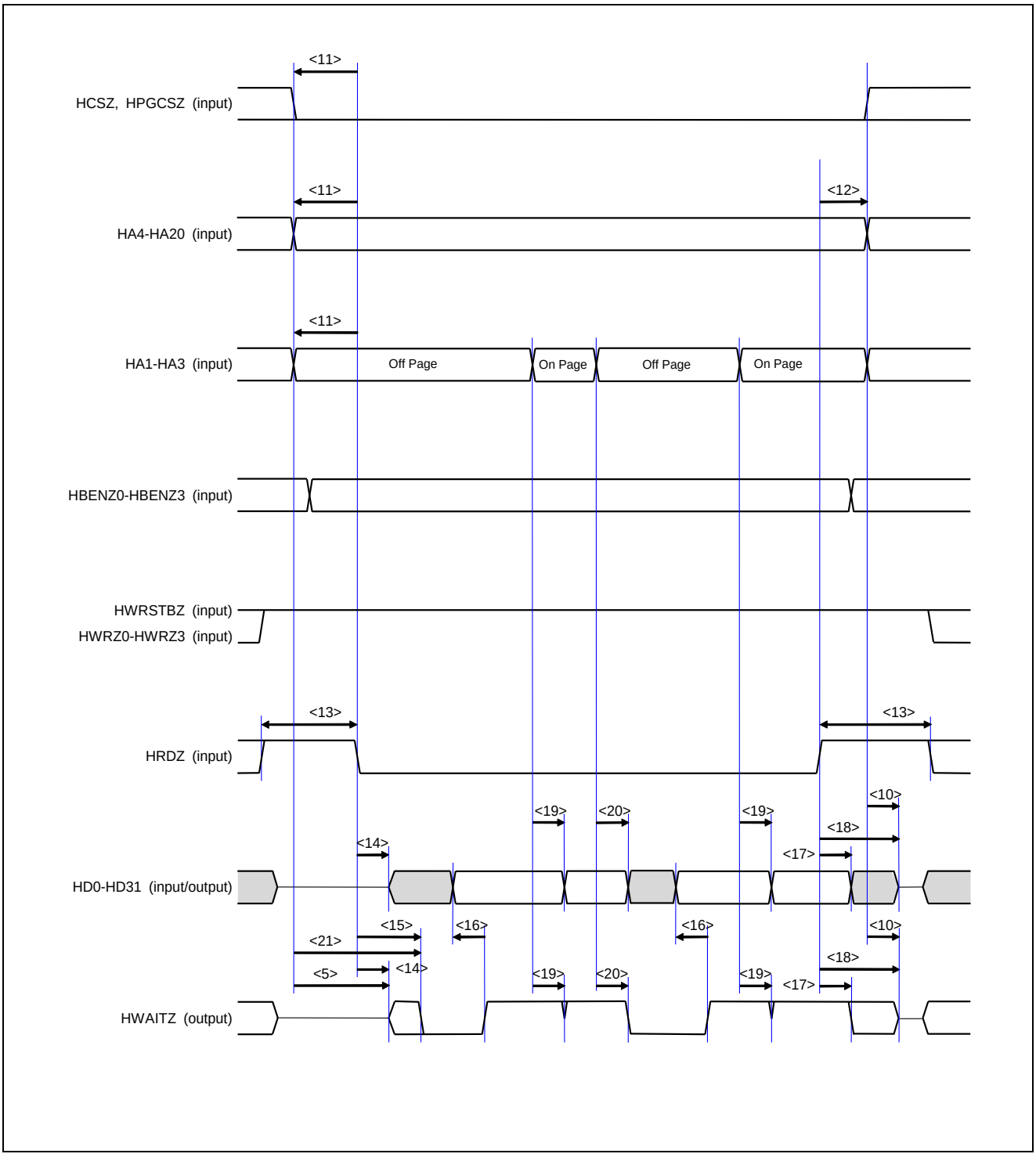


Figure 4.15 External MCU Page-Read Timing (MEMCSEL = L, HIFSYNC = L)

Caution: Supply a stable signal to address/data/control system pins while being accessed.

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(4) Synchronous SRAM Type Transfer Mode

No.	Parameter	Symbol	MIN	MAX	Unit
1	HBUSCLK high-level width	t_{HBHIGH}	$0.5t_{HBUSCLK} - 2.1$	$0.5t_{HBUSCLK} + 2.1$	ns
2	HBUSCLK low-level width	t_{HBLOW}	$0.5t_{HBUSCLK} - 2.1$	$0.5t_{HBUSCLK} + 2.1$	ns
3	HBUSCLK input cycle	$t_{HBUSCLK}$	20	-	ns
4	Address, HCSZ/HPGCSZ input setup time (to HBUSCLK↑)	t_{SKPHA}	4.0	-	ns
5	Address, HCSZ/HPGCSZ input hold time (from HBUSCLK↑)	t_{HKPCS}	1.0	-	ns
6	Address, HCSZ/HPGCSZ input setup time (to HBUSCLK↓)	t_{SKNHA}	4.0	-	ns
7	Address, HCSZ/HPGCSZ input hold time (from HBUSCLK↓)	t_{HKNHA}	1.0	-	ns
8	HWRZ0-HWRZ3 input setup time (to HBUSCLK↑)	t_{SKPHWR}	4.0	-	ns
9	HWRZ0-HWRZ3 input hold time (from HBUSCLK↑)	t_{HKPHWR}	1.0	-	ns
10	HWRZ0-HWRZ3 input setup time (to HBUSCLK↓)	t_{SKNHWR}	4.0	-	ns
11	HWRZ0-HWRZ3 input hold time (from HBUSCLK↓)	t_{HKNHWR}	1.0	-	ns
12	HBCYSTZ, HWRSTBZ input setup time (to HBUSCLK↑)	$t_{SKPHBCY}$	4.0	-	ns
13	HBCYSTZ, HWRSTBZ input hold time (from HBUSCLK↑)	$t_{HKPHBCY}$	1.0	-	ns
14	HBCYSTZ, HWRSTBZ input setup time (to HBUSCLK↓)	$t_{SKNHBCY}$	4.0	-	ns
15	HBCYSTZ, HWRSTBZ input hold time (from HBUSCLK↓)	$t_{HKNHBCY}$	1.0	-	ns
16	HRDZ input setup time (to HBUSCLK↑)	t_{SKPHRD}	4.0	-	ns
17	HRDZ input hold time (from HBUSCLK↑)	t_{HKPHRD}	1.0	-	ns
18	HRDZ input setup time (to HBUSCLK↓)	t_{SKNHRD}	4.0	-	ns
19	HRDZ input hold time (from HBUSCLK↓)	t_{HKNHRD}	1.0	-	ns
20	Data input setup time (to HBUSCLK↑)	t_{SKPHD}	4.0	-	ns
21	Data input hold time (from HBUSCLK↑)	t_{HKPHD}	1.0	-	ns
22	Data input setup time (to HBUSCLK↓)	t_{SKNHD}	4.0	-	ns
23	Data input hold time (from HBUSCLK↓)	t_{HKNHD}	1.0	-	ns
24	Data output delay time (from HRDZ↓)	t_{DKNHRD}	2.0	-	ns
25	Data output hold time (from HRDZ↑)	t_{HKPHRD}	-	13.6	ns
26	Data output delay time (from HBUSCLK↑)	t_{DKPHD}	2.0	10.0	ns
27	Data output delay time (from HBUSCLK↓)	t_{DKNHD}	2.0	10.0	ns
28	HWAITZ output delay time (from HBUSCLK↑)	t_{DKPHWT}	2.0	10.0	ns
29	HWAITZ output delay time (from HBUSCLK↓)	t_{DKNHWT}	2.0	10.0	ns
30	Data output hold time (from HCSZ/HPGCSZ ↑)	t_{HKPHCS}	-	13.6	ns

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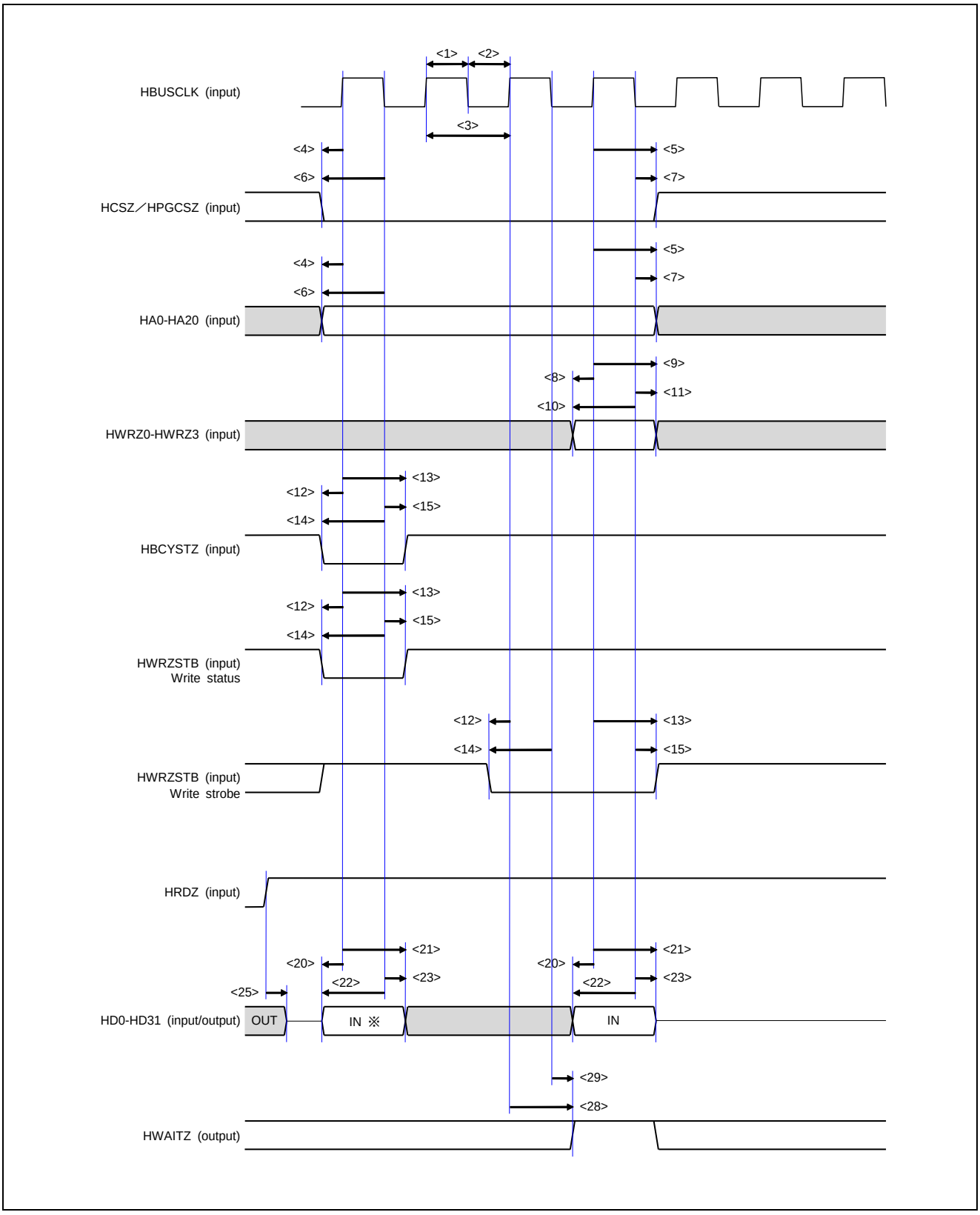


Figure 4.16 External MCU Write Timing (MEMCSEL = H, ADMUXMODE = H)

Remark: Address is input in A/D multiplex mode.

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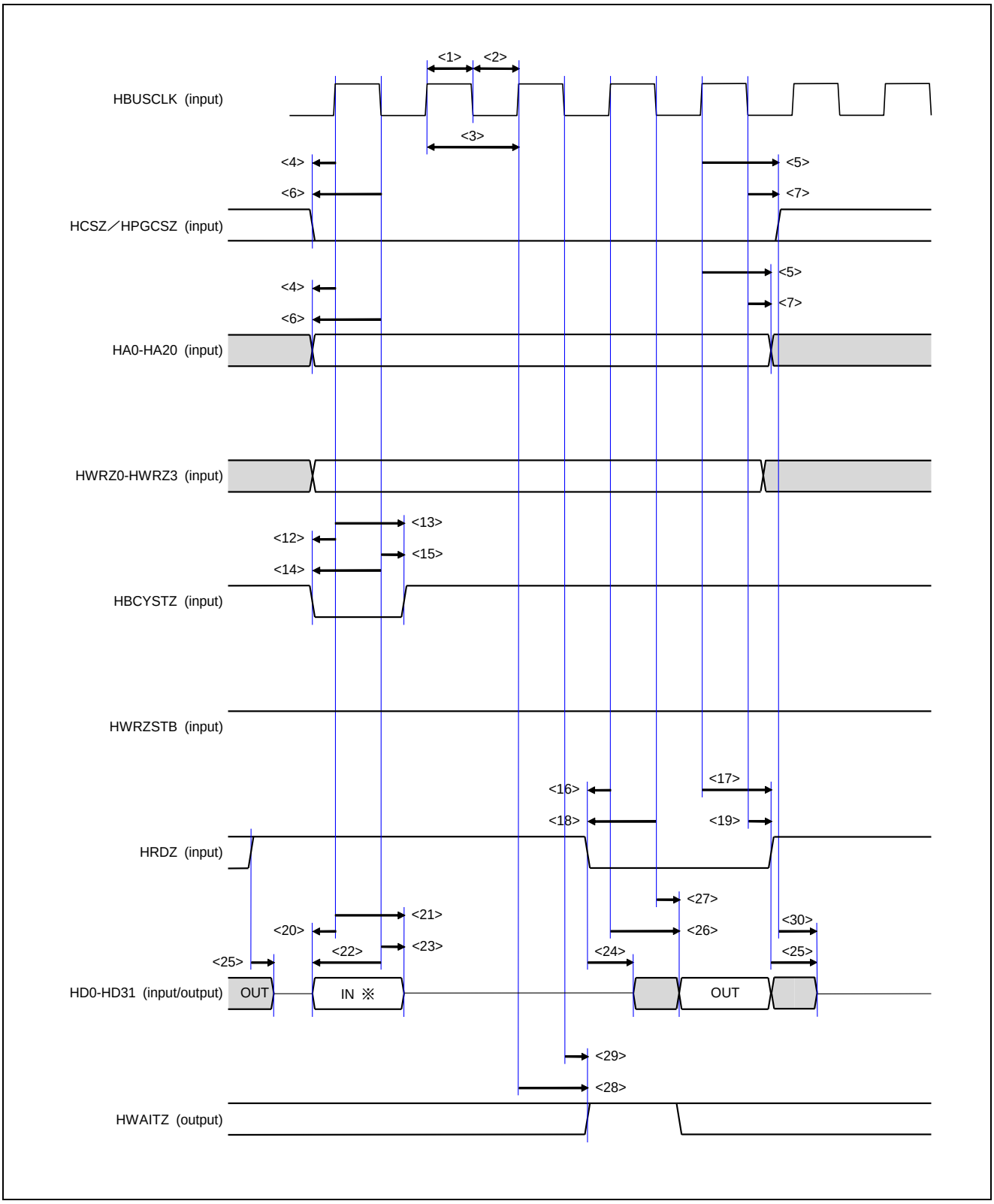


Figure 4.17 External MCU Read Timing (MEMCSEL = H, ADMUXMODE = H)

Remark: Address is input in A/D multiplex mode.

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4.8.5 Serial Flash ROM Interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
SMSCK output cycle	t_{SFRCYC}	C_L = 15 pF	20	-	ns
SMSCK high level width	t_{SMCKH}		0.5 t_{SFRCYC} – 2.0	0.5 t_{SFRCYC} + 2.0	ns
SMSCK low level width	t_{SMCKL}		0.5 t_{SFRCYC} – 2.0	0.5 t_{SFRCYC} + 2.0	ns
SMSCK rise time	t_{SMCKR}		–	1.9	ns
SMSCK fall time	t_{SFRCYC}		–	1.9	ns
Delay time from a falling of SMCSZ to a rising of SMSCK	$t_{DSMCSCK}$	C_L = 15 pF Freq = 50 MHz	6.0 Note	–	ns
Hold time until a rising of SMCSZ from a rising of SMSCK	$t_{DSMCKCS}$	C_L = 15 pF Freq = 50 MHz	9.0 Note	–	ns
SMCSZ high level width	t_{SMCSH}	C_L = 15 pF	14 Note	–	ns
SMSI input setup time (to SMSCK↓)	t_{SSMI}	-	6.0	-	Ns
SMSI input hold time (from SMSCK↓)	t_{HSMI}	-	0	-	ns
SMSI output delay time (from SMSCK↓)	t_{DSMI}	C_L = 15 pF	-1.0	5.0	ns
SMSO input setup time (to SMSCK↓)	t_{SSMO}	-	6.0	-	ns
SMSO input hold time (from SMSCK↓)	t_{HSMO}	-	0	-	ns
SMSO output delay time (from SMSCK↓)	t_{DSMO}	C_L = 15 pF	-1.0	5.0	ns

Note: Timing can be extended by setting of SFMSSC register.
Please refer to 12.2.2 Chip Selection Control Register (SFMSSC) of User's Manual (Peripheral Modules).

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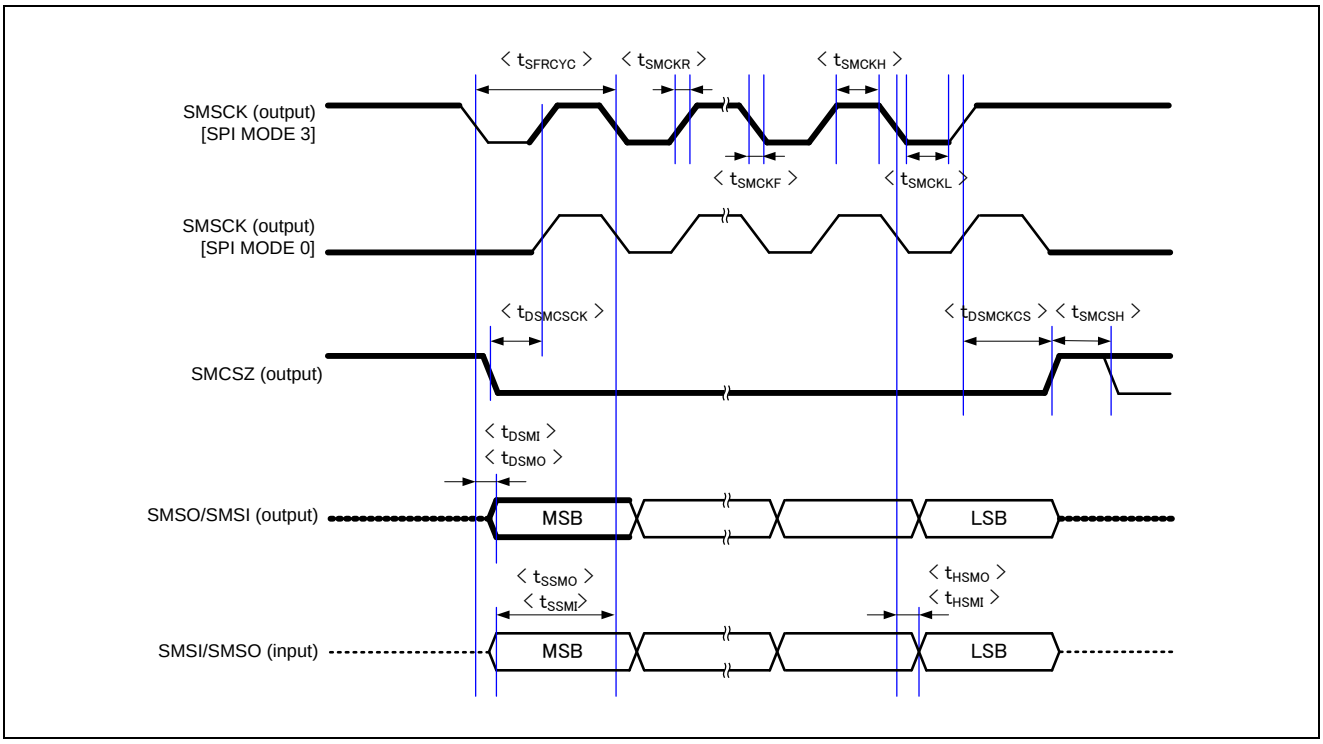


Figure 4.18 Serial Flash Rom Access Timing Diagram

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4.8.6 External DMA Interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
DMAREQZn, RTDMAREQZ input setup time (from BUSCLK↑)	t_{SKDR}	-	7.0	-	ns
DMAREQZn, RTDMAREQZ input hold time 1	t_{HKDR1}	-	Until DMAACKZn↓, RTDMAACKZ↓	-	ns
DMAREQZn, REDMAREQZ input hold time 2 (from BUSCLK↑)	t_{HKDR2}	-	-	t_{BUSCLK} Note1 × m Note2 – 7.0	ns
DMAACKZn, RTDMACKZ output delay time (from BUSCLK↑)	t_{DKDA}	C_L = 30pF	2.0	10.0	ns
DMAACKZn, RTDMAACKZ output low level width	t_{WDAL}	-	t_{BUSCLK} Note1 × m Note2 – 8	t_{BUSCLK} Note1 × m Note2 + 8	ns
DMATCZn, RTDMATCZ output delay time (from BUSCLK↑)	t_{DKTC}	C_L = 30pF	2.0	10.0	ns

Notes 1. t_{BUSCLK} is one cycle (10 ns) of BUSCLK.
2. n = 0,1 and m = 1-31 (DMAIFC0, DMAIFC1, RTMDAIFC registers).

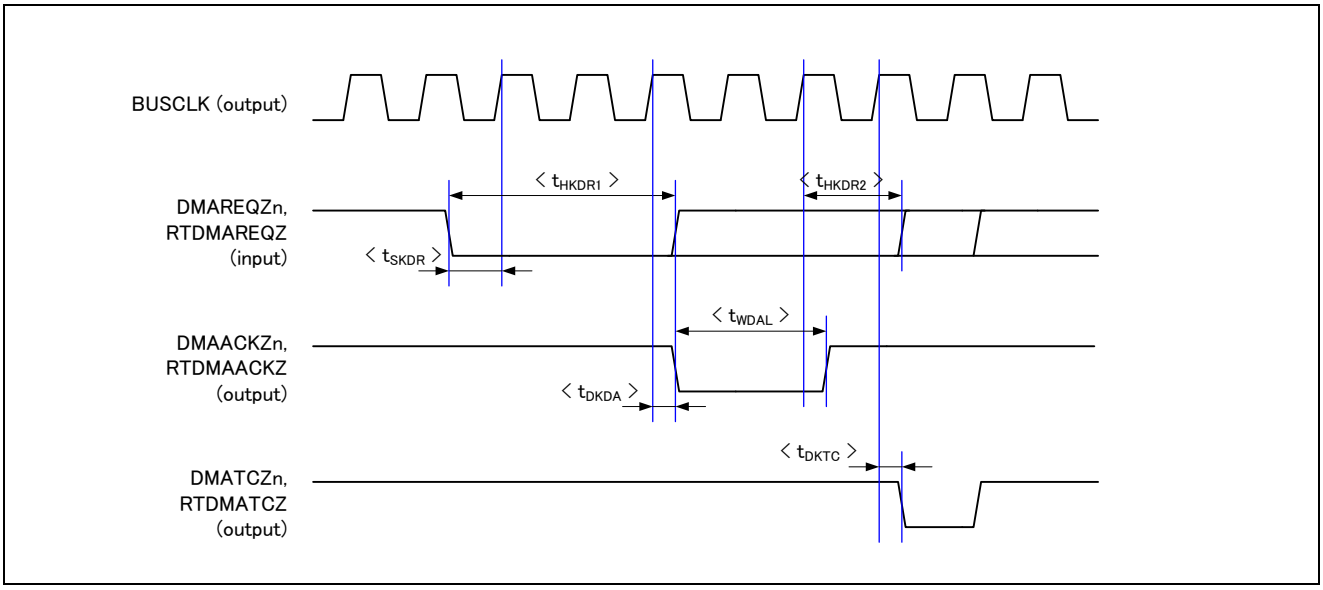


Figure 4.19 External DMA Access Timing Diagram

Remark: n = 0, 1

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4.8.7 CSI Interface

The clocked serial interface (CSI) supports both master and slave mode.

(1) Master mode

Parameter	Symbol	Conditions	MIN	MAX	Unit
CSISCKn output cycle	$t_{CSIMSCK}$	C_L = 15pF	40	-	ns
CSISCKn output high level width	t_{WSKH}	C_L = 15pF	$t_{CSIMSCK}$×0.5 – 5.0	-	ns
CSISCKn output low level width	t_{WSKL}	C_L = 15pF	$t_{CSIMSCK}$×0.5 – 5.0	-	ns
CSISIn input setup time (to CSISCKn↑)	t_{SMSI}	-	8.5	-	ns
CSISIn input setup time (to CSISCKn↓)	t_{SMSI}	-	8.5	-	ns
CSISIn input hold time (from CSISCKn↑)	t_{HMSI}	-	7.0	-	ns
CSISIn input hold time (from CSISCKn↓)	t_{HMSI}	-	7.0	-	ns
CSISOn output delay time (from CSISCKn↑)	t_{DMSO}	C_L = 15pF	-	7.0	ns
CSISOn output delay time (from CSISCKn↓)	t_{DMSO}		-	7.0	ns
CSISOn output hold time (from CSISCKn↑)	t_{HMSO}		$t_{CSIMSCK}$ × 0.5 – 5.0	-	ns
CSISOn output hold time (from CSISCKn↓)	t_{HMSO}		$t_{CSIMSCK}$ × 0.5 – 5.0	-	ns

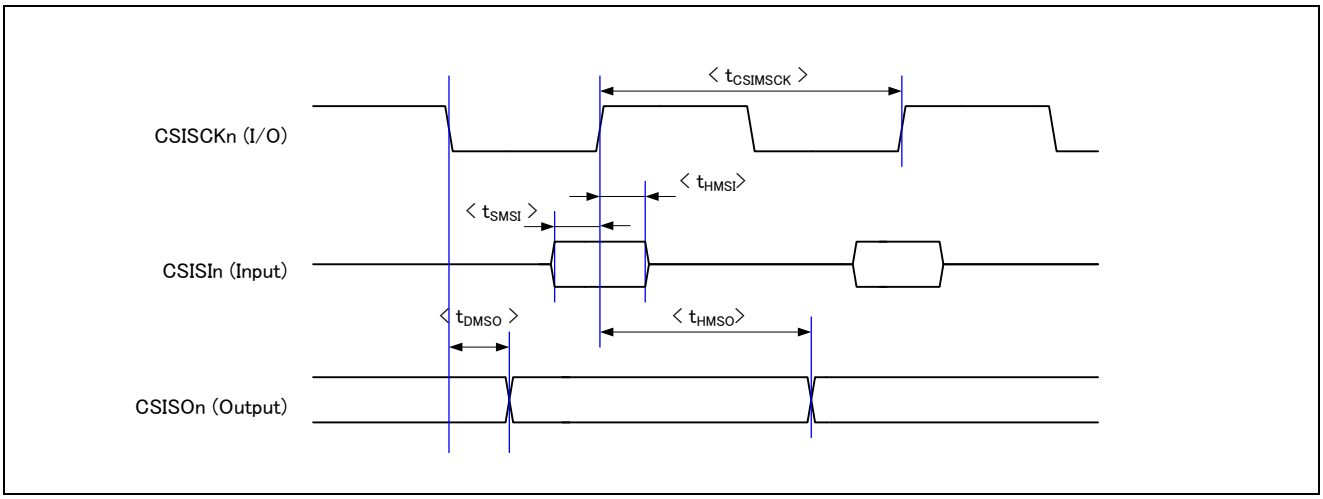


Figure 4.20 CSI Access Timing Diagram (Master Mode)

Remarks 1. n = 0, 1

2. Above timing diagram shows the case for when "Data Output from CSISCKn↓" and "Data Input from CSISCKn↑". See the timing diagram according to the operating mode.

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(2) Slave mode

Parameter	Symbol	Conditions	MIN	MAX	Unit
CSISCKn input cycle	$t_{CSISSCK}$	-	60	-	ns
CSISCKn input high level width	t_{WSKH}	-	$t_{CSIMSCK}$×0.5 – 5.0	-	ns
CSISCKn input low level width	t_{WSKL}	-	$t_{CSIMSCK}$×0.5 – 5.0	-	ns
CSISIn input setup time (to CSISCKn↑)	t_{SSSI}	-	10.0	-	ns
CSISIn input setup time (to CSISCKn↓)	t_{SSSI}	-	10.0	-	ns
CSISIn input hold time (from CSISCKn↑)	t_{HSSI}	-	15	-	ns
CSISIn input hold time (from CSISCKn↓)	t_{HSSI}	-	15	-	ns
CSISOn output delay time (from CSISCKn↑)	t_{DSSO}	C_L = 15pF	-	10.0	ns
CSISOn output delay time (from CSISCKn↓)	t_{DSSO}		-	10.0	ns
CSISOn output hold time (from CSISCKn↑)	t_{HSSO}		$t_{CSISSCK}$ × 0.5 – 5.0	-	ns
CSISOn output hold time (from CSISCKn↓)	t_{HSSO}		$t_{CSISSCK}$ × 0.5 – 5.0	-	ns

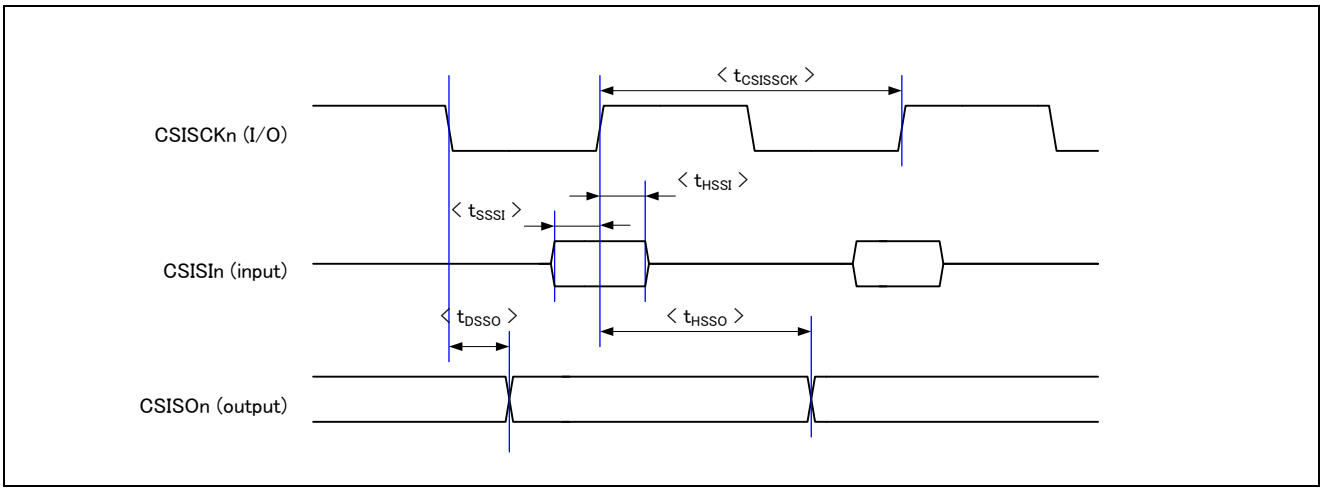


Figure 4.21 CSI Access Timing Diagram (Slave Mode)

Remarks 1. n = 0, 1

2. Above timing diagram shows the case for when "Data Output from CSISCKn↓" and "Data Input from CSISCKn↑". See the timing diagram according to the operating mode.

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4.8.8 I2C Interface

Parameter		Symbol	Conditions	Normal mode		High speed mode		Unit
				MIN	MAX	MIN	MAX	
SCL clock frequency		t_{SCL}	C_L = 30pF	0	100	0	400	kHz
Bus-free time between the stop condition and start condition		t_{BUF}		4.7	-	1.3	-	µs
Hold time		t_{HSTA}		4.0	-	0.6	-	µs
SCL clock low-level width		t_{SCLL}		4.7	-	1.3	-	µs
SCL clock high-level width		t_{SCLH}		4.0	-	0.6	-	µs
Setup time for the start and restart conditions		t_{SSTA}		4.7	-	0.6	-	µs
Data hold time	For a CBUS compatible master	t_{HDAT}		5.0	-	-	-	µs
	For an IIC bus			0	-	0	0.9	µs
Data setup time		t_{SDAT}		250	-	100	-	ns
SDA and SCL signal rise time		t_{SCLR}		-	1000	20 + 0.1C_b	300	ns
SDA and SCL signal fall time		t_{SCLF}		-	300	20 + 0.1C_b	300	ns
Stop condition setup time		t_{SSTO}		4.0	-	0.6	-	µs
Pules width of spike suppressed by input filter		t_{SP}		-	-	0	50	ns
Capacitance load of each bus line		C_b	-	-	400	-	400	pF

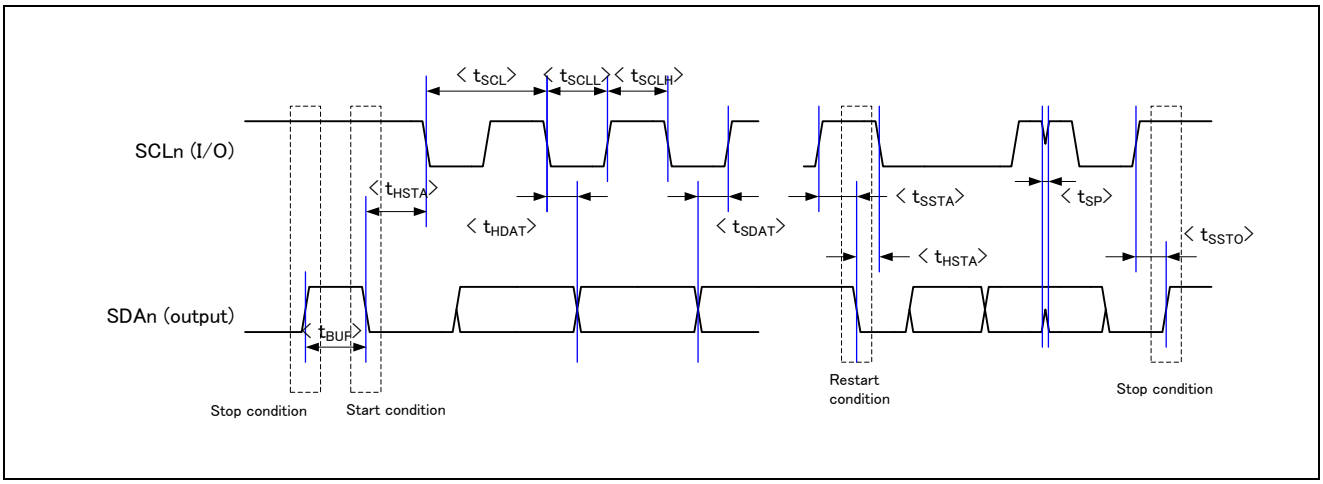


Figure 4.22 I2C Access Timing Diagram

Remark 1 n = 0, 1

t_{SCLR} and t_{SCLF} are omitted from the diagram.

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4.8.9 CAN Interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
Internal delay time	t_{NODE}	C_L = 30pF	-	75	ns

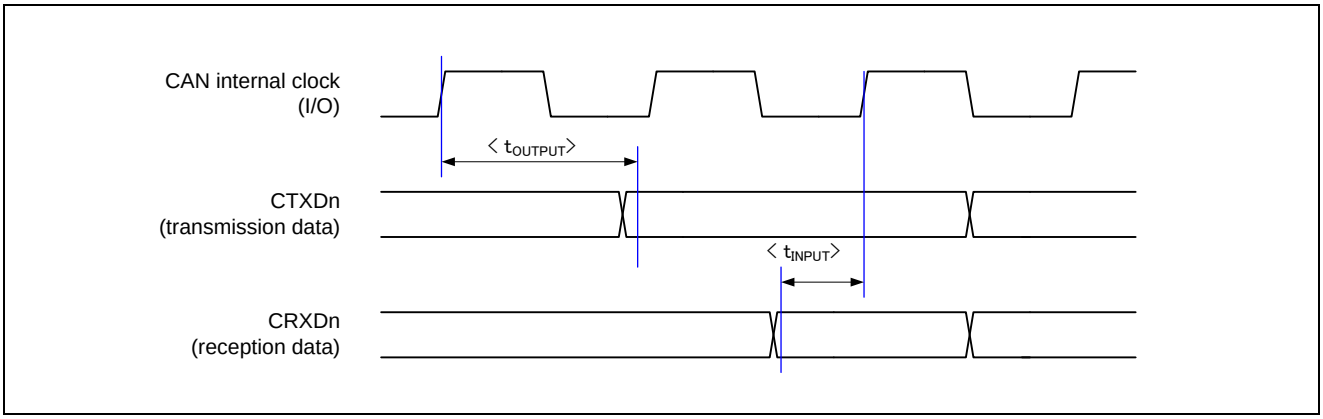


Figure 4.23 CAN Access Timing Diagram

Internal delay time (t_{NODE}) = Internal transmission delay time (t_{OUTPUT}) + Internal reception delay time (t_{INPUT})

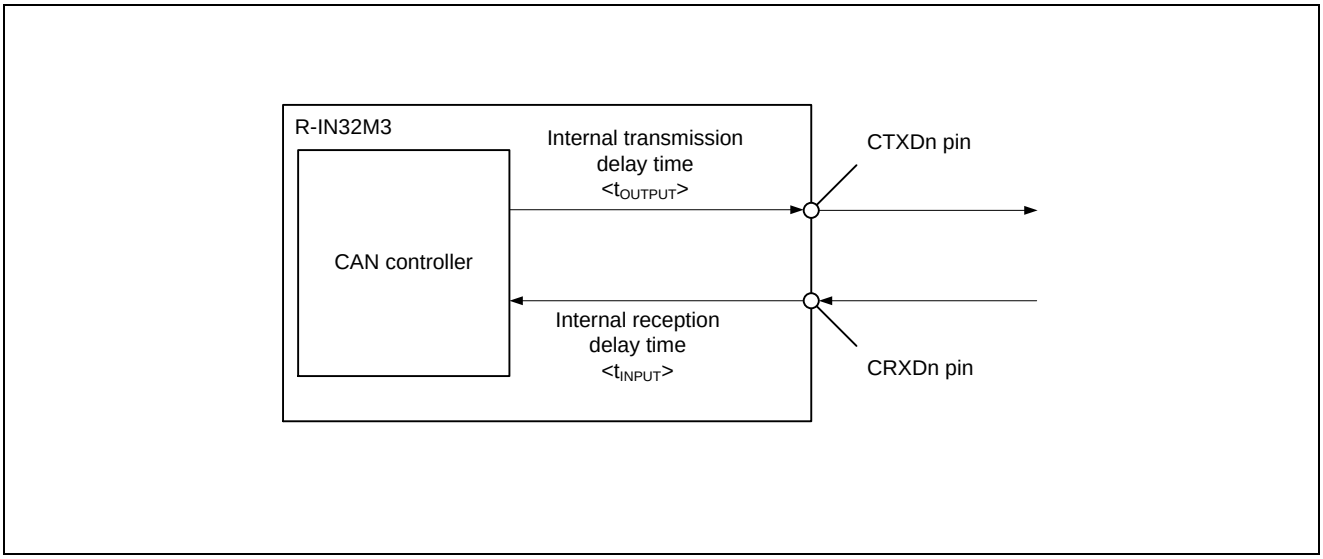


Figure 4.24 CAN Access Timing (Supplementary Information)

Remarks 1. CAN internal clock (f_{CAN}): CAN baud late clock

2. n = 0,1

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4.8.10 Ethernet Interface (R-IN32M3-CL only)

(1) GMII interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
ETHn_GTXC output cycle	t_{GTXC}	C_L = 13pF	8	-	ns
ETHn_RXC input cycle	t_{GRXC}	-	8	-	ns
ETHn_TXDm output delay time (from ETHn_GTXC↑)	t_{DGTKTD}	C_L = 13pF	0.5	5.5	ns
ETHn_TXEN, ETHn_TXER output delay time (from ETHn_GTXC↑)	t_{DGTKTE}	C_L = 13pF	0.5	5.5	ns
ETHn_RXDm input setup time (to ETHn_RXC↑)	t_{SGRDRK}	-	2.0	-	ns
ETHn_RXDm input hold time (from ETHn_RXC↑)	t_{HGRDRK}	-	0	-	ns
ETHn_RXDV, ETHn_RXER input setup time (to ETHn_RXC↑)	t_{SGRVRK}	-	2.0	-	ns
ETHn_RXDV, ETHn_RXER input hold time (from ETHn_RXC↑)	t_{HGRVRK}	-	0	-	ns

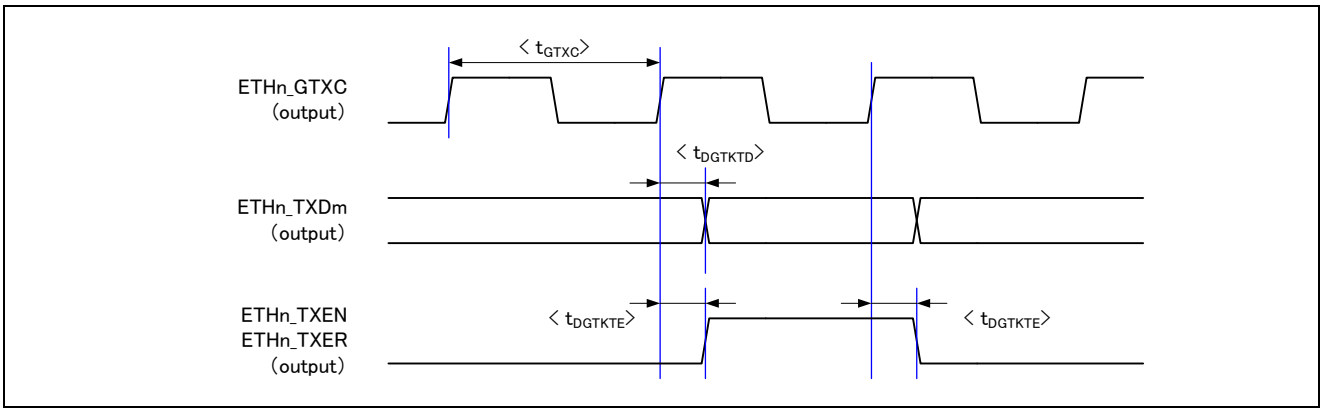


Figure 4.25 Ethernet Access Timing Diagram (GMII Transmission)

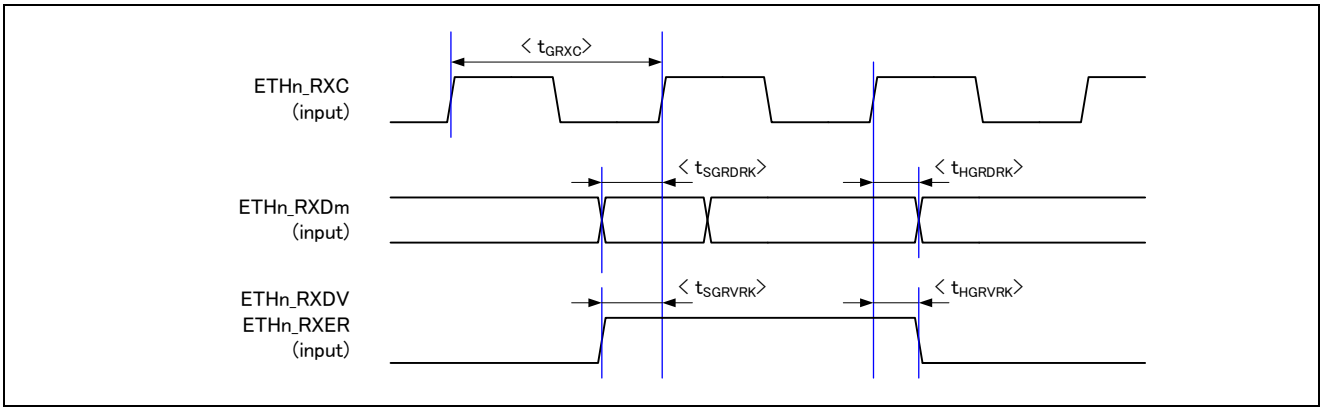


Figure 4.26 Ethernet Access Timing Diagram (GMII Reception)

Remark: n = 0, 1, m = 0-7

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(2) MII interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
ETHn_TXC input cycle	t_{TXC}	-	40	-	ns
ETHn_RXC input cycle	t_{RXC}	-	40	-	ns
ETHn_TXDm output delay time (from ETHn_TXC↑)	t_{DTKTD}	C_L = 30pF	0	25	ns
ETHn_TXEN, ETHn_TXER output delay time (from ETHn_TXC↑)	t_{DTKTE}	C_L = 30pF	0	25	ns
ETHn_RXDm input setup time (to ETHn_RXC↑)	t_{SRDRK}	-	10	-	ns
ETHn_RXDm input hold time (from ETHn_RXC↑)	t_{HRDRK}	-	10	-	ns
ETHn_RXDV, ETHn_RXER input setup time (to ETHn_RXC↑)	t_{SRVRK}	-	10	-	ns
ETHn_RXDV, ETHn_RXER input hold time (from ETHn_RXC↑)	t_{HRVRK}	-	10	-	ns

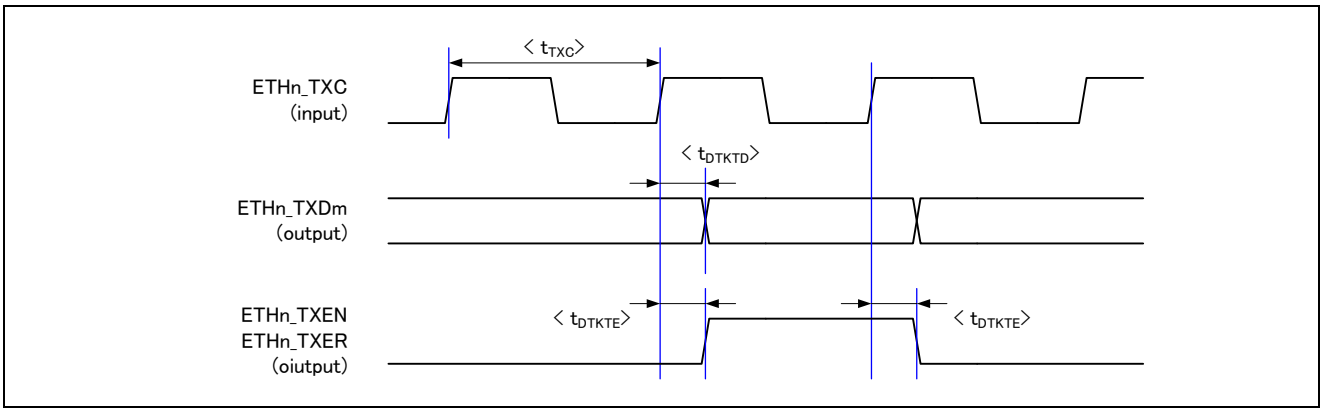


Figure 4.27 Ethernet Access Timing Diagram (MII Transmission)

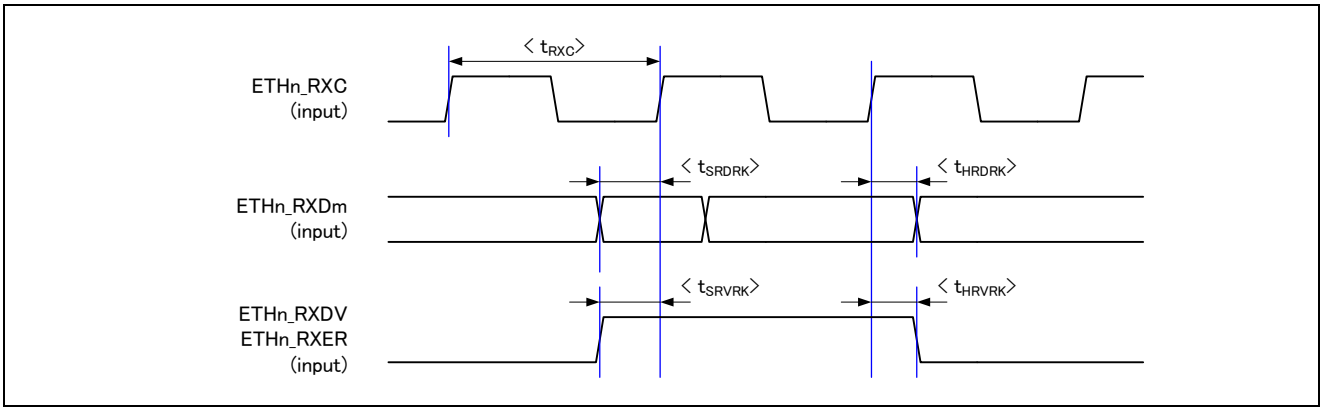


Figure 4.28 Ethernet Access Timing (MII Reception)

Remark: n = 0, 1, m = 0-7

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(3) Serial management interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
ETH_MDC output cycle	t_{MDC}	C_L = 30pF	80	-	ns
ETH_MDIO input setup time (to ETH_MDC↑)	t_{SMDIO}		10	-	ns
ETH_MDIO input hold time (from ETH_MDC↑)	t_{HMDIO}		0	-	ns
ETH_MDIO output delay time (from ETH_MDC↑)	t_{DMDIO}		20	-	ns

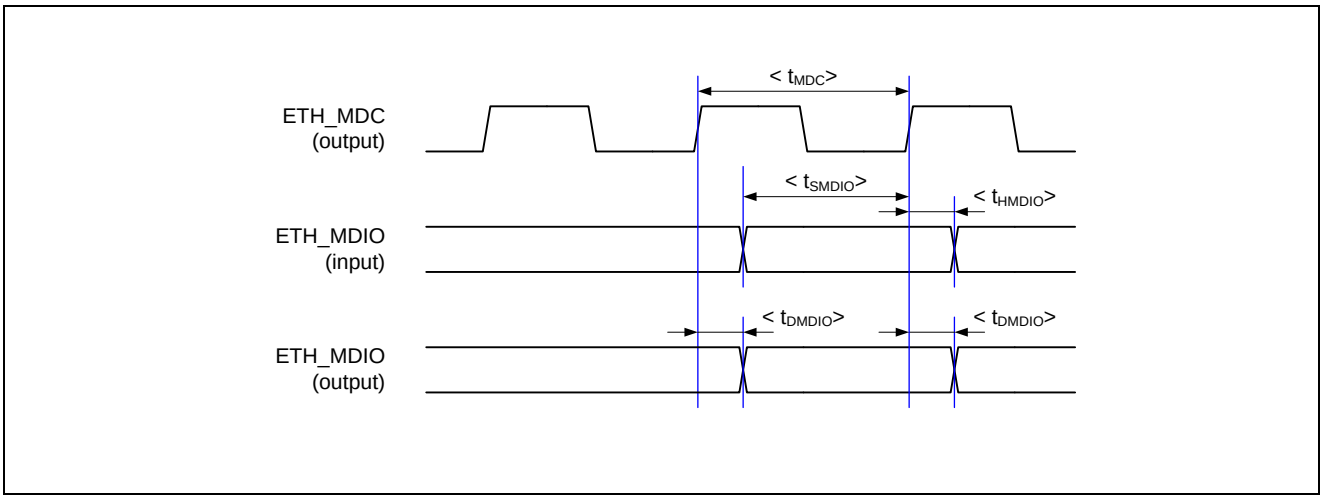


Figure 4.29 Ethernet Access Timing Diagram (Serial Management)

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4.8.11 Debug Interface

(1) Debug serial interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
TCK input cycle	t_{TCK}	-	20	-	ns
TMS input setup time (to TCK↑)	t_{STMS}	-	6.5	-	ns
TMS input hold time (from TCK↑)	t_{HTMS}	-	0	-	ns
TDI input setup time (to TCK↑)	t_{STDI}	-	6.5	-	ns
TDI input hold time (from TCK↑)	t_{HTDI}	-	0	-	ns
TDO output delay time (from TCK↓)	t_{DTDO}	C_L = 30pF	3.0	13.0	ns

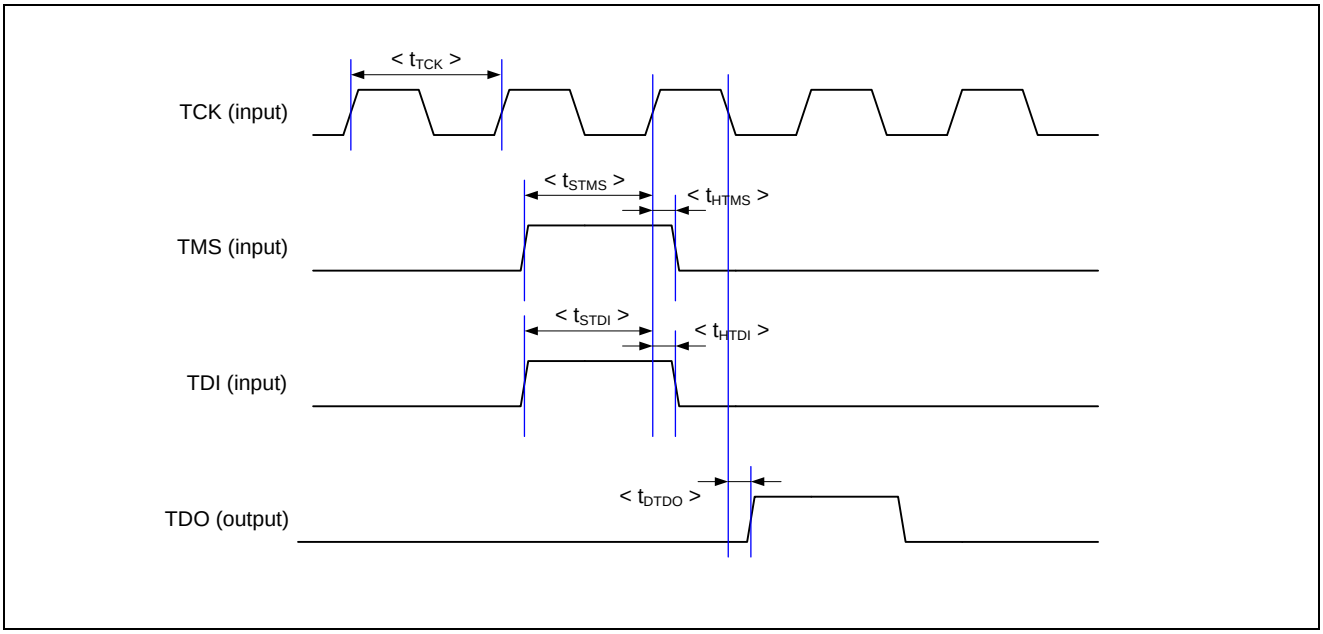


Figure 4.30 Debug Serial Interface

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(2) Trace interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
TRACECLK output frequency	t_{TRCCLK}	C_L = 15pF	20	-	ns
TRACEDATA output delay time (from TRACECLK)	$t_{DTRCDAT}$	C_L = 15pF	0.26	8.43	ns

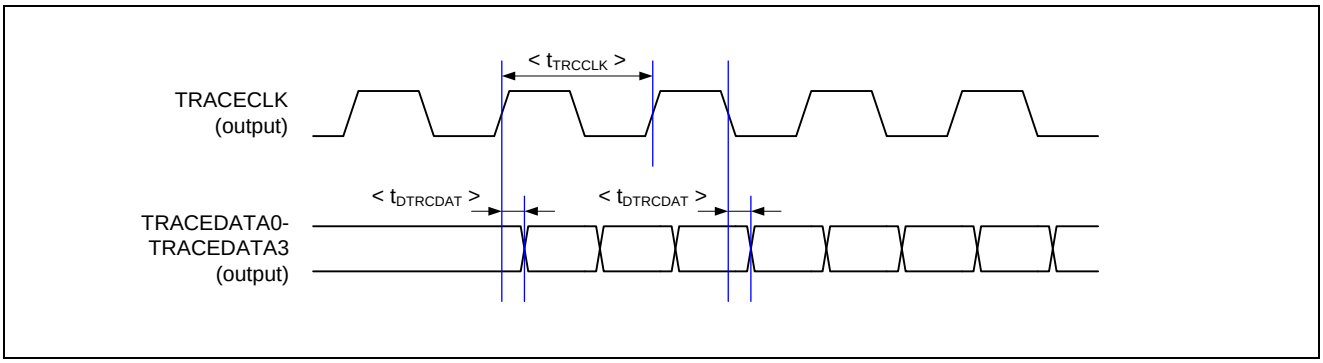
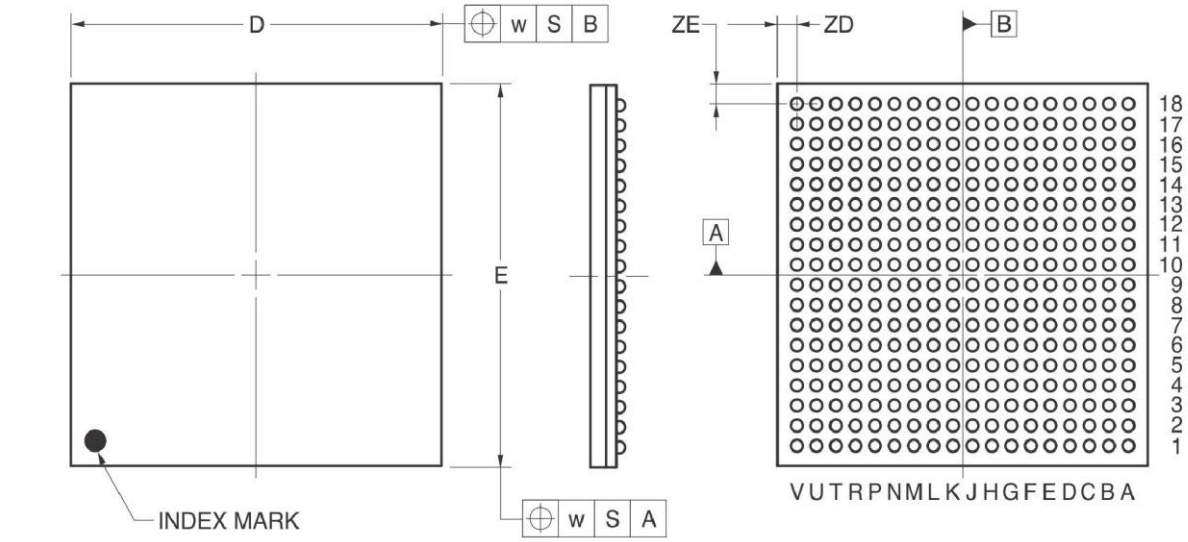


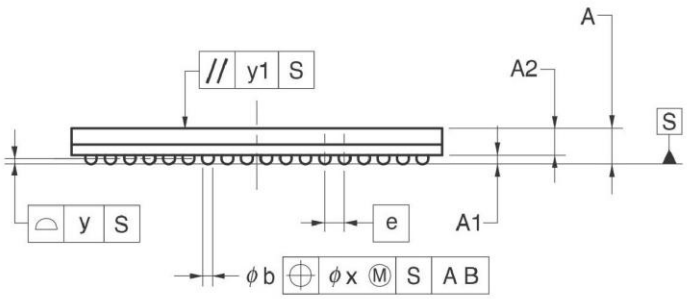
Figure 4.31 Trace Interface

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5. Package Drawing

324-PIN PLASTIC BGA (19x19)





(UNIT:mm)

ITEM	DIMENSIONS
D	19.00±0.10
E	19.00±0.10
w	0.30
e	1.00
A	1.83±0.12
A1	0.50±0.10
A2	1.33
b	0.60±0.10
x	0.10
y	0.15
y1	0.35
ZD	1.00
ZE	1.00

P324F1-100-HN4-1

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REVISION HISTORY	R-IN32M3 Series Data Sheet

Rev.	Date	Description	
		Page	Summary
Preliminary 1.00	2011.06.14	-	First edition issued
Preliminary 2.00	2012.12.03	overall	Change the description of “CC-Link IE Field” “CC-Link IE Field network” → “CC-Link IE Field”
		12-13	Addition of ***2.1 Pin Placement***
		14-16	Modification of ***2.3.1 Ethernet Signal***
		20	Modification of pin name of ***2.3.5 Port Signal, Real-time port Signal***
		26	Modification of level during reset of ***2.3.9 Timer I/O Signal***
		28	Addition of new pin information of ***2.3.14 System Signal***
		29	Addition of new pin information of ***2.3.15 Test Signal***
		30	Addition of new pin information of ***2.3.16 Operation mode Setting Signal***
		36	Addition of new pin information of ***2.4.4Test Signal***
		39-62	Addition of ***3 Specification***
		65-68	Modification of the description of output buffer of ***4 Electrical Specifications***
		69	Addition of ***4.6 Power-on/off sequence***
		70-89	Addition of ***4.7 AC characteristics***
Preliminary 3.00	2013.1.17	2	Modification of Access to External Memory of ***1.3 Overview***
		3	Modification of status of CC-Link of ***1.3 Overview*** Addition EtherPHY Information of ***1.3 Overview***
		4	Modification of block diagram of R-IN32M3-EC of ***1.4 INTERNAL BLOCK DIAGRAM***
		5	Modification of block diagram of R-IN32M3-CL of ***1.4 INTERNAL BLOCK DIAGRAM***
		14	Modification of list of PHY Interface of ***2.3.1 Ethernet Signal***
		16	Modification of level during reset of PHYLINK0/1 of ***2.3.1 Ethernet Signal***
		17	Modification of level during reset of CATSYNC1 of ***2.3.2 EtherCAT Slave Controller Signal***
		18	Addition of WAITZ1-3 port and list of note of ***2.3.3 External Memory Interface Signal***
		25	Modification of level during reset of ***2.3.8 External Interrupt Input Signal***
		26	Modification of level during reset of TIN2/TOUT2 of ***2.3.8 External Interrupt Input Signal*** and level during reset of ***2.3.10 Watchdog Timer Output Signal***
		30	Modification of level during reset of ***2.3.16 CC-Link (Remote device station)***
		31	Addition the signal of VDDQ_PECL_B0/ VDDQ_PECL_B1 of ***2.3.17 System signal***
		34	Modification of Required Connection when not in use of ETH0_TXC of ***2.4.1 Ethernet Signal***

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Rev.	Date	Description	
		Page	Summary
Preliminary 3.00	2013.1.17	36	Modification of Required Connection when not in use of TRSTZ of ***2.4.4 Test Signal***
		64	Addition the figure of HW-RTOS structure of ***3.20 Hardware Real-time OS***
		65	Addition the list of service call of ***3.20 Hardware Real-time OS***
1.00	Mar 29,2013	overall	Modification of English expressions
		overall	Change the description of “CC-Link IE Field” “CC-Link IE Field Slave” → “CC-Link IE Field (Intelligent device station)”
		overall	Change the description of “CC-Link” “CC-Link (Slave)” → “CC-Link (Remote device station)”
		1	Modification of the contents of ***1.1 Introduction***
		14	Modification of the status of ETH_MDC during the reset of ***2.3.1 Ethernet Signals*** Modification of the contents of Note of ***2.3.1 Ethernet Signals***
		18	Modification of the status of BUSCLK during the reset of ***2.3.3 External Memory Interface Signals***
		19	Modification of the status of HD0-HD15 during the reset of ***2.3.4 External MPU Interface Signals***
		31	Addition the signals of HOTRESETZ, VDDQ_MII, CLKOUT25M0, CLKOUT25M1 of ***2.3.17 System Signals*** Modification of the function of PONRZ of ***2.3.17 System Signals***
		53	Modification of the status of the kind of supported station of ***3.12 CC-Link Function***
		78	Modification of the example calculation of ***4.7.3 External memory interface signals (1)***
		78	Modification of the MIN calculation result at the time of 30pF of ***4.7.3 External memory interface signals (2)***
		81	Modification of the MIN calculation result at the time of 30pF of ***4.7.3 External memory interface signals (3)***
		84	Addition the ***4.7.4 External microcomputer interface signal***
2.00	Dec 9 ,2013	overall	Change the kind of CC-Link station to support
		3	Standby mode deletion of Table1.1 Overview of R-IN32M3
		6 to 10	Modification of the accessible area of EtherCAT of ***1.5 Memory Map***
		28	Addition explanation of Function of ***2.1.14 CC-Link IE Field Signals***
		31	Modification of the function of VDD15 of ***2.3.17 System Signals*** Addition the note to VDDQ_MII of ***2.3.17 System Signals***
		47	Modification of WDT overflow time of ***3.7 Watchdog Timer***
		71	Addition of the value of Supply current of ***4.4 DC Characteristics***
		73	Modification of the contents of ***4.6 Power-on/off sequence***
		80	Modification of the contents of ***4.7.3 External memory interface signals (3)***
		81	Modification of the contents of ***Figure 4.6 Memory controller read timing diagram (synchronous memory)***
		92	Modification of the value of output delay time of ETHn_TXDm/ETHn_TXEN, ETHn_TXER of ***4.7.10 Ethernet interface (1)***

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Rev.	Date	Description	
		Page	Summary
2.01	Feb 07 ,2014	6, 10	Modification of the accessible area of EtherCAT of ***1.5 Memory Map***
		30	Add ***CCM_CLK80M*** pins to list of ***2.3.16 CC-Link Signals (Remote device station)***
		33	Modification of Boot mode select of ***2.3.19 Operation mode Setting Signals***
		37	Addition the resister value for Pull-up/down
		39	Modification of title name of ***2.4.8 CC-Link Signal (Intelligent device station, Remote device station)***
		72	Delete the description of 5kΩ row of ***4.5 Pull-up/down Resister Values***
		71	Addition Table4.6 DC Characteristics TYP value
		86	Addition the description at 4.7.5 Serial flash ROM interface
2.02	Apr 18 ,2014	overall	Modification of ***CC-Link Signals (Remote device station)***
		39	Modification of the description about 'recommended connection' and addition a caution description at ***2.4.7 CC-Link IE Field Signal***
2.03	May 30 ,2014	73	Add a notes of "4.6 Power-on-off sequence"
2.04	Dec 25 ,2014	3	Change status for Intelligent device station for CC-Link in ***1.3 Overview***
		6 to 10	Modification of the accessible area of EtherCAT of ***1.5 Memory Map***
		31	Modify the property for FB pin from "-" to "Input"
		76	Modify the description of MIN value for low level width in ***4.7.2 Reset signals***
		86	Add description for "Asynchronous mode" in ***4.7.4 External microcomputer interface signal***.
3.00	Aug 31,2015	83 to 93	Correction the timing information of ***4.7.4 External Microcomputer Interface Signal***
3.01	Sep 18,2015	88 to 91	Add description for "Synchronous mode (CC-Link IE Field)" in ***4.7.4 External microcomputer interface signal***.
4.00	Nov 30,2015	14 to 36	Add description of "Symbol and Abbreviation", port functions of synchronous burst access memory controller at ***2.3 Signals by Function***.
		15	Add a Note of Ethernet Transmit ports at ***2.3.1(1) PHY Interface***.
		19	Modify the "Level during reset" for BUSCLK and add Note1 at ***2.3.3 External Memory Interface Signals***.
		27	Modify the "Level during reset" for TRACECLK at ***2.3.11 Trace Signals***.
		29	Add a Note for CCI_WAITEDGEH and CCI_WRLENH at ***2.3.14 CC-Link IE Field (Intelligent device station) Signals***.
		30	Modify the "Function" for CCM_CLK80M at ***2.3.15 CC-Link Signals (Intelligent device station)***.
		31	Add a Note2 for CCM_CLK80M at ***2.3.16 CC-Link Signals (Remote device station)***.
		32	Modify the "Function" for XT1/XT2, OSCTH, JTAGSEL and "Active" for OSCTH and "Level during reset" for RSTOUTZ, CLKOUT25M0/1 at ***2.3.17 System Signals***.
		36	Add the combinations of available operating mode at ***2.3.19 Operation Mode Setting Signal***.
		39	Modify "I/O" for XT2 and "Recommended connection when not in use" for OSCTH, JTAGSEL at ***2.4.3 System Signals***.

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Rev.	Date	Description	
		Page	Summary
4.00	Nov 30,2015	42	Modify “Recommended connection when not in use” at ***2.4.6 Operating Mode Setting Signals***.
		46	Modify “Table3.1” at ***3.3 EtherCAT Slave Controller Function***.
		51	Add “External event count function” at ***3.8.1 Features***.
		65-66	Modify “QINT” and add “Remark” at ***3.20.1 Features***.
		72	Add ***4.6 Terminal Capacity Values***.
		74	Modify “MAX” values for CCI_CLK2_097M at ***4.8.1(1) Input clock characteristics***.
		78-82	Modify a Note for Figure4.4, Figure4.5 and Add WAITZ1-WAITZ3 for Figure4.6, Figure4.7 at ***4.8.3(3) Synchronous burst access MEMC access timing***.
		100	Modify “Symbol” for DMAACKZn, RTDMAACKZoutput low level width at ***4.8.6 External DMA Interface***.
		101-102	Add “Symbol” for CSISCKn output high/low level width and “Remark” at ***4.8.7 CSI Interface***.
		105-106	Modify the signals “ETHn_RXDm” at ***4.8.10 Ethernet Interface***.
		107	Modify “Parameter” and “MAX” value for TRACEDATA output delay time at ***4.8.11(2) Trace interface***.
4.01	Feb 28, 2017	30	Modify description of the CCM_MDIN0-3 signals at ***2.3.15 CC-Link Pins (Intelligent Device Station)***. (complement)
		58	Modify interface system, synchronous relationship, and buffers at ***3.14.1(1) External MCU Interface***. (complement)
		59	Modify description of address conversion at ***3.14.1(2) AHB master port function***. (expression alignment)
			Explicitly notate applicable modes at ***3.14.1(3) Status check function***. (complement)
		60	Change from “state” to “wait” at ***3.15.1 Features***. (expression alignment)
		61	Change pin names for wait signal at ***3.16.1 Features***. (error correction)
		62	Add the ECC error interrupt function at ***3.17.1 Features***. (new function)
			Correct operation of the AHB bus at occurrence of a 2-bit ECC error at ***3.17.2 Read Buffer***. (error correction)
		63	Change expression of Header Endec at ***3.18 Data RAM***. (expression alignment)
			Add an ECC error interrupt function at ***3.18.1 Features***. (new function)
		64	Add an ECC error interrupt function at ***3.19.1 Features***. (new function)
		65	Add a supported function “Internal DMA/Buffer Allocator/Header EnDec” at ***3.20.1 Features***. (new function)
		71	Delete the column of 5kΩ resistor from Table 4.6 Input leakage current (error correction) and modify the symbol for the voltage of high-level output (I_{OL}→I_{OH}) in Table 4.7 (error correction) at ***4.4 DC Characteristics***.

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Rev.	Date	Description	
		Page	Summary
5.00	Dec 28, 2018	3	1.3 Overview, Table 1.2 Overview of R-IN32M3 (2/2) Description of 1.5 V power supply for internal PHY was added.
		6, 7, 10 to 12	1.5 Memory Maps Note describing that the addresses the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the select boot mode, was added. Figure 1.1 Memory Map (All) (R-IN32M3-EC) Figure 1.2 Memory Map (All) (R-IN32M3-CL) Figure 1.6 External MCU Interface Area (R-IN32M3-EC) Figure 1.7 External MCU Interface Area (R-IN32M3-CL)
		6, 7	1.5 Memory Maps Figure 1.1 Memory Map (All) (R-IN32M3-EC) Figure 1.2 Memory Map (All) (R-IN32M3-CL) Locations of instruction RAM area and instruction RAM mirror area were corrected.
		10 to 12	1.5 Memory Maps Figure 1.6 External MCU Interface Area (R-IN32M3-EC) Figure 1.7 External MCU Interface Area (R-IN32M3-CL) “Instruction RAM area” was corrected to “Instruction RAM mirror area”.
		23	2.3.5 Port Pins and Real-time Port Pins The pin name indicated as “CCM_IRZ” was modified to “CCM_IRLZ”.
		31	2.3.15 CC-Link Pins (Intelligent Device Station) The name and functional descriptions of the CC-Link (intelligent device station) pins were modified.
		70	4.2 Absolute Maximum Ratings, Table 4.4 Absolute Maximum Ratings 1.5 V type was added as the condition for power supply voltage.
		71	4.3 Recommended Operating Conditions, Table 4.5 Recommended Operating Conditions 1.5 V power supply was added as the condition for power supply voltage.
		93, 95	4.8.4 External MCU Interface Pins, (3) Asynchronous Mode Figure 4.14 External MCU Read Timing (MEMCSEL = L, HIFSYNC = L) Specification of “Address input hold time when advance reading” was added
		100	4.8.5 Serial Flash ROM Interface Specifications of $t_{DSMCSCK}$ and $t_{DSMCKCS}$ were modified.
		—	Error corrected, description modified, and contents and expressions adjusted
5.01	Jan. 12, 2021	3	1.3 Overview Description on no support of EtherCAT P was added.

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Instructions for the use of product

In this section, the precautions are described for over whole of CMOS device.
Please refer to this manual about individual precaution:
When there is a mention unlike the text of this manual, a mention of the text takes first priority

1.Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

-The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2.Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

-The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3.Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

-The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4.Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

-When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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