AN-1802 LP38512TJ-ADJ Evaluation Board

1 Introduction

This board is designed to allow the evaluation of the LP38512TJ-ADJ voltage regulator. Each board is assembled and tested in the factory. This evaluation board has the TO-263 THIN 5-lead package mounted, and the output voltage is set to 1.20 V.

2 General Description

The LP38512TJ-ADJ is an adjustable LDO linear regulator capable of suppling up to 1.5A of output current, and incorporates an Enable.

The device has been designed to work with 10 µF input and output ceramic capacitors. Footprints areas for C_{IN} and C_{OUT} will allow for a variety of sizes.

3 Operation

The input voltage, applied between V_{IN} and GND, must be no less than 2.25 V, which is the low end of the operating range voltage, no greater than 5.5 V, which is the high end of the operating range voltage.

The input voltage should also be at least 500 mV greater than the set V_{OUT}.

Loads can be connected to V_{OUT} with reference to GND.

V_{OUT} and V_{IN} test points are provided on the board to allow accurate measurements directly onto the input and output pins of the device, eliminating any voltage drop on the PCB traces or connecting wires to the load.

4 Setting V_{OUT}

The output voltage is set using the external resistive divider R1 and R2. The output voltage is given by the formula:

$$V_{OUT} = V_{ADJ} \times (1 + (R1 / R2)) \quad (1)$$

It is recommended that the values selected for R1 and R2 are such that the parallel value is less than 1.00 kΩ. This is to prevent internal parasitic capacitances on the ADJ pin from interfering with the F_Z pole set by R1 and C_{FF}.

$$((R1 \times R2) / (R1 + R2)) \leq 1.00\ k\Omega \quad (2)$$

Table 1 lists some suggested, best fit, standard ±1% resistor values for R1 and R2, and a standard ±10% capacitor values for C_{FF}, for a range of V_{OUT} values. Other values of R1, R2, and C_{FF} are available that will give similar results.

Table 1. Suggested Components

V_{OUT}	R1	R2	C_{FF}	F_Z
0.80 V	1.07 kΩ	1.78 kΩ	4700 pF	31.6 kHz
1.00 V	1.00 kΩ	1.00 kΩ	4700 pF	33.8 kHz
1.20 V	1.40 kΩ	1.00 kΩ	3300 pF	34.4 kHz
1.50 V	2.00 kΩ	1.00 kΩ	2700 pF	29.5 kHz
1.80 V	2.94 kΩ	1.13 kΩ	1500 pF	36.1 kHz
2.00 V	1.02 kΩ	340Ω	4700 pF	33.2 kHz
2.50 V	1.02 kΩ	255Ω	4700 pF	33.2 kHz
3.00 V	1.00 kΩ	200Ω	4700 pF	33.8 kHz
3.30 V	2.00 kΩ	357Ω	2700 pF	29.5 kHz

For additional information on how resistor tolerances affect the calculated V_{OUT} value, see *AN-1378 Method for Calculating Output Voltage Tolerances in Adjustable Regulators* (SNVA112).

The LP38512TJ-ADJ evaluation board is assembled with a 1.40 kΩ ±1% resistor for R1, and a 1.00 kΩ ±1% resistor for R2. This sets V_{OUT} to 1.20 V.

$$V_{OUT} = 500\ mV \times (1 + (1.40\ k\Omega / 1.00\ k\Omega)) = 1.20\ V \quad (3)$$

5 Selecting C_{FF}

A capacitor placed across the gain resistor R1 provides additional phase margin to improve load transient response of the device. This capacitor, C_{FF}, in parallel with R1, forms a zero in the loop response given by the formula in Equation 4:

$$F_Z = (1 / (2 \times \pi \times C_{FF} \times R1)) \quad (4)$$

The value for C_{FF} should be selected to set a zero frequency (F_Z) between 25 kHz and 50 kHz using the formula in Equation 5:

$$C_{FF} = 1 / (2 \times \pi \times F_Z \times R1) \quad (5)$$

The closest standard 10% value is adequate for C_{FF}.

The LP38512TJ-ADJ Evaluation board is assembled with a 3300 pF capacitor for C_{FF}. This sets F_Z to approximately 34 kHz.

$$F_Z = (1 / (2 \times \pi \times 3300\ pF \times 1.40\ k\Omega)) = 34.4\ kHz \quad (6)$$

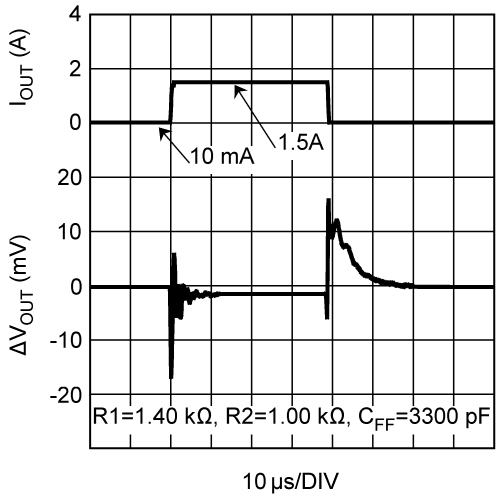


Figure 1. 10 mA to 1.5A Load Transient Response

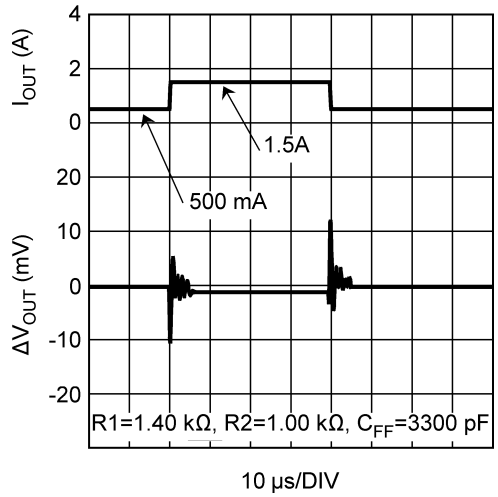


Figure 2. 500 mA to 1.5A Load Transient Response

6 Enable Function

ON/OFF control is provided by supplying a logic level signal to the Enable pin. A minimum V_{EN} value of 1.2 V is typically required at this pin to enable the LDO output. The LDO output will be shutdown when the V_{EN} value is typically 0.6 V or less. The V_{EN} threshold incorporates approximately 100 mV of hysteresis.

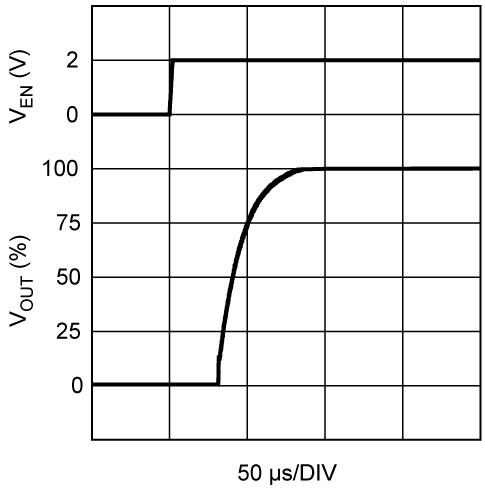


Figure 3. V_{OUT} vs V_{EN}

The Enable pin has no internal default bias and must not be left floating. The Enable pin must be actively driven to the appropriate voltage level. In applications where the LP38513TJ is operated continuously, the Enable pin can be connected directly to V_{IN}. The LP38512TJ-ADJ evaluation board is assembled with a 10 kΩ resistor (R3) to provide pull-up to V_{IN}.

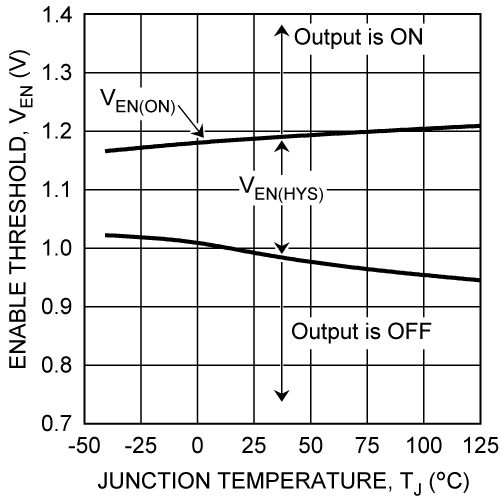


Figure 4. Enable Thresholds

7 Power Dissipation

The TO-263 THIN package alone has a junction to ambient thermal resistance (θ_{JA}) rating of 67°C/W. When mounted on the LP38512TJ-ADJ evaluation board, the θ_{JA} rating is approximately 35°C/W.

Although there is only approximately 0.20 square inches (0.45in x 0.45in) of 1 ounce copper area immediately under the package body, the top copper surface area is extended to additional copper area on the bottom of the board by fifteen thermal vias.

With the 35°C/W thermal rating, the LP38512TJ-ADJ evaluation board dissipates a maximum of 2.8W with T_A = 25°C.

For a comparison of the TO-263 THIN package to the standard TO-263 package, see *AN-1797 TO-263 THIN Package* (SNVA328).

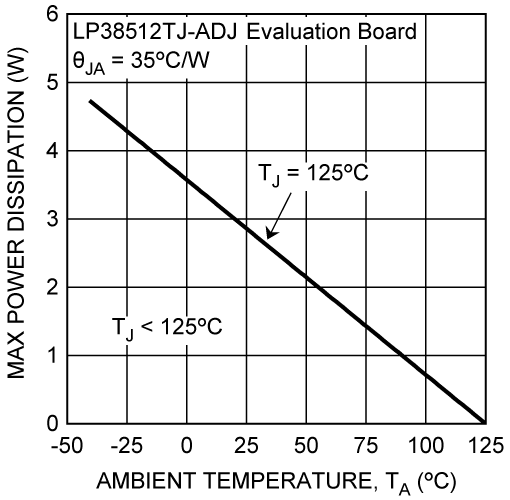
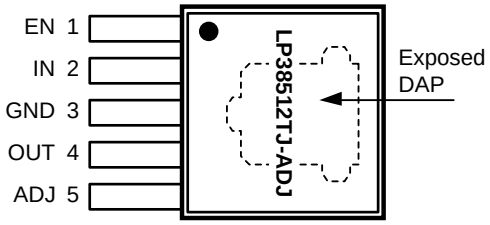


Figure 5. Maximum Power Dissipation vs Ambient Temperature

7.1 Connection Diagram



7.2 Schematic Diagram

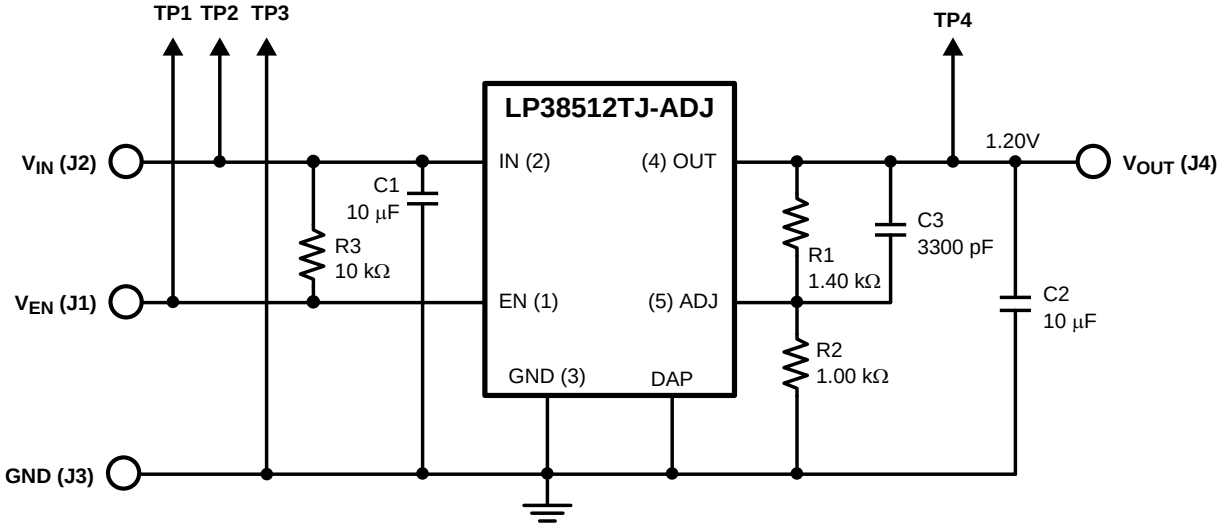


Figure 6. Evaluation Board Schematic.

8 PCB Layout

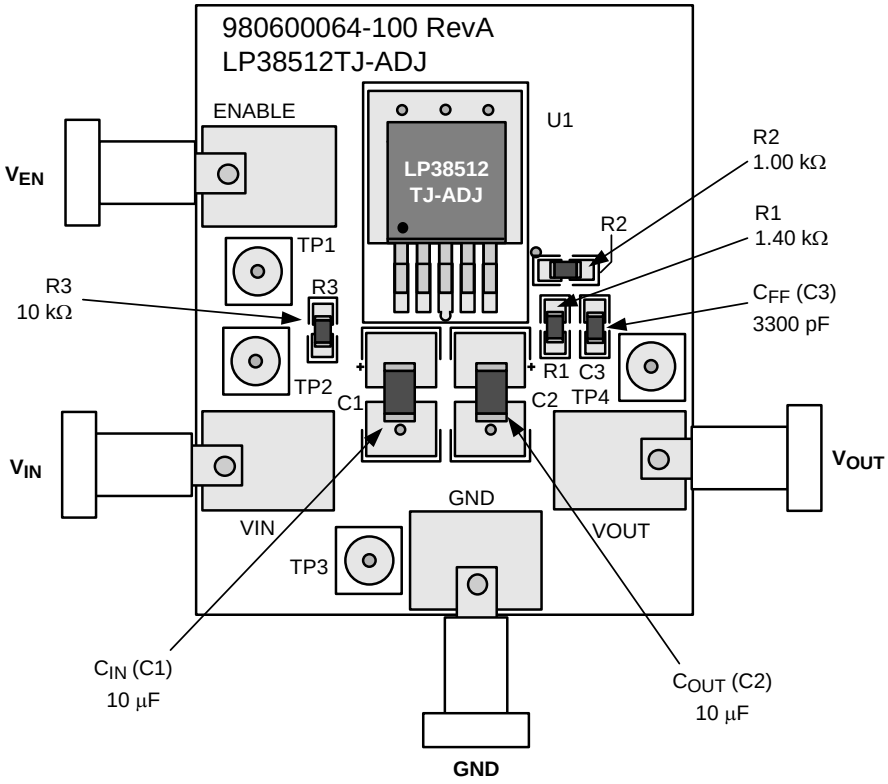


Figure 7. Evaluation Board Component and Pin Layout

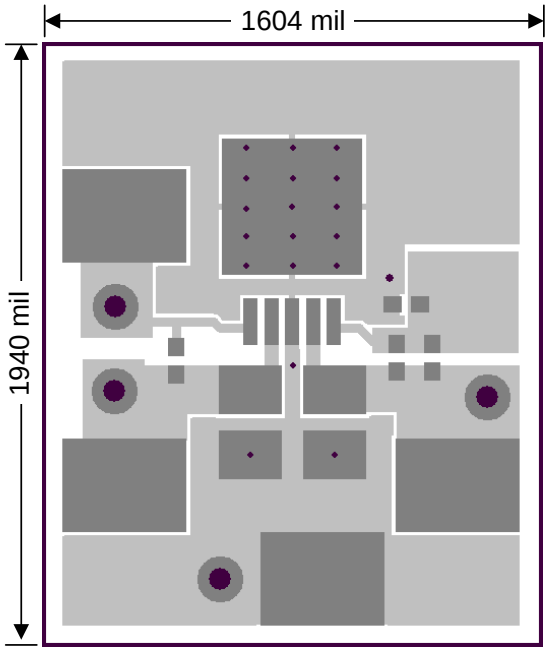


Figure 8. Top Side Copper Area

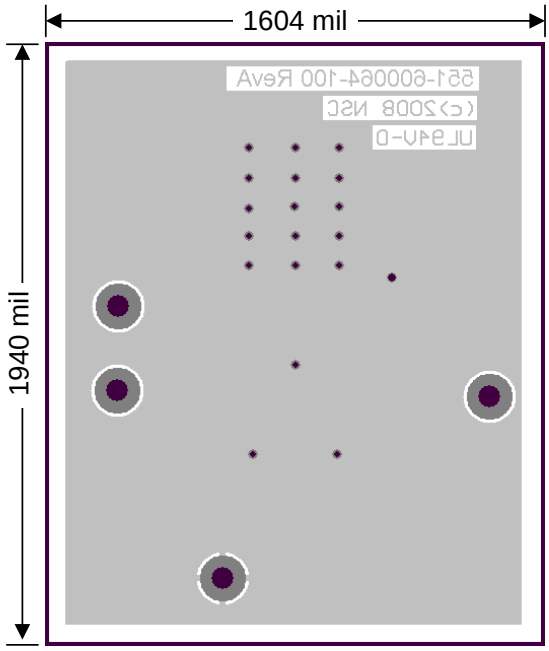


Figure 9. Bottom Side Copper Area

Table 2. Bill of Materials

ID	Name	Description	Manufacturer	Part Number
PCB	PCB	Printed Circuit Board LP38512TJ-ADJ Evaluation Board	Texas Instruments	600064
U1	U1	LP38512	Texas Instruments	LP38512
C1	C_{IN}	Capacitor: 10 µF; ±10%; MLCC; 10 V; X7R; 1210	AVX	1210ZC106KAT2A
C2	C_{OUT}	Capacitor: 10 µF;, ±10%; MLCC; 10 V; X7R; 1210		1210ZC106KAT2A
C3	C_{FF}	Capacitor: 3300 pF;, ±10%; MLCC; 50 V; X7R; 0805	KEMET	C0805C332K5RAC
J1	V_{EN}	Banana Jack : Insulated Solder Terminal; White	Johnson Components	108-0901-001
J2	V_{IN}	Banana Jack : Insulated Solder Terminal; Red		108-0902-001
J3	GND	Banana Jack : Insulated Solder Terminal; Black		108-0903-001
J4	V_{OUT}	Banana Jack : Insulated Solder Terminal; Orange		108-0906-001
R1	R1	Resistor: 1.40 kΩ, ±1%; Thick Film; 125 mW; ±100 ppm; 0805	VISHAY DALE	CRCW08051K40FK
R2	R2	Resistor: 1.00 kΩ, ±1%; Thick Film; 125 mW; ±100 ppm; 0805		CRCW08051K00FK
R3	R3	Resistor: 10.0 kΩ, ±1%; Thick Film; 125 mW; ±100 ppm; 0805		CRCW080510K0FK
TP1	TP_{EN}	Turret Terminal : Mounting Hole Diameter = 0.062”	Keystone	1593–2
TP2	TP_{IN}			
TP3	TP_{GND}			
TP4	TP_{OUT}			

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