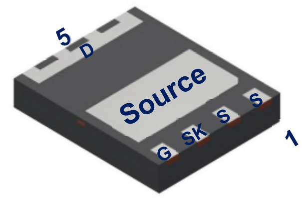
IGLR60R260D1

600V CoolGaN™ enhancement-mode Power Transistor



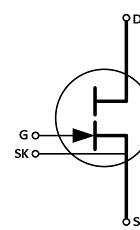
Features

- Enhancement mode transistor – Normally OFF switch
- Ultra fast switching
- No reverse-recovery charge
- Capable of reverse conduction
- Low gate charge, low output charge
- Superior commutation ruggedness
- Qualified for industrial applications according to JEDEC Standards (JESD47 and JESD22)

Gate	4
Drain	5
Kelvin Source	3
Source	1,2

Benefits

- Improves system efficiency
- Improves power density
- Enables higher operating frequency
- System cost reduction savings
- Reduces EMI



Applications

Industrial and consumer SMPS based on the half-bridge topology (half-bridge topologies for hard and soft switching such as Totem pole PFC, high frequency LLC, Hybrid Flyback and ACF).
For other applications: review CoolGaN™ reliability white paper and contact Infineon regional support

Table 1 Key Performance Parameters at T_j = 25 °C

Parameter	Value	Unit
$V_{DS,max}$	600	V
$R_{DS(on),max}$	260	mΩ
$Q_{G,typ}$	1.5	nC
$I_{D,pulse}$	15.9	A
Q_{oss} @ 400 V	11.5	nC
Q_{rr}	0	nC

Table 2 Ordering Information

Type / Ordering Code	Package	Marking	Related links
IGLR60R260D1	PG-TSON-8-7	60R260D	see Appendix A

Table of Contents

1 Maximum ratings

at T_j = 25 °C, unless otherwise specified. Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact your local Infineon sales office.

Table 3 Maximum ratings

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Drain Source Voltage, continuous [1]	$V_{DS,max}$	-	-	600	V	V_{GS} = 0 V
Drain source destructive breakdown voltage [2]	$V_{DS,bd}$	800	-	-	V	V_{GS} = 0 V, I_{DS} = 3.2 mA
Drain source voltage, pulsed [2]	$V_{DS,pulse}$	- -	- -	750 650	V V	T_j = 25 °C; V_{GS} ≤ 0 V; ≤1 hour of total time T_j = 125 °C, V_{GS} ≤ 0 V; ≤1 hour of total time
Switching surge voltage, pulsed [2]	$V_{DS,surge}$	-	-	750	V	DC bus voltage = 700 V; turn off $V_{DS,pulse}$ = 750 V; turn on $I_{D,pulse}$ = 7.1 A; T_j = 105 °C; f ≤ 100 kHz, t ≤ 100 secs (10 million pulses)
Continuous current, drain source	I_D	-	-	10.4	A	T_C = 25 °C;
Pulsed current, drain source [3,4]	$I_{D,pulse}$	-	-	15.9	A	T_C = 25 °C; I_G = 6.9 mA; See Figure 3;
Pulsed current, drain source [4,5]	$I_{D,pulse}$	-	-	7.7	A	T_C = 125 °C; I_G = 6.9 mA; See Figure 4;
Gate current, continuous [4,5,6]	$I_{G,avg}$	-	-	5.3	mA	T_j = -40 °C to 150 °C;
Gate current, pulsed [4,6]	$I_{G,pulse}$	-	-	530	mA	T_j = -40 °C to 150 °C; t_{PULSE} = 50 ns, f=100 kHz
Gate source voltage, continuous [6]	V_{GS}	-10	-	-	V	T_j = -40 °C to 150 °C;
Gate source voltage, pulsed [6]	$V_{GS,pulse}$	-25	-	-	V	T_j = -40 °C to 150 °C; t_{PULSE} = 50 ns, f = 100 kHz; open drain
Power dissipation	P_{tot}	-	-	52	W	T_C = 25 °C
Operating temperature	T_j	-40	-	150	°C	
Storage temperature	T_{stg}	-40	-	150	°C	Max shelf life depends on storage conditions.
Drain-source voltage slew-rate	dV/dt			200	V/ns	

1 All devices are 100% tested at I_{DS} = 3.2 mA to assure V_{DS} ≥ 800 V
2 Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation
3 Limits derived from product characterization, parameter not measured during production
4 Ensure that average gate drive current, $I_{G,avg}$ is ≤ 5.3 mA. Please see figure 27 for $I_{G,avg}$, $I_{G,pulse}$ and I_G details
5 Parameter is influenced by rel-requirements. Please contact the local Infineon Sales Office to get an assessment of your application
6 We recommend using an advanced driving technique to optimize the device performance. Please see gate drive application note for details

2 Thermal characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	-	-	2.4	°C/W	
Reflow soldering temperature	T_{sold}	-	-	260	°C	MSL3

3 Electrical characteristics

at T_j = 25 °C, unless specified otherwise

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	0.9 0.7	1.2 1.0	1.6 1.4	V	I_{DS} = 0.69 mA; V_{DS} = 10 V; T_j=25 °C I_{DS} = 0.69 mA; V_{DS} = 10 V; T_j=125 °C
Gate-Source reverse clamping voltage	$V_{GS,\ clamp}$	-	-	-8	V	I_{GSS} = -1 mA
Drain-Source leakage current	I_{DSS}	- -	0.26 5.3	26 -	µA	V_{DS} = 600 V; V_{GS} = 0 V; T_j = 25 °C V_{DS} = 600 V; V_{GS} = 0 V; T_j = 150 °C
Drain-Source leakage current at application conditions[1]	I_{DSSapp}	-	15.9	-	µA	V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C
Drain-Source on-state resistance	$R_{DS(on)}$	- -	0.2 0.37	0.260 -	Ω	I_G = 6.9 mA; I_D = 2.11 A; T_j = 25 °C I_G = 6.9 mA; I_D = 2.11 A; T_j = 150 °C
Gate resistance	$R_{G,int}$	-	0.77	-	Ω	LCR impedance measurement; f = f_{res} ; open drain;

Table 6 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	110	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 1 MHz
Output capacitance	C_{oss}	-	20	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 1 MHz
Reverse Transfer capacitance	C_{rss}	-	0.25	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 1 MHz
Effective output capacitance, energy related [2]	$C_{o(er)}$	-	22.4	-	pF	V_{DS} = 0 to 400 V
Effective output capacitance, time related [3]	$C_{o(tr)}$	-	28.7	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V; Id = const
Output charge	Q_{oss}	-	11.5	-	nC	V_{DS} = 0 to 400 V
Turn- on delay time	$t_{d(on)}$	-	12	-	ns	see Figure 23
Turn- off delay time	$t_{d(off)}$	-	14	-	ns	see Figure 23
Rise time	t_r	-	7	-	ns	see Figure 23
Fall time	t_f	-	30	-	ns	see Figure 23

[1] Parameter represents end of use leakage in applications
[2] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as Coss while VDS is rising from 0 to 400 V
[3] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as Coss while VDS is rising from 0 to 400 V

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate charge	Q_G	-	1.5	-	nC	I_{GS} = 0 to 2.6 mA; V_{DS} = 400 V; I_D = 2.11 A

Table 8 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	-	2	2.5	V	V_{GS} = 0 V; I_{SD} = 2.11 A
Pulsed current, reverse	$I_{S,pulse}$	-	-	15.9	A	I_G = 6.9 mA
Reverse recovery charge	Q_{rr} [1]	-	0	-	nC	I_S = 2.11 A, V_{DS} = 400 V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

[1] Excluding Qoss

4 Electrical characteristics diagrams

at T_j = 25 °C, unless specified otherwise

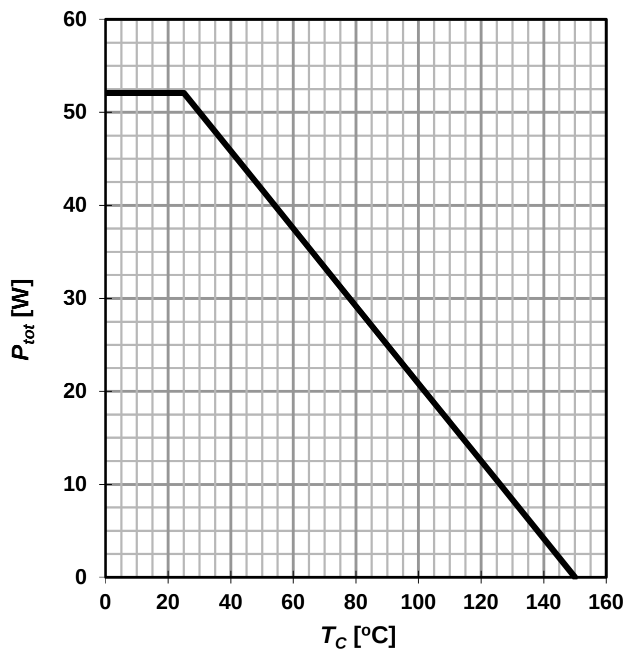
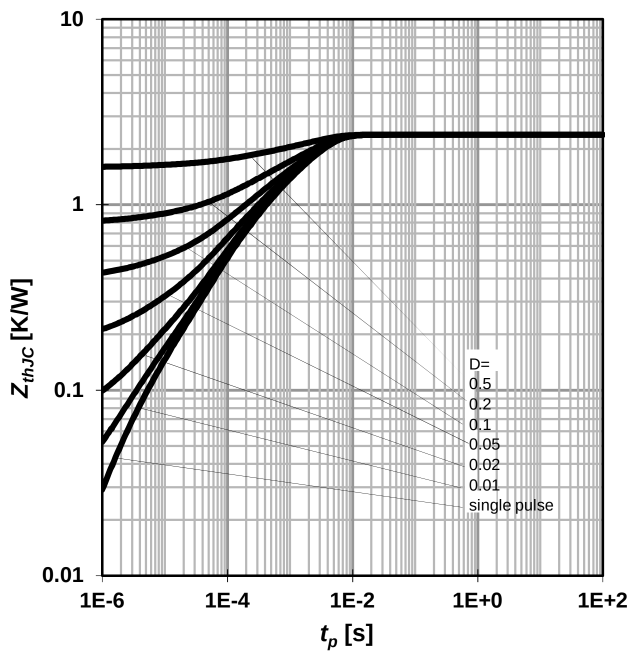
Figure 1 Power dissipation	Figure 2 Max. transient thermal impedance
	
$P_{tot}=f(T_c)$	$Z_{thJC}=f(t_p, D)$

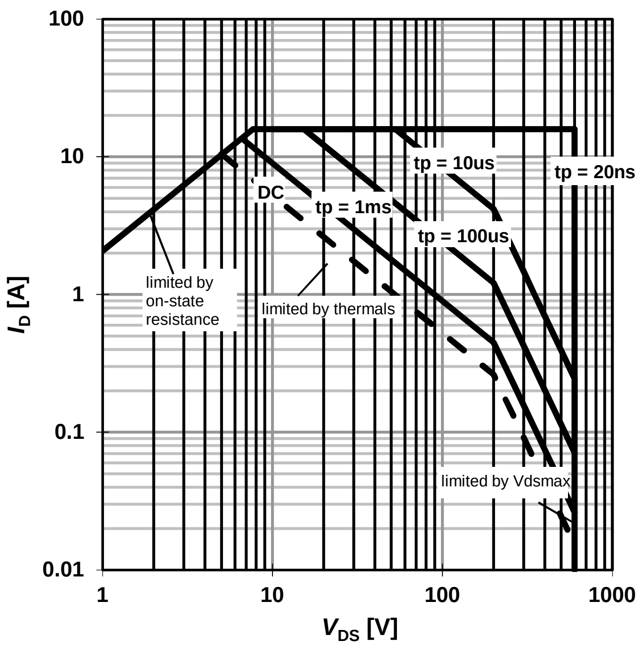
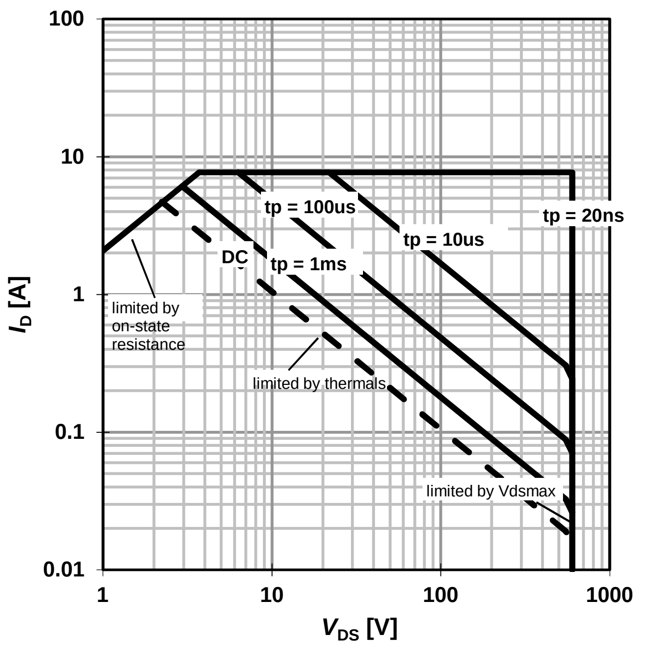
Figure 3 Safe operating area	Figure 4 Safe operating area
	
$I_D=f(V_{DS})$; T_C = 25 °C	$I_D=f(V_{DS})$; T_C = 125 °C

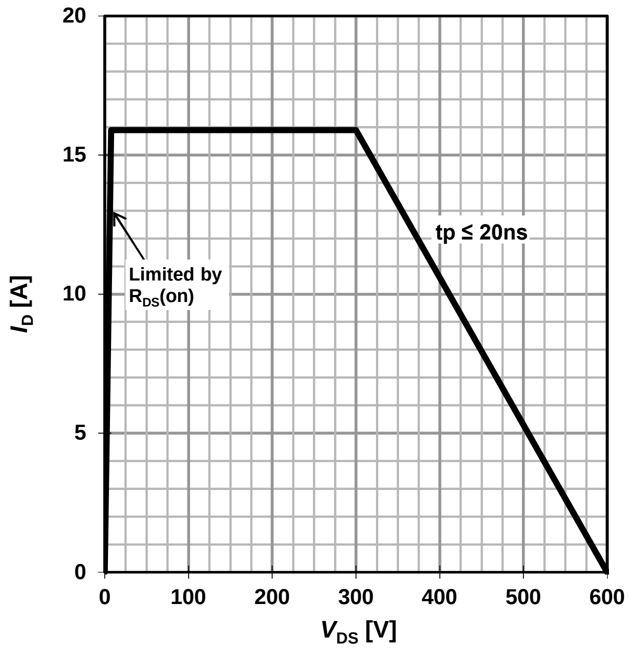
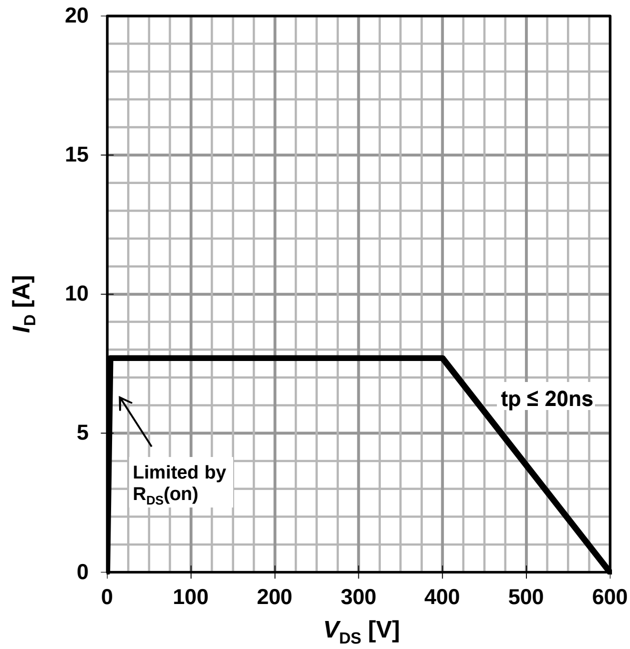
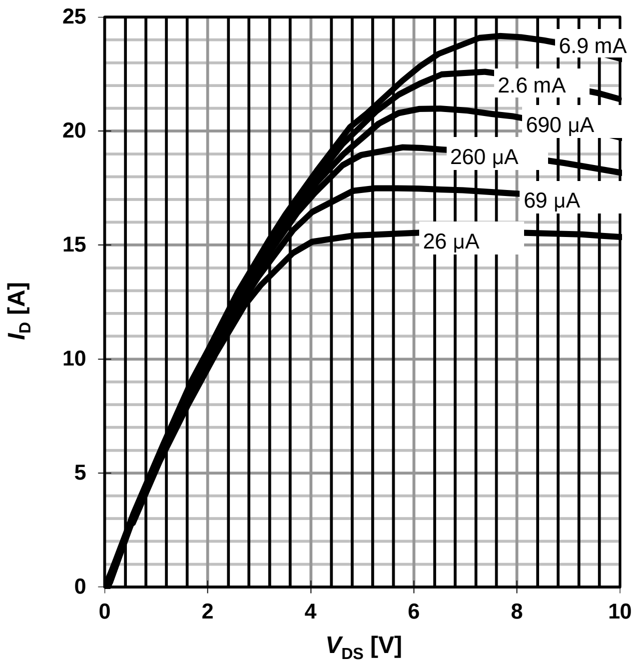
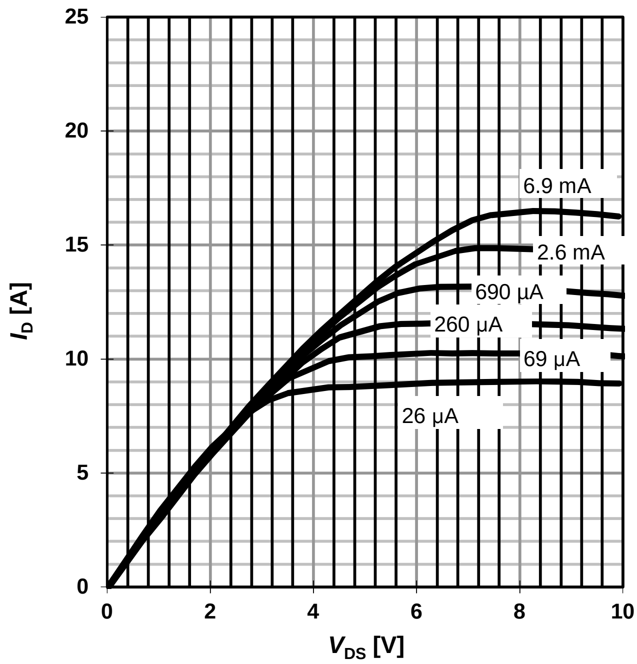
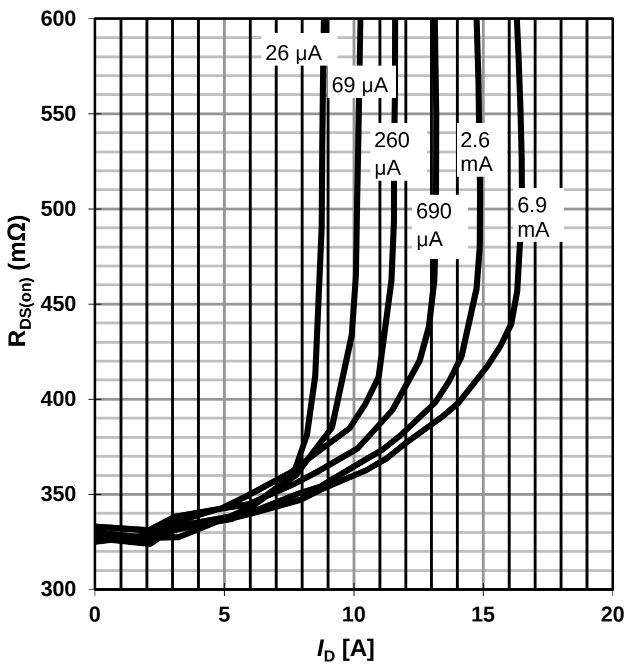
Figure 5 **Repetitive safe operating area**[1]	Figure 6 **Repetitive safe operating area**[1]
	
Tc = 25 °C; T_j ≤ 150 °C	Tc = 125 °C; T_j ≤ 150 °C

Figure 7 **Typ. output characteristics**	Figure 8 **Typ. output characteristics**
	
$I_D=f(V_{DS},I_G)$; T_j = 25 °C	$I_D=f(V_{DS},I_G)$; T_j = 125 °C

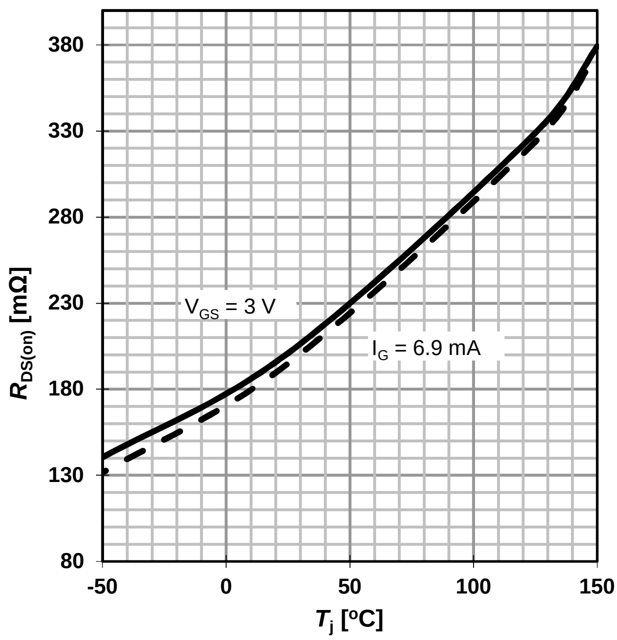
[1] Parameter is influenced by rel-requirements. Please contact the local Infineon Sales Office to get an assessment of your application.

Figure 9 Typ. Drain-source on-state resistance



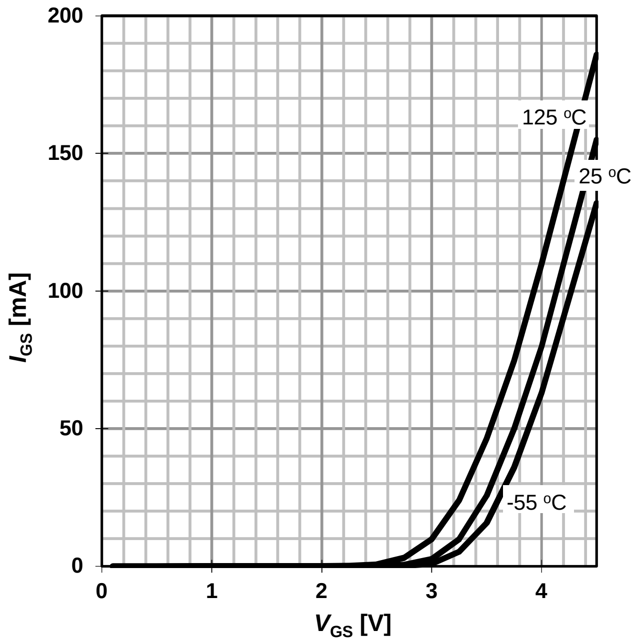
$R_{DS(on)}=f(I_D,I_G)$; T_j = 125 °C

Figure 10 Drain-source on-state resistance



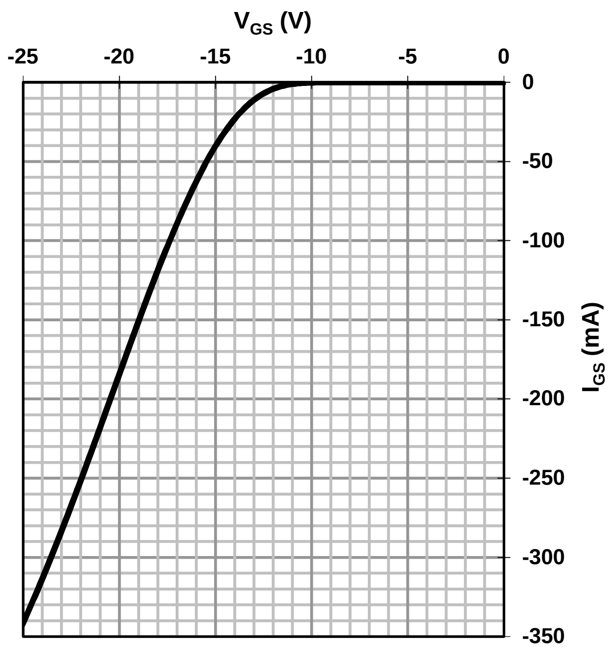
$R_{DS(on)}=f(T_j)$; I_D = 2.11 A

Figure 11 Typ. gate characteristics forward



$I_{GS}=f(V_{GS},T_j)$; open drain

Figure 12 Typ. gate characteristics reverse



$I_{GS}=f(V_{GS})$; T_j = 25 °C

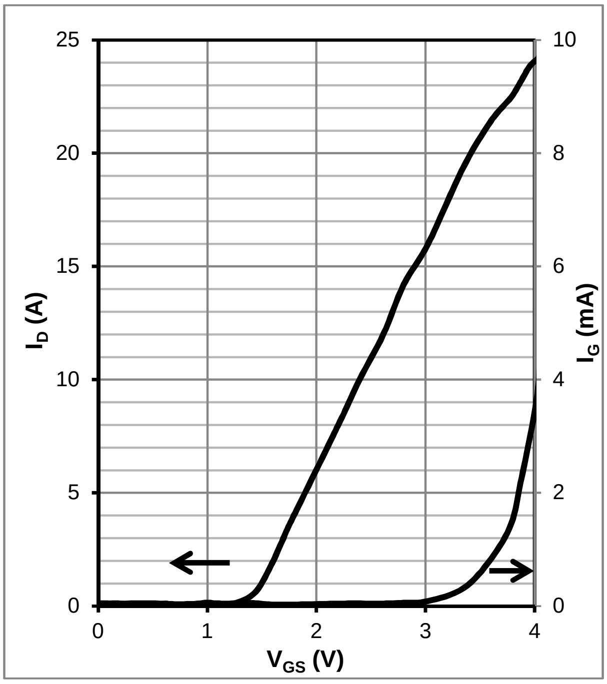
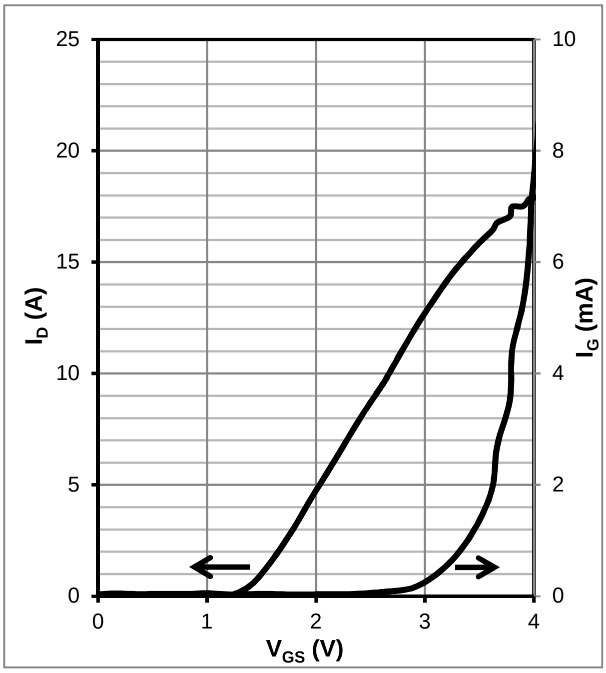
Figure 13 Typ. transfer characteristics	**Figure 14 Typ. transfer characteristics**
	
I_D, I_G =$f(V_{GS})$; V_{DS} = 8 V; T_j = 25 °C	I_D, I_G =$f(V_{GS})$; V_{DS} = 8 V ; T_j = 125 °C

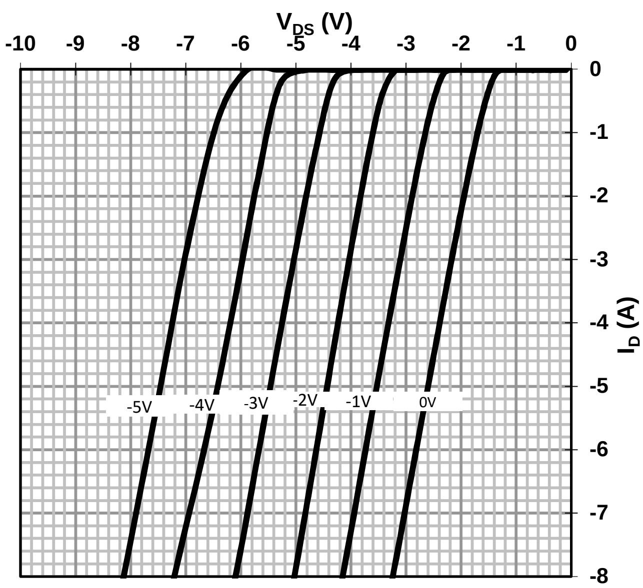
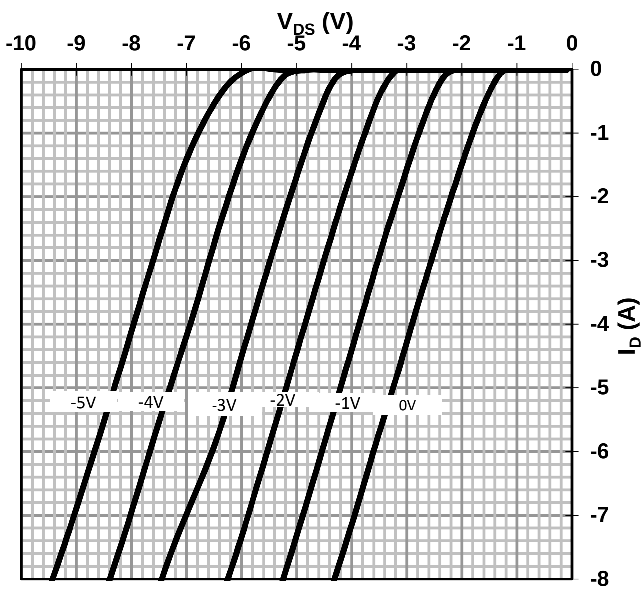
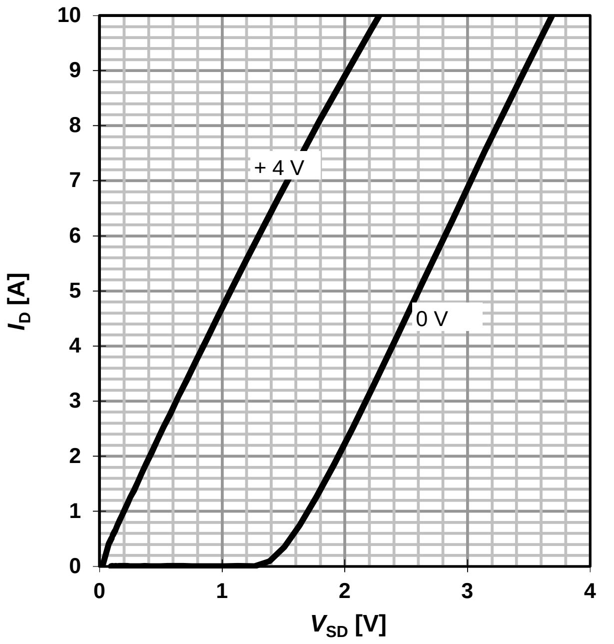
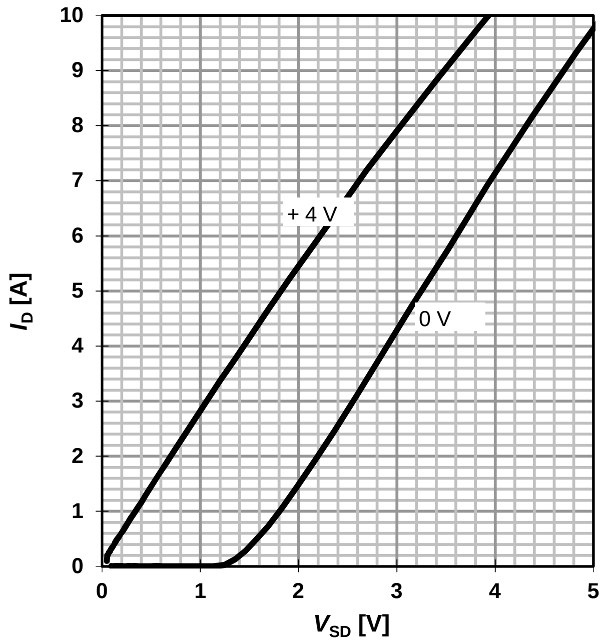
Figure 15 Typ. channel reverse characteristics	**Figure 16 Typ. channel reverse characteristics**
	
V_{DS}=$f(I_D, V_{GS})$; T_j = 25 °C	V_{DS}=$f(I_D, V_{GS})$; T_j = 125 °C

Figure 17 Typ. channel reverse characteristics



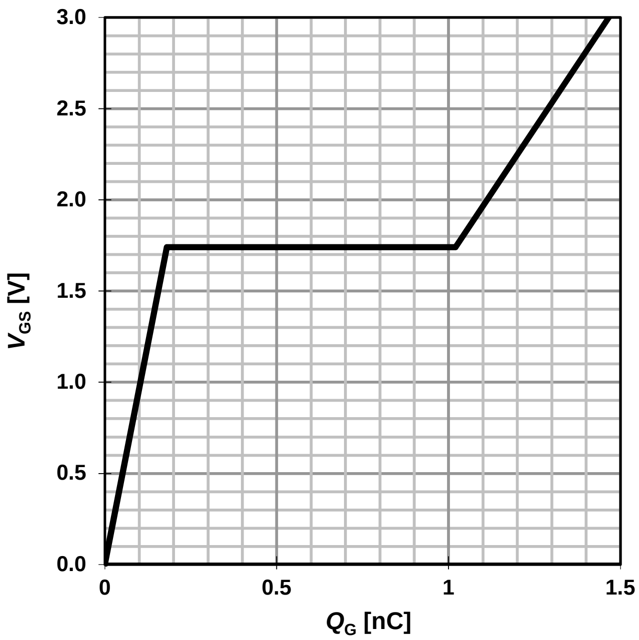
I_D=*f*(V_{DS}, V_{GS}); T_j = 25 °C

Figure 18 Typ. channel reverse characteristics



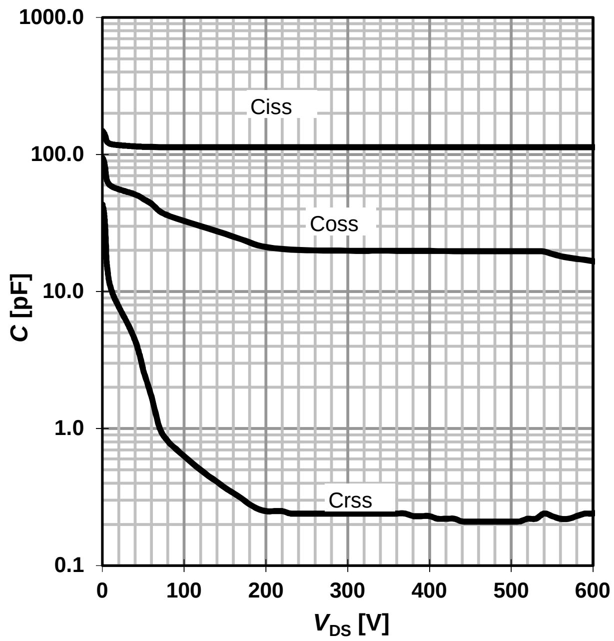
I_D=*f*(V_{DS}, V_{GS}); T_j = 125 °C

Figure 19 Typ. gate charge

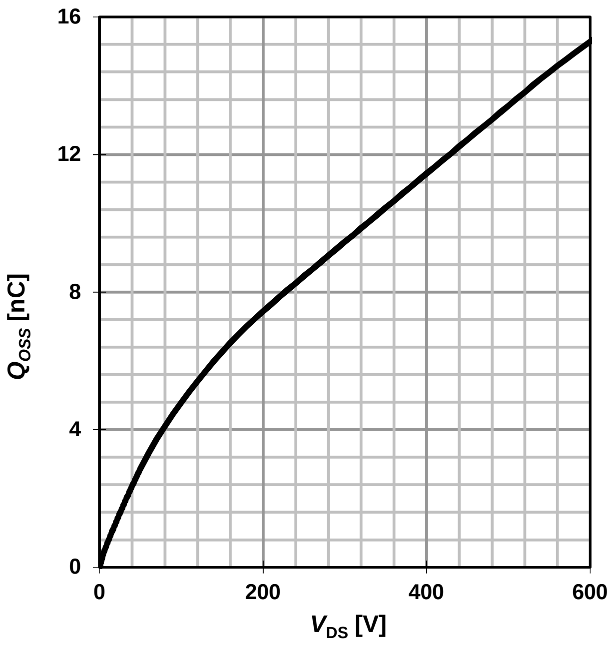
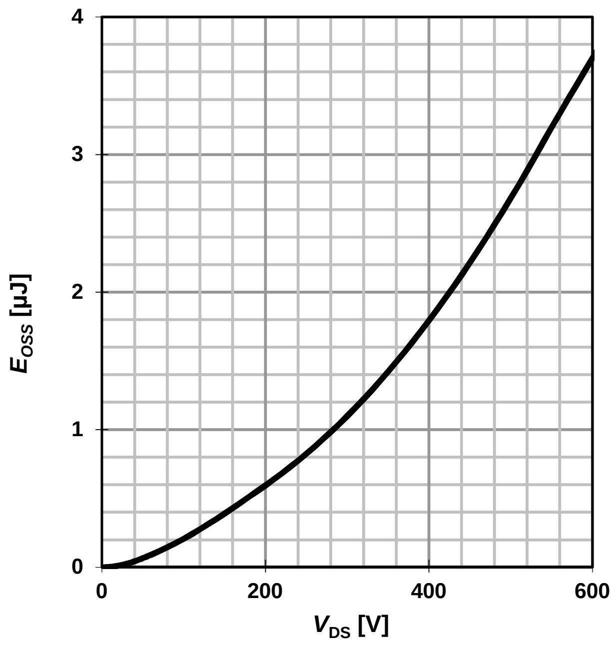


V_{GS} = *f*(Q_G); V_{DCLINK} = 400 V; I_D = 2.11 A

Figure 20 Typ. capacitances

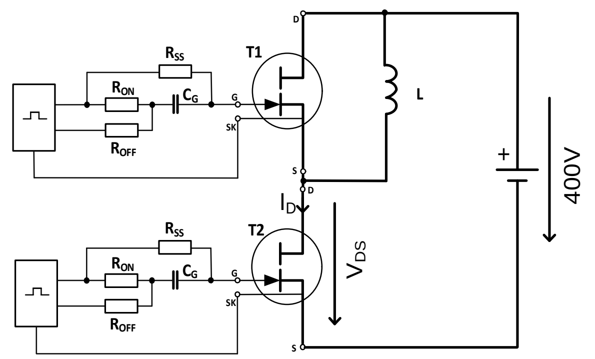


C_{xSS} = *f*(V_{DS})

Figure 21 Typ. output charge	**Figure 22 Typ. Coss stored Energy**
	
$Q_{OSS} = f(V_{DS})$	$E_{OSS} = f(V_{DS})$

5 Test Circuits

Figure 23 Switching times with inductive load



I_D=2.11 A, R_{ON}=20 Ω; R_{OFF}=20 Ω; R_{SS}=1230 Ω;
C_G=0.9 nF; V_{DRV} = 12 V

Figure 24 Switching times waveform

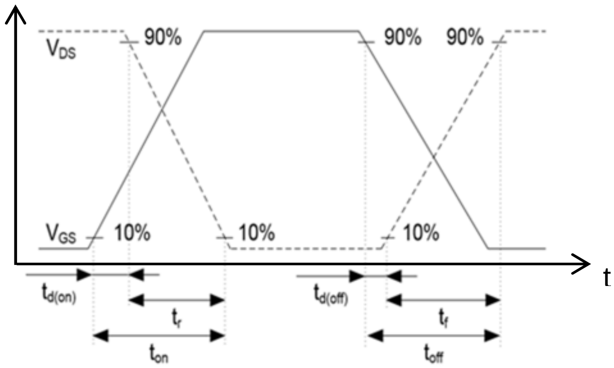
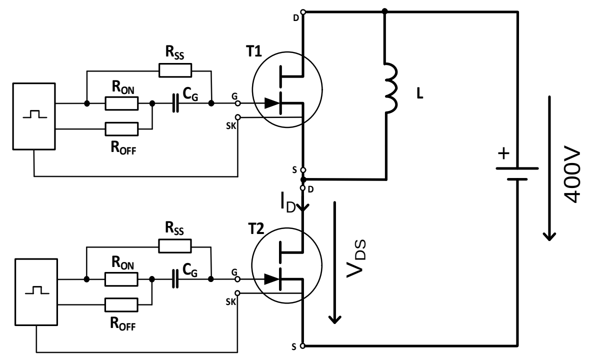
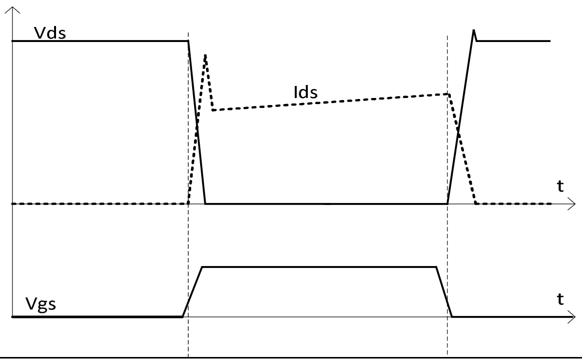


Figure 25 Reverse Channel Characteristics Test



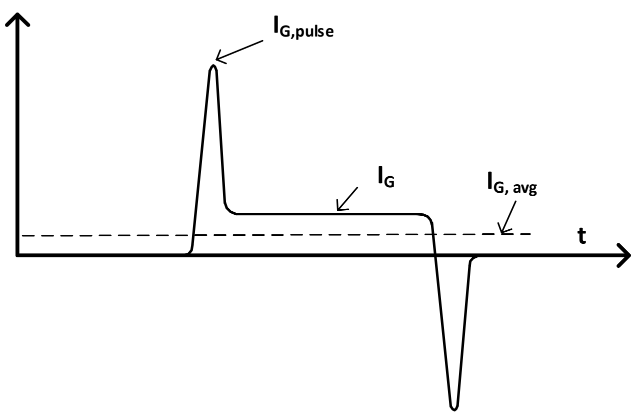
I_D=2.11 A, R_{ON}=20 Ω; R_{OFF}=20 Ω; R_{SS}=1230 Ω;
C_G=0.9 nF; V_{DRV} = 12 V

Figure 26 Typical Reverse Channel Recovery



The recovery charge is Q_{OSS} only, no additional Q_{rr}

Figure 27 Gate current switching waveform



6 Package Outlines

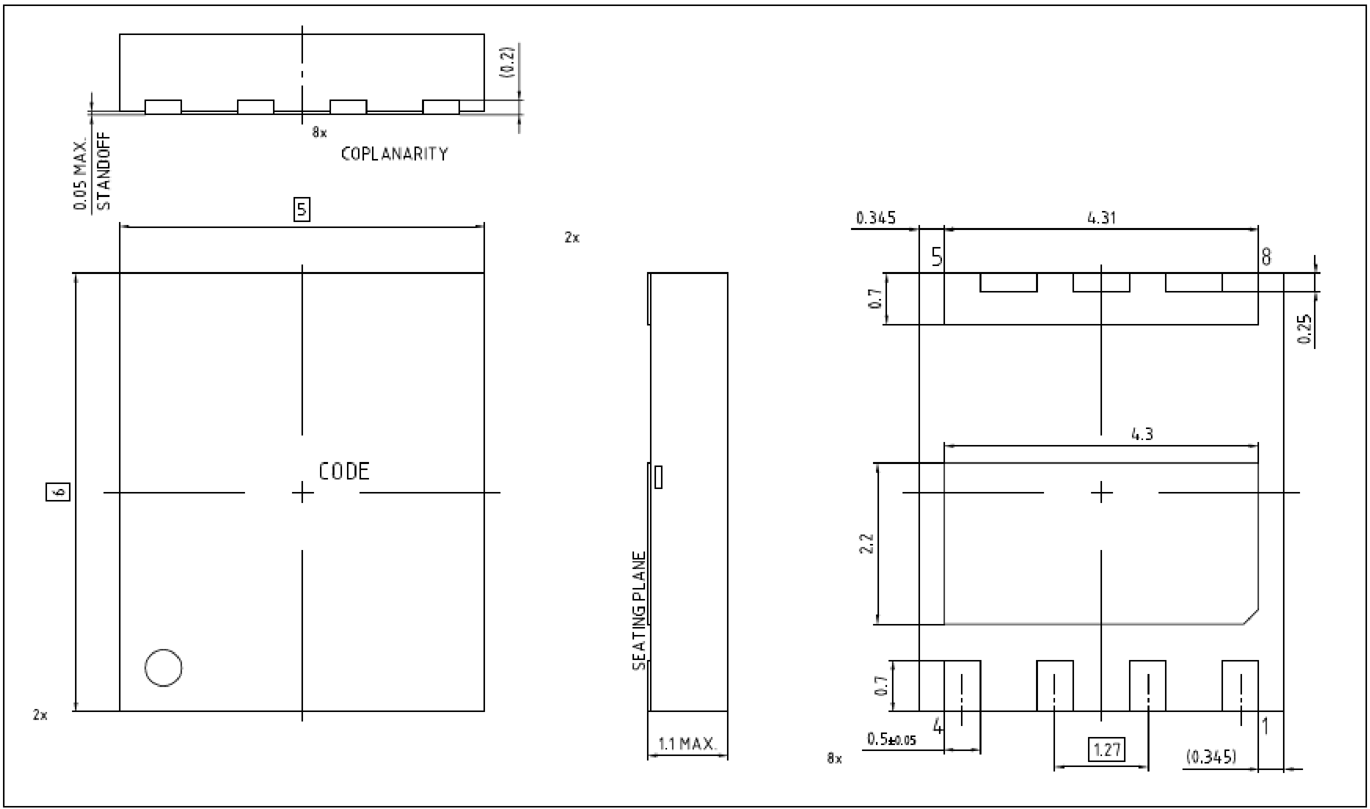


Figure 28 PG-TSON-8-7 Package Outline, dimensions (mm)

7 Appendix A

Table 9 Related links

- **IFX CoolGaN™ webpage: www.infineon.com/why-coolgan**
- **IFX CoolGaN™ reliability white paper: www.infineon.com/gan-reliability**
- **IFX CoolGaN™ gate drive application note: www.infineon.com/driving-coolgan**
- **IFX CoolGaN™ applications information:**
  - **www.infineon.com/gan-in-server-telecom**
  - **www.infineon.com/gan-in-wirelesscharging**
  - **www.infineon.com/gan-in-audio**
  - **www.infineon.com/gan-in-adapter-charger**

8 Revision History

Major changes since the last revision

Revision	Date	Description of change
2.0	2022-11-11	Final release

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