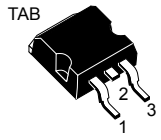
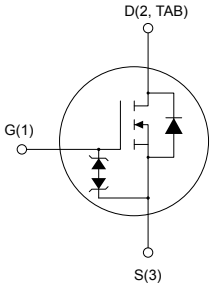
N-channel 900 V, 280 mΩ typ., 15 A MDmesh K5 Power MOSFET in a D²PAK package



D²PAK



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Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STB16N90K5	900 V	330 mΩ	15 A

- Very low FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Product status link
STB16N90K5

Product summary	
Order code	STB16N90K5
Marking	16N90K5
Package	D²PAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	15	A
I_D	Drain current (continuous) at T_C = 100 °C	9	A
I_{DM} (1)	Drain current (pulsed)	60	A
P_{TOT}	Total power dissipation at T_C = 25 °C	190	W
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	
T_J	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 15 A, di/dt ≤ 100 A/µs; V_{DS} peak ≤ $V_{(BR)DSS}$, V_{DD}= 450 V.*
3. *V_{DS} ≤ 720 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.66	°C/W
R_{thJA} (1)	Thermal resistance, junction-to-ambient	30	°C/W

1. *When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	5	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	380	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	900			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 900 V			1	µA
		V_{GS} = 0 V, V_{DS} = 900 V, T_C = 125 °C (1)			50	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 7.5 A		280	330	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1027	-	pF
C_{oss}	Output capacitance		-	106	-	pF
C_{rss}	Reverse transfer capacitance		-	1.6	-	pF
$C_{o(er)}$ (1)	Equivalent capacitance energy related	V_{GS} = 0 V, V_{DS} = 0 to 720 V	-	51	-	pF
$C_{o(tr)}$ (2)	Equivalent capacitance time related			141	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	1(3)	4.9	9(3)	Ω
Q_g	Total gate charge	V_{DD} = 720 V, I_D = 15 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	29.7	-	nC
Q_{gs}	Gate-source charge		-	7.3	-	nC
Q_{gd}	Gate-drain charge		-	17.7	-	nC

1. *$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*
2. *$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*
3. *Specified by design, not tested in production.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 450 V, I_D = 7.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	28.8	-	ns
t_r	Rise time		-	36	-	ns
$t_{d(off)}$	Turn-off delay time		-	46	-	ns
t_f	Fall time		-	9.8	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		15	A
I_{SDM} (1)	Source-drain current (pulsed)		-		60	A
V_{SD} (2)	Forward on voltage	I_{SD} = 15 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 15 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	458		ns
Q_{rr}	Reverse recovery charge		-	8.13		µC
I_{RRM}	Reverse recovery current		-	35.5		A
t_{rr}	Reverse recovery time	I_{SD} = 15 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_J = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	546		ns
Q_{rr}	Reverse recovery charge		-	9.2		µC
I_{RRM}	Reverse recovery current		-	33.7		A

1. *Pulse width limited by safe operating area*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

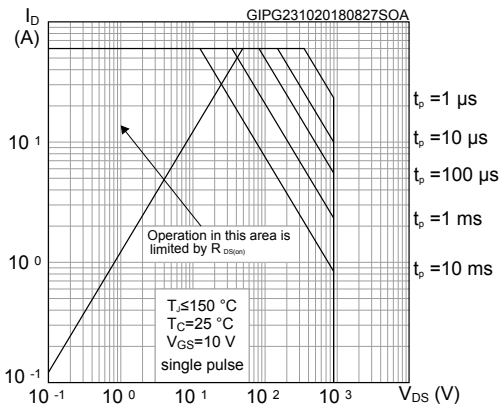


Figure 2. Normalized transient thermal impedance

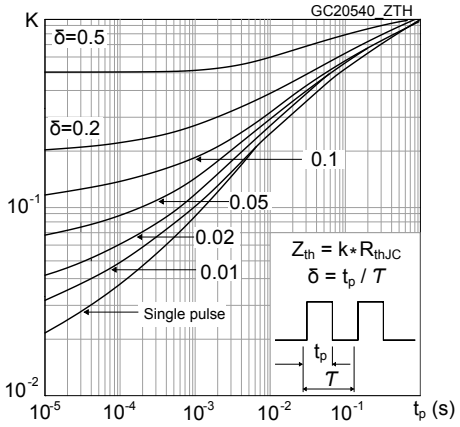


Figure 3. Typical output characteristics

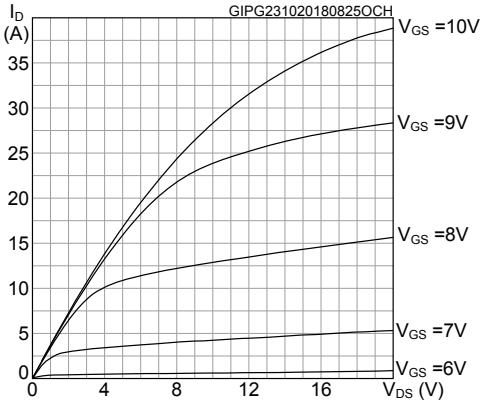


Figure 4. Typical transfer characteristics

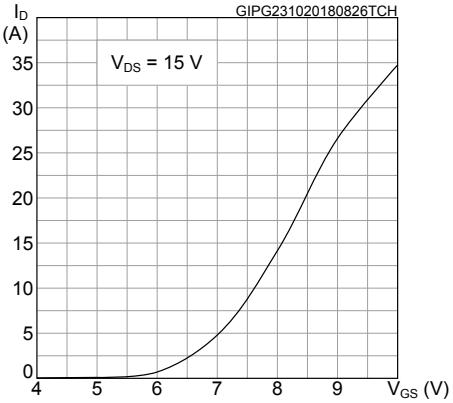


Figure 5. Normalized breakdown voltage vs temperature

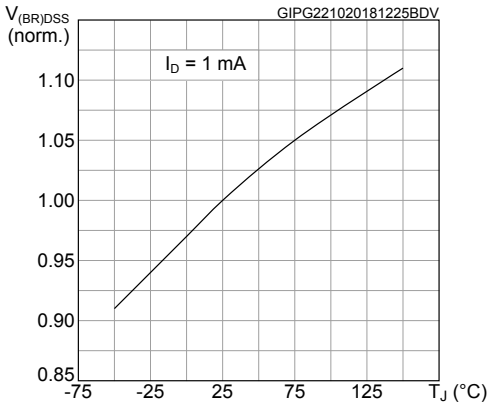


Figure 6. Typical drain-source on-resistance

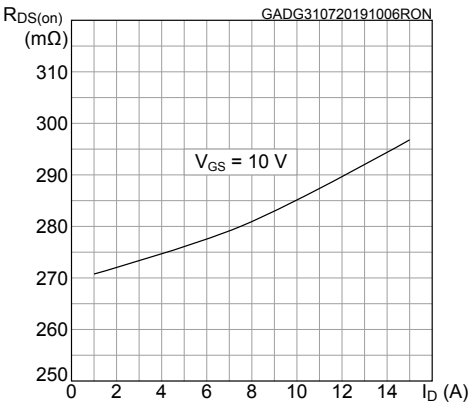


Figure 7. Typical gate charge characteristics

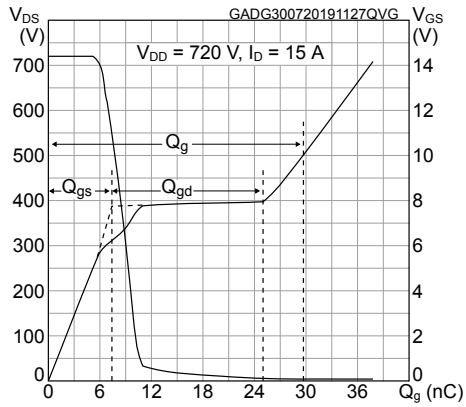


Figure 8. Typical capacitances vs voltage

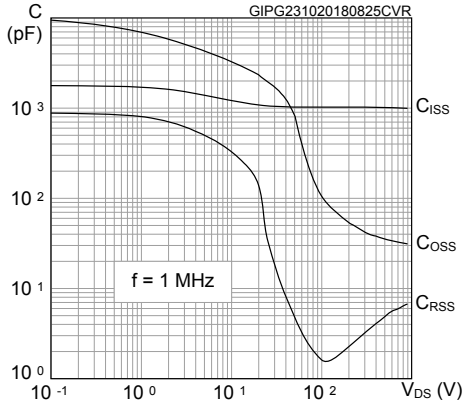


Figure 9. Normalized threshold voltage vs temperature

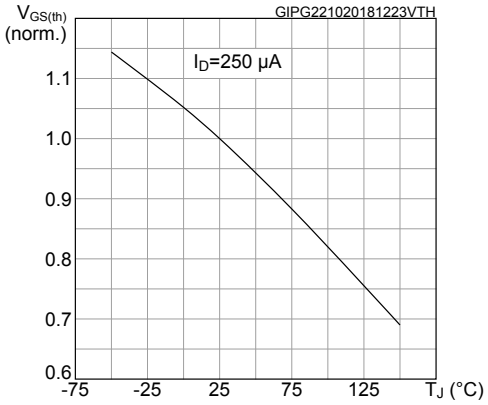


Figure 10. Normalized on-resistance vs temperature

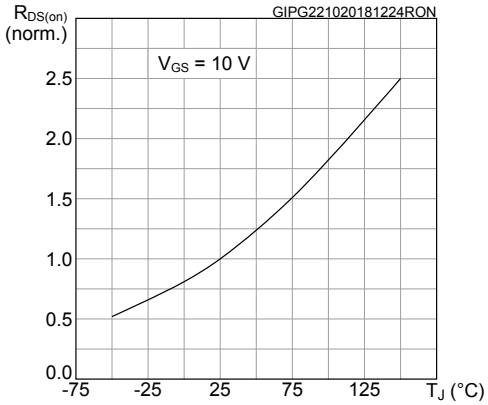


Figure 11. Maximum avalanche energy vs temperature

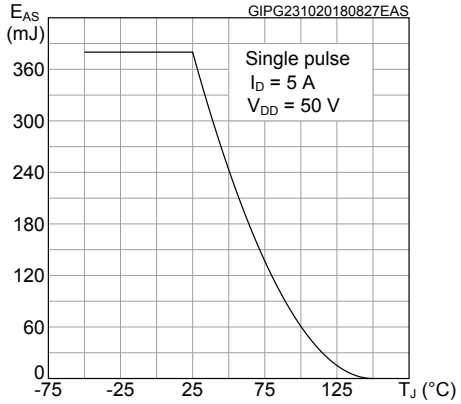
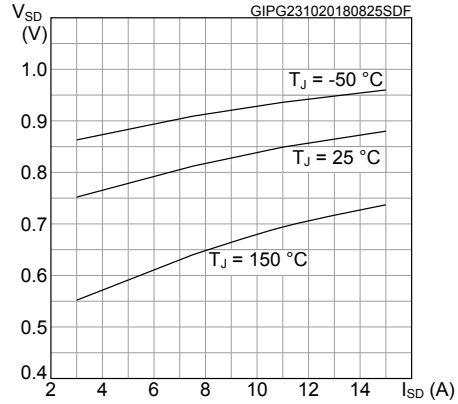


Figure 12. Typical source-drain diode characteristics



3 Test circuits

Figure 13. Test circuit for resistive load switching times

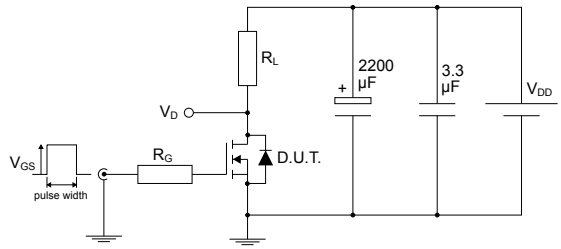


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Figure 14. Test circuit for gate charge behavior

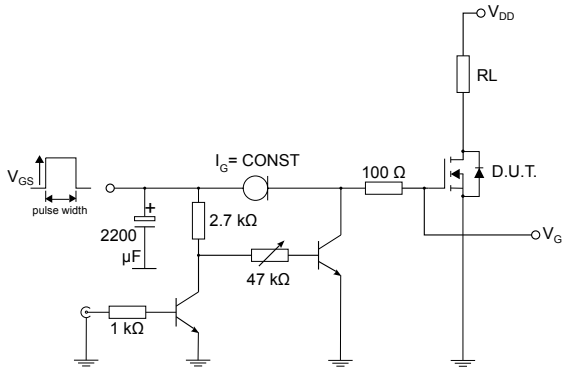

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Figure 15. Test circuit for inductive load switching and diode recovery times

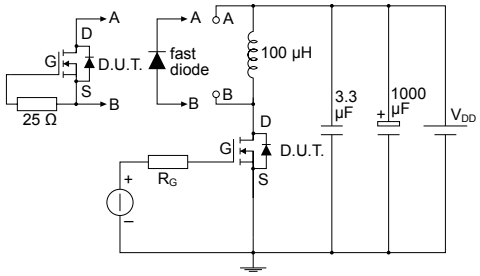

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Figure 16. Unclamped inductive load test circuit

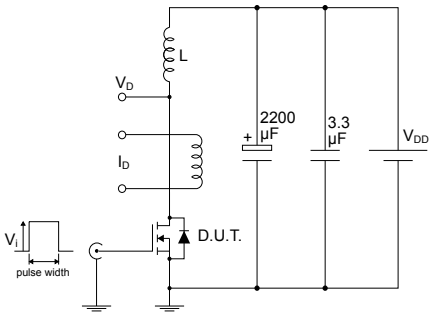

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Figure 17. Unclamped inductive waveform

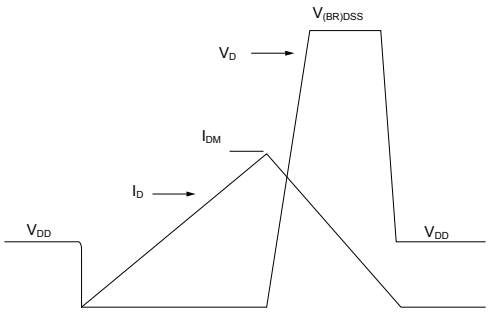

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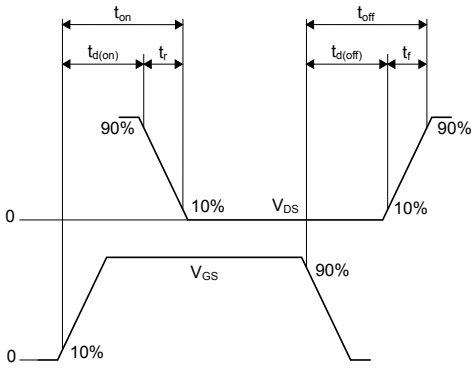
Figure 18. Switching time waveform



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4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type B package information

Figure 19. **D²PAK (TO-263) type B package outline**

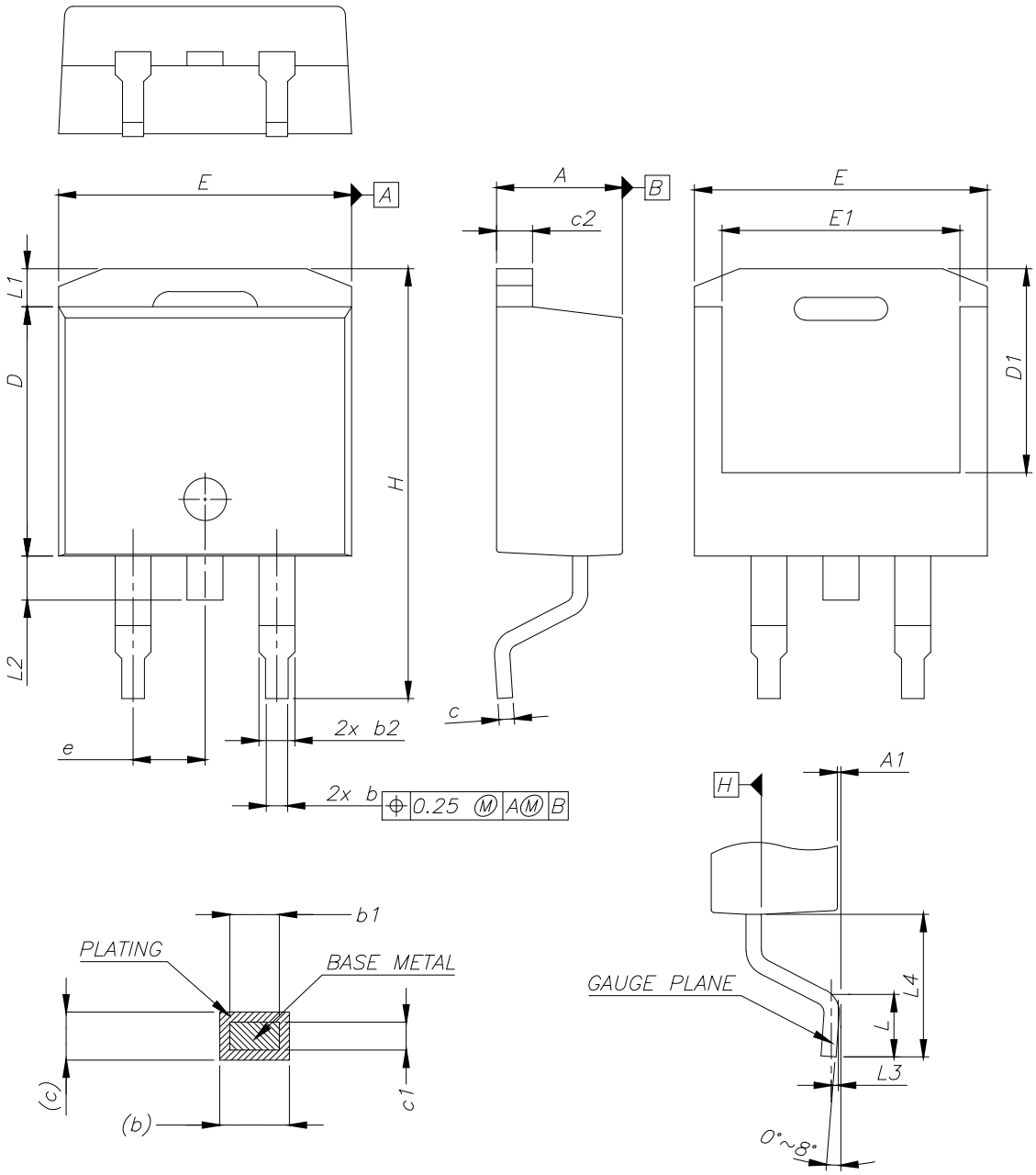

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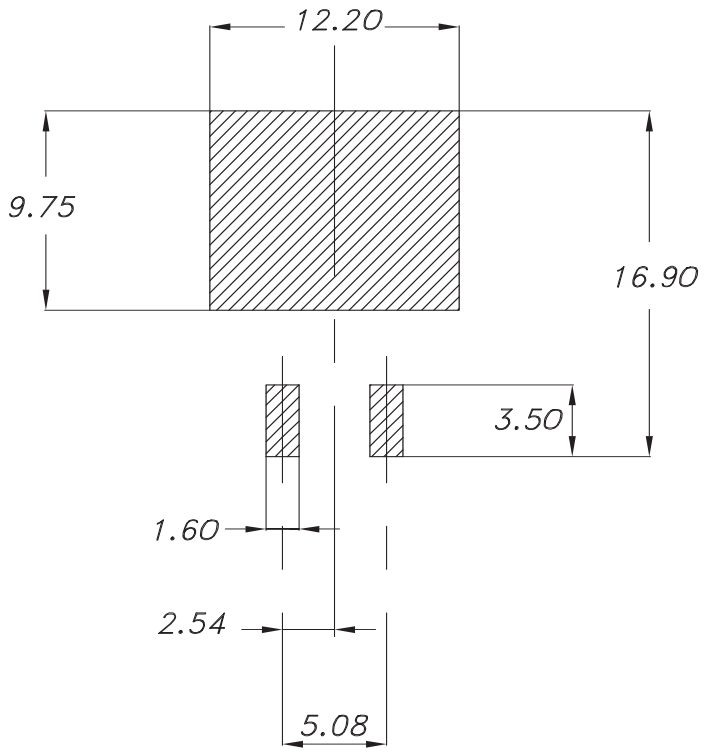
Table 8. D²PAK (TO-263) type B mechanical data

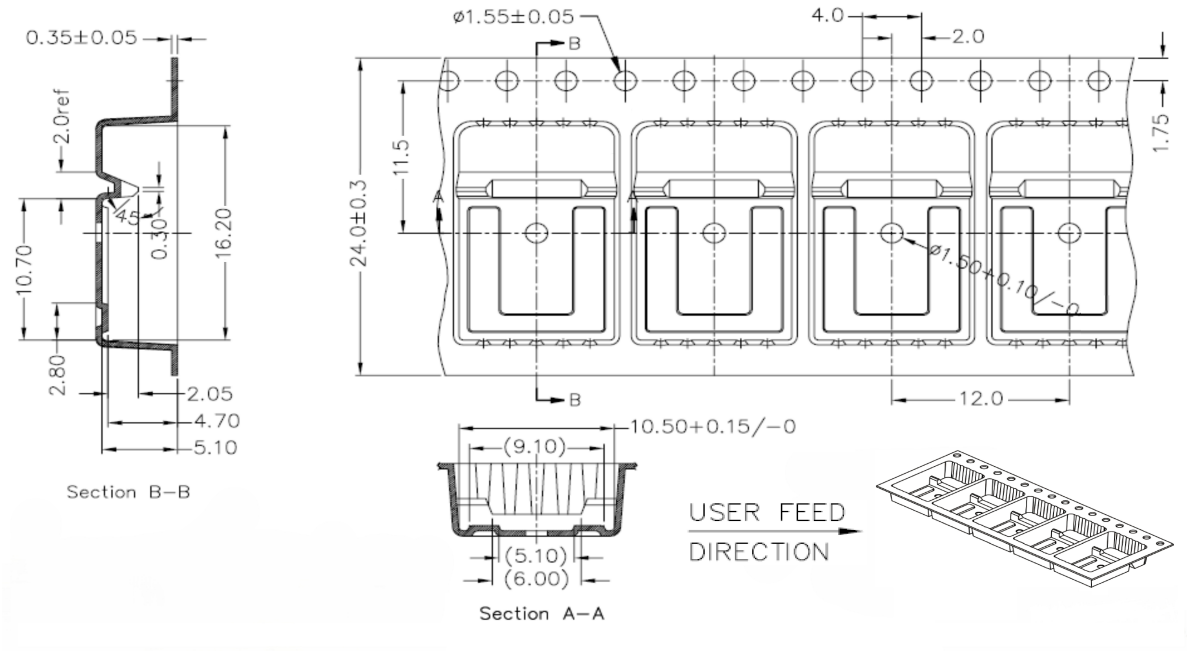
Dim.	mm		
	Min.	Typ.	Max.
A	4.36		4.56
A1	0.00		0.25
b	0.70		0.90
b1	0.51		0.89
b2	1.17		1.37
c	0.38		0.694
c1	0.38		0.534
c2	1.19		1.34
D	8.60		9.00
D1	6.90		7.50
E	10.15		10.55
E1	8.10		8.70
e	2.54 BSC		
H	15.00		15.60
L	1.90		2.50
L1			1.65
L2			1.78
L3		0.25	
L4	4.78		5.28

Figure 20. D²PAK (TO-263) recommended footprint (dimensions are in mm)



4.2 D²PAK packing information

Figure 21. D²PAK tape drawing (dimensions are in mm)



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Revision history

Table 9. **Document revision history**

Date	Revision	Changes
23-Oct-2018	1	Initial release.
05-Aug-2019	2	Updated *Section 2.1: Electrical characteristics (curves)*. Minor text changes.
21-Aug-2025	3	Updated Section 4: Package information. Minor text changes.

Contents

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