# MC74HCT573A

# Octal 3-State Noninverting Transparent Latch with LSTTL Compatible Inputs

## High−Performance Silicon−Gate CMOS

The MC74HCT573A is identical in pinout to the LS573. This device may be used as a level converter for interfacing TTL or NMOS outputs to High−Speed CMOS inputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold times becomes latched.

The Output Enable input does not affect the state of the latches, but when Output Enable is high, all device outputs are forced to the high−impedance state. Thus, data may be latched even when the outputs are not enabled.

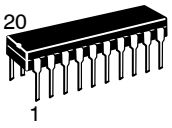
The HCT573A is identical in function to the HCT373A but has the Data Inputs on the opposite side of the package from the outputs to facilitate PC board layout.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS−Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 10 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 234 FETs or 58.5 Equivalent Gates
  - — Improved Propagation Delays
  - — 50% Lower Quiescent Power
- These Devices are Pb−Free and are RoHS Compliant

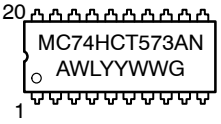
**ON Semiconductor**

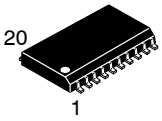
**http://onsemi.com**

**MARKING DIAGRAMS**

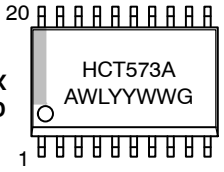


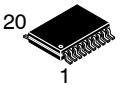

**PDIP−20**
**N SUFFIX**
**CASE 738**



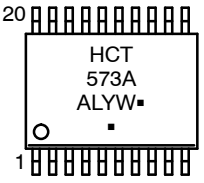



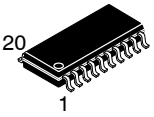

**SOIC−20**
**DW SUFFIX**
**CASE 751D**




**TSSOP−20**
**DT SUFFIX**
**CASE 948E**




**SOEIAJ−20**
**F SUFFIX**
**CASE 967**


| | | |
|---|---|---|
| A | = | Assembly Location |
| WL, L | = | Wafer Lot |
| YY, Y | = | Year |
| WW, W | = | Work Week |
| G or ▪ | = | Pb−Free Package |

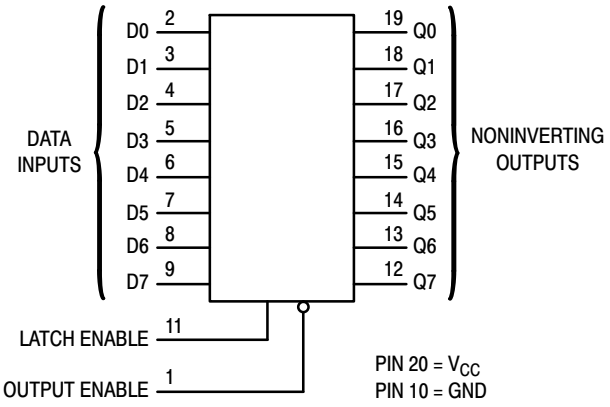
(Note: Microdot may be in either location)

### ORDERING INFORMATION

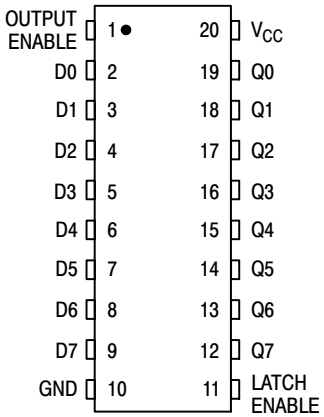
| Device | Package | Shipping† |
|---|---|---|
| MC74HCT573ANG | PDIP−20 | 18 / Rail |
| MC74HCT573ADWR2G | SOIC−20 | 1000 / Reel |
| MC74HCT573ADTR2G | TSSOP−20 | 2500 / Reel |
| MC74HCT573AFELG | SOEIAJ−20 | 2000 / Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

## LOGIC DIAGRAM




## PIN ASSIGNMENT




## FUNCTION TABLE

| Inputs | | | Output |
|---|---|---|---|
| **Output Enable** | **Latch Enable** | **D** | **Q** |
| L | H | H | H |
| L | H | L | L |
| L | L | X | No Change |
| H | X | X | Z |

X = Don't Care
Z = High Impedance

| Design Criteria | Value | Units |
|---|---|---|
| Internal Gate Count* | 58.5 | ea |
| Internal Gate Propagation Delay | 1.5 | ns |
| Internal Gate Power Dissipation | 5.0 | μW |
| Speed Power Product | 0.0075 | pJ |

*Equivalent to a two−input NAND gate.

## MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | − 0.5 to + 7.0 | V |
| $V_{in}$ | DC Input Voltage (Referenced to GND) | − 0.5 to $V_{CC}$ + 0.5 | V |
| $V_{out}$ | DC Output Voltage (Referenced to GND) | − 0.5 to $V_{CC}$ + 0.5 | V |
| $I_{in}$ | DC Input Current, per Pin | ± 20 | mA |
| $I_{out}$ | DC Output Current, per Pin | ± 25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | ± 50 | mA |
| $P_D$ | Power Dissipation in Still Air Plastic DIP†<br>SOIC Package†<br>TSSOP Package† | 750<br>500<br>450 | mW |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, TSSOP or SOIC Package) | 260 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: −10 mW/°C from 65° to 125°C
SOIC Package: −7 mW/°C from 65° to 125°C
TSSOP Package: −6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range GND ≤ ($V_{in}$ or $V_{out}$) ≤ $V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | 4.5 | 5.5 | V |
| $V_{in}$, $V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | − 55 | + 125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time (Figure 1) | 0 | 500 | ns |

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | − 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $V_{IH}$ | Minimum High−Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ − 0.1 V<br>$\|I_{out}\|$ ≤ 20 μA | 4.5<br>5.5 | 2.0<br>2.0 | 2.0<br>2.0 | 2.0<br>2.0 | V |
| $V_{IL}$ | Maximum Low−Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ − 0.1 V<br>$\|I_{out}\|$ ≤ 20 μA | 4.5<br>5.5 | 0.8<br>0.8 | 0.8<br>0.8 | 0.8<br>0.8 | V |
| $V_{OH}$ | Minimum High−Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{out}\|$ ≤ 20 μA | 4.5<br>5.5 | 4.4<br>5.4 | 4.4<br>5.4 | 4.4<br>5.4 | V |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{out}\|$ ≤ 6.0 mA | 4.5 | 3.98 | 3.84 | 3.7 | |
| $V_{OL}$ | Maximum Low−Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{out}\|$ ≤ 20 μA | 4.5<br>5.5 | 0.1<br>0.1 | 0.1<br>0.1 | 0.1<br>0.1 | V |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{out}\|$ ≤ 6.0 mA | 4.5 | 0.26 | 0.33 | 0.4 | |
| $I_{in}$ | Maximum Input Leakage Current | $V_{in}$ = $V_{CC}$ or GND | 5.5 | ± 0.1 | ± 1.0 | ± 1.0 | μA |
| $I_{OZ}$ | Maximum Three−State Leakage Current | Output in High−Impedance State<br>$V_{in}$ = $V_{IL}$ or $V_{IH}$<br>$V_{out}$ = $V_{CC}$ or GND | 5.5 | ± 0.5 | ± 5.0 | ± 10 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in}$ = $V_{CC}$ or GND<br>$I_{out}$ ≤ 0 μA | 5.5 | 4.0 | 40 | 160 | μA |
| $\Delta I_{CC}$ | Additional Quiescent Supply Current | $V_{in}$ = 2.4 V, Any One Input<br>$V_{in}$ = $V_{CC}$ or GND, Other Inputs<br>$I_{out}$ = 0 μA | | ≥ − 55°C | 25°C to 125°C | | |
| | | | 5.5 | 2.9 | 2.4 | | mA |

**AC ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5.0 V ± 10%, $C_L$ = 50 pF, Input $t_r = t_f$ = 6.0 ns)

| Symbol | Parameter | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|
| | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Input D to Output Q (Figures 1 and 5) | 30 | 38 | 45 | ns |
| $t_{PLH}$ $t_{PHL}$ | Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5) | 30 | 38 | 45 | ns |
| $T_{PLZ}$, $T_{PHZ}$ | Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6) | 28 | 35 | 42 | ns |
| $t_{TZL}$, $t_{TZH}$ | Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6) | 28 | 35 | 42 | ns |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Transition Time, any Output (Figures 1 and 5) | 12 | 15 | 18 | ns |
| $C_{in}$ | Maximum Input Capacitance | 10 | 10 | 10 | pF |
| $C_{out}$ | Maximum Three–State Output Capacitance (Output in High–Impedance State) | 15 | 15 | 15 | pF |

| | | Typical @ 25°C, $V_{CC}$ = 5.0 V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Per Enabled Output)* | 48 | pF |

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

**TIMING REQUIREMENTS** ($V_{CC}$ = 5.0 V ± 10%, $C_L$ = 50 pF, Input $t_r = t_f$ = 6.0 ns)

| Symbol | Parameter | Fig. | Guaranteed Limit | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | – 55 to 25°C | | ≤ 85°C | | ≤ 125°C | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{su}$ | Minimum Setup Time, Input D to Latch Enable | 4 | 10 | | 13 | | 15 | | ns |
| $t_h$ | Minimum Hold Time, Latch Enable to Input D | 4 | 5.0 | | 5.0 | | 5.0 | | ns |
| $t_w$ | Minimum Pulse Width, Latch Enable | 2 | 15 | | 19 | | 22 | | ns |
| $t_r$, $t_f$ | Maximum Input Rise and Fall Times | 1 | | 500 | | 500 | | 500 | ns |

## SWITCHING WAVEFORMS

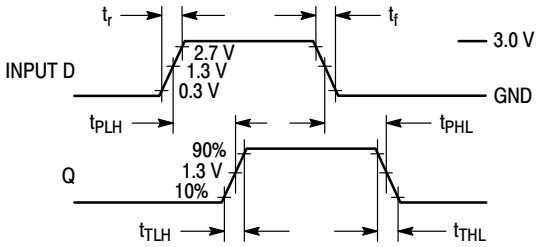



**Figure 1.**

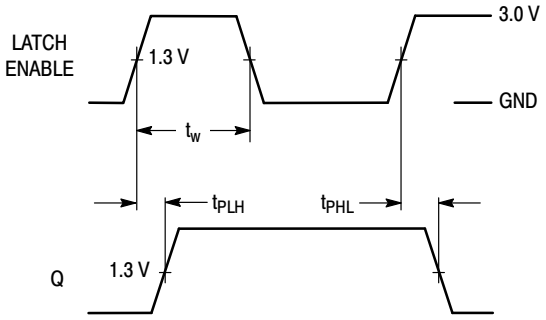



**Figure 2.**

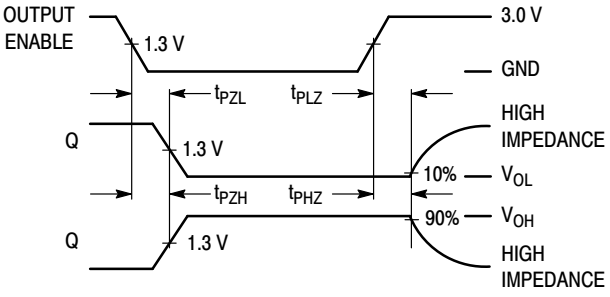



**Figure 3.**

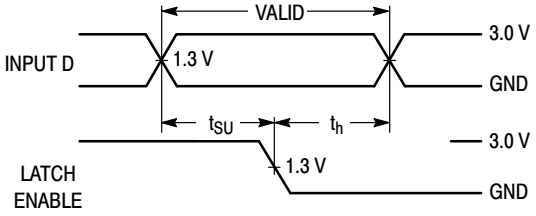
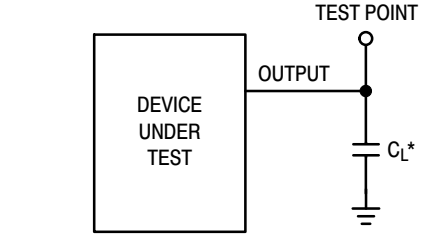
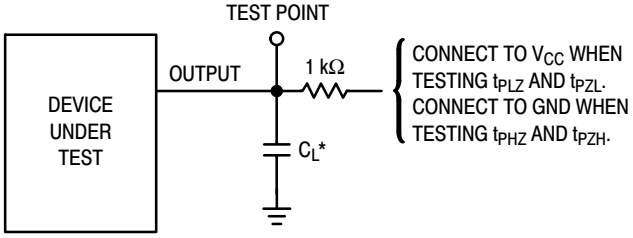



**Figure 4.**




*Includes all probe and jig capacitance

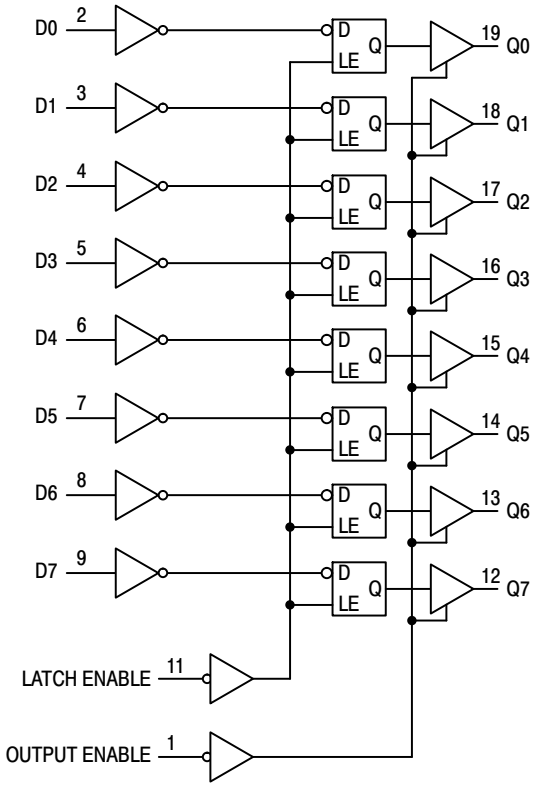
**Figure 5. Test Circuit**




*Includes all probe and jig capacitance

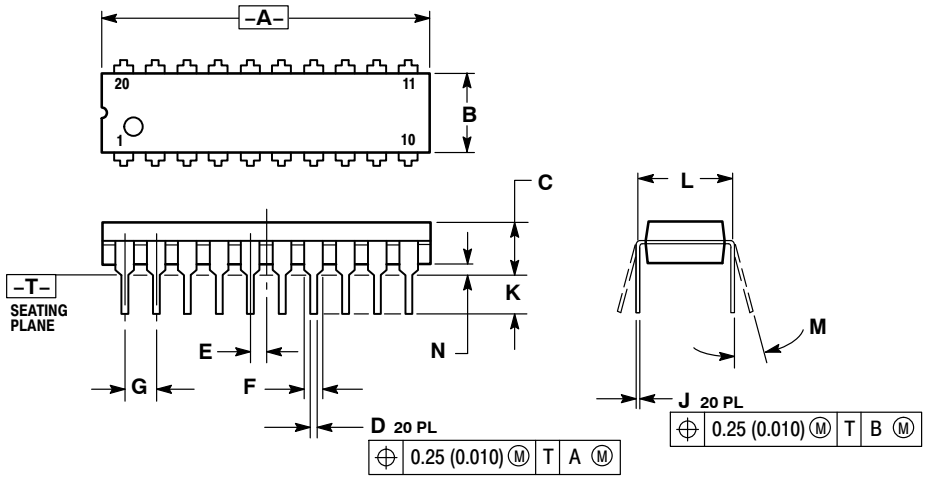
**Figure 6. Test Circuit**

### EXPANDED LOGIC DIAGRAM



## PACKAGE DIMENSIONS

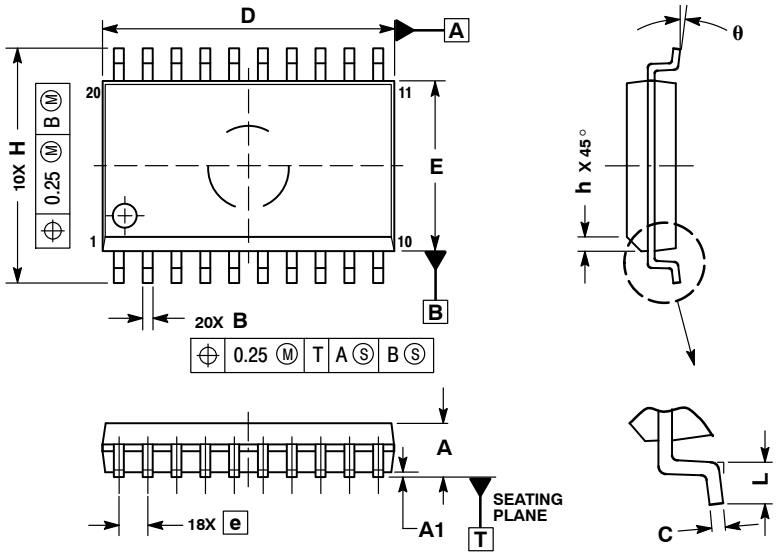
**PDIP−20**
**N SUFFIX**
PLASTIC DIP PACKAGE
CASE 738−03
ISSUE E




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 1.010 | 1.070 | 25.66 | 27.17 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.150 | 0.180 | 3.81 | 4.57 |
| D | 0.015 | 0.022 | 0.39 | 0.55 |
| E | 0.050 BSC | | 1.27 BSC | |
| F | 0.050 | 0.070 | 1.27 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.140 | 2.80 | 3.55 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.020 | 0.040 | 0.51 | 1.01 |

**SOIC−20**
**DW SUFFIX**
CASE 751D−05
ISSUE G

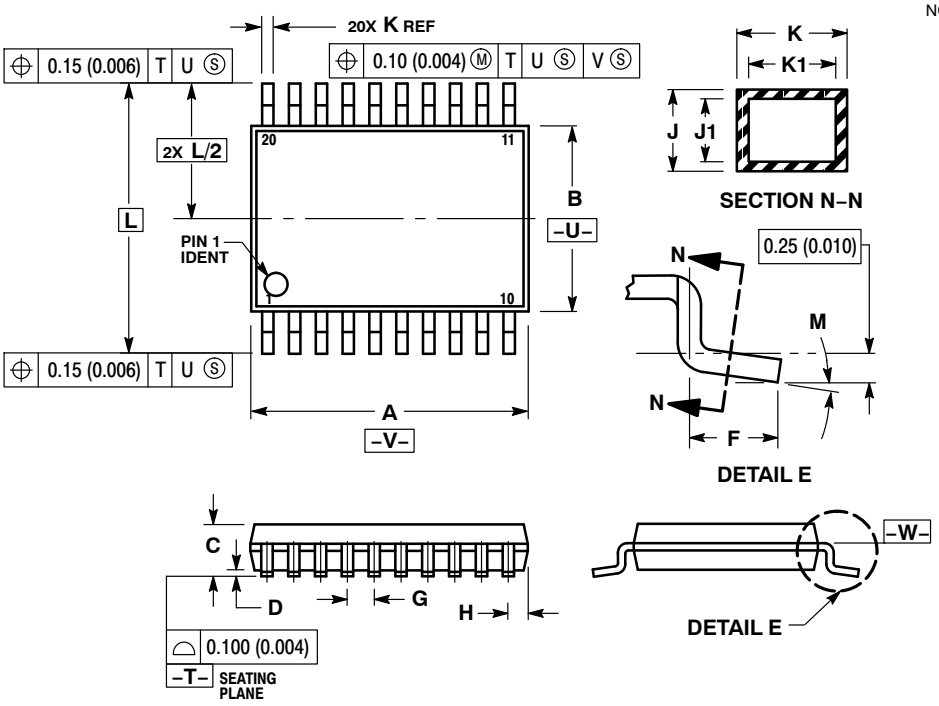



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

## PACKAGE DIMENSIONS

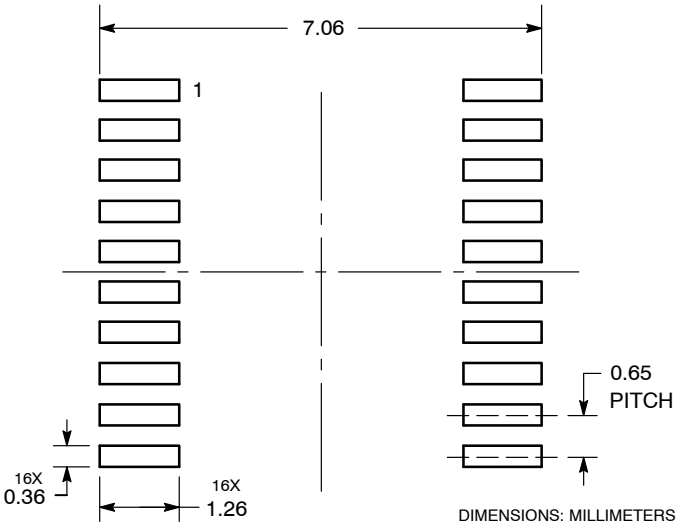
**TSSOP−20**
**DT SUFFIX**
CASE 948E−02
ISSUE C




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

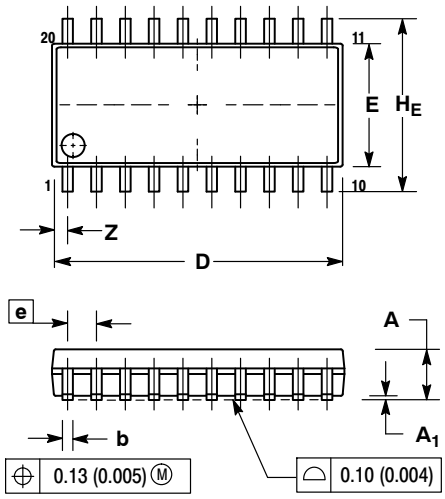
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

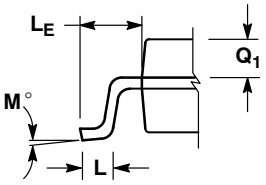
### SOLDERING FOOTPRINT



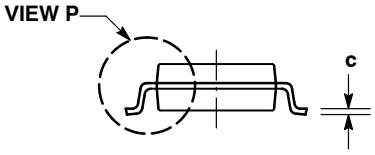
## PACKAGE DIMENSIONS

**SOEIAJ–20**
**F SUFFIX**
CASE 967–01
ISSUE A




**DETAIL P**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 ( 0.018).

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| $A_1$ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.15 | 0.25 | 0.006 | 0.010 |
| D | 12.35 | 12.80 | 0.486 | 0.504 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| $H_E$ | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| $L_E$ | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| $Q_1$ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 0.81 | --- | 0.032 |



## PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT**:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
**Phone**: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
**Fax**: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
**Email**: orderlit@onsemi.com

**N. American Technical Support**: 800–282–9855 Toll Free USA/Canada
**Europe, Middle East and Africa Technical Support:**
Phone: 421 33 790 2910
**Japan Customer Focus Center**
Phone: 81–3–5773–3850

**ON Semiconductor Website**: **www.onsemi.com**

**Order Literature**: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative