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MAX25608

12-Switch, High-Brightness LED Matrix Manager for Automotive Front Lights

General Description

The MAX25608/MAX25608B/MAX25608C/MAX25608E 12-switch matrix manager ICs for automotive lighting applications include a 12-switch array for bypassing individual LEDs in a single- or dual-string application. They feature 12 individually controlled n-channel MOSFET switches rated for 14V with an on-resistance of 0.06Ω. A single current source can be used to power all of the LEDs connected in series. Individual LEDs can be dimmed by turning on and off the bypass switches across each LED. The devices can also be configured in dual-string applications with six switches in series per string. Each switch can be connected across one, two, or three LEDs in series. These devices also allow for parallel connection of two switches to bypass high-current LEDs. The ICs also include an internal charge pump that provides power for the gate drive for the LED bypass switches.

The MAX25608/MAX25608B/MAX25608C/MAX25608E feature a serial interface (UART) for serial communication. The MAX25608/MAX25608C/MAX25608E can be used in full-duplex applications, and the MAX25608B can be used in half-duplex applications, such as with CAN transceivers. The MAX25608 has spread spectrum enabled on the charge pump clock, and the MAX25608B/MAX25608C/MAX25608E have spread spectrum disabled on the charge pump clock. Each switch can be turned fully on, fully off, or dimmed with or without fade transitions through the serial interface. The ICs feature open-LED protection as well as open- and short-LED fault reporting through the serial interface. The devices are available in a 28-pin TSSOP package with exposed pad.

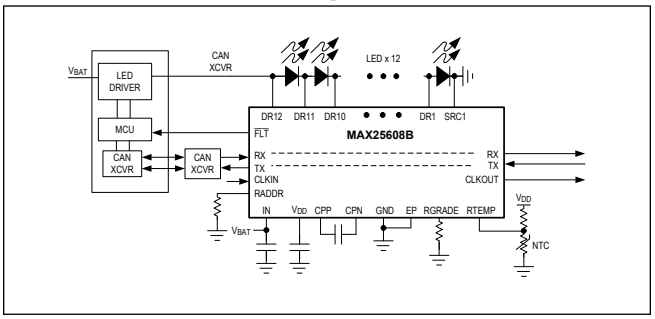
Applications

- Automotive Matrix LED Systems
- Adaptive Drive Beam Lights

Benefits and Features

- Automotive Ready: AEC-Q100 Qualified
- Flexible Configuration
  - Up to 12 Switches in Series for Single String
  - Two Sub Strings of Six Series Switches per String
- Robust Serial Interface
  - Multidrop UART Communication Interface
  - Up to 16 Addressable Devices
  - Compatible with CAN Physical Layer (MAX25608B)
- Optimal PWM Dimming Arrangement Provides Excellent Dimming Performance
  - Programmable 12-Bit PWM Dimming
  - Fade Transition Between PWM Dimming States
  - Internal or External Clock for PWM Dimming
  - Programmable Slew Rate for EMI Control
- Protection Features and Package Improve Reliability
  - Open-LED Protection
  - NTC Temperature Monitor
  - Programmable Open- and Short-LED Threshold
  - Open and Shorted-LED Fault Reporting
  - Open-Trace Fault Reporting (MAX25608E)
  - Thermally Enhanced, 28-Pin TSSOP-EP

Simplified Block Diagram



Ordering Information appears at end of data sheet.

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Absolute Maximum Ratings

IN to GND ..... -0.3V to +65V
V_{DD} to GND ..... -0.3V to +2.5V
CPN to GND ..... -0.3V to +65V
CPP to GND ..... -0.3V to +70V
CPP to CPN ..... -0.3V to +6V
CPP to DRx ..... -0.3V to +70V
DR12 to GND ..... -0.3V to +65V
DRx to DR(x-1) ..... -0.3V to +16V
DR6 to GND ..... -0.3V to +65V
SRCx to GND ..... -0.3V to +65V
RTEMP, RGRADE, CLKIN, CLKOUT, RADDR to GND .. -0.3V to V_{VDD} + 0.3V
RX, TX, $\overline{FLT}$ to GND ..... -0.3V to +6V
Continuous Power Dissipation (multilayer board) (T_A = 70°C, derate 40.57mW/°C above +70°C) 3245.44mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -40°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

28 TSSOP

Package Code	U28E+6C
Outline Number	**21-0108**
Land Pattern Number	**90-100175**
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	24.6°C/W
Junction to Case (θ_{JC})	1.5°C/W

For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

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Electrical Characteristics

(V_{IN} = 5V, T_A = T_J = -40°C to +125°C (*Note 1*), unless otherwise noted. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGES						
Supply Voltage	V_{IN}	Operating voltage range	4.0		60	V
Input Current	I_{IN}	V_{IN} = 5V		4.2	6	mA
Input POR Threshold	V_{IN-POR}	V_{IN} rising	3.6		3.9	V
Charge Pump DRAINn Input Current	I_{INQP}				6	mA
Charge-Pump Operating Voltage	V_{CPP}				65	V
VDD_UVLO Rising Threshold	UVLO_R_TH		1.61		1.69	V
VDD_UVLO Falling Threshold	UVLO_F_TH		1.54		1.63	V
LED DIMMING						
Internal Oscillator Frequency	f_{OSC}	Used for charge pump and PWM dimming of LEDs		16.384		MHz
LED PWM Dimming Frequency Range	f_{DIM}		100		2000	Hz
LED SWITCHES						
Single-Switch On-Resistance	R_{DSON}			0.060		Ω
On-Resistance with Series Switches 6–1 on				0.36	0.75	Ω
On-Resistance with Series Switches 12–7 on				0.36	0.75	Ω
Open LED Threshold (Rising)	VOTH	VOTH code = 0x0	12.0	14.0	15.0	V
		VOTH code = 0x1	8.3	9.33	10.0	
Short LED Threshold (Rising)	VSTH	VSTH code = 000	1.26	1.40	1.54	V
		VSTH code = 001	3.24	3.6	3.96	
		VSTH code = 010	3.6	4.00	4.4	
		VSTH code = 011	4.95	5.5	6.05	
		VSTH code = 100	5.4	6.0	6.6	
		VSTH code = 101	5.94	6.6	7.26	
		VSTH code = 110	6.48	7.2	7.92	
		VSTH code = 111	6.93	7.70	8.47	
Maximum Switch Current	I_{SW}	Thermally limited		1.6		A
LED Slew-Rate Setting 0	SR_LED_0	0 to 6V step, 10% to 90% rise/fall time, LED_SLEW[2:0] = 0x0		160		µs
LED Slew-Rate Setting 1	SR_LED_1	0 to 6V step, 10% to 90% rise/fall time, LED_SLEW[2:0] = 0x1		81		µs
LED Slew-Rate Setting 2	SR_LED_2	0 to 6V step, 10% to 90% rise/fall time, LED_SLEW[2:0] = 0x2		48		µs

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Electrical Characteristics (continued)

(V_{IN} = 5V, T_A = T_J = -40°C to +125°C (*Note 1*), unless otherwise noted. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LED Slew-Rate Setting 3	SR_LED_3	0 to 6V step, 10% to 90% rise/fall time, LED_SLEW[2:0] = 0x3		26		µs
LED Slew-Rate Setting 4	SR_LED_4	0 to 6V step, 10% to 90% rise/fall time, LED_SLEW[2:0] = 0x4		17		µs
LED Slew-Rate Setting 5	SR_LED_5	0 to 6V step, 10% to 90% rise/fall time, LED_SLEW[2:0] = 0x5		10		µs
LED Slew-Rate Setting 6	SR_LED_6	0 to 6V step, 10% to 90% rise/fall time, LED_SLEW[2:0] = 0x6		5.0		µs
Open Trace Threshold		Minimum current required to detect open trace (MAX25608E)			260	mA
DIGITAL INPUTS – CLKIN, Rx						
Input High Voltage	V_{IH}		1.4			V
Input Low Voltage	V_{IL}				0.4	V
CLKIN Input Frequency	f_{CLK}		0.30		20.0	MHz
DIGITAL OUTPUTS – Tx, FLTB, CLKOUT						
Output Low Voltage	V_{OL}	I_{SINK} = 2mA			0.4	V
CLKOUT High Voltage	V_{OH}	I_{SRC} = 2mA	V_{DD} - 0.4			V
THERMAL SHUTDOWN						
Thermal Warning Threshold	TH_WARN	Rising temperature		140		°C
Thermal Warning Hysteresis				15		°C
Thermal Shutdown	TH_SHDN	Rising temperature		165		°C
Thermal Shutdown Hysteresis	HYS_SHDN			15		°C
CHARGE PUMP						
Charge-Pump Frequency	f_{CPP}			16.384		MHz
Charge-Pump Output Voltage	V_O	V_{CPP} - V_{CPN}, I_{CPP} = 350µA	3.7		6.0	V
Charge-Pump Power-Good Threshold	V_{CPP_OK}	Rising threshold		4.0		V
UART TIMING						
UART Write Bit Rate	F_{UART}	MAX25608/MAX25608B/MAX25608C/ MAX25608E	10		950	kbps
UART Read Bit Rate	F_{UART}	MAX25608/MAX25608C/MAX25608E	10		950	kbps
		MAX25608B	10		580	

Note 1: The MAX25608 and MAX25608B/C/E are designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5000 hours.

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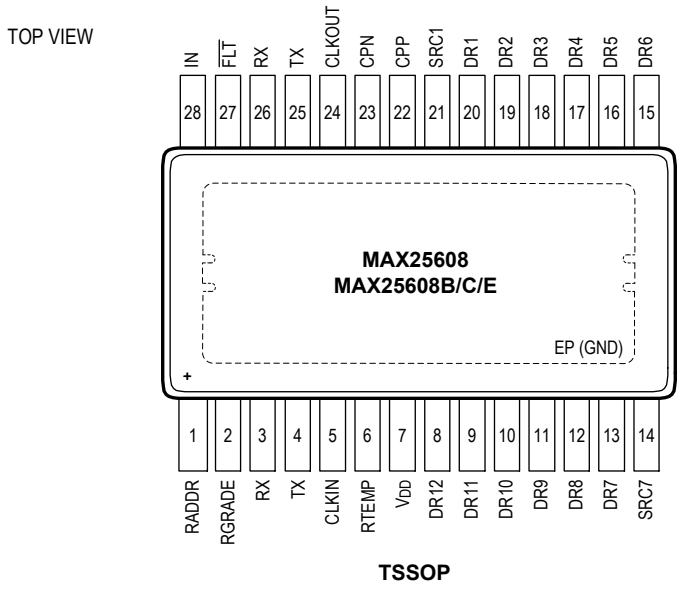
Pin Configuration



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Pin Description

PIN	NAME	FUNCTION
1	RADDR	Device ID Resistor. Connect a resistor value from RADDR to GND to set the UART Device ID.
2	RGRADE	LED Binning Resistor Connection. Connect a LED binning resistor from this pin to GND.
3, 26	RX	UART Receive Input. If the driver to this pin is CMOS output, no pull-up resistor is needed. If the driver to this pin is open drain, add a 1.5kΩ pull-up resistor.
4, 25	TX	UART Transmit Output. Add a 1.5kΩ pull-up resistor.
5	CLKIN	CLK Input. Can be optionally used to sync the device with an external digital clock signal.
6	RTEMP	NTC Divider ADC Input. Connect to NTC resistor divider to enable remote temperature sensing.
7	V_{DD}	LDO Output. Nominal voltage is 1.8V. Connect a bypass capacitor between V_{DD} and GND.
8	DR12	Drain of Internal Switch 12. Add a 0.1µF capacitor from DR12 to GND.
9	DR11	Drain of Internal Switch 11.
10	DR10	Drain of Internal Switch 10.
11	DR9	Drain of Internal Switch 9.
12	DR8	Drain of Internal Switch 8.
13	DR7	Drain of Internal Switch 7.
14	SRC7	Source of Internal Switch 7.
15	DR6	Drain of Internal Switch 6. For two-string applications, connect a 0.1µF ceramic capacitor from DR6 to GND.
16	DR5	Drain of Internal Switch 5.
17	DR4	Drain of Internal Switch 4.
18	DR3	Drain of Internal Switch 3.
19	DR2	Drain of Internal Switch 2.
20	DR1	Drain of Internal Switch 1.
21	SRC1	Source of Internal Switch 1.
22	CPP	Charge Pump Capacitor Positive Connection. Connect a 0.1µF ceramic capacitor from CPP to CPN.
23	CPN	Charge Pump Capacitor Negative Connection. Connect a 0.1µF from CPP to CPN.
24	CLKOUT	After startup, can be optionally configured with UART to drive a clock signal to other devices, or act as a pass-through for the CLKIN input.
27	$\overline{FLT}$	Open-Drain Fault Indicator. Goes low when a fault condition is present.
28	IN	Connect external bypass capacitor to GND.
—	EP/GND	Exposed Pad Ground Connection. Connect this pad to a contiguous ground plane.

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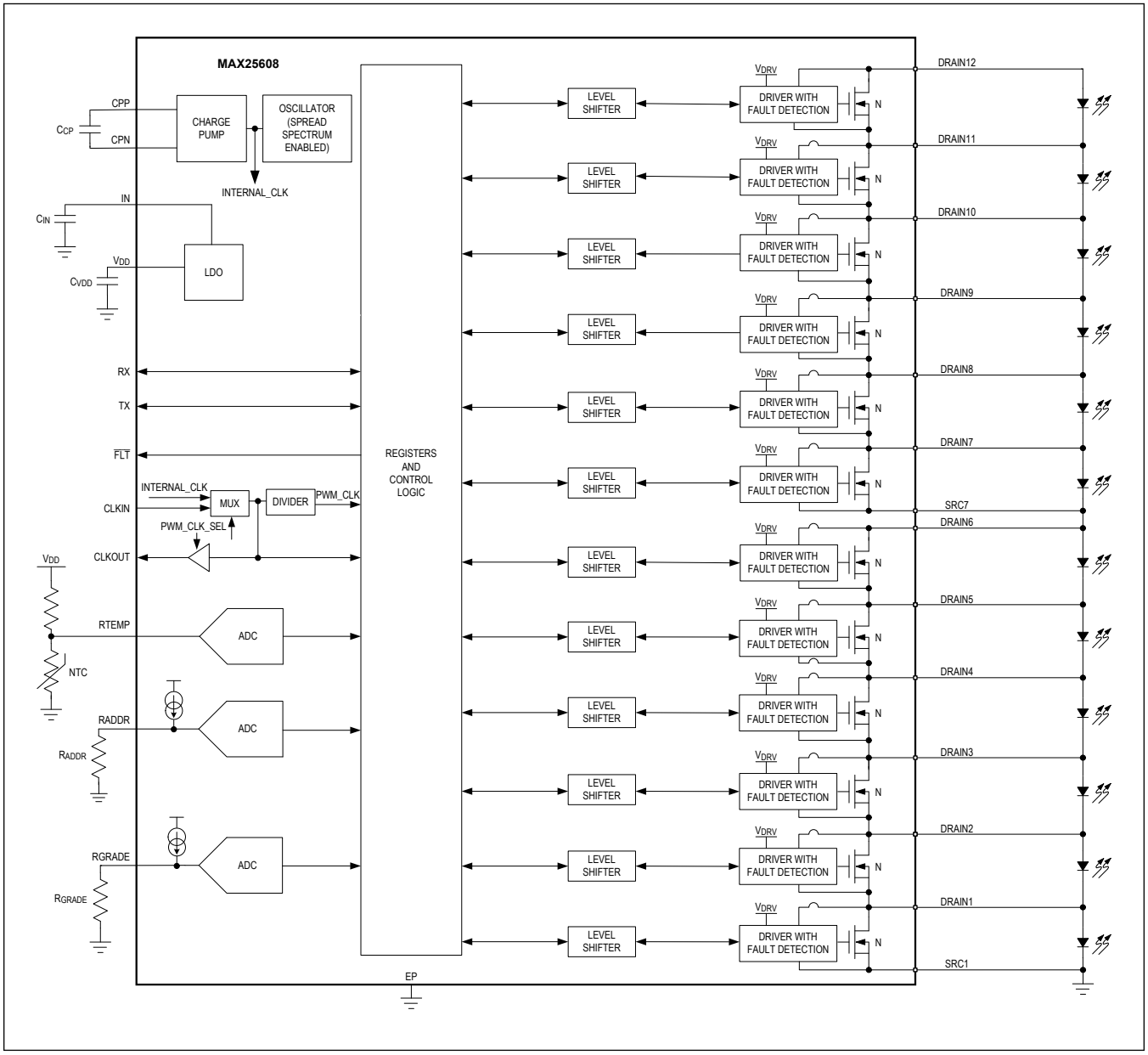
Functional Diagrams

MAX25608 Block Diagram



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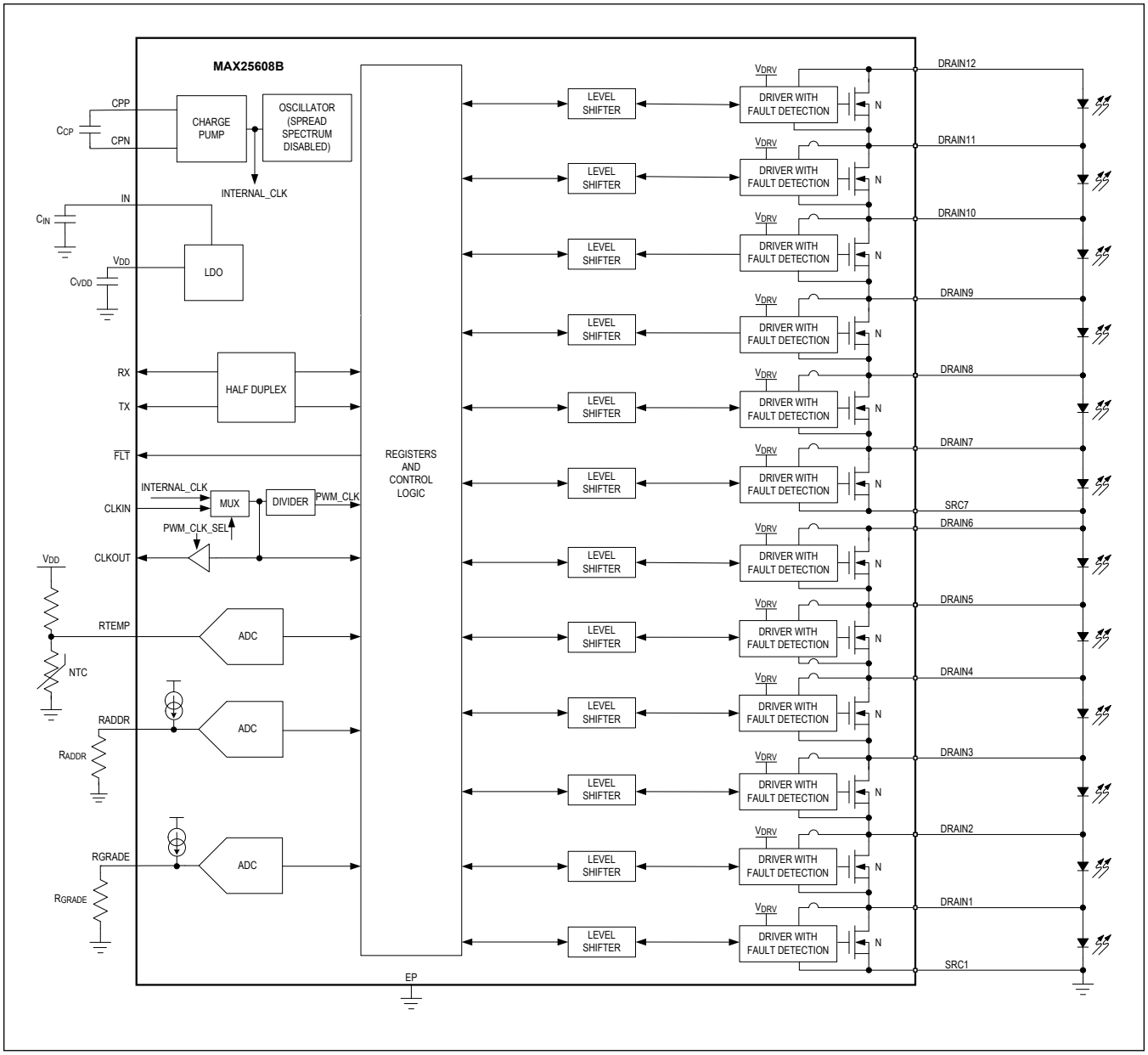
MAX25608B Block Diagram



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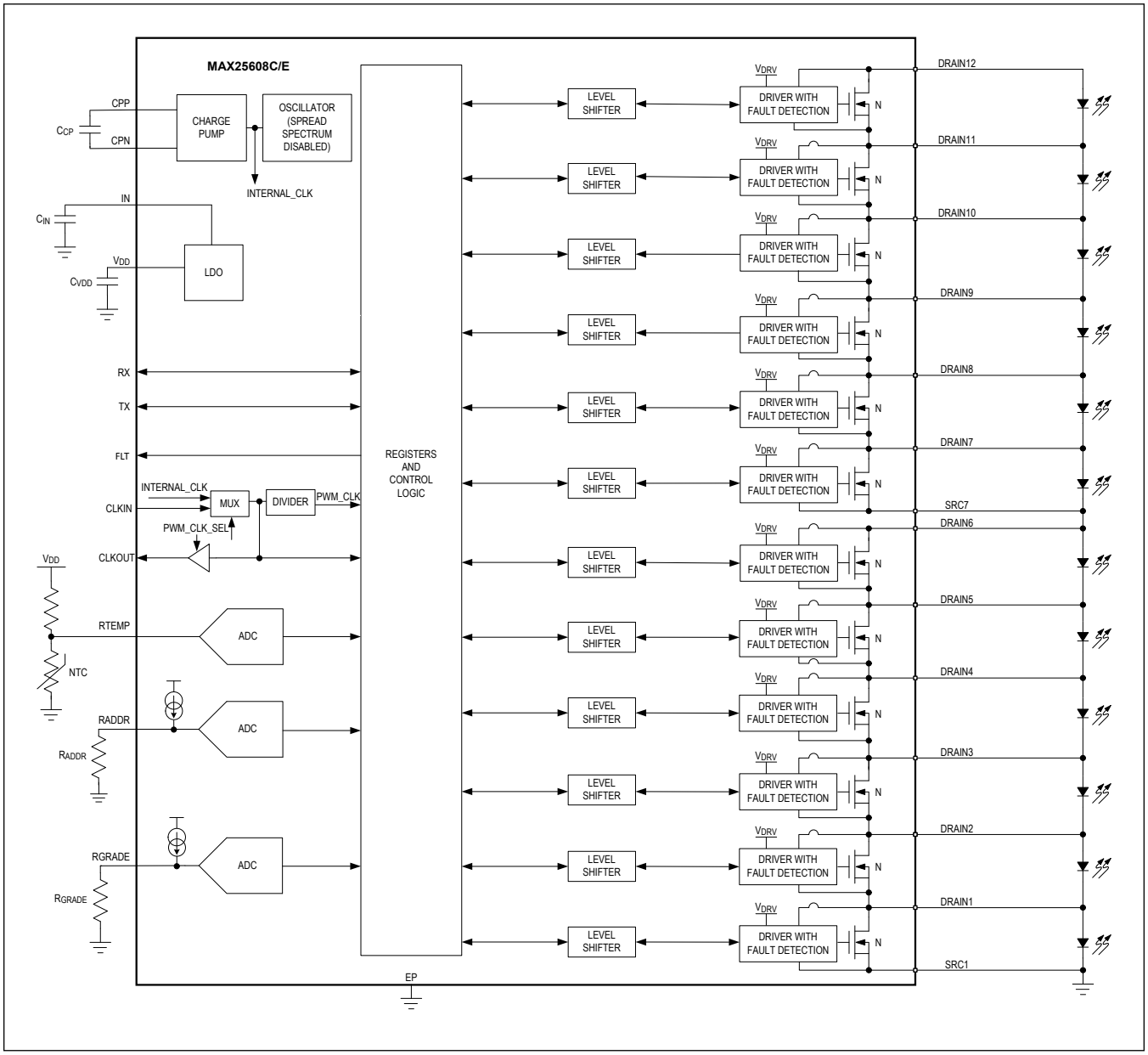
MAX25608C/E Block Diagram



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Detailed Description

Power-on Reset and VDD_UVLO

Once the IC is powered, an internal power-on reset (POR) signal sets all the registers to their default states. All twelve switches are in the on state upon a POR (all LEDs are off). The LEDs remain off until a command is received by the UART. To ensure reliable operation, the IN supply voltage (V_{IN}) must be greater than V_{IN-POR}. If V_{IN} falls below V_{IN-POR} and the V_{DD} regulator output falls below VDD_UVLO, the registers reset to their default state. The IN voltage must be greater than V_{IN-POR} and V_{DD} must be above VDD_UVLO for proper operation. The bypass switches remain in their default on state until the UART is used to enable LED dimming.

Internal Switches

Each switch connected between DRAINn and DRAINn-1 has a typical on-resistance of 0.06Ω. This measurement includes the on-resistance of the internal switch and the resistance of the bond wires to the DRAINn and DRAINn-1 pads. Each bypass switch, when driven to an off state, allows the string current to flow through the corresponding parallel-connected LED, turning the LEDs on. Driving the bypass switch to an on state shunts the current through the bypass switch and turns the LEDs off. Each bypass switch can have one, two, or three LEDs in series across it.

Power-up Sequence

To avoid LED flash while turning ON the power in the system, proper power up sequence has to be followed. First, the matrix manager device MAX25608/MAX25608B/MAX25608C/MAX25608E power must be applied. The device comes up with all the switches ON as soon as it is powered up. The bit SW_GO_EN in register SW_GO (0x01) is 0. The current source driving the LEDs should be enabled after that and so now the current will flow through the closed switches of the device and LEDs will not light up. After that, the required PWM duty cycle can be set up through the UART interface and then the SW_GO_EN is set to 1. This way, the LEDs light up with the required duty cycle.

When the device is running and if the LED current source is disconnected/broken for some reason, the LEDs can light up because of the bias currents flowing through the source/drain pins of the device. The total bias current seen can be close to 180µA on the bottom-most switch drain pin. To avoid the lighting up of the LEDs, 10kΩ resistors can be added across the switches, if needed. This case of undesired LED lighting up can also be managed by setting the SW_GO_EN bit to 0 when there is a fault from the current source.

Spread Spectrum

The MAX25608 has spread spectrum turned on in the charge pump oscillator clock for better EMI performance. The MAX25608B/C/E have spread spectrum turned off on the charge pump oscillator. The proprietary charge pump design gives a good EMI performance even without the spread spectrum option. Spread spectrum is internally turned OFF when a UART transaction happens. When an external clock is used, spread spectrum is used only for the charge pump in the spread-spectrum enabled device (MAX25608). PWM uses the external clock when the external clock is applied instead of internal clock.

The MAX25608 device that has spread spectrum on may show flicker at a duty cycle of <5%. For <5% duty cycle applications with full duplex UART communication, use the MAX25608C/E to avoid flicker.

Programming Options

Pin Resistor Decode Table

Multiple devices can be used in a multidrop UART bus with an external µC acting as the controller. The resistor on RADDR is used to program the UART device ID.

Table 1. Device ID Table

DECODED VALUE OF RADDR RESISTOR	DEVICE ID
0x0	0x0
0x1	0x1

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Table 1. Device ID Table (continued)

DECODED VALUE OF RADDR RESISTOR	DEVICE ID
...	...
0xF	0xF

Resistor Programming Table

A resistor connected between pins RADDR and GND is used to configure the device ID, and the resistor connected between pins RGRADE and GND is used for LED binning. The IC provides 16 levels of detection between 0 and 1.2V on RADDR/RGRADE pins. The pins source 400µA, allowing the use of an external resistor between RADDR/RGRADE and GND to set the voltage level. See Table 2 for recommended RGRADE/RADDR resistor values.

Table 2. RADDR/RGRADE Recommended Values

RGRADE/RADDR[3:0] DECODE VALUE	RGRADE/RADDR RESISTOR VALUE (Ω, 1%)
0000	95
0001	200
0010	309
0011	422
0100	536
0101	649
0110	768
0111	909
1000	1050
1001	1210
1010	1400
1011	1620
1100	1870
1101	2150
1110	2490
1111	2870

PWM Dimming

The IC provides 12-bit programmable dimming on each individual switch. An internal 12-bit counter (COUNT) is generated according to the clock settings. The switch turns off when COUNT is equal to the delay set by the corresponding PSFT register and stays off until the COUNT exceeds the sum of PSFT and PWM duty-control registers. In this way, the duty cycle and relative phase shift of the individual switches can be set independently (see Figure 1).

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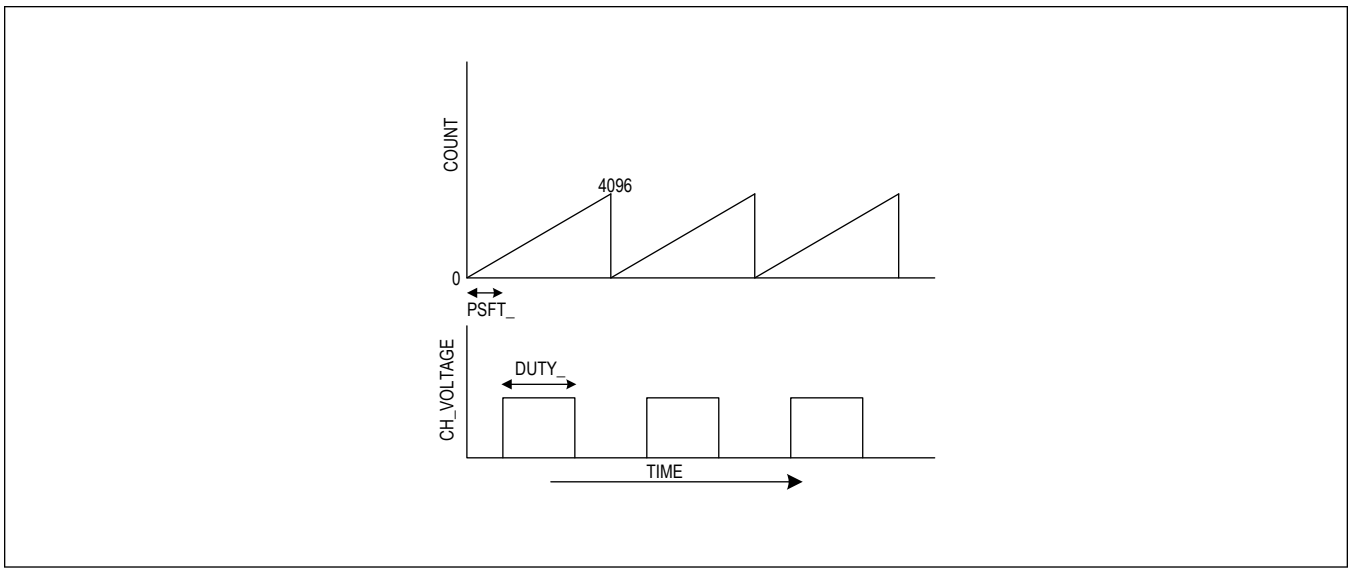

Figure 1. PWM Dimming

PWM Clock and Synchronous Operation with Multiple Devices

The PWM clock for the IC can be selected from the internal oscillator or from an external clock source driving the CLKIN pin. When an external clock is applied, only the PWM generation uses this clock. The CLKOUT pin can be configured to pass either the CLKIN or the internal oscillator as an output to other devices. In this manner, a single clock signal can be used to synchronize all devices. The PWM clock source and CLKIN/CLKOUT function are configured through PWM_CLK[1:0] in the CNFG_GEN (0x02) register. The default value is from the internal oscillator with the CLKIN and CLKOUT disabled. When the part is configured for external clock and if the external clock is missing, the part automatically switches to the internal clock.

PWM dimming frequency is programmable by setting the value of the DIV[1:0] bits in the CNFG_GEN (0x02) register, which sets the divide ratio for both the internal (16.38MHz) and external clock sources. Note that if a different external clock source is used, the PWM frequency will scale as a ratio of internal (16.38MHz) to external clock frequency for a fixed frequency divider value.

Synchronized operation with multiple devices is achieved through the following steps:

1. Set the SW_GO_EN bit to 0.

2. Select the controller device based on the resistor on RADDR pin and set the PWM_CLK[1:0] bits in the CNFG_GEN (0x02) register to use the internal oscillator and CLKOUT active.

3. Select the peripheral devices individually based on the resistor on RADDR pin and set the PWM_CLK[1:0] bits in the CNFG_GEN (0x02) register to keep the CLKIN and CLKOUT active. Connect the CLKOUT of the controller device to the CLKIN of the first peripheral device and the CLKOUT of the first peripheral device to the CLKIN of the 2nd peripheral device and so on.

4. Use the Global write command to set the SW_GO_EN bit to 1. All the PWM clocks of the devices will be synchronized now.

Dimming With and Without Fade

Each switch of the IC can be independently programmed to perform dimming without fade transition or dimming with fade transition. For dimming without fade transition, the dimming changes from the initial value to the target value in one dimming cycle. For dimming with fade transition, the dimming changes transitionally step by step, starting from the initial value to the target value in multiple dimming cycles, following a predetermined exponential curve.

To enable dimming with fade transition, set the FADE bit to 1 and the DUTY bits to the target value for the specific switches. Each transitional step value is calculated using 12 bits according to the following formula:

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DUTYnext = DUTYnow x CF

where DUTY is the duty cycle expressed as an integer value between 1 and 4096 (12-bit resolution), and CF is the constant factor.

CF = 1.0625 and CF = 0.9375 for an up transition and down transition, respectively.

DUTYnext continues to be updated according to the formula until DUTYnext reaches the target value.

For example, as shown in Figure 2, if a command is sent to increase the duty cycle from 10% to 20% updating every four PWM cycles, then the next duty cycle will be 409 x 1.0625 = 434, or 10.6% duty. This value will be held for four PWM cycles, and then would be updated again to 461 (11.25% duty).

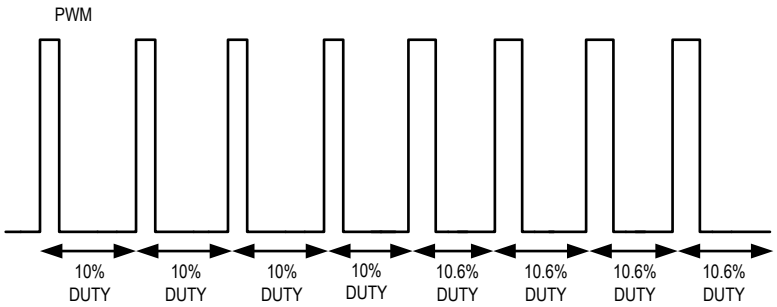

Figure 2. Starting from 10% Duty, Updating Every Four PWM Cycles

The number of dimming cycles that the duty cycle is held for is defined by the TDIM_ register for the switch. The number of transitional steps depends on the distance between the initial value and the target value. The maximum number of transitional steps from 1/4096 to 4096/4096 is 146 steps. See Figure 3 for the up-transition curve. The maximum number of transitional steps from 4096/4096 to 1/4096 is 123 steps. See Figure 4 for the down-transition curve.

Each step runs TDIM_ PWM dimming cycles, and each dimming cycle consists of 8,192 clock cycles by default, therefore t_{STEP} = TDIM_ x 8,192. The 8,192 clock cycles timer can also be changed to 16,384, 32,768, or 65,536 clock cycles by programming bits [3:2] in register address 0x02.

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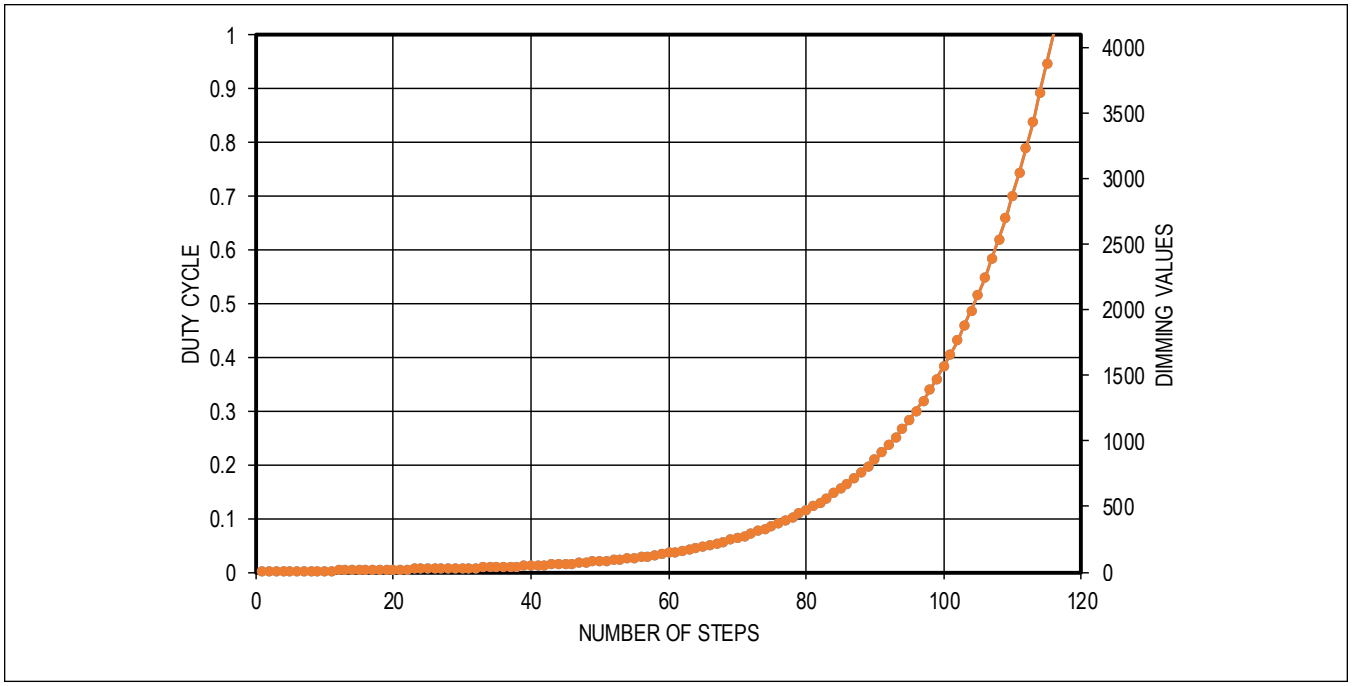

Figure 3. Up-Transition Curve

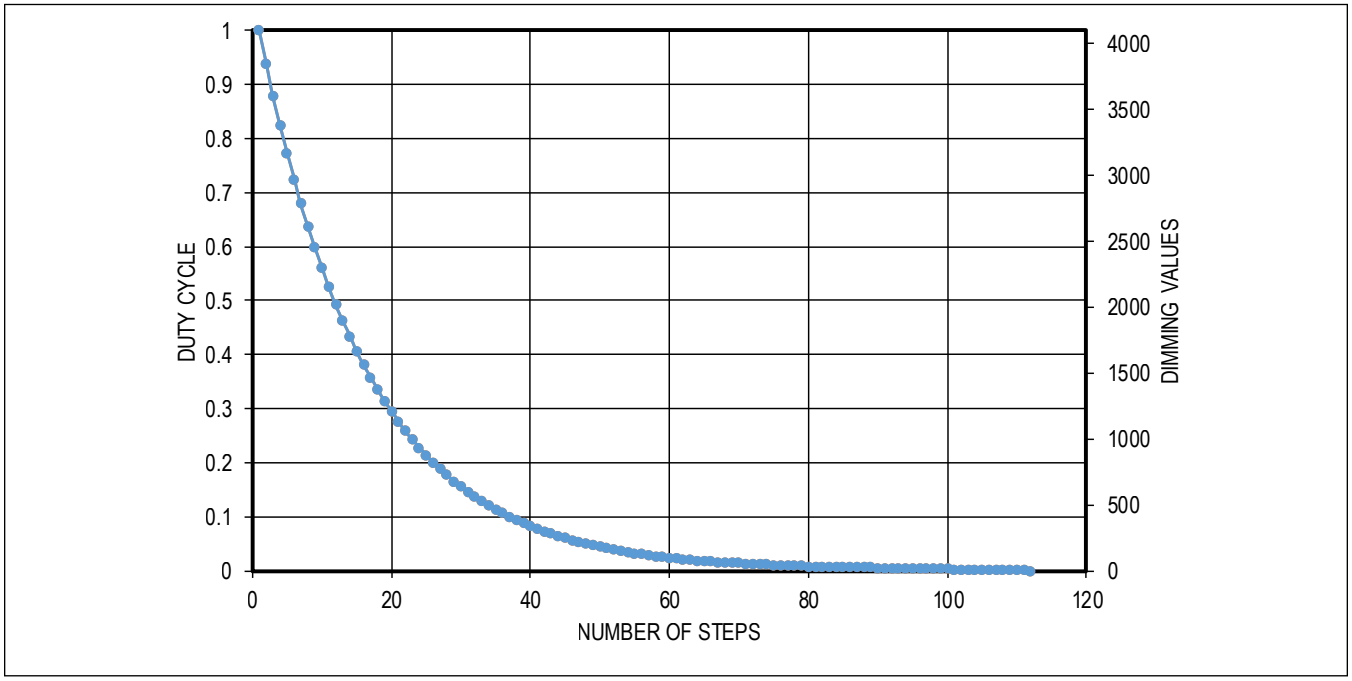

Figure 4. Down-Transition Curve

RTEMP

The RTEMP pin is an auxiliary 8-bit ADC input that is suitable for use with an external NTC resistive divider for monitoring external temperature. In this way, a remote NTC resistor can be used to monitor the external LED temperature for current derating and system monitoring. The 8-bit code is updated with a period of 200 microseconds and can be read back

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using the UART RTEMP register (0x15).

Fault Pin Behaviour

The $\overline{FLT}$ pin will assert whenever one or more of these conditions is present:

- One or more floating domain gate drivers have detected an open-LED fault; in this case, the switch(es) with Open LED faults remain closed until the power is reset
- One or more floating domain gate drivers have detected a short-LED fault condition
- Thermal warning/shutdown
- RGRADE pin is open, shorted to ground, or out of range
- UART errors happen

LED Fault Detection and Protection

The IC is able to detect a shorted LED and an open LED. To detect and report a LED fault, several conditions must be met. First, the LED switch must be operating, then the duty cycle must be greater than 0 since both LED-open and LED-short detection require the switch to be open. Open-fault detection is possible with a PWM duty cycle of 100% and short detection is not possible with 100% PWM duty cycle. For 100% PWM duty cycle requirements, the duty cycle may be set to 99.9% or lower to detect short LED faults. In general, it takes up to one dimming cycle to make sure these conditions have been met after a fault condition is applied. This period depends on the PWM dimming frequency.

LED Open-Fault Detection and Protection

An open-LED fault is triggered when the voltage between the individual LED switch DRAIN node and switch SOURCE node exceeds V_{OTH} and is reported in register OPEN_LED_STAT (0x13). The switch is closed when an open-LED is detected and remains closed. By default, the open fault results in the $\overline{FLT}$ pin being driven low; however, open faults can be masked by writing 0b1 to the MSK_OPEN_LED bit in the CNFG_MSK (0x0C) register. If an open-LED fault is detected multiple times, it is recommended that the OPEN__LED_OVRD (0x09) register be updated to force the corresponding LED switch to remain closed continuously to provide a bypass for the faulty LED.

For applications with 1 LED across the switch, use the open threshold setting as either 9.33V (typ) or 14V (typ). For applications with 2 or 3 LEDs across each switch, use the open threshold setting of 14V (typ).

Resetting Slew Rate, Open, and Short Threshold Registers with V_{IN} Cold Crank

When a cold-crank event happens, the input supply to the IC can go down to around 1.5V and come back up. The slew rate, open, and short threshold registers need to be reset properly in this condition.

After a V_{IN} cold-crank event, send a write command to the CNFG_GEN_1 register that has a change in at least 1 bit, and then resend the required data. This ensures that the part operates with the intended register values after a cold-crank event.

LED Short Detection

A short-LED fault is triggered when the voltage between the switch DRAIN node and the switch SOURCE node is below V_{STH} for an open switch condition, and is reported in the SHRT_LED_STAT (0x12) register. The LED short comparator is sampled at the end of each LED pulse to avoid false detections during the beginning of the pulse. No action is taken with the switch in response to detecting a short-LED fault, thus continuing to operate as programmed. The short fault, by default, results in $\overline{FLT}$ being driven low; however, short faults can be masked by writing 0b1 to MSK_SHRT_LED in the CFG_MSK (0x0C) register.

The Low Duty Threshold register (0x16) is used to filter out LED fault signals during short duty cycles when the voltage across the switch might not settle to a final value, causing an invalid detection of the Short LED condition. When the DUTY register of a switch is less than LOW_DUTY_TH, the SHORT_LED signal is masked and SHORT_LED_STAT is not asserted for that switch.

Open-Trace Detection (MAX25608E Only)

An open-trace fault is triggered when the current through the closed switch is less than 230mA (max) and is reported in the OPEN_TRACE_STAT (0x14) register. No action is taken with the channel switch in response to detecting an open trace with it continuing to operate as programmed. By default, the open-trace fault results in the FLT output being

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driven low; however, open-trace faults can be masked by writing 0b1 to MSK_OPEN_TRACE in the CNFG_MSK (0x0C) register.

The open-trace fault is sampled before the rising PWM edge, which is the edge turning the switch from on to off. If there is an open trace to the drain side of the switch, the switch above it has to be open during the PWM rising edge of the switch that is detecting the condition. For example, if there is an open trace on the drain side of SW2, as shown in Figure 5, then switch SW3 must be open when SW2 is turning off and, similarly, for detecting an open-trace condition on the drain of SW1 (SW2 must be open when SW1 is turning off). For the top-most switch SW3 drain connection and the bottom most switch source connection, there is no constraint to detect the open-trace condition.

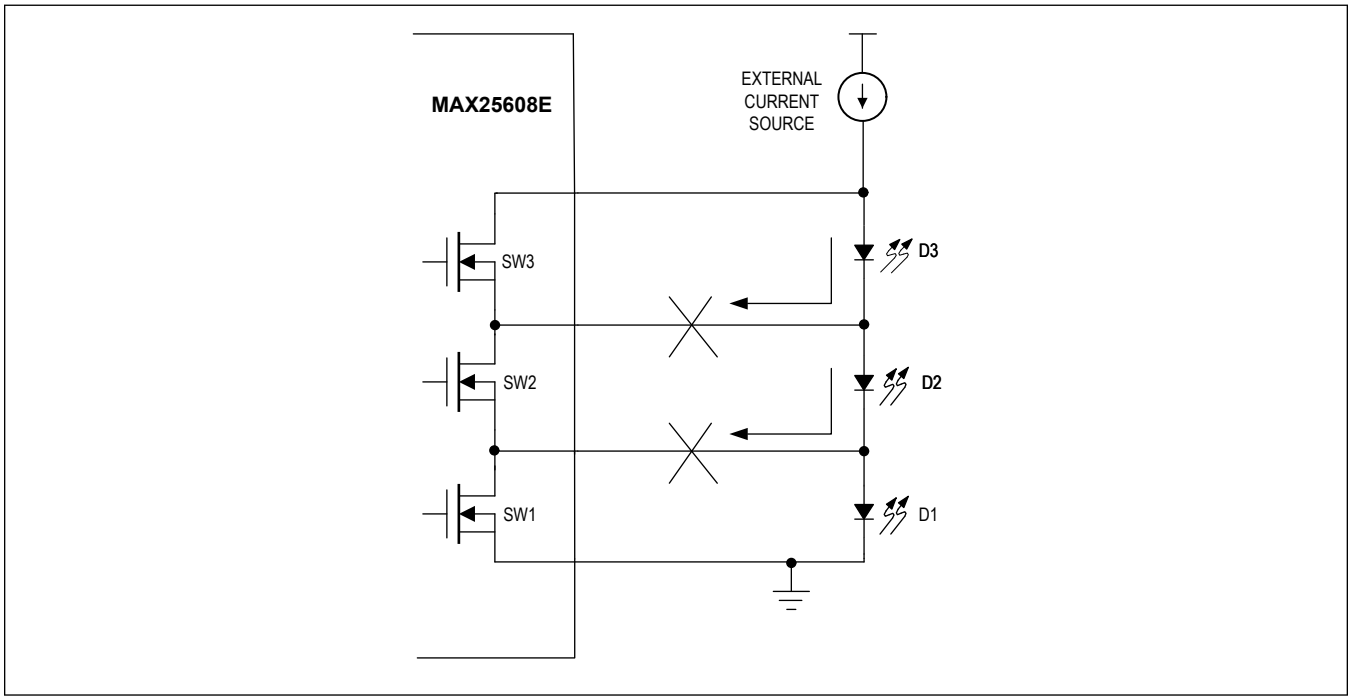

Figure 5. Open-Trace Detection in MAX25608E

Unused Switches and Pins

If some of the switches in the IC are unused, it is recommended to SHORT the pins of the unused switches together and leave it open (do not connect to ground). All of the faults associated with these unused switches should be masked using the appropriate bits in CNFG_MSK_LED.

If the RTEMP/RGRADE pin is unused, connect it to ground.

The CLKIN pin should be grounded, except for the applications when it is needed to synchronize to an external clock.

The CLKOUT pin should be left floating if the part is used independently. For applications with more than one part, see the *PWM Clock and Synchronous Operation with Multiple Devices* section.

Thermal Shutdown

The IC features an on-chip temperature-protection circuit to prevent the device from overheating.

When the die temperature rises above the thermal-warning threshold (+140°C), the TH_WARN bit is set, causing the $\overline{FLT}$ pin to be asserted but no action taken with the switches. If asserted, the $\overline{FLT}$ pin remains asserted until the die temperature drops below the thermal-warning threshold, and the TH_WARN register bit is cleared by writing a 1. To clear the TH_WARN bit, the die temperature must be below the thermal-warning threshold. The UART communication works as usual when the part hits thermal warning threshold.

When the die temperature rises above the thermal-shutdown threshold (+160°C), the TH_SHDN bit in STAT_GEN

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register (0x10) is set, causing the $\overline{FLT}$ pin to be asserted and all switches to either be closed (LEDs turned off) or opened (LEDs turned on), depending on the value of the TH_SHDN_ACT bit in CNFG_MSK_GEN (0x0C) register. The UART communication is active but the switches remain either open or closed till the thermal shutdown hysteresis level is reached. When the device recovers from thermal shutdown, it resumes operation from where it was before the thermal shutdown. The $\overline{FLT}$ pin remains asserted until the die temperature drops below the thermal-warning threshold, and both the TH_WARN and TH_SHDN bits are cleared in the STAT_GEN (0x10) register by writing 1 to both bits. The TH_WARN and TH_SHDN status bits are cleared on write.

PCB Layout

Careful PCB layout is critical to achieve clean, stable operation. Follow these guidelines for good PCB layout:

1. The bypass capacitors on pins IN and VDD should be close to the devices. The exposed pad is the ground of the device, and the bypass capacitors should be connected to this ground.
2. The charge pump capacitor between pins CPP and CPN should be close to the device and traces should be short.
3. Connect a 100nF decoupling capacitor on DR12 pin for single-string application. Connect a 100nF decoupling capacitor on DR12 and DR6 pins for dual-string applications.
4. The connection from the current source (LED driver) to the LEDs should be done so that the high LED currents do not flow in the ground of the MAX25608 matrix IC board. For example, if the LEDs and the MAX25608 IC are on the same board, the return LED current from the bottom-most LED or the bottom switch between DR1 and SRC1 should be returned through a separate trace to the connector going to the LED driver board. This ensures that high LED currents do not flow in the MAX25608 IC board. Do not connect the SRC1 pin to the ground of the MAX25608 IC board.
5. For applications where the current source is in the same board as the MAX25608 IC, do not connect SRC1 pin to the exposed pad ground of the MAX25608 IC. The SRC1 pin switch current should return to the LED driver current source through a ground plane without affecting the ground of the MAX25608 IC.

UART Serial Interface

Overview

The MAX25608/MAX25608C/MAX25608E include a full-duplex UART serial interface and the MAX25608B includes a half-duplex (supports CAN physical layer) UART serial interface to enable fully programmable matrix manager functionality. The system ECU/MCU acts as the UART controller, driving read/write packets on the Rx line and receiving packets on the Tx line. The Rx and Tx lines can connect up to 16 devices on a common bus using a star topology. The device address of each IC is pin-programmable using an external resistor to ground on the RADDR pin. Devices can be addressed individually using their Device ID[3:0]. They can also be simultaneously addressed using the General Call ID or by using the programmable Cluster Call ID value.

The baud rate of incoming UART packets on Rx is automatically detected by the device, from a minimum of 10kbps up to a maximum of 950kbps. The device then returns frames on the Tx line at the same baud rate, according to the packet format described in the *UART Frame Format* section.

Device Connections

The UART interface ensures compatibility with standard microcontrollers from a variety of manufacturers. The MAX25608B also enables the use of CAN transceivers for applications where the matrix manager is remote from the microcontroller. The Rx line should be driven by the microcontroller controller. It can be connected to an individual device or to multiple devices in a star topology. The Tx line is an open-drain output. Multiple devices can share the same Tx connection as well. No external timing reference is required, the device automatically detects the bit rate on each Rx packet and adjusts the bit rate of the Tx response accordingly.

UART Packet Format

The MAX25608/MAX25608C/MAX25608E features full-duplex UART communication capabilities—it is able to send and receive data at the same time. Read and write packets can be sent back to back with a minimum delay of at least one bit period between each packet, as shown in Figure 6. This format should also be followed for global/cluster commands for the MAX25608B. The 1-bit length delay is not needed if using two stop bits.

Spacing of one stop bit (1-bit length) between packets is needed.

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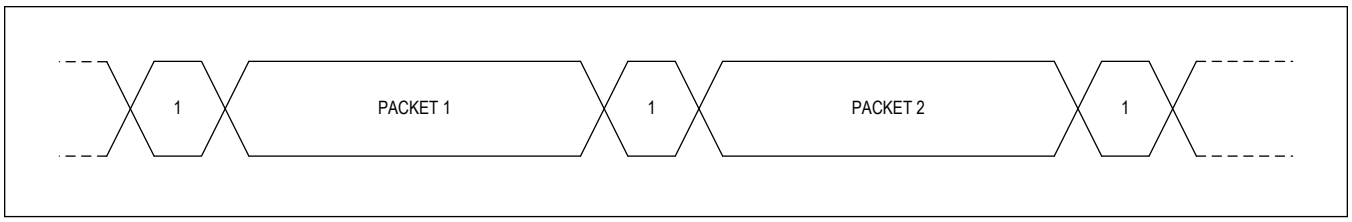

Figure 6. Back-to-Back Write/Read Packets for MAX25608/MAX25608C/MAX25608E

For the MAX25608B version, if using individual write or read commands, the next message may be sent only after the response frames have concluded and after a delay of 1-bit length. This means that for an individual write command, the next message may be sent after the ACK frame has concluded and after a 1-bit length delay, while for a read command the next message may be sent after the three response frames have been sent and a 1-bit delay length. This format is illustrated in Figure 7 and Figure 8.

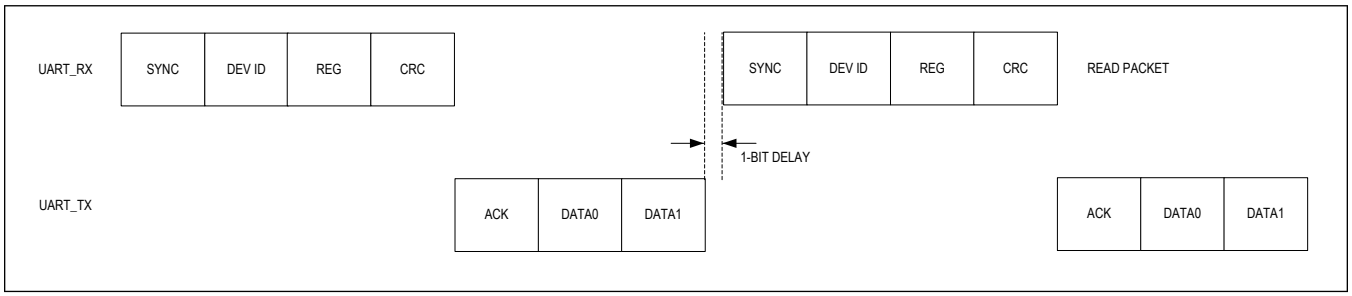

Figure 7. Back-to-Back Read Packet Format for MAX25608B

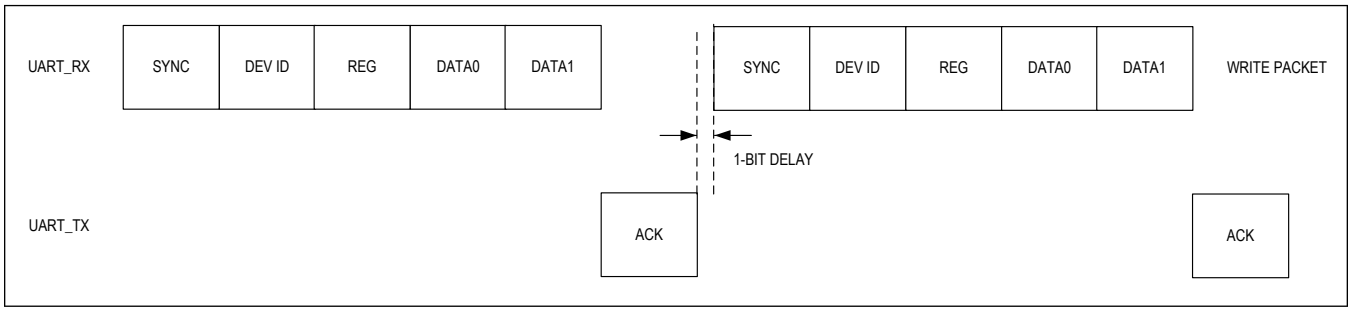

Figure 8. Back-to-Back Write Packet Format for MAX25608B

UART Frame and Interframe Format

Read/write packets are composed from multiple UART frames. Each frame consists of one start bit, eight data bits, one parity bit (even), and two stop bits. The parity bit will be high if the number of ones in the data bits is odd, otherwise it will be low.

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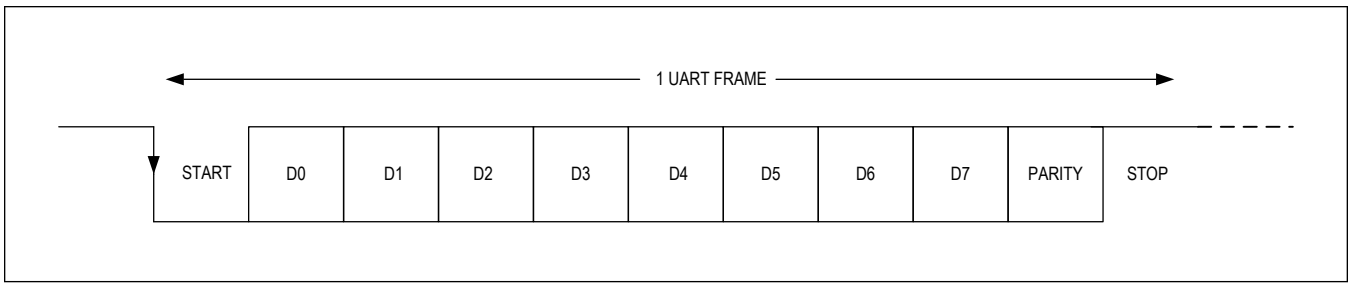

Figure 9. Frame Format

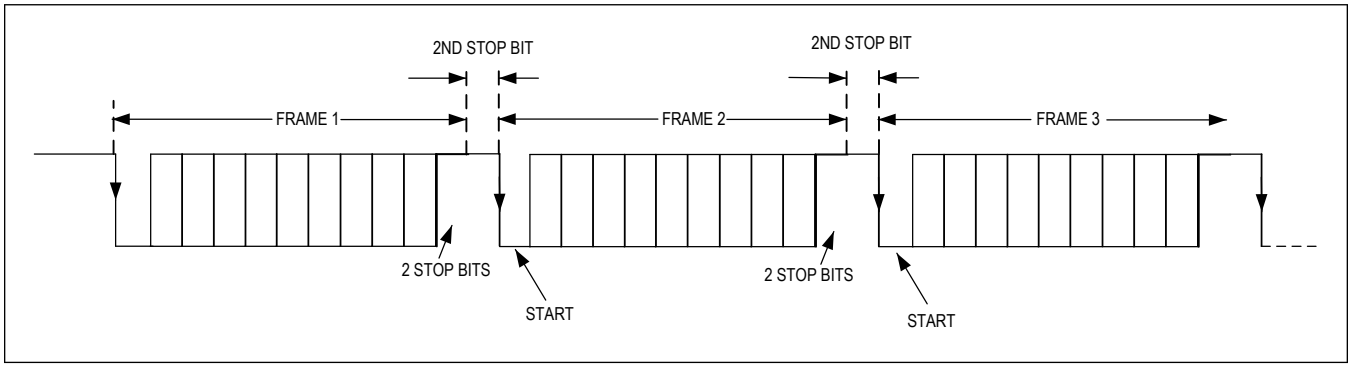

Figure 10. Interframe Format

Between frames, there should be no delay between the second STOP bit and the start of the next frame START bit. If there is a delay between second STOP bit and the start of the next frame START bit, the delay should not exceed 0.5x the bit length minus 350ns. For example, if the baud rate is 950kbps, the delay should not exceed 176ns, and for a baud rate of 500kbps the delay should not exceed 650ns. If these conditions are violated, a bit-sampling error may occur. This will result in a failure to ACK and an assertion of one or more of the following STAT_UART bits: RX_CRC_ERR, RX_PL_PERR, RX_PL_STOP_ERR.

Rx Rise and Fall Times

When the Rx line is driving many of the devices (16x maximum devices can be connected), the capacitive loading on the Rx line becomes high, causing the rise and fall times to become longer. As shown in Figure 11, the Rx bit length generated inside the part is different than the real Rx bit length. If the difference between t_R and t_F starts to become longer than 30ns, the device will extract a slower baud rate. If longer rise and fall times cannot be avoided, a lower baud rate may be selected, or a buffer may be used to reduce the rise and fall times.

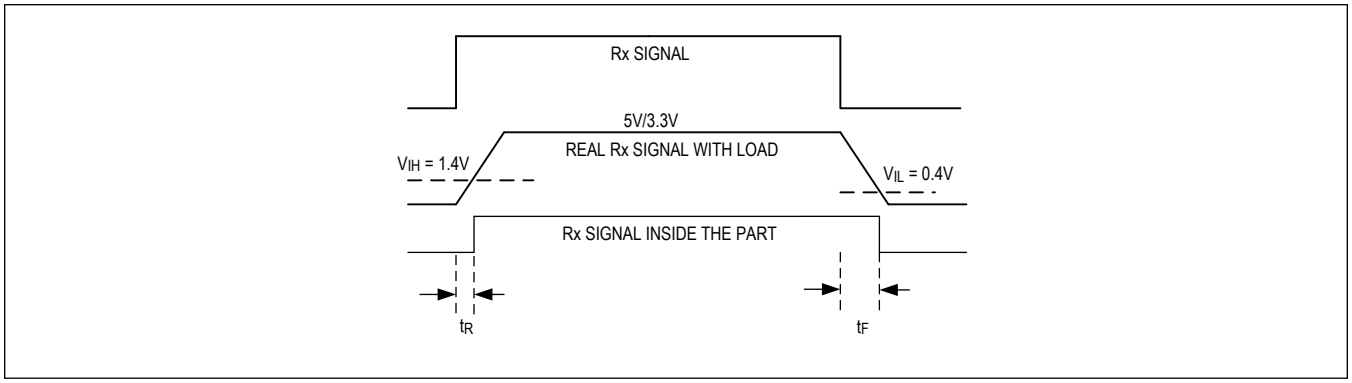

Figure 11. Rx Rise Time and Fall Time

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Synchronization and Acknowledge Frames

Each read/write packet must begin with a special Synchronization (SYNC) frame. This is a UART frame containing the data x79. The device synchronizes to the baud rate starting with the start bit of the SYNC frame. Once the falling edge of the start bit is detected, an internal frame counter is started. This counter counts the number of system clocks throughout the SYNC frame. Once the rising edge of D0 is detected, a second level counter starts and counts the number of system clocks until the next level shift. Once the system detects the falling edge of D0, the level counter is compared to one half of the frame counter. The level counter gets reset on the falling edge of D0, and the number of clocks from D1 to the rising edge of D3 are counted. Once the rising edge of D3 is detected, the system compares the level counter again to one half of the frame counter. This process is then repeated a third time for bits D3 through D6. The level counter and half of the frame counter are compared a third time. If all three comparisons are positive, the SYNC frame is accepted as valid, and the baud rate is determined as the frame counter divided by 8.

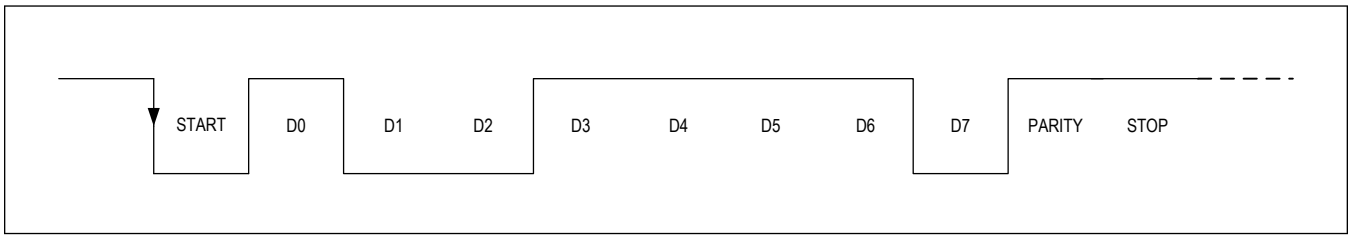

Figure 12. SYNC Frame

Each response packet always begins with a special Acknowledge (ACK) frame. This is a UART frame containing the data xC3.

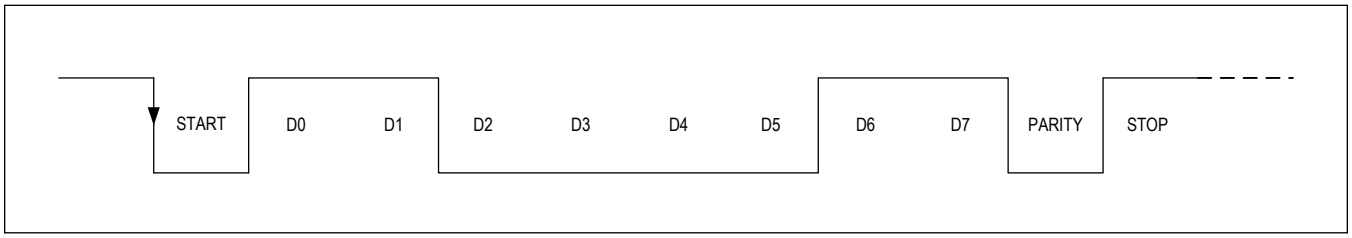

Figure 13. ACK Frame

Device ID and Address Frame Format

Each device in the star configuration should be assigned a unique device ID number using the resistor connected to the RADDR pin. There are 16 possible device IDs that can be assigned in this way, from x00 to x0F (see Table 2).

In addition to addressing devices individually, the device also supports Global Call and Cluster Call write commands. A Global write command addresses all devices on the bus. A Cluster call addresses all devices with a matching cluster call ID in the CNFG_UART register. To perform a Cluster call, first an individual write transaction must occur to assign a Cluster ID (CID) to a particular device (see *CNFG_UART (0x07)*). After each device of interest is given a CID, a Cluster call may be performed by setting the Global/Cluster bit to 1, setting the R/W bit to 0, and writing the 6-bit CID. Data can then be written to all devices with a matching CID. To perform a Global call, set the Global/Cluster bit to 1, the R/W bit to 0, and the address bits to 0x00. This will address all devices on the bus. When performing a Global/Cluster call, the device will not respond with an ACK frame. Back-to-back Global/Cluster call write packets with a 1-bit length delay can be sent with the MAX25608B device. Read commands cannot use the Global/Cluster Call option and must be addressed to a specific device ID.

The address frame data bits are assigned as follows: the MSB is the Global/Cluster call bit, the next 6 bits are the device ID, and the LSB is the Read/Write bit.

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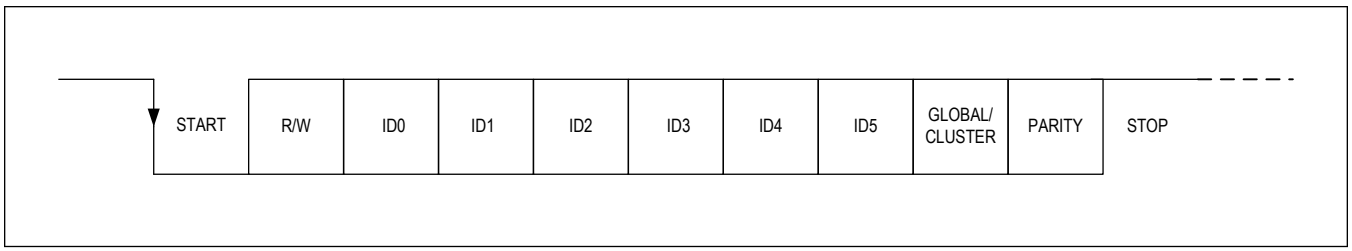

Figure 14. Device ID and Address Frame

Write Transactions

Each write packet consists of five UART frames on the Rx pin. The first frame is the SYNC frame. The second frame consists of the Global/Cluster call flag, then the 6-bit device ID, and then the R/W bit. The R/W bit is low for a write command. The third frame is the register of the address being written to. The fourth frame is the lower byte of the data being written. The fifth and final frame includes the upper 5 bits of the data being written along with the 3-bit CRC code. Upon receiving a valid write packet, the device responds with an ACK frame on the Tx pin for an individual write.

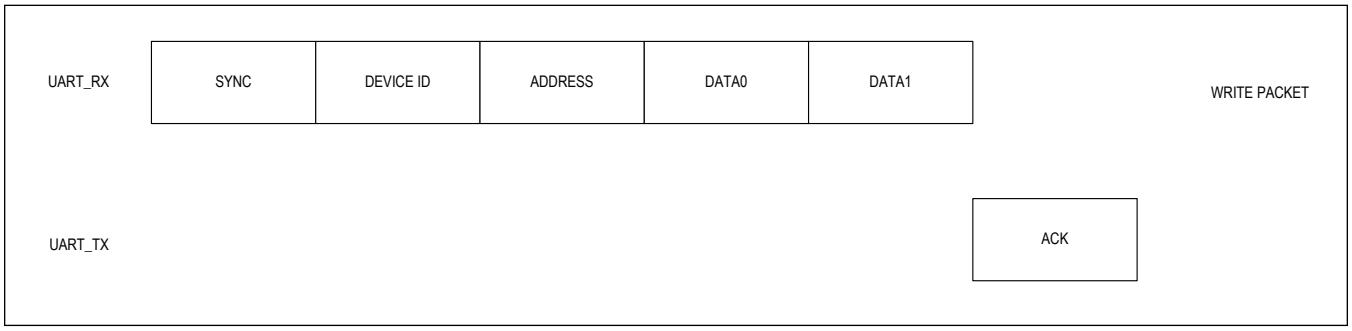

Figure 15. Write Packet

Read Transactions

Each read command consists of four UART frames on the Rx pin. The first frame is the SYNC frame. The second frame consists of the Global/Cluster call bit set low, then the 6-bit device ID, and then the R/W bit set high. The third frame is the register address being written to, which is set by the RADDR value. The fourth and final frame includes the 3-bit CRC code, with the remaining 5 data bits set to 0. Upon receiving a valid read command, the device responds with three frames on the Tx pin. The first frame is the ACK frame. The second frame is the lower 8 data bits of the register being read. The third frame is the 3-bit CRC code, followed by the 5 MSBs of the register being read.

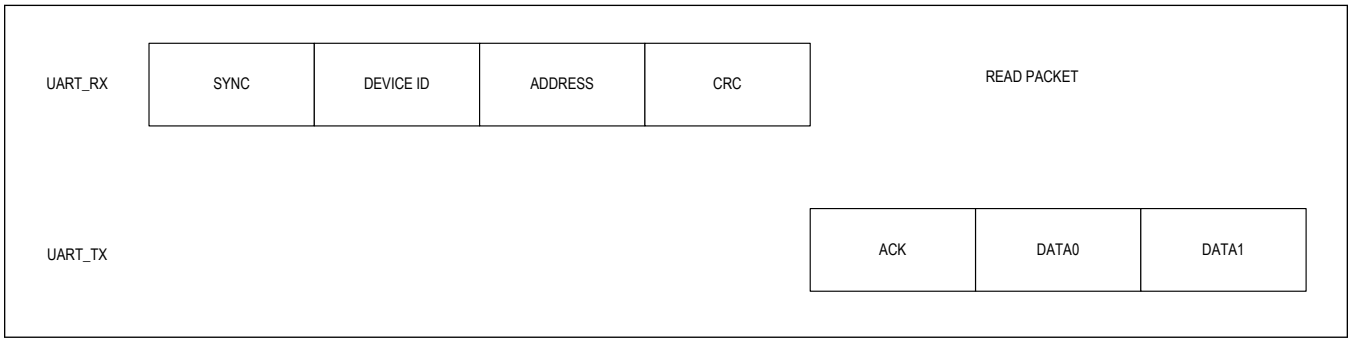

Figure 16. Read Packet

CRC Error Checking

Read/Write transactions are protected using a 3-bit cyclic redundancy check (CRC) on the packet. The CRC is provided

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by the controller on last 3 data bits of each UART_RX packet. For a write transaction, the CRC is calculated using: the 6 data bits of the second frame along with the Global/Cluster bit and the R/W bit, the data byte of the third frame, the data byte of the fourth frame, and the 5 data bits of the fifth frame for a write transaction. For a read transaction, the same process is followed, excluding the fifth frame of data as it is not included during a read transaction. Concerning the calculation of the CRC itself, the 3 bits to be appended are calculated using the LSB of each frame first in a descending order. Meaning that, starting with the second frame, the CRC is calculated starting with the LSB of the data bits of the frame, then moves on to the third, and then stops at the fourth (for a read transaction) or at the fifth (for a write transaction). For response frames on read packets, the device appends its own 3-bit CRC code to the 13-bit read data using the same polynomial.

The CRC calculation uses the polynomial $x^3 + x^1 + 1$ with a starting value of 000.

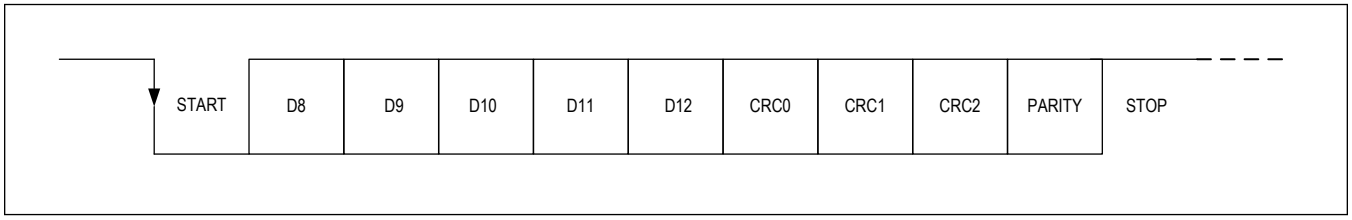

Figure 17. Final Frame

The final frame contains the upper 5 bits of data and the 3 CRC bits.

UART Watchdog Function

The device UART Watchdog feature sets the switches into a preconfigured state in the event of UART communication bus failures. If the CNFG_WATCHDOG bits are set to a nonzero value set, the device asserts a UART_WATCHDOG fault when the UART_RX pin has been inactive for more than the time set by the CNFG_WATCHDOG bits. For lower baud rate applications, the watchdog timer should be configured to be longer than the spacing between the packets. The watchdog timer begins counting when there is no communication on the Rx line, including the space needed between the packets for the MAX25608B. When the UART_WATCHDOG fault is set, the FLT output is asserted low, and the state of the channel switches is set to the value of the WD_LED_STATE register. The default value of WD_LED_STATE is x00, which opens all 12 switches in the event of a watchdog fault. The fault can be masked by setting the MSK_UART_ERR bit in the CNFG_MASK_GEN register. The fault status is cleared by writing a 1 to the UART_WATCHDOG bit. When the fault status is cleared, the switches resume operation according to the values of the PWM registers.

UART Communication Error Handling

In the event that there is an error in communication on UART_RX, it asserts the relevant fault status bit in STAT_UART (x11) and asserts the FLT output. The UART communications faults can be masked by setting the MSK_UART_ERR bit. Faults are cleared by writing 1 to the STAT_UART bits. The following communications errors result in fault assertion:

- UART Watchdog Timeout: UART_RX stops transitioning for more than the time set by the CNFG_WATCHDOG bits in the CONFG_UART register.
- RX_TIMEOUT_ERR: If there is no communication on the Rx line for more than a 16-bit length between frames, this bit will be asserted. If a watchdog timer is set by CNFG_UART, the part will enter into the default LED state set by CNFG_WATCHDOG. Write a 1 to clear this fault to continue normal communication.
- RX_CRC_ERR: Invalid CRC code detected on a UART transaction.
- RX_SYNC_PERR: Parity error in the SYNC frame
- RX_PL_PERR: Parity error in the payload frame
- RX_SYNC_STOP_ERR: Rx SYNC frame stop bit error.
- RX_PL_STOP_ERR: Stop error bit detected in Rx data frames.
- RX_PL_START_ERR: Start error bit detected in Rx data frames.
- Delay between frames exceeds half of a bit length minus 350ns.

UART Timeout Conditions

Timeout is defined as a period of time where the MAX25608/MAX25608B/MAX25608C/MAX25608E do not acknowledge

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any inputs from the Rx line. If the part has received an invalid SYNC frame, timeout will last the default 35ms. If the part has received a valid SYNC frame, but the interframe gap has exceeded 16 times the bit length, then timeout will last for only 16 times the bit length. When the MAX25608/MAX25608B/MAX25608C/MAX25608E enters timeout, any communication sent on the Rx line will cause the timeout period to reset. To bring the part out of timeout, no communication should be sent for the duration of the timeout period. After this time, communication can resume as normal. (See the Figure 18 flowchart for guidance on timeout conditions.) The following list shows under what conditions timeout will occur.

35ms Timeout:

- RX_SYNC_PERR
- RX_SYNC_STOP
- Incorrect SYNC frame

16x Bit Length Timeout:

- RX_TIMEOUT_ERR-- This error will cause the switches to go to the state set by the WD_LED_STATE bits in the CNFG_WATCHDOG register.

No Timeout:

- RX_PL_PERR
- RX_PL_START_ERR
- RX_PL_STOP_ERR
- RX_CRC_ERR

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UART Timeout Flowchart

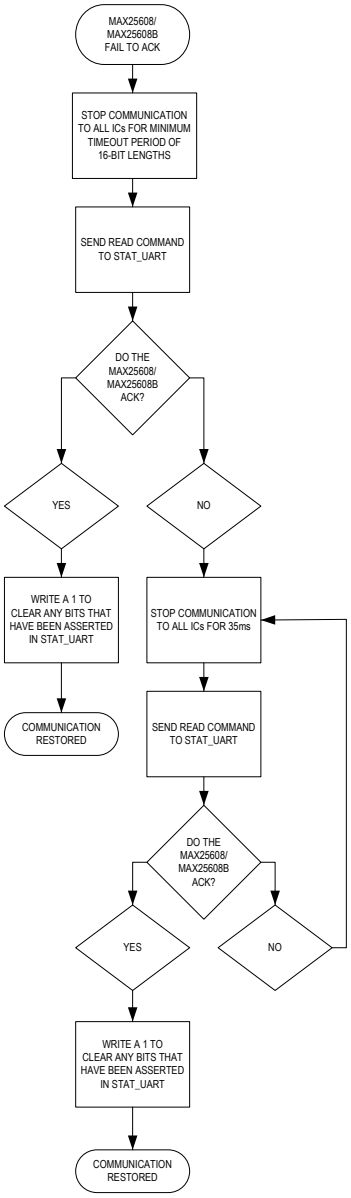

Figure 18. Timeout Flowchart

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Register Map

MAX25608/MAX25608B/MAX25608C/MAX25608E

ADDRESS	NAME	MSB							LSB
USER COMMANDS									
0x00	NO_OP[15:8]				REV_ID[4:0]				
	NO_OP[7:0]	–	–	–	CONSTANT_TEST[4:0]				
0x01	SW_GO[15:8]				–	–	–	–	–
	SW_GO[7:0]	–	–	–	–	–	–	–	SW_GO_EN
0x02	CNFG_GEN_1[15:8]				–	–	–	–	VOTH[1]
	CNFG_GEN_1[7:0]	VOTH[0]	LED_SLEW[2:0]			DIV[1:0]		PWM_CLK_SEL[1:0]	
0x04	CNFG_GEN_2[15:8]				–	VSTH_4[2:0]			VSTH_3[2]
	CNFG_GEN_2[7:0]	VSTH_3[1:0]		VSTH_2[2:0]			VSTH_1[2:0]		
0x05	CNFG_GEN_3[15:8]				–	VSTH_8[2:0]			VSTH_7[2]
	CNFG_GEN_3[7:0]	VSTH_7[1:0]		VSTH_6[2:0]			VSTH_5[2:0]		
0x06	CNFG_GEN_4[15:8]				–	VSTH_12[2:0]			VSTH_11[2]
	CNFG_GEN_4[7:0]	VSTH_11[1:0]		VSTH_10[2:0]			VSTH_9[2:0]		
0x07	CNFG_UART[15:8]				–	–	–	CNFG_WATCHDOG[3:2]	
	CNFG_UART[7:0]	CNFG_WATCHDOG[1:0]		CID[5:0]					
0x08	CNFG_WATCHDOG[15:8]				–	WD_LED_STATE[11:8]			
	CNFG_WATCHDOG[7:0]	WD_LED_STATE[7:0]							
0x09	CNFG_OPEN_OVRD[15:8]				–	OPEN_LED_OVR[11:8]			
	CNFG_OPEN_OVRD[7:0]	OPEN_LED_OVR[7:0]							
0x0A	CNFG_GROUPA[15:8]				–	GROUPA_SEL[11:8]			
	CNFG_GROUPA[7:0]	GROUPA_SEL[7:0]							
0x0B	CNFG_GROUPB[15:8]				–	GROUPB_SEL[11:8]			
	CNFG_GROUPB[7:0]	GROUPB_SEL[7:0]							
0x0C	CNFG_MSK_GEN[15:8]				TH_SHDN_ACT	–	–	–	–
	CNFG_MSK_GEN[7:0]	–	MSK_UART_ERR	MSK_OPEN_TRACE	MSK_OPEN_LED	MSK_SHORT_LED	MSK_CP_RDY_N	MSK_RADC_ERR	MSK_TH_WARN
0x0D	CNFG_MSK_LED[15:8]				–	CNFG_MSK_LED[11:8]			
	CNFG_MSK_LED[7:0]	CNFG_MSK_LED[7:0]							
0x0E	STAT_RADC[15:8]				–	–	–	–	–

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ADDRESS	NAME	MSB							LSB
	STAT_RADC[7:0]	–	–	–	RADC_DONE	RADDR_OVER_RANGE	RGRADE_OVER_RANGE	RADDR_UNDER_RANGE	RGRADE_UNDER_RANGE
0x0F	STAT_RES_CODE[15:8]				–	–	–	–	–
	STAT_RES_CODE[7:0]	DEV_ID[3:0]				RGRADE[3:0]			
0x10	STAT_GEN[15:8]				–	–	OTP_CRC_ERR	CONFIG_NOT_DONE	RADC_ERR
	STAT_GEN[7:0]	EXT_CLK_ERR	UART_ERR	OPEN_TRACE	OPEN_LED	SHORT_LED	CP_RDY_N	TH_SHDN	TH_WARN
0x11	STAT_UART[15:8]				–	–	–	–	UART_WATCHDOG
	STAT_UART[7:0]	RX_TIMEOUT_ERR	RX_CRC_ERR	RX_SYNC_PERR	RX_PL_PERR	RX_SYNC_STOP_ERR	RX_PL_STOP_ERR	RX_PL_START_ERR	–
0x12	STAT_SHORT_LED[15:8]				–	SHORT_LED_STAT[11:8]			
	STAT_SHORT_LED[7:0]	SHORT_LED_STAT[7:0]							
0x13	STAT_OPEN_LED[15:8]				–	OPEN_LED_STAT[11:8]			
	STAT_OPEN_LED[7:0]	OPEN_LED_STAT[7:0]							
0x14	STAT_OPEN_TRACE[15:8]				–	OPEN_TRACE_STAT[11:8]			
	STAT_OPEN_TRACE[7:0]	OPEN_TRACE_STAT[7:0]							
0x15	RTEMP[15:8]				–	–	–	–	–
	RTEMP[7:0]	RTEMP[7:0]							
0x16	LOW_DUTY_TH[15:8]				–	LOW_DUTY_TH[11:8]			
	LOW_DUTY_TH[7:0]	LOW_DUTY_TH[7:0]							
0x20	PSFT_GRP[15:8]				–	–	–	PSFT_GROUP[1:0]	
	PSFT_GRP[7:0]	PSFT[7:0]							
0x21	PSFT_1[15:8]				–	–	–	–	–
	PSFT_1[7:0]	PSFT_1[7:0]							
0x22	PSFT_2[15:8]				–	–	–	–	–
	PSFT_2[7:0]	PSFT_2[7:0]							
0x23	PSFT_3[15:8]				–	–	–	–	–
	PSFT_3[7:0]	PSFT_3[7:0]							
0x24	PSFT_4[15:8]				–	–	–	–	–
	PSFT_4[7:0]	PSFT_4[7:0]							
0x25	PSFT_5[15:8]				–	–	–	–	–
	PSFT_5[7:0]	PSFT_5[7:0]							
0x26	PSFT_6[15:8]				–	–	–	–	–
	PSFT_6[7:0]	PSFT_6[7:0]							

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ADDRESS	NAME	MSB							LSB
0x27	PSFT_7[15:8]				–	–	–	–	–
	PSFT_7[7:0]	PSFT_7[7:0]							
0x28	PSFT_8[15:8]				–	–	–	–	–
	PSFT_8[7:0]	PSFT_8[7:0]							
0x29	PSFT_9[15:8]				–	–	–	–	–
	PSFT_9[7:0]	PSFT_9[7:0]							
0x2A	PSFT_10[15:8]				–	–	–	–	–
	PSFT_10[7:0]	PSFT_10[7:0]							
0x2B	PSFT_11[15:8]				–	–	–	–	–
	PSFT_11[7:0]	PSFT_11[7:0]							
0x2C	PSFT_12[15:8]				–	–	–	–	–
	PSFT_12[7:0]	PSFT_12[7:0]							
0x30	TDIM_GRP[15:8]				–	–	–	–	–
	TDIM_GRP[7:0]	–	–	TDIM_GROUP[1:0]		–	TDIM[2:0]		
0x31	TDIM_3_2_1[15:8]				–	–	TDIM_3[2:0]		
	TDIM_3_2_1[7:0]	–	TDIM_2[2:0]			–	TDIM_1[2:0]		
0x32	TDIM_6_5_4[15:8]				–	–	TDIM_6[2:0]		
	TDIM_6_5_4[7:0]	–	TDIM_5[2:0]			–	TDIM_4[2:0]		
0x33	TDIM_9_8_7[15:8]				–	–	TDIM_9[2:0]		
	TDIM_9_8_7[7:0]	–	TDIM_8[2:0]			–	TDIM_7[2:0]		
0x34	TDIM_12_11_10[15:8]				–	–	TDIM_12[2:0]		
	TDIM_12_11_10[7:0]	–	TDIM_11[2:0]			–	TDIM_10[2:0]		
0x40	PWM_GRPA_DUTY[15:8]				FADE_A	DUTY_A[11:8]			
	PWM_GRPA_DUTY[7:0]	DUTY_A[7:0]							
0x41	PWM_GRPB_DUTY[15:8]				FADE_B	DUTY_B[11:8]			
	PWM_GRPB_DUTY[7:0]	DUTY_B[7:0]							
0x42	PWM1[15:8]				FADE_1	DUTY_1[11:8]			
	PWM1[7:0]	DUTY_1[7:0]							
0x43	PWM2[15:8]				FADE_2	DUTY_2[11:8]			
	PWM2[7:0]	DUTY_2[7:0]							
0x44	PWM3[15:8]				FADE_3	DUTY_3[11:8]			
	PWM3[7:0]	DUTY_3[7:0]							
0x45	PWM4[15:8]				FADE_4	DUTY_4[11:8]			
	PWM4[7:0]	DUTY_4[7:0]							
0x46	PWM5[15:8]				FADE_5	DUTY_5[11:8]			
	PWM5[7:0]	DUTY_5[7:0]							
0x47	PWM6[15:8]				FADE_6	DUTY_6[11:8]			
	PWM6[7:0]	DUTY_6[7:0]							
0x48	PWM7[15:8]				FADE_7	DUTY_7[11:8]			
	PWM7[7:0]	DUTY_7[7:0]							

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ADDRESS	NAME	MSB							LSB
0x49	PWM8[15:8]				FADE_8	DUTY_8[11:8]			
	PWM8[7:0]	DUTY_8[7:0]							
0x4A	PWM9[15:8]				FADE_9	DUTY_9[11:8]			
	PWM9[7:0]	DUTY_9[7:0]							
0x4B	PWM10[15:8]				FADE_10	DUTY_10[11:8]			
	PWM10[7:0]	DUTY_10[7:0]							
0x4C	PWM11[15:8]				FADE_11	DUTY_11[11:8]			
	PWM11[7:0]	DUTY_11[7:0]							
0x4D	PWM12[15:8]				FADE_12	DUTY_12[11:8]			
	PWM12[7:0]	DUTY_12[7:0]							

Register Details

NO_OP (0x00)

NO_OP is a read-only register that reads the content of Revision ID and test pattern.

BIT				12	11	10	9	8
Field				REV_ID[4:0]				
Reset				0x1				
Access Type				Read Only				
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	–	–	–	CONSTANT_TEST[4:0]				
Reset	–	–	–	0b10001				
Access Type	–	–	–	Read Only				

BITFIELD	BITS	DESCRIPTION
REV_ID	12:8	Revision Information: Reads back 5-bit hardware revision ID.
CONSTANT_TEST	4:0	Test Pattern: 0x11 is always returned in this location for interface checking.

SW_GO (0x01)

SW_GO us a read/write register that enables the PWM signals.

BIT		12	11	10	9	8
Field		–	–	–	–	–
Reset		–	–	–	–	–
Access Type		–	–	–	–	–

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BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	SW_GO_EN
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SW_GO_EN	0	Switching Enable signal. Enables LED dimming operation and starts dimming counters. If SW_GO_EN = 0, all LED switches are closed and all PWM counters in the LED Controller are reset to 0. If SW_GO_EN = 1, all LED switches operate according to their programmed values and all PWM counters start counting from 0. SW_GO_EN must be low in order to change any of the CNFG_GEN_1/2/3/4 registers. If SW_GO_EN is high, the configuration change does not complete. The SW_GO_EN command should be issued after CP_RDY_N transitions low on STAT_GEN, ensuring CLK is present and CPP voltage is valid.	0x0: All LED switches are closed, and all PWM counters are reset to 0. 0x1: All LED switches operate according to their programmed values, and all PWM counters start counting from 0.

CNFG_GEN_1 (0x02)

CNFG_GEN_1 is a read/write access register that controls the dimming clock divider ratio, the slew rate of the LED switches, the threshold used for the Open LED fault-detection function, and the functionality of the CLK pin.

SW_GO_EN should be set low before changing any configuration registers.

BIT				12	11	10	9	8
Field				–	–	–	–	VOTH[1]
Reset				–	–	–	–	0b00
Access Type				–	–	–	–	Write, Read

BIT	7	6	5	4	3	2	1	0
Field	VOTH[0]	LED_SLEW[2:0]			DIV[1:0]		PWM_CLK_SEL[1:0]	
Reset	0b00	0x7			0b00		0b00	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
VOTH	8:7	Sets the Open LED Threshold	0x0: 14V 0x1: 9.33V 0x2: Reserved 0x3: Reserved

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BITFIELD	BITS	DESCRIPTION	DECODE
LED_SLEW	6:4	Slew Control for the Internal LED Gate Driver. This register should only be written when SW_GO_EN = 0.	VALUE: DECODE 0x0: 0.04V/µs 0x1: 0.062V/µs 0x2: 0.11V/µs 0x3: 0.20V/µs 0x4: 0.31V/µs 0x5: 0.5V/µs 0x6: 1.0V/µs
DIV	3:2	PWM Dimming-Frequency Select	0x0: Internal/external clock frequency divided by 8,192 0x1: Internal/external clock frequency divided by 16,384 0x2: Internal/external clock frequency divided by 32,768 0x3: Internal/external clock frequency divided by 65,536
PWM_CLK_SEL	1:0	Determines internal/external PWM clock and direction of the CLK pin.	

VALUE	PWM CLOCK	CLKIN	CLKOUT
0x0	Internal	Disabled	Disabled
0x1	Internal	Disabled	Enabled
0x2	CLKIN	Enabled	Disabled
0x3	CLKIN	Enabled	Enabled

CNFG_GEN_2 (0x04)

CNFG_GEN_2 controls the Short LED threshold (VSTH) of switches 1, 2, 3, and 4.

SW_GO_EN should be set low before changing any configuration registers.

BIT		12	11	10	9	8
Field		–	VSTH_4[2:0]			VSTH_3[2]
Reset		–	0x0			0x0
Access Type		–	Write, Read			Write, Read

BIT	7	6	5	4	3	2	1	0
Field	VSTH_3[1:0]		VSTH_2[2:0]			VSTH_1[2:0]		
Reset	0x0		0x0			0x0		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
VSTH_4	11:9	Sets the Short LED Threshold Value for Switch 4	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V

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BITFIELD	BITS	DESCRIPTION	DECODE
VSTH_3	8:6	Sets the Short LED Threshold Value for Switch 3	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V
VSTH_2	5:3	Sets the Short LED Threshold Value for Switch 2	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V
VSTH_1	2:0	Sets the Short LED Threshold Value for Switch 1	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V

CNFG_GEN_3 (0x05)

CNFG_GEN_3 controls the Short LED threshold (VSTH) of switches 5, 6, 7, and 8.

SW_GO_EN should be set low before changing any configuration registers.

BIT		12	11	10	9	8
Field		–	VSTH_8[2:0]			VSTH_7[2]
Reset		–	0x0			0x0
Access Type		–	Write, Read			Write, Read

BIT	7	6	5	4	3	2	1	0
Field	VSTH_7[1:0]		VSTH_6[2:0]			VSTH_5[2:0]		
Reset	0x0		0x0			0x0		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
VSTH_8	11:9	Sets the Short LED Threshold Value for Switch 8	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V

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BITFIELD	BITS	DESCRIPTION	DECODE
VSTH_7	8:6	Sets the Short LED Threshold Value for Switch 7	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V
VSTH_6	5:3	Sets the Short LED Threshold Value for Switch 6	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V
VSTH_5	2:0	Sets the Short LED Threshold Value for Switch 5	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V

CNFG_GEN_4 (0x06)

CNFG_GEN_4 controls the Short LED threshold (VSTH) of switches 9, 10, 11, and 12.

SW_GO_EN should be set low before changing any configuration registers.

BIT		12	11	10	9	8
Field		–	VSTH_12[2:0]			VSTH_11[2]
Reset		–	0x0			0x0
Access Type		–	Write, Read			Write, Read

BIT	7	6	5	4	3	2	1	0
Field	VSTH_11[1:0]		VSTH_10[2:0]			VSTH_9[2:0]		
Reset	0x0		0x0			0x0		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
VSTH_12	11:9	Sets the Short LED Threshold Value for Switch 12	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V

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BITFIELD	BITS	DESCRIPTION	DECODE
VSTH_11	8:6	Sets the Short LED Threshold Value for Switch 11	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V
VSTH_10	5:3	Sets the Short LED Threshold Value for Switch 10	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V
VSTH_9	2:0	Sets the Short LED Threshold Value for Switch 9	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V

CNFG_UART (0x07)

CNFG_UART is a read/write access register that controls how the UART is configured, namely the cluster ID assignment and the operation of the UART Watchdog Timer.

BIT				12	11	10	9	8
Field				–	–	–	CNFG_WATCHDOG[3:2]	
Reset				–	–	–	0x0	
Access Type				–	–	–	Write, Read	
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	CNFG_WATCHDOG[1:0]		CID[5:0]					
Reset	0x0		0b000001					
Access Type	Write, Read		Write, Read					

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BITFIELD	BITS	DESCRIPTION	DECODE
CNFG_WATCHDOG	9:6	This field controls the duration of the UART Watchdog Timer. When CNFG_WATCHDOG is set to a nonzero value, and no valid UART commands are received for a duration set by the CNFG_WATCHDOG field, the UART_Watchdog status bit is set. When the UART_Watchdog status bit is set: (1) The FLT pin is asserted. (2) The state of the switches is set according to the WD_LED_STATE register.	0x0: Disabled 0x1: 200µs 0x2: 500µs 0x3: 1ms 0x4: 2ms 0x5: 5ms 0x6: 10ms 0x7: 20ms 0x8: 50ms 0x9: 100ms 0xA: 200ms 0xB: 500ms 0xC: 1s 0xD: 2s 0xE: 5s 0xF: 5s
CID	5:0	Cluster Identification: During a cluster call write transaction, the UART accepts the transaction if the received CID[5:0] matches the contents of this register.	

CNFG_WATCHDOG (0x08)

BIT		12	11	10	9	8
Field		–	WD_LED_STATE[11:8]			
Reset		–	0x0			
Access Type		–	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	WD_LED_STATE[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
WD_LED_STATE	11:0	Sets the state of LEDs when watchdog timeout and Rx timeout conditions are detected.	0x0: Switch Open 0x1: Switch Closed

CNFG_OPEN_OVRD (0x09)

OPEN_OVRD is a read/write register that overrides the LED switching control signals. When this feature is disabled, the LED switch operates normally. When this feature is enabled, the LED switch is always forced to a closed position (i.e., the LED duty cycle is zero, regardless of the DUTY or TDIM settings).
The intent is to allow the µP to manually force the switch to stay closed after it has determined the particular LED is permanently opened. This further suppresses fault signals from the switch(es) since LED faults are only detected when the switch opens.

BIT		12	11	10	9	8
Field		–	OPEN_LED_OVR[11:8]			
Reset		–	0x000			
Access Type		–	Write, Read			

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BIT	7	6	5	4	3	2	1	0
Field	OPEN_LED_OVR[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
OPEN_LED_OVR	11:0	Open-LED Override: Program these bits to force the corresponding switch(es) to always be closed. This overrides the state of the corresponding DUTY registers.	0x0: Normal 0x1: LED switch is always closed.

CNFG_GROUPA (0x0A)

CNFG_GRPA is a read/write register that allows the user to assign particular LED drivers to this group. LED drivers assigned to this group respond to qualified transactions on the following registers:

- PSFT_GRP (if PSFT_GROUP==0001)
- TDIM_GROUP (if TDIM_GROUP=0001)
- PWM_GRPA_DUTY

BIT		12	11	10	9	8
Field		–	GROUPA_SEL[11:8]			
Reset		–	0x000			
Access Type		–	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	GROUPA_SEL[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
GROUPA_SEL	11:0	Set high if assigning a register to GroupA.	0x0: Not assigned 0x1: Assigned

CNFG_GROUPB (0x0B)

CNFG_GRPB is a read/write register that allows the user to assign particular LED drivers to this group. LED drivers assigned to this group respond to qualified transactions on the following registers:

- PSFT_GRP (if PSFT_GROUP==00010)
- TDIM_GROUP (if TDIM_GROUP=0010)
- PWM_GRPB_DUTY

BIT		12	11	10	9	8
Field		–	GROUPB_SEL[11:8]			
Reset		–	0x000			
Access Type		–	Write, Read			

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BIT	7	6	5	4	3	2	1	0
Field	GROUPB_SEL[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
GROUPB_SEL	11:0	Set high if assigning a register to GroupB.	0x0: Not assigned 0x1: Assigned

CNFG_MSK_GEN (0x0C)

CNFG_MSK is a read/write access register that controls the masking of fault conditions from the $\overline{FLT}$ pin.

BIT				12	11	10	9	8
Field				TH_SHDN_ACT	–	–	–	–
Reset				0b0	–	–	–	–
Access Type				Write, Read	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	MSK_UART_ERR	MSK_OPEN_TRACE	MSK_OPEN_LED	MSK_SHORT_LED	MSK_CP_RDY_N	MSK_RADC_ERR	MSK_TH_WARN
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TH_SHDN_ACT	12	Thermal-Shutdown Action: This bit selects whether to open or close the LED switches when a TH_SHDN is high.	0x0: Closes all LED switches. 0x1: Opens all LED switches.
MSK_UART_ERR	6	Masks UART_ERR to FAULTB.	0x0: UART_ERR being set high asserts the $\overline{FLT}$ pin. 0x1: UART_ERR bit does not assert the $\overline{FLT}$ pin.
MSK_OPEN_TRACE	5	Masks all open-trace detections to $\overline{FLT}$ pin.	0x0: Any OPEN_TRACE__ detects assert the $\overline{FLT}$ pin. 0x1: Any OPEN_TRACE__ detects do not assert the $\overline{FLT}$ pin.
MSK_OPEN_LED	4	Masks all open-LED detections to $\overline{FLT}$ pin.	0x0: Any OPEN_LED__ detections assert the $\overline{FLT}$ pin. 0x1: Any OPEN_LED__ detections do not assert the $\overline{FLT}$ pin.
MSK_SHORT_LED	3	Masks all STAT_SHORT_LED detections to $\overline{FLT}$ pin	0x0: Any STAT_SHORT_LED bits set high assert the $\overline{FLT}$ pin. 0x1: Any STAT_SHORT_LED bits set high do not assert the $\overline{FLT}$ pin.
MSK_CP_RDY_N	2	Mask CP_RDY_N to FAULTB.	0x0: CP_RDY_N asserts the $\overline{FLT}$ pin. 0x1: CP_RDY_N does not assert the $\overline{FLT}$ pin.
MSK_RADC_ERR	1	Masks RADC_ERR to FAULTB.	0x0: No masking of RADC_ERR. 0x1: Mask RADC_ERR from generating fault.

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BITFIELD	BITS	DESCRIPTION	DECODE
MSK_TH_WARN	0	Mask-Thermal Warning to FAULTB.	0x0: TH_WARN asserts the $\overline{FLT}$ pin. 0x1: TH_WARN does not assert the $\overline{FLT}$ pin.

CNFG_MSK_LED (0x0D)

CNFG_MSK_LED prevents LED faults from asserting the $\overline{FLT}$ pin. This allows the µP to instruct the part to ignore faults from a particular LED when that LED is deliberately not populated in the application.

BIT				12	11	10	9	8
Field				–	CNFG_MSK_LED[11:8]			
Reset				–	0x000			
Access Type				–	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	CNFG_MSK_LED[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CNFG_MSK_LED	11:0	Set bit(s) high to mask OPEN_LED and SHORT_LED from those LEDs asserting $\overline{FLT}$ pin.

STAT_RADC (0x0E)

Status indicators for RGRADE and RADDR decoding

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	RADC_DONE	RADDR_OVER_RANGE	RGRADE_OVER_RANGE	RADDR_UNDER_RANGE	RGRADE_UNDER_RANGE
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RADC_DONE	4	Status Indicator for RADDR/RGRADE decoding	0x0: RADC measurement incomplete 0x1: RADC measurement is complete
RADDR_OVER_RANGE	3	Indicates that the RADDR resistor value is above the supported range.	0x0: Normal operation 0x1: RADDR Over Range, or an open is detected.
RGRADE_OVER_RANGE	2	Indicates that the RGRADE resistor value is above the supported range.	0x0: Normal operation 0x1: RGRADE Over Range, or an open is detected.
RADDR_UNDER_RANGE	1	Indicates that the RADDR resistor value is below the supported range.	0x0: Normal operation 0x1: RADDR Under Range, or a short detected.

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BITFIELD	BITS	DESCRIPTION	DECODE
RGRADE_UNDER_RANGE	0	Indicates that the RGRADE resistor value is below the supported range.	0x0: Normal operation 0x1: RGRADE under range, or a short detetcted.

STAT_RES_CODE (0x0F)

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	DEV_ID[3:0]				RGRADE[3:0]			
Reset								
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION
DEV_ID	7:4	Decoded value of the RADDR external resistor. This value is used to set the UART Device ID.
RGRADE	3:0	Decoded value of the external RGRADE resistor.

STAT_GEN (0x10)

STAT_GEN is a read/write register that provides general operations and warnings. $\overline{FLT}$ pin is asserted whenever any of these bits is high, unless the corresponding MASK bit is set.

BIT				12	11	10	9	8
Field				–	–	OTP_CRC_ERR	CONFIG_NOT_DONE	RADC_ERR
Reset				–	–	0b0	0b0	0b0
Access Type				–	–	Read Only	Read Only	Read Only
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	EXT_CLK_ERR	UART_ERR	OPEN_TRACE	OPEN_LED	SHORT_LED	CP_RDY_N	TH_SHDN	TH_WARN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Write 1 to Clear, Read	Write 1 to Clear, Read

BITFIELD	BITS	DESCRIPTION	DECODE
OTP_CRC_ERR	10	OTP CRC Error Bit. Indicates that a CRC error has been detected when reading back the internal OTP memory. Status bit only, does not assert $\overline{FLT}$ pin.	

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BITFIELD	BITS	DESCRIPTION	DECODE
CONFIG_NOT_DONE	9	This bit indicates that the UART interface has not completed programming the LED switch configuration, triggered by writing CNFG_GEN. The controller should ensure this bit is low before attempting to program CNFG_GEN. This bit does not assert the $\overline{FLT}$ pin.	0x0: Configuration complete; ready for new CNFG_GEN command. 0x1: Configuration not complete.
RADC_ERR	8	This signal indicates that the RGRADE read operation is not complete. When the signal goes low, the read is complete and RGRADE[3:0] in register 0x0F is valid. This signal asserts the $\overline{FLT}$ pin.	0x0: RADC completes. 0x1: RADC error.
EXT_CLK_ERR	7	EXT_CLK_ERR is asserted when the part is configured to use the CLKIN pin as the reference clock (PWM_CLK_SEL = x2 or x3) and the external clock is slower than the minimum operating frequency.	0x0: CLKIN operating in spec. 0x1: External Clock Error.
UART_ERR	6	UART_ERR is asserted if any of the error bits in CNFG_UART are set.	0x0: UART is operating normally. 0x1: At least one of UART errors has been asserted.
OPEN_TRACE	5	OPEN_TRACE is asserted if any OPEN_TRACE_STAT bit is high.	0x0: All LED drivers operating normally. 0x1: At least one LED driver has open-trace detected.
OPEN_LED	4	OPEN_LED is asserted if any OPEN_LED_STAT bit is high.	0x0: All LED drivers operating normally. 0x1: At least one LED driver has open detected.
SHORT_LED	3	SHORT_LED is asserted if any SHORT_LED_STAT bit is high.	0x0: All LED drivers operating normally. 0x1: At least one LED driver has short detected.
CP_RDY_N	2	CP_RDY_N is a read-only bit that indicates that the charge-pump voltage is below the operating threshold.	0x0: CP operating normally. 0x1: CP is below V_{CPP_OK} threshold.
TH_SHDN	1	Thermal Shutdown. Latched, write 1 to clear.	
TH_WARN	0	Thermal Warning. Latched, write 1 to clear.	0x0: Normal operation. 0x1: Device has exceeded the thermal-warning threshold.

STAT_UART (0x11)

BIT				12	11	10	9	8
Field				–	–	–	–	UART_WATCHDOG
Reset				–	–	–	–	0b0
Access Type				–	–	–	–	Write 1 to Clear, Read
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	RX_TIMEOUT_ERR	RX_CRC_ERR	RX_SYNC_PERR	RX_PL_PERR	RX_SYNC_STOP_ERR	RX_PL_STOP_ERR	RX_PL_START_ERR	–
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	–
Access Type	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	–

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BITFIELD	BITS	DESCRIPTION	DECODE
UART_WATCHDOG	8	The UART Watchdog Timer will assert whenever there has been no activity on the UART_RX pin for the time duration set by the CNFG_WATCHDGOG field in the CNFG_UART register.	
RX_TIMEOUT_ERR	7	This bit shall be asserted if there are no UART_RX transitions for more than 16 bit lengths between the frames and the switches will go to the state set by the CNFG_WATCHDOG register.	0x0: Normal operation. 0x1: UART Rx times out.
RX_CRC_ERR	6	CRC Error Indicator	0x0: Normal operation. 0x1: CRC Error: At least one UART transaction rejected due to a failed CRC check.
RX_SYNC_PERR	5	Parity Error in Rx Sync Frame detected	0x0: Normal operation. 0x1: Rx Sync Frame parity error detected.
RX_PL_PERR	4	Parity Error detected on Rx Payload data	0x0: Normal operation. 0x1: UART Rx payload parity error detected.
RX_SYNC_STOP_ERR	3	Rx Sync Frame Stop Bit Error detected	0x0: Normal operation. 0x1: Rx Sync Frame STOP bit error detected
RX_PL_STOP_ERR	2	UART Stop Bit Error detected in Rx Data Frames	0x0: Normal operation. 0x1: Rx Payload Frame STOP bit error.
RX_PL_START_ERR	1	UART Start Bit Error on Rx Data Frame	0x0: Normal operation. 0x1: Rx Payload Frame START bit error.

STAT_SHORT_LED (0x12)

STAT_SHORT_LED is a read/write register that provides short-detect information on the 12 LED output drivers.

BIT		12	11	10	9	8
Field		–	SHORT_LED_STAT[11:8]			
Reset		–	0x000			
Access Type		–	Write 1 to Clear, Read			

BIT	7	6	5	4	3	2	1	0
Field	SHORT_LED_STAT[7:0]							
Reset	0x000							
Access Type	Write 1 to Clear, Read							

BITFIELD	BITS	DESCRIPTION
SHORT_LED_STAT	11:0	Indicates that a LED short has been detected.

STAT_OPEN_LED (0x13)

STAT_OPEN is a read/write register that provides open-detect information on the 12 LED output drivers.

BIT		12	11	10	9	8
Field		–	OPEN_LED_STAT[11:8]			
Reset		–	0x000			
Access Type		–	Write 1 to Clear, Read			

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BIT	7	6	5	4	3	2	1	0
Field	OPEN_LED_STAT[7:0]							
Reset	0x000							
Access Type	Write 1 to Clear, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
OPEN_LED_STAT	11:0	Indicates that an open-LED condition has been detected.	0x0: Normal 0x1: Open LED

STAT_OPEN_TRACE (0x14)

STAT_OPEN_TRACE is a read-only register that provides open-trace fault information on the 12 LED output drivers.

BIT				12	11	10	9	8
Field				–	OPEN_TRACE_STAT[11:8]			
Reset				–	0x000			
Access Type				–	Write 1 to Clear, Read			
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	OPEN_TRACE_STAT[7:0]							
Reset	0x000							
Access Type	Write 1 to Clear, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
OPEN_TRACE_STAT	11:0	Indicates an open trace has been detected.	0x0: Normal 0x1: Open trace

RTEMP (0x15)

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	RTEMP[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
RTEMP	7:0	Raw 8-bit ADC value representing the ratio of the voltage at the RTEMP pin relative to the voltage at the V_{DD} pin. This value can be used in conjunction with an external NTC resistor network to provide remote temperature sensing functionality.

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LOW_DUTY_TH (0x16)

BIT				12	11	10	9	8
Field				–	LOW_DUTY_TH[11:8]			
Reset				–	0x10			
Access Type				–	Write, Read			
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	LOW_DUTY_TH[7:0]							
Reset	0x10							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
LOW_DUTY_TH	11:0	The Low Duty Threshold is used to filter out LED fault signals during short duty cycles when the voltage across the switch might not settle to a final value, causing invalid detection of the Short LED condition. When the DUTY register of a switch is less than LOW_DUTY_TH, the SHORT_LED signal is masked and SHORT_LED_STAT is not asserted for that switch. If using slew rate control, the LED short detection will only happen after the part is finished slewing.

PSFT_GRP (0x20)

PSFT_GRP is a read/write register that allows the user to assign the same phase shift to one or more LED drivers. The contents of PSFT are written to the desired group specified by PSFT_GROUP.

Example:

If PSFT_GROUP == Group A, PSFT == 0001, and LED11, LED9, and LED6 are assigned to Group A (through CNFG_GRPA), then PSFT_11, PSFT_9, and PSFT_6 contain 0001 after the transaction is executed.

BIT				12	11	10	9	8
Field				–	–	–	PSFT_GROUP[1:0]	
Reset				–	–	–	0x1	
Access Type				–	–	–	Write, Read	
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	PSFT[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_GROUP	9:8	Group Select: Bit 8: Group A selected Bit 9: Group B selected Multiple groups can be selected at a time. **Note:** 00 is not a valid selection, the transaction is not executed and the 4-bit value is unchanged.
PSFT	7:0	Phase Select.

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PSFT_1 (0x21)

PSFT_1 is a read/write register that controls the phase shift for LED1.

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	PSFT_1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_1	7:0	LED1 Phase Select.

PSFT_2 (0x22)

PSFT_2 is a read/write register that controls the phase shift for LED2.

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	PSFT_2[7:0]							
Reset	0x15							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_2	7:0	LED2 Phase Select.

PSFT_3 (0x23)

PSFT_3 is a read/write register that controls the phase shift for LED3.

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	PSFT_3[7:0]							
Reset	0x2A							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION
PSFT_3	7:0	LED3 Phase Select.

PSFT_4 (0x24)

PSFT_4 is a read/write register that controls the phase shift for LED4.

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	PSFT_4[7:0]							
Reset	0x40							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_4	7:0	LED4 Phase Select.

PSFT_5 (0x25)

PSFT_5 is a read/write register that controls the phase shift for LED5.

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	PSFT_5[7:0]							
Reset	0x55							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_5	7:0	LED5 Phase Select.

PSFT_6 (0x26)

PSFT_6 is a read/write register that controls the phase shift for LED6.

BIT		12	11	10	9	8
Field		–	–	–	–	–
Reset		–	–	–	–	–
Access Type		–	–	–	–	–

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BIT	7	6	5	4	3	2	1	0
Field	PSFT_6[7:0]							
Reset	0x6A							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_6	7:0	LED6 Phase Select.

PSFT_7 (0x27)

PSFT_7 is a read/write register that controls the phase shift for LED7.

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	PSFT_7[7:0]							
Reset	0x80							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_7	7:0	LED7 Phase Select.

PSFT_8 (0x28)

PSFT_8 is a read/write register that controls the phase shift for LED8.

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	PSFT_8[7:0]							
Reset	0x95							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_8	7:0	LED8 Phase Select.

PSFT_9 (0x29)

PSFT_9 is a read/write register that controls the phase shift for LED9.

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BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	PSFT_9[7:0]							
Reset	0xAA							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_9	7:0	LED9 Phase Select.

PSFT_10 (0x2A)

PSFT_10 is a read/write register that controls the phase shift for LED10.

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	PSFT_10[7:0]							
Reset	0xC0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_10	7:0	LED10 Phase Select.

PSFT_11 (0x2B)

PSFT_11 is a read/write register that controls the phase shift for LED11.

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	PSFT_11[7:0]							
Reset	0xD5							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_11	7:0	LED11 Phase Select.

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PSFT_12 (0x2C)

PSFT_12 is a read/write register that controls the phase shift for LED12.

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	PSFT_12[7:0]							
Reset	0xEA							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_12	7:0	LED12 Phase Select.

TDIM_GRP (0x30)

TDIM_GRP is a read/write register that allows the user to assign the same dimming period to one or more LED drivers. The contents of TDIM are written to the desired group specified by TDIM_GROUP.

Example:

If TDIM_GROUP == Group A, PSFT == 001, and LED12, LED9, and LED6 are assigned to Group A (through CNFG_GRPA), then TDIM_12, TDIM_9, and TDIM_6 contain 001 after the transaction is executed.

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	–	–	TDIM_GROUP[1:0]		–	TDIM[2:0]		
Reset	–	–	0x1		–	0b000		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TDIM_GROUP	5:4	Group Select: Bit 4: Group A selected Bit 5: Group B selected Multiple groups can be selected at a time. **Note:** 0000 is not a valid selection, the transaction is not executed and the 4-bit value is unchanged.	

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BITFIELD	BITS	DESCRIPTION	DECODE
TDIM	2:0	Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period 0x1: Update PWM duty cycle every 2 PWM periods 0x2: Update PWM duty cycle every 4 PWM periods 0x3: Update PWM duty cycle every 8 PWM periods 0x4: Update PWM duty cycle every 16 PWM periods 0x5: Update PWM duty cycle every 32 PWM periods 0x6: Update PWM duty cycle every 32 PWM periods 0x7: Update PWM duty cycle every 32 PWM periods 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)

TDIM_3_2_1 (0x31)

TDIM_3_2_1 is a read/write register that controls the dimming period for LED drivers 3, 2, and 1.

BIT				12	11	10	9	8
Field				–	–	TDIM_3[2:0]		
Reset				–	–	0b000		
Access Type				–	–	Write, Read		
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	–	TDIM_2[2:0]			–	TDIM_1[2:0]		
Reset	–	0b000			–	0b000		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TDIM_3	10:8	LED3 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)

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BITFIELD	BITS	DESCRIPTION	DECODE
TDIM_2	6:4	LED2 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)
TDIM_1	2:0	LED1 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)

TDIM_6_5_4 (0x32)

TDIM_6_5_4 is a read/write register that controls the dimming period for LED drivers 6, 5, and 4.

BIT				12	11	10	9	8
Field				–	–	TDIM_6[2:0]		
Reset				–	–	0b000		
Access Type				–	–	Write, Read		
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	–	TDIM_5[2:0]			–	TDIM_4[2:0]		
Reset	–	0b000			–	0b000		
Access Type	–	Write, Read			–	Write, Read		

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BITFIELD	BITS	DESCRIPTION	DECODE
TDIM_6	10:8	LED6 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)
TDIM_5	6:4	LED5 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)
TDIM_4	2:0	LED4 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)

TDIM_9_8_7 (0x33)

TDIM_9_8_7 is a read/write register that controls the dimming period for LED drivers 9, 8, and 7.

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BIT				12	11	10	9	8
Field				–	–	TDIM_9[2:0]		
Reset				–	–	0b000		
Access Type				–	–	Write, Read		

BIT	7	6	5	4	3	2	1	0
Field	–	TDIM_8[2:0]			–	TDIM_7[2:0]		
Reset	–	0b000			–	0b000		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TDIM_9	10:8	LED9 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)
TDIM_8	6:4	LED8 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)

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BITFIELD	BITS	DESCRIPTION	DECODE
TDIM_7	2:0	LED7 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)

TDIM_12_11_10 (0x34)

TDIM_12_11_10 is a read/write register that controls the dimming period for LED drivers 12, 11, and 10.

BIT				12	11	10	9	8
Field				–	–	TDIM_12[2:0]		
Reset				–	–	0b000		
Access Type				–	–	Write, Read		
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	–	TDIM_11[2:0]			–	TDIM_10[2:0]		
Reset	–	0b000			–	0b000		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TDIM_12	10:8	LED12 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)

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BITFIELD	BITS	DESCRIPTION	DECODE
TDIM_11	6:4	LED11 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)
TDIM_10	2:0	LED10 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)

PWM_GRPA_DUTY (0x40)

PWM_GRPA_DUTY is a read/write register that allows the user to assign the same duty cycle and enable/disable PWM dimming to one or more LED drivers.

The contents of DUTY_A are written to LEDs assigned to Group A.

Example:

If DUTY_A == 0x0AA and LED11, LED8, and LED5 are assigned to Group A (through CNFG_GRPA), then DUTY_11, DUTY_8, and DUTY_5 contain 0x0AA after the transaction is executed.

BIT		12	11	10	9	8
Field		FADE_A	DUTY_A[11:8]			
Reset		0b0	0x000			
Access Type		Write, Read	Write, Read			

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BIT	7	6	5	4	3	2	1	0
Field	DUTY_A[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FADE_A	12	Group A PWM Dimming Enable	0x0: Disabled 0x1: Enabled
DUTY_A	11:0	Group A Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xfff = 100% duty cycle	

PWM_GRPB_DUTY (0x41)

PWM_GRPB_DUTY is a read/write register that allows the user to assign the same duty cycle and enable/disable PWM dimming to one or more LED drivers.

The contents of DUTY_B are written to LEDs assigned to Group B.

Example:

If DUTY_B == 0x0AA and LED11, LED9, and LED6 are assigned to Group B (through CNFG_GRPB), then DUTY_11, DUTY_9, and DUTY_6 contain 0x0AA after the transaction is executed.

BIT				12	11	10	9	8
Field				FADE_B	DUTY_B[11:8]			
Reset				0b0	0x000			
Access Type				Write, Read	Write, Read			
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	DUTY_B[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FADE_B	12	Group B PWM Dimming Enable	0x0: Enabled 0x1: Disabled
DUTY_B	11:0	Group B Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xfff = 100% duty cycle	

PWM1 (0x42)

PWM1 is a read/write register that configures the LED1 duty cycle and enables/disables PWM dimming.

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BIT				12	11	10	9	8
Field				FADE_1	DUTY_1[11:8]			
Reset				0b0	0x000			
Access Type				Write, Read	Write, Read			
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	DUTY_1[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FADE_1	12	LED1 PWM Dimming Enable	0x0: Enabled 0x1: Disabled
DUTY_1	11:0	LED1 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xfff = 100% duty cycle	

PWM2 (0x43)

PWM2 is a read/write register that configures the LED2 duty cycle and enables/disables PWM dimming.

BIT				12	11	10	9	8
Field				FADE_2	DUTY_2[11:8]			
Reset				0b0	0x000			
Access Type				Write, Read	Write, Read			
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	DUTY_2[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FADE_2	12	LED2 PWM Dimming Enable	0x0: Enabled 0x1: Disabled
DUTY_2	11:0	LED2 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xfff = 100% duty cycle	

PWM3 (0x44)

PWM3 is a read/write register that configures the LED3 duty cycle and enables/disables PWM dimming.

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BIT				12	11	10	9	8
Field				FADE_3	DUTY_3[11:8]			
Reset				0b0	0x000			
Access Type				Write, Read	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	DUTY_3[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FADE_3	12	LED3 PWM Dimming Enable	0x0: Enabled 0x1: Disabled
DUTY_3	11:0	LED3 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xfff = 100% duty cycle	

PWM4 (0x45)

PWM4 is a read/write register that configures the LED4 duty cycle and enables/disables PWM dimming.

BIT				12	11	10	9	8
Field				FADE_4	DUTY_4[11:8]			
Reset				0b0	0x000			
Access Type				Write, Read	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	DUTY_4[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FADE_4	12	LED4 PWM Dimming Enable	0x0: Enabled 0x1: Disabled
DUTY_4	11:0	LED4 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xfff = 100% duty cycle	

PWM5 (0x46)

PWM5 is a read/write register that configures the LED5 duty cycle and enables/disables PWM dimming.

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BIT				12	11	10	9	8
Field				FADE_5	DUTY_5[11:8]			
Reset				0b0	0x000			
Access Type				Write, Read	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	DUTY_5[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FADE_5	12	LED5 PWM Dimming Enable	0x0: Enabled 0x1: Disabled
DUTY_5	11:0	LED5 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xfff = 100% duty cycle	

PWM6 (0x47)

PWM6 is a read/write register that configures the LED6 duty cycle and enables/disables PWM dimming.

BIT				12	11	10	9	8
Field				FADE_6	DUTY_6[11:8]			
Reset				0b0	0x000			
Access Type				Write, Read	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	DUTY_6[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FADE_6	12	LED6 PWM Dimming Enable	0x0: Enabled 0x1: Disabled
DUTY_6	11:0	LED6 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xfff = 100% duty cycle	

PWM7 (0x48)

PWM7 is a read/write register that configures the LED7 duty cycle and enables/disables PWM dimming.

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BIT				12	11	10	9	8
Field				FADE_7	DUTY_7[11:8]			
Reset				0b0	0x000			
Access Type				Write, Read	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	DUTY_7[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FADE_7	12	LED7 PWM Dimming Enable	0x0: Enabled 0x1: Disabled
DUTY_7	11:0	LED7 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xfff = 100% duty cycle	

PWM8 (0x49)

PWM8 is a read/write register that configures the LED8 duty cycle and enables/disables PWM dimming.

BIT				12	11	10	9	8
Field				FADE_8	DUTY_8[11:8]			
Reset				0b0	0x000			
Access Type				Write, Read	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	DUTY_8[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FADE_8	12	LED8 PWM Dimming Enable	0x0: Enabled 0x1: Disabled
DUTY_8	11:0	LED8 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xfff = 100% duty cycle	

PWM9 (0x4A)

PWM9 is a read/write register that configures the LED9 duty cycle and enables/disables PWM dimming.

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BIT				12	11	10	9	8
Field				FADE_9	DUTY_9[11:8]			
Reset				0b0	0x000			
Access Type				Write, Read	Write, Read			
BIT	7	6	5	4	3	2	1	0
Field	DUTY_9[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FADE_9	12	LED9 PWM Dimming Enable	0x0: Enabled 0x1: Disabled
DUTY_9	11:0	LED9 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xfff = 100% duty cycle	

PWM10 (0x4B)

PWM10 is a read/write register that configures the LED10 duty cycle and enables/disables PWM dimming.

BIT				12	11	10	9	8
Field				FADE_10	DUTY_10[11:8]			
Reset				0b0	0x000			
Access Type				Write, Read	Write, Read			
BIT	7	6	5	4	3	2	1	0
Field	DUTY_10[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FADE_10	12	LED10 PWM Dimming Enable	0x0: Enabled 0x1: Disabled
DUTY_10	11:0	LED10 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xfff = 100% duty cycle	

PWM11 (0x4C)

PWM11 is a read/write register that configures the LED11 duty cycle and enables/disables PWM dimming.

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BIT				12	11	10	9	8
Field				FADE_11	DUTY_11[11:8]			
Reset				0b0	0x000			
Access Type				Write, Read	Write, Read			
BIT	7	6	5	4	3	2	1	0
Field	DUTY_11[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FADE_11	12	LED11 PWM Dimming Enable	0x0: Enabled 0x1: Disabled
DUTY_11	11:0	LED11 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xfff = 100% duty cycle	

PWM12 (0x4D)

PWM12 is a read/write register that configures the LED12 duty cycle and enables/disables PWM dimming.

BIT				12	11	10	9	8
Field				FADE_12	DUTY_12[11:8]			
Reset				0b0	0x000			
Access Type				Write, Read	Write, Read			
BIT	7	6	5	4	3	2	1	0
Field	DUTY_12[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FADE_12	12	LED12 PWM Dimming Enable	0x0: Enabled 0x1: Disabled
DUTY_12	11:0	LED12 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xfff = 100% duty cycle	

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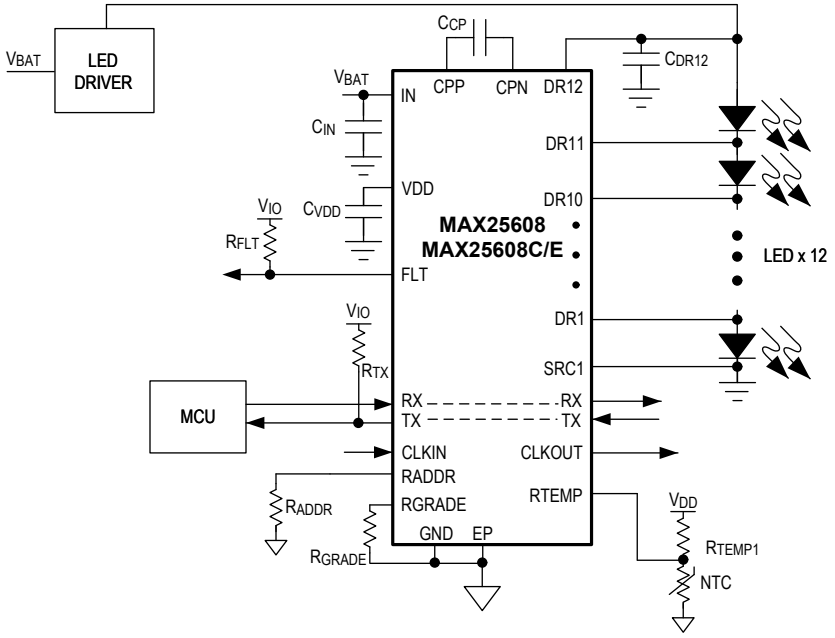
Typical Application Circuits

MAX25608/MAX25608C/MAX25608E



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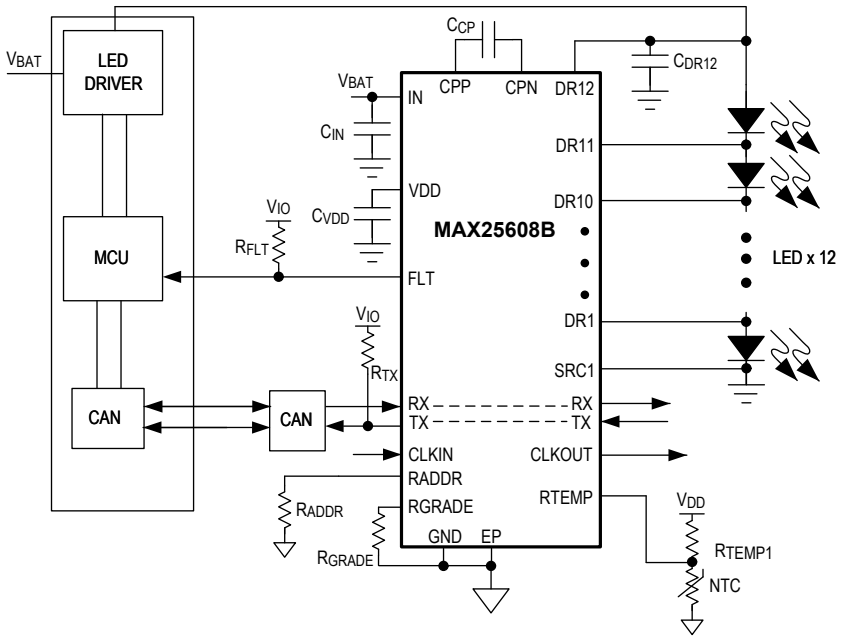
Typical Application Circuits (continued)

MAX25608B



Ordering Information

PART NUMBER	TEMP RANGE	UART COMMUNICATION	SPREAD SPECTRUM	OPEN TRACE	PIN-PACKAGE
MAX25608AUI/V+	-40°C to +125°C	Full duplex	Enabled	Disabled	28 TSSOP-EP*
MAX25608BAUI/V+	-40°C to +125°C	Half duplex	Disabled	Disabled	28 TSSOP-EP*
MAX25608CAUI/V+	-40°C to +125°C	Full duplex	Disabled	Disabled	28 TSSOP-EP*
MAX25608EAUI/V+	-40°C to +125°C	Full duplex	Disabled	Enabled	28 TSSOP-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

/V Denotes an automotive-qualified part.

**EP = Exposed pad.*

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/21	Release for Market Intro	—
1	8/22	Added MAX25608B/MAX25608C in text and diagrams	1, 8–15, 17, 19–26, 30–32, 36, 38-43, 49, 63, 64
2	9/22	Updated Ordering Information table	64
3	10/22	Updated Electrical Characteristics table, Pin Descriptions, and Detailed Description	8, 10, 14, 19, 21, 24
4	3/23	Updated Detailed Description and Typical Application Circuits	16-26, 28, 65–66
5	5/23	Updated Detailed Description and Register Map	14, 16, 23, 34–38, 42
6	11/23	Updated Electrical Characteristics table, Detailed Description, and Register Map	7, 19, 33
7	7/24	Added MAX25608E in General Description, Benefit and Features, Electrical Characteristics, Pin Configurations, Functional Diagram, Detailed Description, Register Map, Typical Applications Circuits, and Ordering Information table	1, 8, 9, 13, 14, 19–30, 40, 42, 43, 45, 65, 66

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