Datasheet

4ch White LED Driver Built-in Current Driver Buck-Boost and Boost DC/DC Converter for Automotive

BD81A44EFV-M BD81A44MUV-M

General Description

BD81A44EFV-M / BD81A44MUV-M is a white LED driver with the capability of withstanding high input voltage (maximum 35 V). This driver has 4ch constant-current drivers in 1-chip, where each channel can draw up to 120 mA (Max), and it is suitable for high illumination LED drive. Furthermore, a buck-boost current mode DC/DC converter is also built to achieve stable operation during power voltage fluctuation. Light modulation (10,000:1@100 Hz dimming function) is possible by PWM input.

Features

- AEC-Q100 Qualified*1
- 4ch Current Driver for LED Drive
- Buck-Boost Current Mode DC/DC Converter
- Control DC/DC Converter Oscillation Frequency by External Synchronized Signal
- LSI Protection Function (UVLO, OVP, TSD, OCP, SCP)
- LED Abnormality Detection Function (Open/Short)
- VOUT Discharge Function (Buck-Boost Structure Limitation)

*1 Grade 1

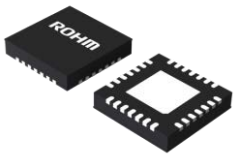
Applications

- Automotive CID (Center Information Display) Panel
- Car Navigation
- Cluster Panel
- HUD (Head Up Display)
- Small and Medium Type LCD Panels for Automotive Use

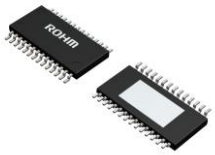
Key Specifications

- Operating Input Voltage Range: 4.5 V to 35 V
- Output LED Current Accuracy: ±3.0 %@50 mA
- DC/DC Oscillation Frequency: 200 kHz to 2200 kHz
- Operating Temperature: -40 °C to +125 °C
- LED Maximum Output Current: 120 mA/ch
- LED Maximum Dimming Ratio: 10,000:1@100 Hz
- PWM Minimum Pulse Width: 1.0 µs

Packages	W (Typ) x D (Typ) x H (Max)
VQFN28SV5050	5.0 mm x 5.0 mm x 1.0 mm
HTSSOP-B28	9.7 mm x 6.4 mm x 1.0 mm

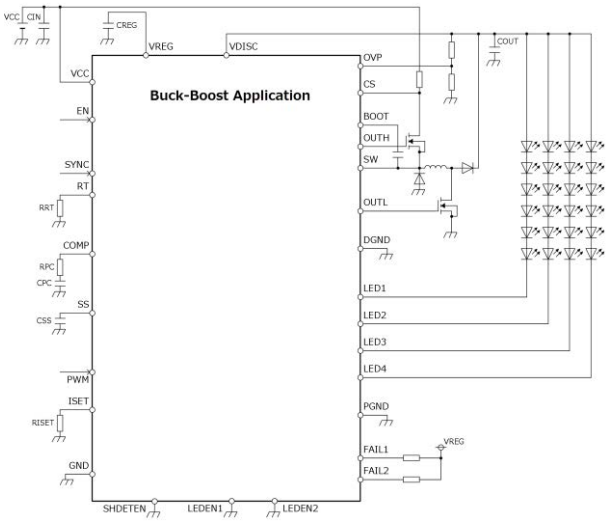


VQFN28SV5050
BD81A44MUV-M



HTSSOP-B28
BD81A44EFV-M

Typical Application Circuit



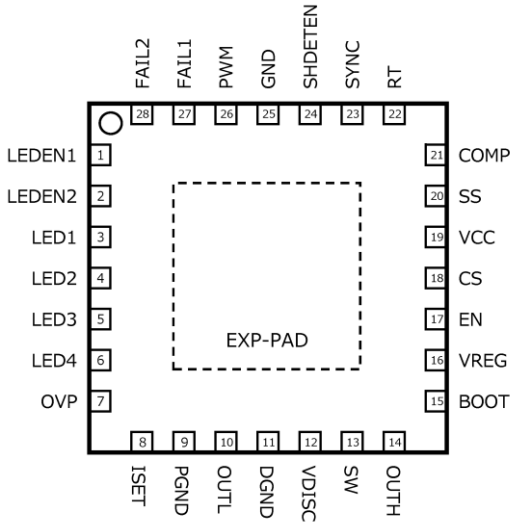
○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays
○This product is protected by U.S. Patent No.7,235,954, No.7,541,785, No.7,944,189.

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Pin Configuration

VQFN28SV5050 (TOP VIEW)



Pin Description

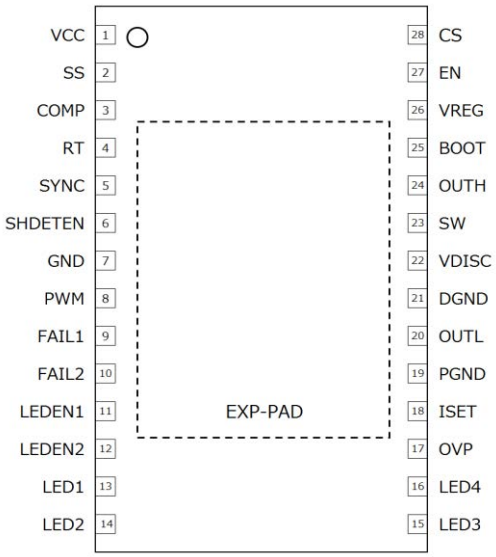
Pin No.	Pin Name	Function
1	LEDEN1	Enable pin 1 for LED output
2	LEDEN2	Enable pin 2 for LED output
3	LED1	LED output pin 1
4	LED2	LED output pin 2
5	LED3	LED output pin 3
6	LED4	LED output pin 4
7	OVP	Over voltage detection pin
8	ISET	LED output current setting pin
9	PGND	LED output GND pin
10	OUTL	Low side FET gate pin
11	DGND	DC/DC converter output GND pin
12	VDISC	Output voltage discharge pin
13	SW	High side FET source pin
14	OUTH	High side FET gate pin
15	BOOT	High side FET driver power supply pin
16	VREG	Internal constant voltage
17	EN	Enable pin
18	CS	DC/DC converter current sense pin
19	VCC	Input power supply pin
20	SS	“Soft Start” capacitor connection
21	COMP	Error Amp output
22	RT	Oscillation frequency setting resistor connect
23	SYNC	External synchronization input pin
24	SHDETEN	Short detection enable signal
25	GND	Small signal GND pin
26	PWM	PWM light modulation signal input pin
27	FAIL1	“Failure” signal output pin 1
28	FAIL2	“Failure” signal output pin 2
-	EXP-PAD	Back side thermal PAD (Connect to GND)

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Pin Configuration

HTSSOP-B28 (TOP VIEW)



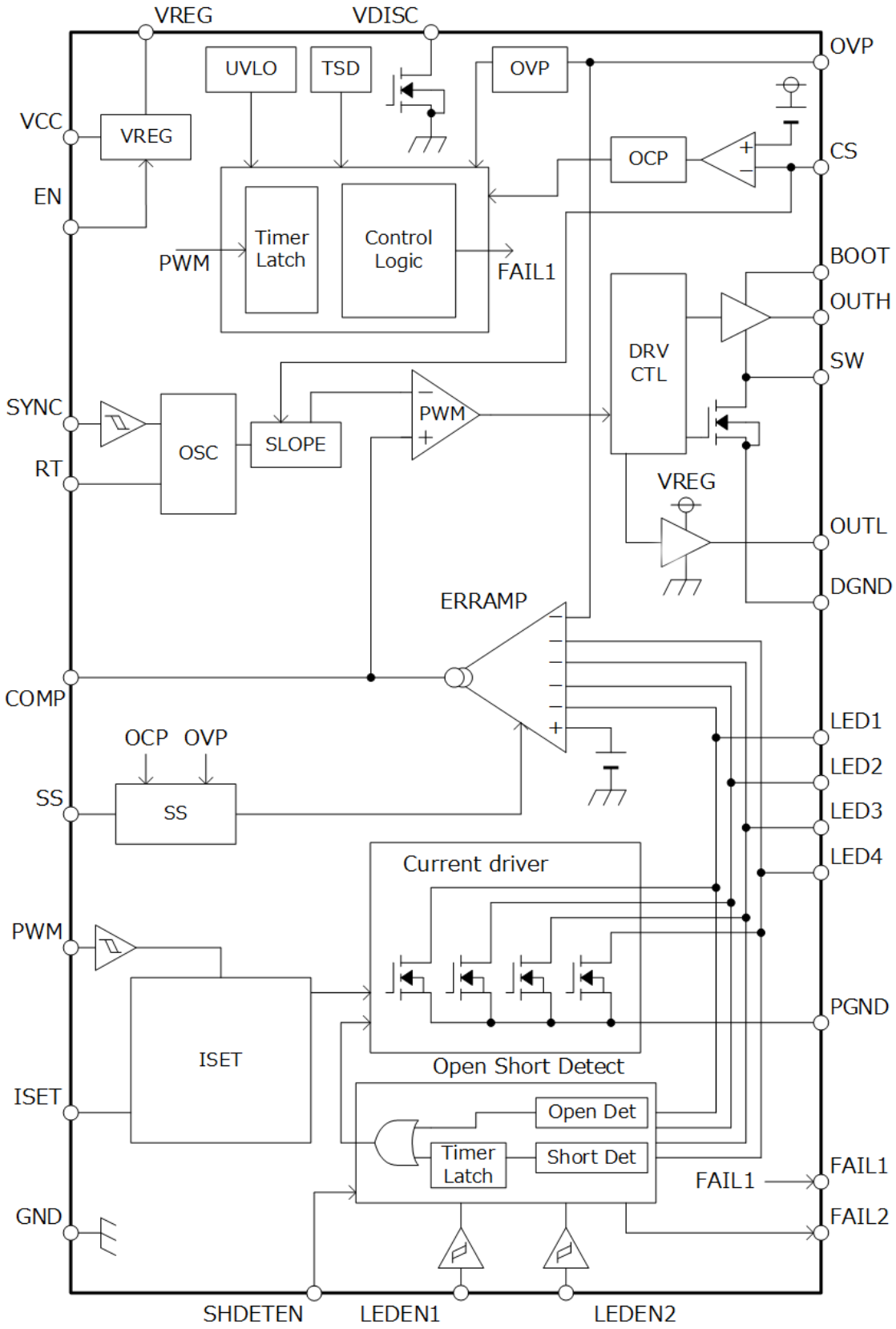
Pin Description

Pin No.	Pin Name	Function
1	VCC	Input power supply pin
2	SS	“Soft Start” capacitor connection
3	COMP	Error Amp output
4	RT	Oscillation frequency setting resistor connect
5	SYNC	External synchronization input pin
6	SHDETEN	Short detection enable signal
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8	PWM	PWM light modulation signal input pin
9	FAIL1	“Failure” signal output pin 1
10	FAIL2	“Failure” signal output pin 2
11	LEDEN1	Enable pin 1 for LED output
12	LEDEN2	Enable pin 2 for LED output
13	LED1	LED output pin 1
14	LED2	LED output pin 2
15	LED3	LED output pin 3
16	LED4	LED output pin 4
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Block Diagram



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Description of Blocks

If there is no description, the mentioned values are typical value.

1. Reference Voltage (VREG)

VREG Block generates 5 V at EN = High, and outputs to the VREG pin. This voltage (V_{VREG}) is used as power supply for internal circuit. It is also used to fix each input pin to High voltage outside IC. It cannot supply power to other parts than this IC. The VREG pin has UVLO function, and it starts operation at VCC ≥ 4.0 V and V_{VREG} ≥ 3.5 V and stops when at VCC ≤ 3.5 V or V_{VREG} ≤ 2.0 V. About the condition to release/detect VREG voltage, refer to Table 2 on section 4 4. Protection Feature. Connect a ceramic capacitor (C_{VREG}) to the VREG pin for phase margin. C_{VREG} range is 1.0 µF to 4.7 µF and recommended value is 2.2 µF. If the C_{VREG} is not connected, it might occur unstable operation e.g. oscillation.

2. Current Driver

Table 1. LED Control Logic

LEDEN1	LEDEN2	LED1	LED2	LED3	LED4
Low	Low	ON	ON	ON	ON
High	Low	ON	ON	ON	OFF
Low	High	ON	ON	OFF	OFF
High	High	ON	OFF	OFF	OFF

If there is the constant-current driver output not to use, make the LED1 to LED4 pins 'open' and turn off the channel, which is not used, with the LEDEN1 and LEDEN2 pins. The truth table for these pins is shown above. If the unused constant-current driver output is set open without the process of the LEDEN1 and LEDEN2 pins, the 'open detection' is activated. The LEDEN1 and LEDEN2 pins are pulled down internally in the IC and it is low at 'open' condition. They can be connected to the VREG pin and fixed to logic High. Logic of the LEDEN1 and LEDEN2 pins are not switchable during these in operation.

(1) Output Current Setting (R_{ISET})

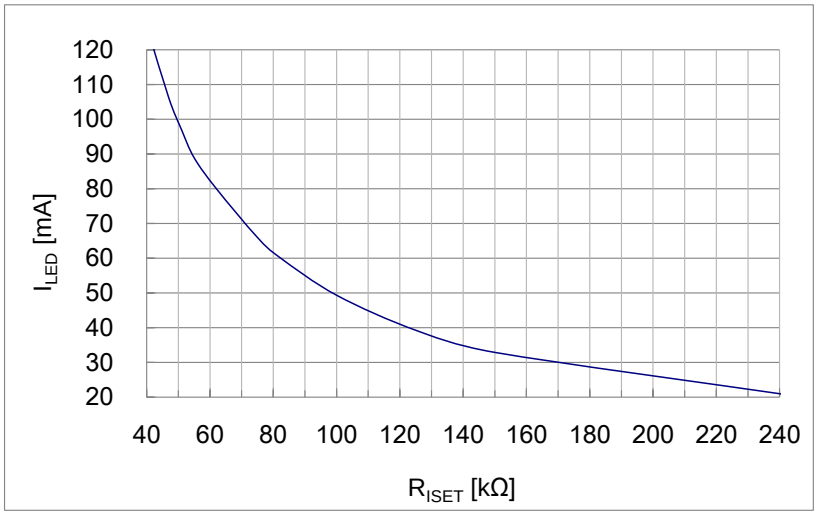


Figure 1. I_{LED} vs R_{ISET}

The Output Current I_{LED} can be obtained by the following equation:

$$I_{LED} = 5000/R_{ISET} \quad [A]$$

The operating range of the R_{ISET} value is from 41 kΩ to 250 kΩ. Additionally, the R_{ISET} value could not be changed during operation. In this IC, ISET-GND short protection is built-in to protect an LED element from excess current when the ISET pin and GND are shorted. If the R_{ISET} value is 4.7 kΩ or less, the IC detects ISET-GND short condition and LED current is turned off.

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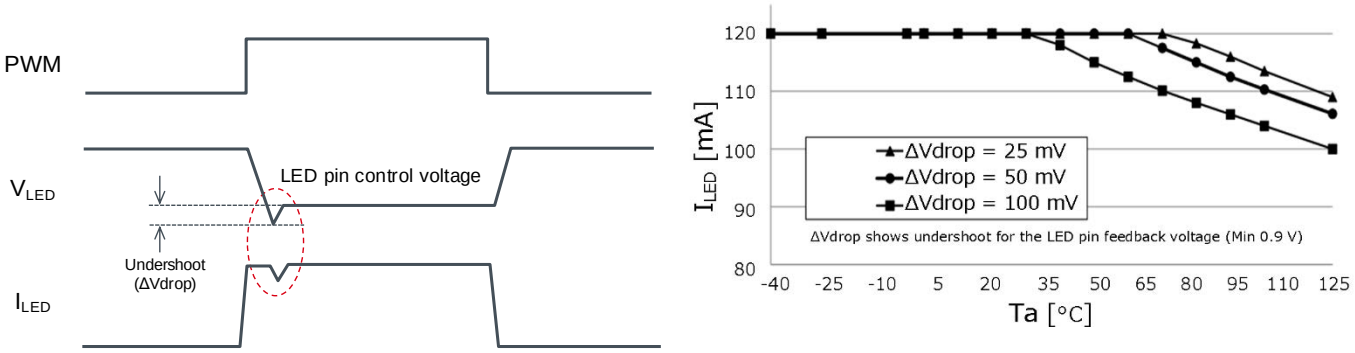
2. Current Driver – continued

<Caution of Large LED Current Setting>

During PWM dimming, the LED pin voltage (V_{LED}) rises when PWM = Low because LED current doesn't flow, and controls V_{LED} to 1 V when PWM = High. When PWM rise up, V_{LED} undershoot may occur depends on LED current setting or external parts including the output capacitor. The undershoot is large especially at high temperature and large LED current.

LED current may decrease instantly as Figure 2(a) shows by the undershoot. The undershoot and the settable LED current are shown in Figure 2(b).

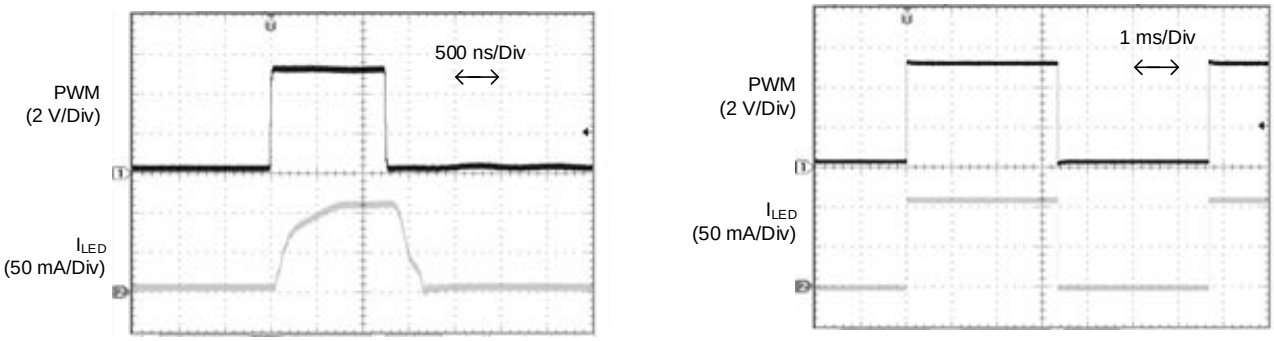
If the LED current is decreased with the undershoot, it may not see as the LED flicker. Evaluate with the actual application certainly, and check at the visual perspective.



(a) Timing Chart of V_{LED}, I_{LED} at PWM Dimming (b) Temperature (Ta) vs LED Current (I_{LED})

Figure 2. Relation Between Undershoot of V_{LED} and LED Current

(2) PWM Dimming Control



(a) PWM = 150 Hz, Duty = 0.02 %, I_{LED} Waveform (b) PWM = 150 Hz, Duty = 50.0 %, I_{LED} Waveform

Figure 3. PWM Dimming Waveform

The current driver ON/OFF is controlled by the PWM pin. The duty ratio of the PWM pin becomes duty ratio of I_{LED}. If PWM dimming is not totally used (i.e. 100 %), fix the PWM pin to High. Output light intensity is the highest at 100 %.

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Description of Blocks – continued

3. Buck-Boost DC/DC Converter

(1) Number of LED in Series Connection

This IC controls output voltage to become 1.0 V by detecting LED cathode voltage (the LED1 to LED4 pins voltage). When multiple LED outputs are operating, it controls LED pin voltage with the highest LED Vf to become 1.0 V. Thus, the output voltage of other LED pins is higher by the variations of Vf. Set up Vf variation to meet the formula below.

$$LED\ Series\ Number\ \times\ Vf\ Variation < Short\ Detection\ Voltage\ (Min) - LED\ Control\ Voltage(Max)$$

(2) Over Voltage Protection (OVP)

The output voltage (VOUT) should be connected to the OVP pin via resistor voltage divider. If the OVP pin voltage is 2.0 V or more, Over Voltage Protection (OVP) is active and stop the DC/DC converter switching. Determine the setting value of OVP function by the total number of the LEDs in the series and the Vf variation. When the OVP pin voltage drops less than 1.94 V after OVP operation, the OVP is released.

$$VOUT\ \geq\ \{(R_{OVP1} + R_{OVP2})\ /\ R_{OVP1}\} \times 2.0$$

where:

$VOUT$ is the Output voltage.

R_{OVP1} is the GND side OVP resistance.

R_{OVP2} is the Output voltage side OVP resistance.

For example, OVP is active when VOUT ≥ 32 V if R_{OVP1} = 22 kΩ and R_{OVP2} = 330 kΩ.

(3) Buck-Boost DC/DC Converter Oscillation Frequency (f_{OSC})

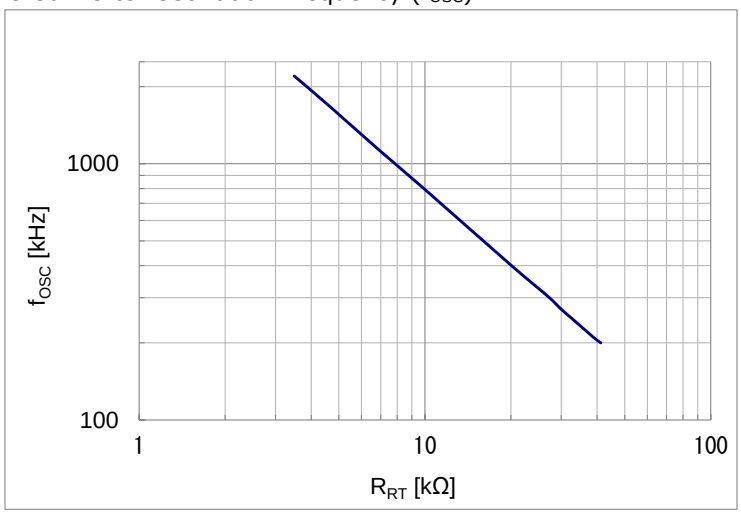


Figure 4. f_{OSC} vs R_{RT}

DC/DC oscillation frequency can be set via a resistor connected to the RT pin. This resistor determines the charge/discharge current to the internal capacitor, thereby changing the oscillation frequency. Set the resistance of R_{RT} using the above data and the equation below.

$$f_{OSC}\ =\ (81 \times 10^5 / R_{RT}) \qquad [\text{kHz}]$$

81 x 10^5 is the constant value determined in the internal circuit.

Take note that operation could not be guaranteed in the case of settings other than the recommended range.

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3. Buck-Boost DC/DC Converter - continued

(4) External Synchronization Oscillation Frequency

By clock signal input to the SYNC pin, the internal oscillation frequency can be synchronized externally. Do not switch from external to internal oscillation if the DC/DC switching is active. The clock input to the SYNC pin is valid only in rising edge. Input the external input frequency within ±20 % of internal oscillatory frequency set by the RT pin resistance.

(5) Soft Start Function (SS)

The soft-start (SS) function can start the output voltage slowly while controlling the current during the start by connecting the capacitance (C_{SS}) to the SS pin. In this way, output voltage overshoot and inrush current can be prevented. When SS function is not used, set the SS pin open. Refer to Setting of the Soft Start Time for the calculation of SS time.

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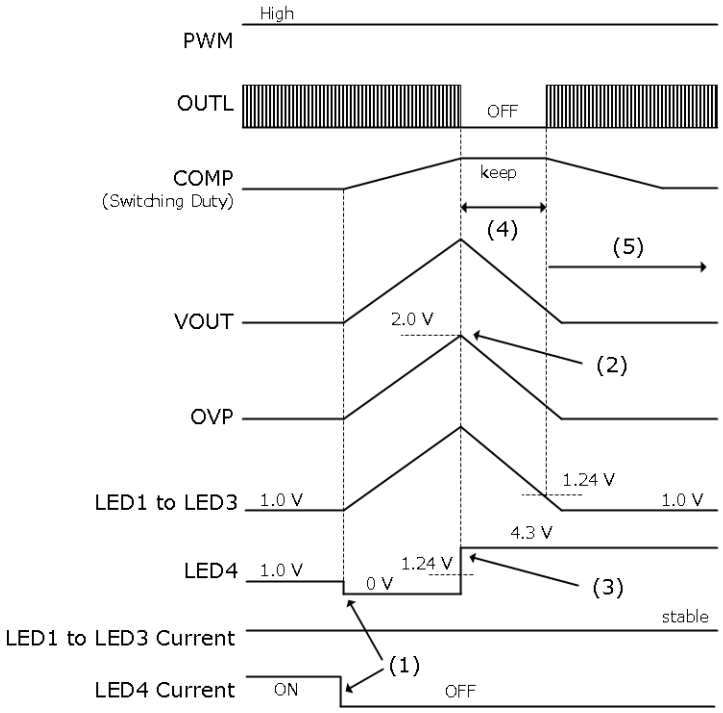
3. Buck-Boost DC/DC Converter - continued

(6) Maximum Duty

When DC/DC switching reaches Maximum Duty, expected VOUT voltage could be not output, and LED lights-out might occur by the reduction of LED output current and detection of ground short protection. Set input condition and load condition such that it does not reach Maximum Duty.

(7) DC/DC Switching Control at Over Voltage Output (LSDET)

When the lowest voltage in LED1 to LED4 pins (DC/DC feedback voltage) is more than 1.24 V, LSDET function works and turns off the switching of the DC/DC converter and maintains the COMP voltage (switching Duty). This function reduces the VOUT voltage quickly and intended to output stable switching Duty when VOUT is higher than the aim voltage. For example, LSDET works at the time of the LED4 OPEN detection. The timing chart example is described below.



(1) LED4 is OPEN and LED4 current does not flow, LED4 pin voltage is 0 V.

(2) VOUT is increase because of LED4 pin voltage is 0 V. Therefore OVP rises to 2.0 V, and LED4 becomes the OPEN detection state.

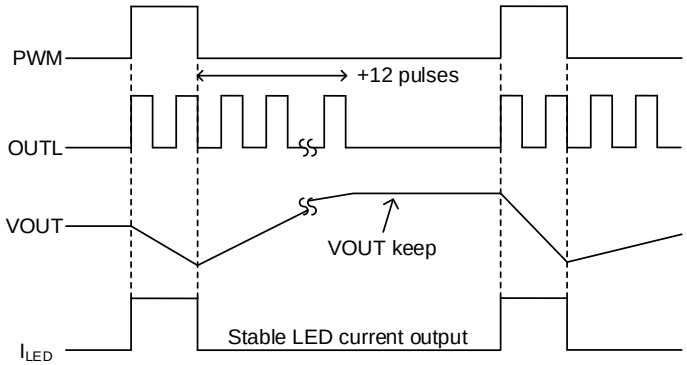
(3) LED4 pin voltage pulls up to 4.3 V in the IC by the OPEN detection.

(4) Because LED1 to LED4 pin becomes more than 1.24 V, LSDET function works. DCDC switching is OFF and COMP pin voltage is kept by LSDET function. VOUT is decrease because DC/DC switching is OFF.

(5) LED1 to LED3 pin voltages decrease with a drop of VOUT. And LSDET function is released when any of them is 1.24 V or less. DC/DC switching is turned on again and COMP pin voltage is controlled to appropriate duty.

(8) PWM Pulse and DC/DC Switching

After the fall of the PWM pulse, DC/DC switching is output 12 times and after that, turn off the DC/DC switching during PWM = Low. When PWM becomes High again, the DC/DC switching is on. Because of this, when PWM pulse width is short, it can maintain the output voltage and output the stable LED current.



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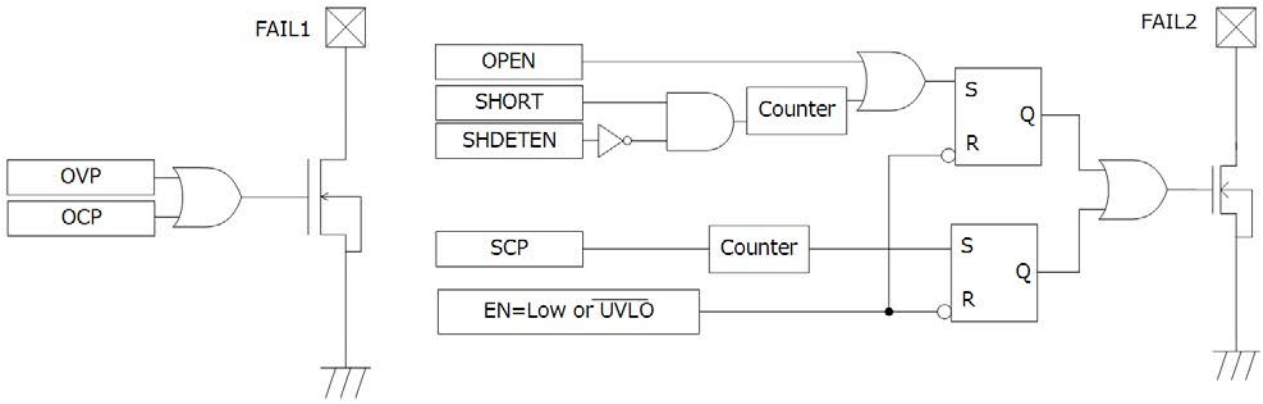
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Description of Blocks – continued

4. Protection Feature

Table 2. Detect Condition of Each Protection Feature and Operation during Detection

Function	Detect Condition		Operation During Detection
	[Detection]	[Release/Cancellation]	
UVLO	VCC ≤ 3.5 V or V_{VREG} ≤ 2.0 V	VCC ≥ 4.0 V and V_{VREG} ≥ 3.5 V	All blocks shut down except VREG
TSD	Ta ≥ 175 °C	Ta ≤ 150 °C	All blocks shut down except VREG
OVP	V_{OVP} ≥ 2.0 V	V_{OVP} ≤ 1.94 V	DC/DC switching OFF
OCP	V_{CS} ≤ VCC-0.2 V	V_{CS} > VCC-0.2 V	DC/DC switching OFF
SCP	V_{OVP} ≤ 0.57 V or Any of V_{LED1} to V_{LED4} is 0.3 V or less (100 ms delay @300 kHz)	EN Reset or UVLO Reset	After SCP delay time, all blocks latch OFF except VREG
LED Open Protection	Any of V_{LED1} to V_{LED4} is 0.3 V or less and V_{OVP} ≥ 2.0 V	EN Reset or UVLO Reset	Only detected channel LED current latches OFF
LED Short Protection	Any of V_{LED1} to V_{LED4} is 4.5 V and more (100 ms delay @300 kHz)	EN Reset or UVLO Reset	After LED Short delay time, only detected channel LED current latches OFF



Protection Flag Output Block Diagram

FAIL1 becomes low when OVP or OCP protection is detected, whereas FAIL2 becomes low when SCP, LED open or LED short is detected. If the FAIL1, FAIL2 pin is not used as a flag output, set the FAIL1, FAIL2 pin open or connect it to GND. The output from the FAIL1 and FAIL2 pins are reset and return to High by starting up of EN or release of UVLO. Also, those output is unstable when EN = Low and detecting UVLO. If the FAIL pin is used as a flag output, it is recommended to pull-up the FAIL1, FAIL2 pins to the VREG pin. The recommended value of pull-up resistance is 100 kΩ.

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4. Protection Feature - continued

(1) Under-Voltage Lock Out (UVLO)

The UVLO shuts down DC/DC converter and Current Driver when VCC ≤ 3.5 V or V_{VREG} ≤ 2.0 V. And UVLO is released by VCC ≥ 4.0 V and V_{VREG} ≥ 3.5 V.

(2) Thermal Shutdown (TSD)

The TSD shuts down DC/DC converter and Current Driver when the Tj 175 °C or more, and releases when the Tj becomes 150 °C or less.

(3) Over Voltage Protection (OVP)

The output voltage of DC/DC converter is detected from the OVP pin voltage, and the over voltage protection is activate if the OVP pin voltage becomes ≥ 2.0 V. When OVP is activated, the switching operation of the DC/DC converter turns off. And the OVP pin voltage becomes ≤ 1.94 V, OVP is released and the switching operation of the DC/DC converter turns on.

(4) Over Current Protection (OCP)

The OCP detects the coil current by monitoring the voltage of the high side resistor, and activates when V_{CS} ≤ VCC-0.2 V. When the OCP is activated, the switching operation of the DC/DC converter turns off. And V_{CS} > VCC-0.2 V, OCP is released and the switching operation of the DC/DC converter turns on.

(5) Short Circuit Protection (SCP)

The SCP can be operated when the SS pin voltage reaches 3.3 V while start-up. When any of the LED1 to LED4 pins voltage becomes 0.3 V or less or V_{OVP} ≤ 0.57 V, the built-in counter operation starts. The clock frequency of counter is the oscillation frequency (f_{OSC}), which is determined by R_{RT}. After it counts 32770, the DC/DC converter and the current driver are latched off. When fosc = 300 kHz, the count time is 100 ms and SCP operates after this count time. If all of the LED pin voltage becomes more than 0.3 V or V_{OVP} ≥ 1.0 V before 32770 count, the counter resets and SCP is not detected.

(6) LED Open Protection

When any of the LED pins voltage is 0.3 V or less and V_{OVP} 2.0 V or more, LED open is detected and latches off the open LED channel only.

(7) LED Short Protection

If any of V_{LED1} to V_{LED4} is 4.5 V or more, the built-in counter operation starts. The clock frequency of counter is the oscillation frequency (f_{OSC}), which is determined by R_{RT}. After it counts 32770, latches off the short LED channel only. When fosc = 300 kHz, the count time is 100 ms and SCP operates after this count time. During PWM dimming, the LED Short Protection is carried out only when PWM = High. If the condition of LED Short is reset while working the counter, the counter resets and LED Short is not detected. When LED Short Detect function will not be used, SHDETEN pin should be connected to VREG before starting. When LED Short Detect function is used, the SHDETEN pim should be connected to GND. In addition, it cannot change SHDETEN voltage (High or Low) during normal operation.

(8) PWM Low Interval Detect

The low interval of PWM input is counted by built-in counter during EN = High. The clock frequency of counter is the oscillation frequency (f_{OSC}), which is determined by R_{RT}. It stops the operation of circuits except VREG at 32768 counts. When f_{OSC} = 300 kHz, the count time is 100 ms and the Low interval of PWM is detected after this count time.

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4. Protection Feature - continued

(9) Output Voltage Discharge Circuit (VOUT Discharge Function)

If start-up with a charge remaining at VOUT, LED might occur flicker. To prevent this, it is necessary to discharge of VOUT when starting-up. If use only resistance for setting OVP to discharge, it takes a lot time for discharging VOUT. Therefore, this product has functionality of circuit for VOUT discharge. VOUT discharge function is available at Buck-Boost application and Buck application. For this case, be sure to connect VOUT and the VDISC pin. It discharges the residual electric charge of VOUT when DC/DC circuit is OFF; changing EN High to Low or operating protect function. The discharge time (t_{DISC}) is expressed in the following equations.

$$t_{DISC} = \frac{3 \times VOUT \times C_{OUT}}{4 \times I_{DISC}} \quad [s]$$

where:

t_{DISC}	is the DC/DC converter output discharge time.
C_{OUT}	is the VOUT capacity.
$VOUT$	is the DC/DC converter output voltage.
I_{DISC}	is the discharge current.

From the graph below, find the I_{DISC} value in 25 % VOUT voltage, and substitute it in the above equation. For example, substitute I_{DISC} value in VOUT = 5 V (approximately 76 mA) in the above equation when using in VOUT = 20 V, and calculate the discharge time.

In order to suppress the flickering of the LED, the time of restarting EN = Low should be secured t_{DISC} or more long.

Always check with actual machine because the t_{DISC} found here is a reference level.

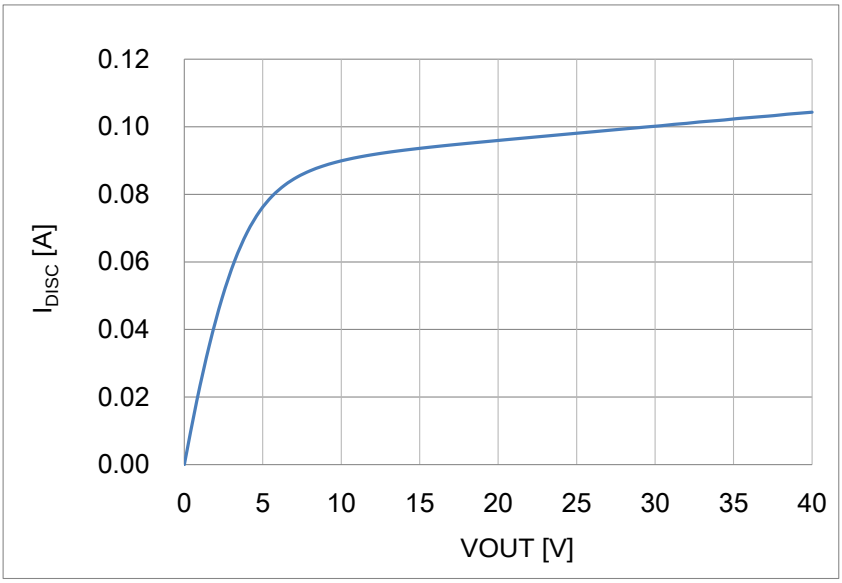


Figure 5. I_{DISC} vs VOUT

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Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	VCC	40	V
BOOT, OUTH Pin Voltage	V_{BOOT}, V_{OUTH}	45	V
SW, CS Pin Voltage	V_{SW}, V_{CS}	40	V
BOOT-SW Pin Voltage	$V_{BOOT-SW}$	7	V
LED1 to LED4, VDISC Pin Voltage	V_{LEDn} (n = 1 to 4), V_{VDISC}	40	V
PWM, SYNC, EN Pin Voltage	V_{PWM}, V_{SYNC}, V_{EN}	-0.3 to +7	V
VREG, OVP, FAIL1, FAIL2, SS, RT Pin Voltage	V_{VREG}, V_{OVP}, V_{FAIL1}, V_{FAIL2}, V_{SS}, V_{RT}	-0.3 to +7 < VCC	V
LEDEN1, LEDEN2, ISET, COMP, OUTL, SHDETEN Pin Voltage	V_{LEDEN1}, V_{LEDEN2}, V_{ISET} V_{COMP}, V_{OUTL}, $V_{SHDETEN}$	-0.3 to +7 < V_{VREG}	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C
LED Maximum Output Current	I_{LED}	120*1	mA

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB board with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

*1 Current level per channel. Set the LED current that does not over Junction Temperature Range (Tj) maximum.

Thermal Resistance*1

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*3	2s2p*4	
VQFN28SV5050				
Junction to Ambient	θ_{JA}	128.50	31.50	°C/W
Junction to Top Characterization Parameter*2	Ψ_{JT}	12	9	°C/W
HTSSOP-B28				
Junction to Ambient	θ_{JA}	107.00	25.10	°C/W
Junction to Top Characterization Parameter*2	Ψ_{JT}	6	3	°C/W

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*5	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

1 Based on JESD51-2A(Still-Air).

2 The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

3 Using a PCB board based on JESD51-3.

4 Using a PCB board based on JESD51-5, 7.

*5 This thermal via connects with the copper pattern of all layers.

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Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage*1	VCC	4.5	12	35	V
Operating Temperature	Topr	-40	+25	+125	°C
DC/DC Oscillation Frequency	f_{OSC}	200	300	2200	kHz
External Synchronized Frequency*2 *3	f_{SYNC}	Higher of 200 or f_{OSC} x 0.8	300	Lower of 2200 or f_{OSC} x 1.2	kHz
External Synchronized Pulse Duty	D_{SYNC}	40	50	60	%

*1 This indicates the voltage near the VCC pin. Be careful of voltage drop by the impedance of power line.
*2 When external synchronization frequency is not used, connect the SYNC pin to open or GND.
*3 When external synchronization frequency is used, do not change to internal oscillation frequency along the way.

Operating Conditions (External Constant Range)

Parameter	Symbol	Min	Typ	Max	Unit
VREG Capacity	C_{VREG}	1.0	2.2	4.7	µF
LED Current Setting Resistance	R_{ISET}	41	100	250	kΩ
Oscillation Frequency Setting Resistance	R_{RT}	3.6	27	41	kΩ
Soft Start Capacity Setting	C_{SS}	0.047	0.1	0.47	µF

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Electrical Characteristics(Unless otherwise specified, VCC = 12 V, Ta = -40 °C to +125 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Circuit Current	I_{CC}	-	-	10	mA	EN = High, SYNC = High, RT = OPEN, PWM = Low, ISET = OPEN, CIN = 10 µF
Standby Current	I_{ST}	-	-	10	µA	EN = Low, VDISC = OPEN
[VREG]						
Reference Voltage	V_{VREG}	4.5	5.0	5.5	V	I_{VREG} = -5 mA, C_{VREG} = 2.2 µF
[OUTH]						
OUTH High Side ON-Resistor	R_{ONHH}	1.5	3.5	7.0	Ω	I_{OUTH} = -10 mA
OUTH Low Side ON-Resistor	R_{ONHL}	0.8	2.5	5.5	Ω	I_{OUTH} = 10 mA
OCP Detection Voltage	V_{OLIMIT}	VCC-0.22	VCC-0.20	VCC-0.18	V	
[OUTL]						
OUTL High Side ON-Resistor	R_{ONLH}	1.50	3.50	10.00	Ω	I_{OUTL} = -10 mA
OUTL Low Side ON-Resistor	R_{ONLL}	0.80	2.50	5.50	Ω	I_{OUTL} = 10 mA
[SW]						
SW ON-Resistor	R_{ON_SW}	4.0	10.0	25.0	Ω	I_{SW} = 10 mA
[ERRAMP]						
LED Control Voltage	V_{LED}	0.9	1.0	1.1	V	
COMP Sink Current	$I_{COMPSINK}$	35	80	145	µA	V_{LEDn} = 2 V (n = 1 to 4), V_{COMP} = 1 V
COMP Source Current	$I_{COMPSOUCE}$	-145	-80	-35	µA	V_{LEDn} = 0.5 V (n = 1 to 4), V_{COMP} = 1 V
[Oscillator]						
Oscillation Frequency 1	f_{OSC1}	285	300	315	kHz	R_{RT} = 27 kΩ
Oscillation Frequency 2	f_{OSC2}	1800	2000	2200	kHz	R_{RT} = 3.9 kΩ
[OVP]						
OVP Detection Voltage	V_{OVP1}	1.9	2.0	2.1	V	V_{OVP}: Sweep up
OVP Hysteresis Width	$V_{OVPHYS1}$	0.02	0.06	0.10	V	V_{OVP}: Sweep down

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Electrical Characteristics - continued(Unless otherwise specified, VCC = 12 V, Ta = -40 °C to +125 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
[UVLO]						
UVLO Detection Voltage	V_{UVLO}	3.2	3.5	3.8	V	VCC: Sweep down
UVLO Hysteresis Width	V_{UHYS}	0.25	0.50	0.75	V	VCC: Sweep up, V_{VREG} > 3.5 V
[LED Output]						
LED Current Relative Dispersion	I_{LED1}	-3	-	+3	%	I_{LED} = 50 mA, Ta = 25 °C $\Delta I_{LED1} = (I_{LEDn}/I_{LEDn_AVG}-1)x\ 100$ (n = 1 to 4)
		-5	-	+5	%	I_{LED} = 50 mA, Ta = -40 °C to +125 °C $\Delta I_{LED1} = (I_{LEDn}/I_{LEDn_AVG}-1)x\ 100$ (n = 1 to 4)
LED Current Absolute Dispersion	I_{LED2}	-3	-	+3	%	I_{LED} = 50 mA, Ta = 25 °C $\Delta I_{LED2} = (I_{LEDn}/50\ mA-1) \times 100$ (n = 1 to 4)
		-5	-	+5	%	I_{LED} = 50 mA, Ta = -40 °C to +125 °C $\Delta I_{LED2} = (I_{LEDn}/50\ mA-1) \times 100$ (n = 1 to 4)
ISET Voltage	V_{ISET}	0.9	1.0	1.1	V	R_{ISET} = 100 kΩ
PWM Minimum Pulse Width	t_{MIN}	1	-	-	µs	f_{PWM} = 100 Hz to 20 kHz, I_{LED} = 20 mA to 100 mA
PWM Frequency	f_{PWM}	0.1	-	20	kHz	
[Protection Circuit]						
LED Open Detection Voltage	V_{OPEN}	0.2	0.3	0.4	V	V_{LEDn} :(n = 1 to 4) Sweep down
LED Short Detection Voltage	V_{SHORT}	4.2	4.5	4.8	V	V_{LEDn} :(n = 1 to 4) Sweep up
LED Short Detection Latch OFF Delay Time	t_{SHORT}	70	100	130	ms	R_{RT} = 27 kΩ
SCP Latch OFF Delay Time	t_{SCP}	70	100	130	ms	R_{RT} = 27 kΩ
PWM Latch OFF Delay Time	t_{PWM}	70	100	130	ms	R_{RT} = 27 kΩ
ISET-GND Short Protection Impedance	$I_{SETPROT}$	-	-	4.7	kΩ	
LSDET Detection Voltage	V_{LSDET}	-	1.24	-	V	
[Logic Input Voltage]						
Input High Voltage	V_{INH}	2.1	-	V_{VREG}	V	EN, SYNC, PWM, SHDETEN, LEDEN1, LEDEN2
Input Low Voltage	V_{INL}	GND	-	0.8	V	EN, SYNC, PWM, SHDETEN, LEDEN1, LEDEN2
Input Current	I_{IN}	15	50	100	µA	V_{IN} = 5 V (EN, SYNC, SHDETEN, PWM, LEDEN1, LEDEN2)
[FAIL Output (Open Drain)]						
FAIL Low Voltage	V_{OL}	-	0.1	0.2	V	I_{FAIL} = 0.1 mA

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Typical Performance Curves

(Reference Data. Unless otherwise specified, Ta = -40 °C to +125 °C)

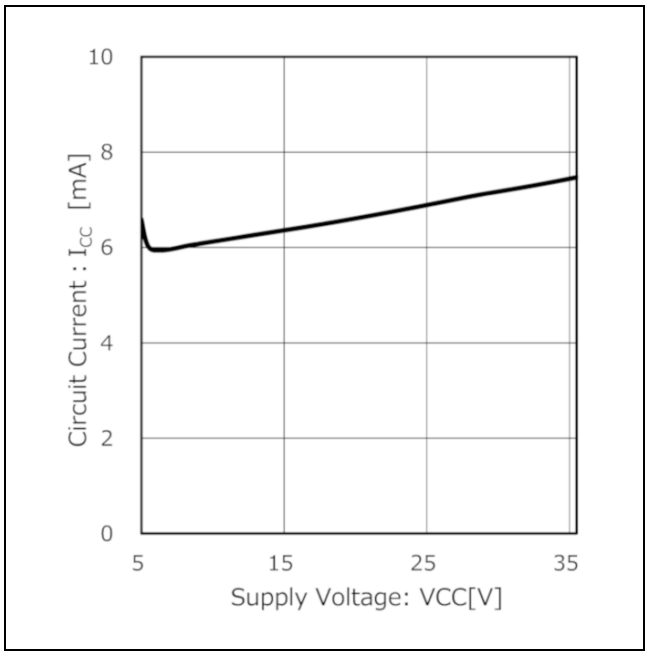


Figure 6. Circuit Current vs Power Supply Voltage
(VCC = 4.5 V to 35 V, V_{EN} = 3.3 V,
V_{PWM} = 0 V)

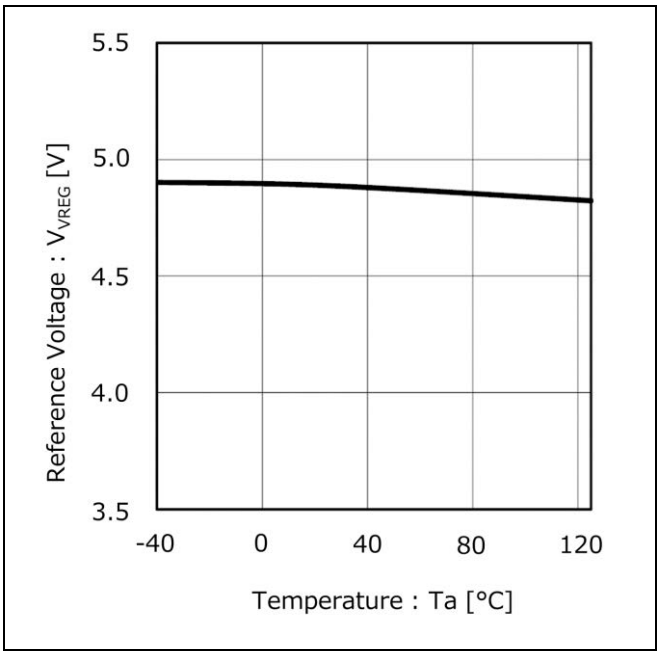


Figure 7. Reference Voltage vs Temperature
(VCC = 12 V V_{EN} = 3.3 V, V_{PWM} = 0 V)

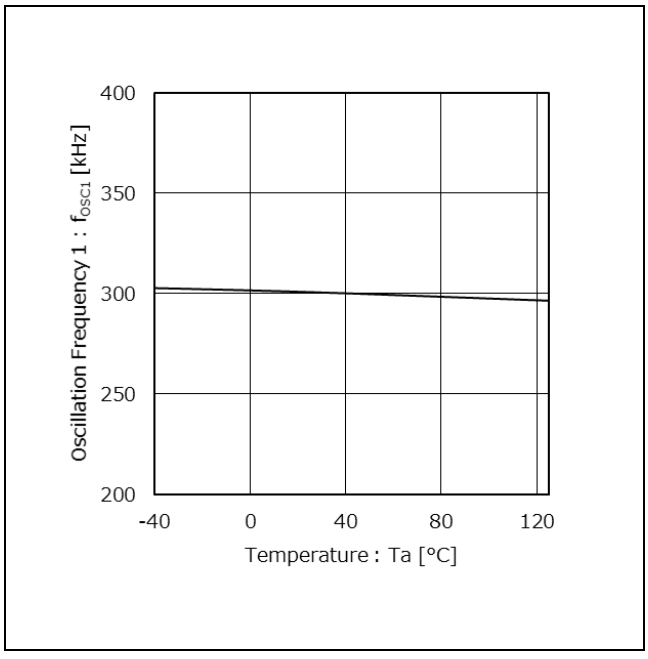


Figure 8. Oscillation Frequency 1 vs Temperature
(@300 kHz, VCC = 12 V, V_{EN} = 3.3 V, R_{RT} = 27 kΩ)

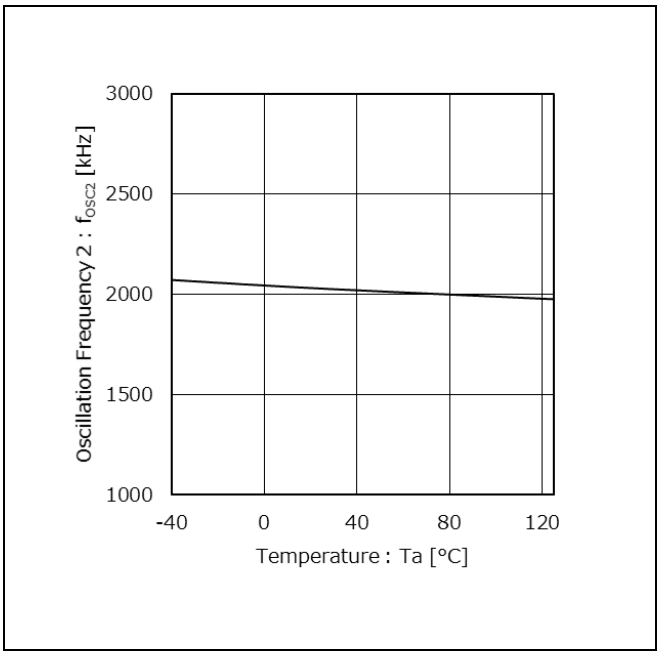


Figure 9. Oscillation Frequency 2 vs Temperature
(@2000 kHz, VCC = 12 V, V_{EN} = 3.3 V,
R_{RT} = 3.9 kΩ)

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Typical Performance Curves - continued

(Reference Data. Unless otherwise specified, Ta = -40 °C to +125 °C)

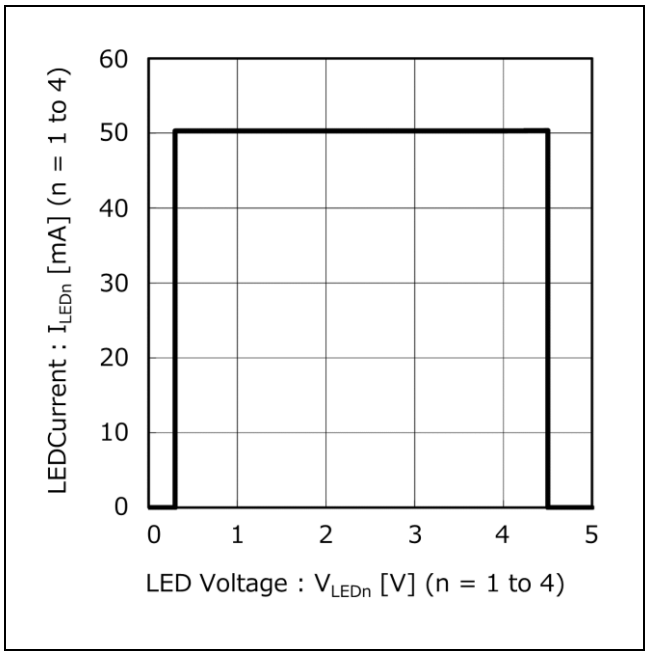


Figure 10. LED Current vs LED Voltage
(Ta = 25°C, VCC = 12 V, V_{EN} = 3.3 V,
V_{LEDn} = sweep (n = 1 to 4))

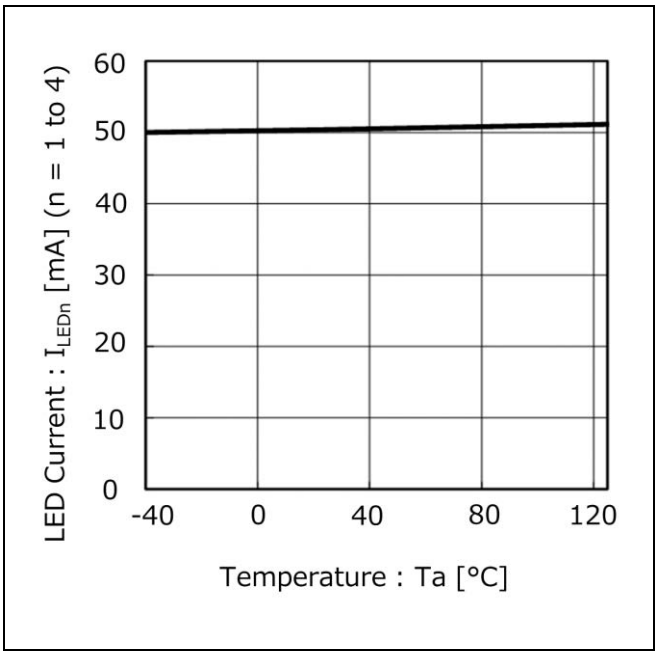


Figure 11. LED Current vs Temperature
(VCC = 12 V, V_{EN} = 3.3 V,
V_{LEDn} = 2 V (n = 1 to 4), V_{PWM} = V_{VREG})

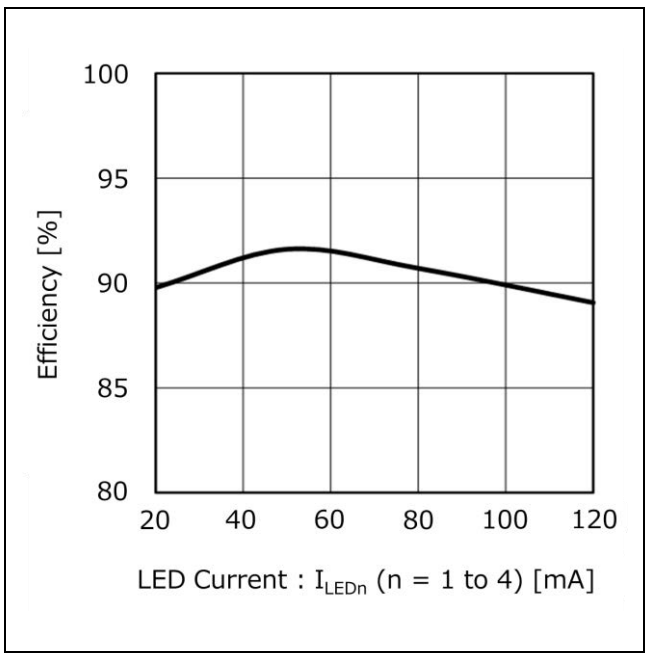


Figure 12. Efficiency vs LED Current(n = 1 to 4)
(Buck-Boost Application)
(Ta = 25 °C, VCC = 12 V,V_{EN} = 3.3 V, V_{PWM} = V_{VREG},
4 LED loads per channel, all channels have loads)

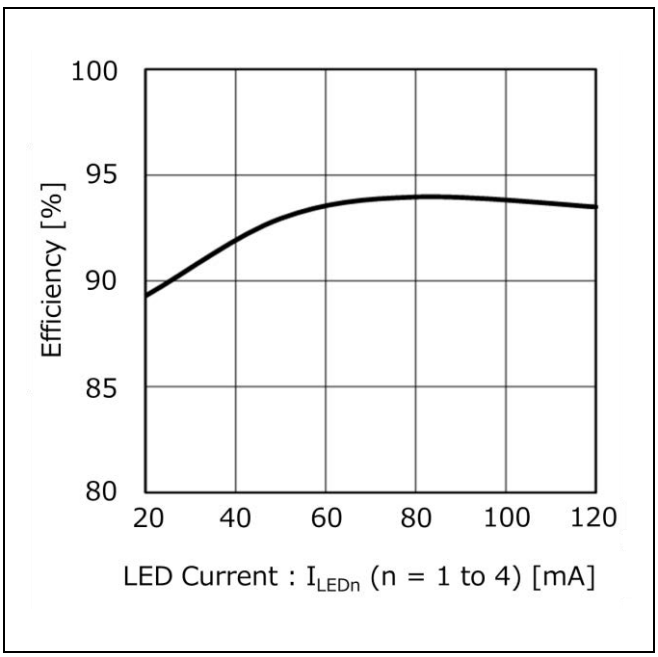
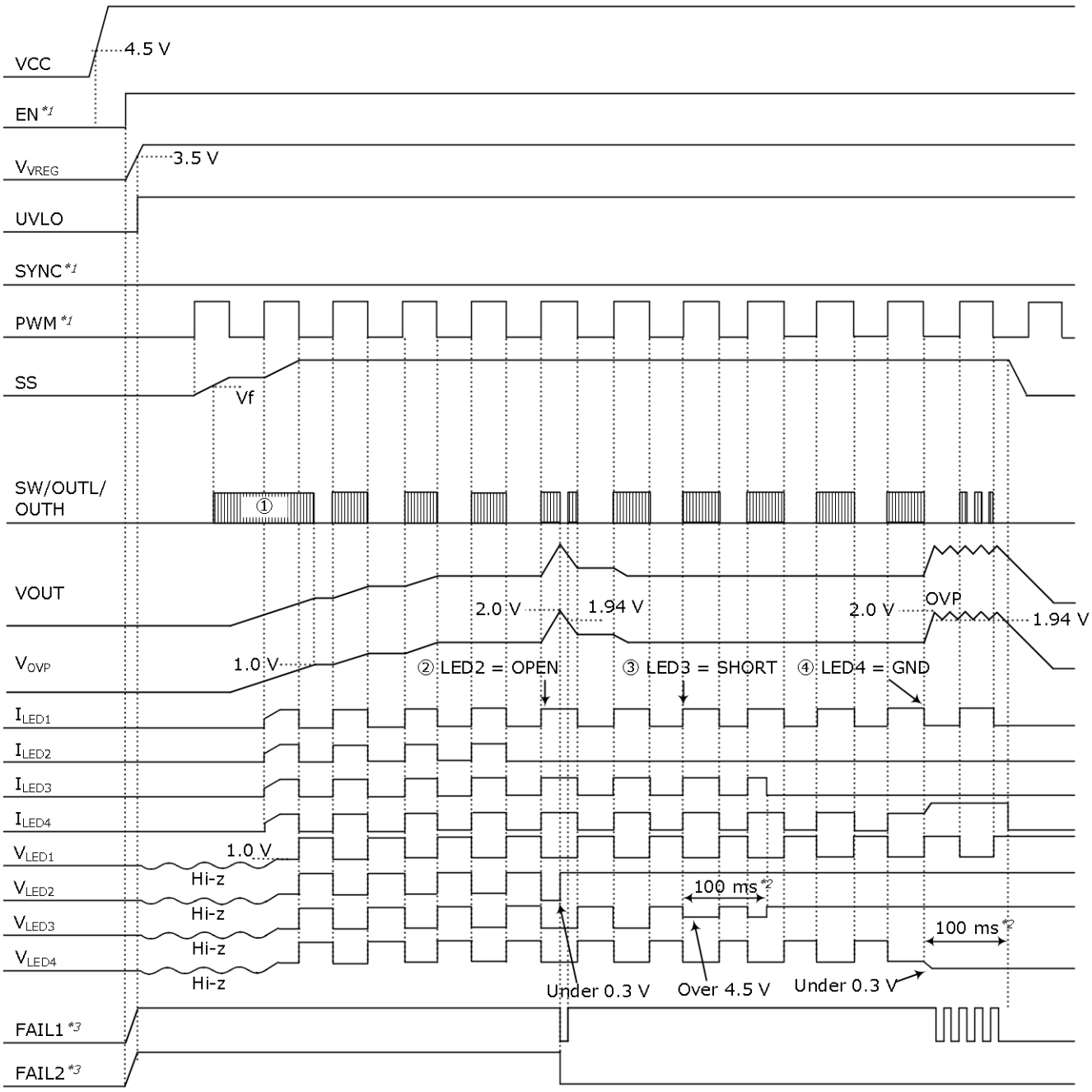


Figure 13. Efficiency vs LED Current(n = 1 to 4)
(Boost Application)
(Ta = 25 °C, VCC = 12 V,V_{EN} = 3.3 V, V_{PWM} = V_{VREG},
8 LED loads per channel, all channels have loads)

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Timing Chart (Start-up and Protection)



*1 EN is input after input VCC in the timing chart above, but there is no problem to input EN, PWM, and SYNC before input VCC. EN is judged as Low at V_{EN} is 0.8 V or less and as High at V_{EN} is 2.1 V or more. Do not use this IC in the condition of V_{EN} is between 0.8 V and 2.1 V.

*2 The count time of 32770 clk x $1/f_{OSC}$. In case of fosc=300 kHz, the count time is 100 ms(typ).

*3 The above timing chart is when the FAIL1 and FAIL2 pins are pulled up to the VREG pin.

① When V_{OVP} is less than 1.0 V, regardless of PWM input, the DC/DC switching operation is active (Pre-Boost function). And if V_{OVP} reaches 1.0 V, the Pre-Boost is finished. Only when PWM is activated, switches to the Normal mode which operates the DC/DC switching. When VOVP at the time of the start is 0.57 V or less, pre-boost function is effective.

② When V_{LED2} is 0.3 V or less and V_{OVP} is 2.0 V or more, LED Open Protect is active and LED2 is turned OFF. Then FAIL2 becomes Low.

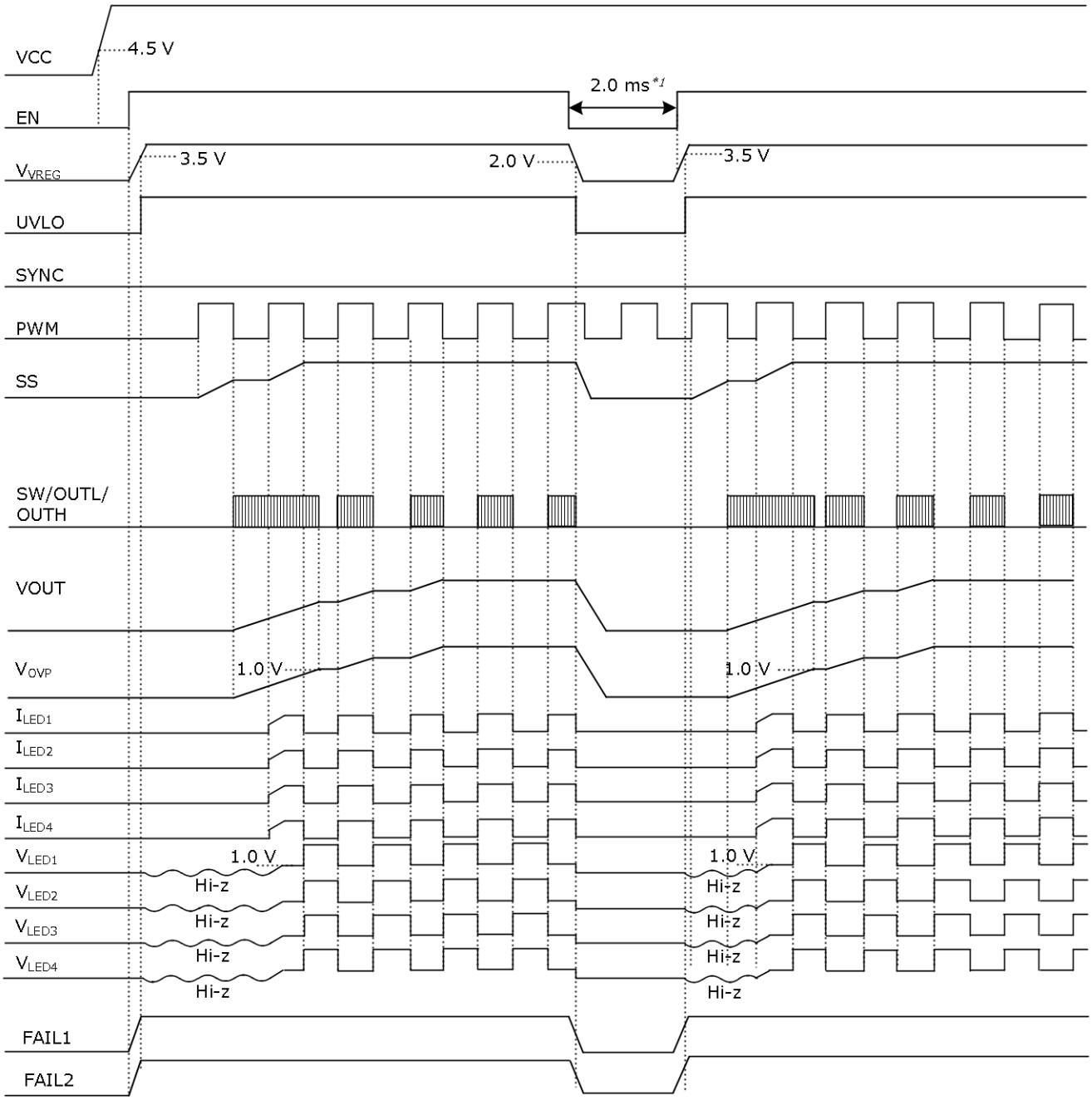
③ If the condition of V_{LED3} is 4.5 V or more and passes 100 ms (@f_{OSC} = 300 kHz), LED3 is turned OFF. Then FAIL2 becomes Low.

④ When V_{LED4} is shorted to GND, increase the VOUT voltage. Then V_{OVP} rises 2.0 V or more and detect OVP. FAIL1 becomes Low. If OVP occurs, DC/DC switching is OFF and decrease the VOUT voltage, then OVP repeats ON/OFF. And DC/DC switching and LED current of each channel is turned OFF after 100 ms by detecting ground short protection. (In case of f_{OSC} = 300 kHz).

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Timing Chart (Start-up and EN Restart)



*1 The Low section during EN restart requires 2.0 ms or more.

Restart after VOUT voltage is discharged. VOUT Discharge Function or external discharge switch is recommended. If EN is restarted with remaining VOUT voltage, LED flickering might occur.

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Application Examples

When using as Boost DC/DC converter

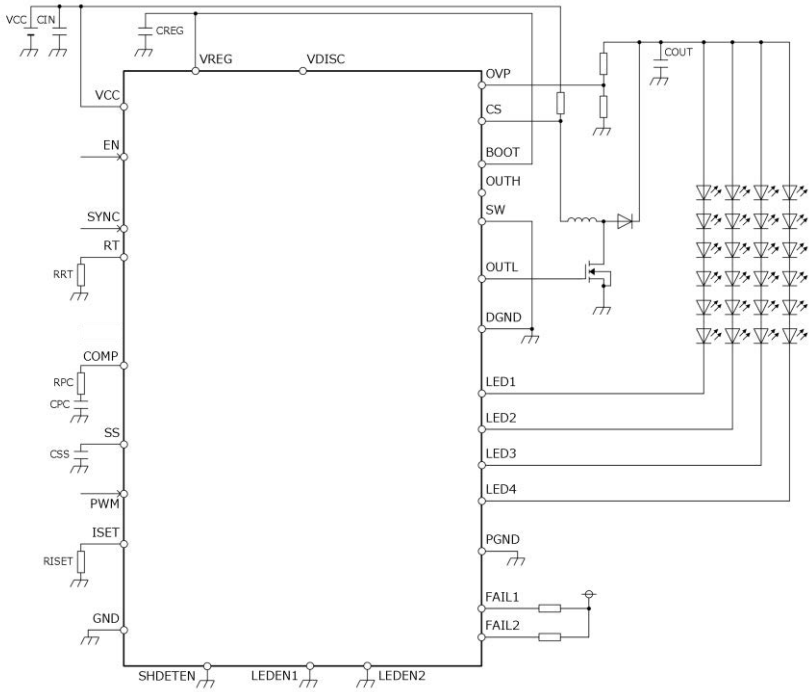


Figure 14. Boost application Circuit

If the VOUT pin or the LED pin is shorted in this case, the overcurrent from V_{IN} cannot be prevented. To prevent overcurrent, carry out measure such as inserting fuse of which value is OCP setting value or more and is part's rating current or less in between VCC and R_{CS}.

When using as Buck DC/DC Converter

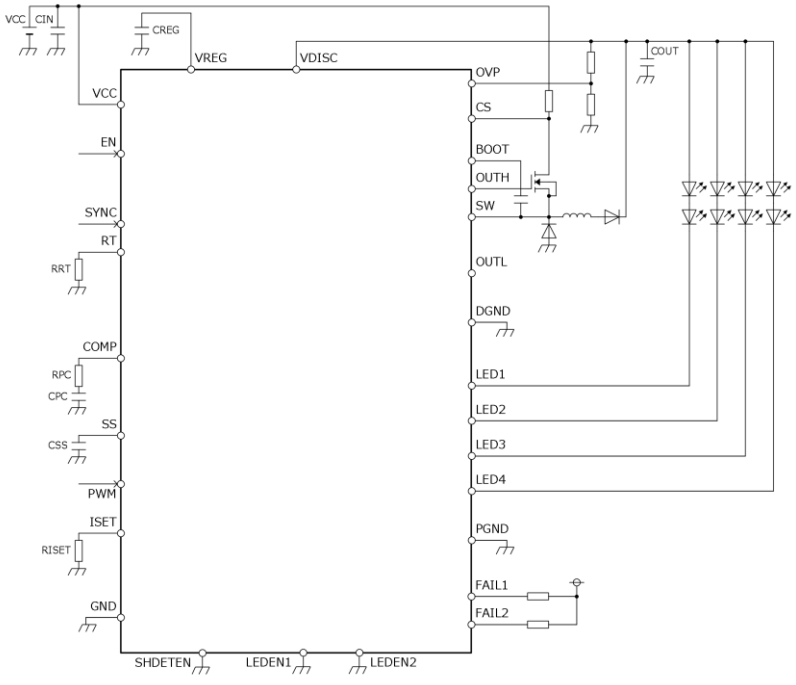


Figure 15. Buck Application Circuit

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PCB Application Circuit Diagram

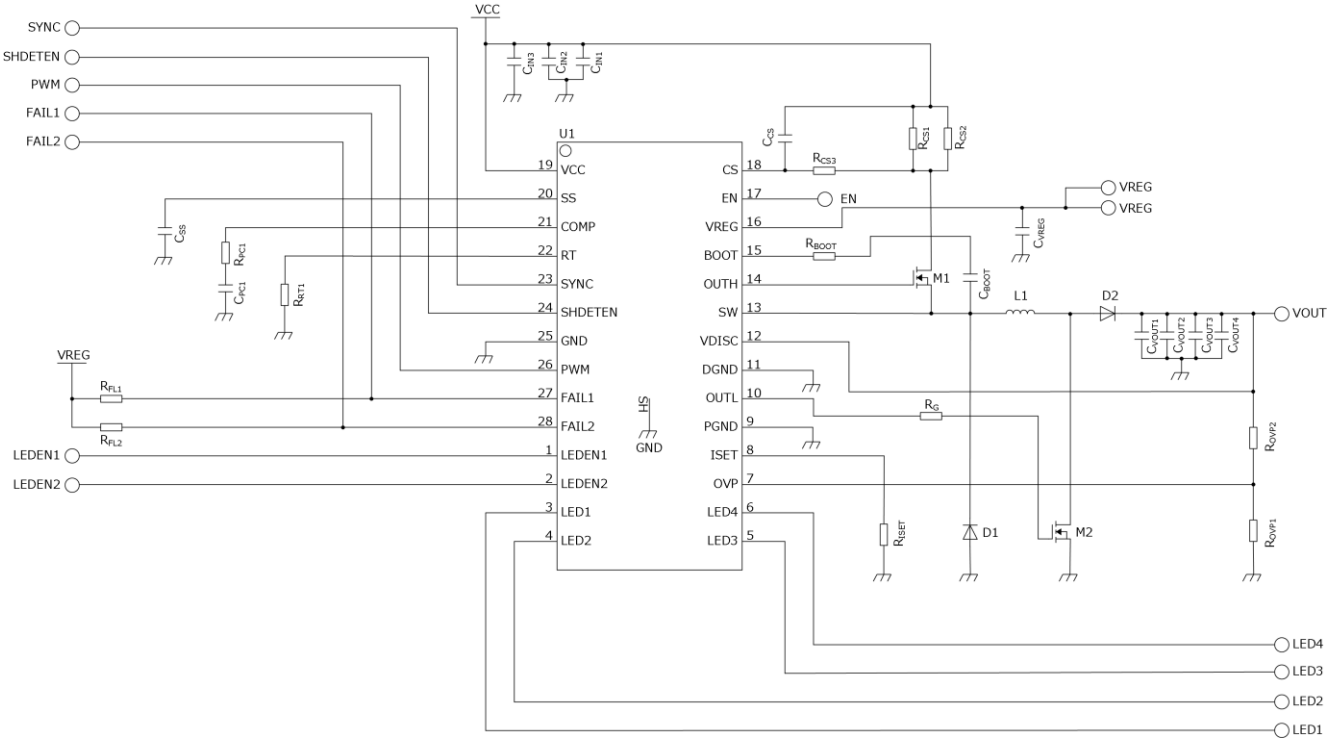


Figure 16. PCB Application Circuit

- Arrange R_{RT} resistor near the RT pin and do not attach capacitor.
- Arrange R_{ISET} resistor near the ISET pin and do not attach capacitor.
- Attach the decoupling capacitor of C_{IN} and C_{VREG} to IC pin as close as possible.
- Keep the impedance low because large current might flow into DGND and PGND.
- Be careful not to occur noise in the ISET, RT, and COMP pins.
- Since PWM, OUTH, OUTL, SW, SYNC and LED1 to LED4 have switching, avoid affecting the surrounding patterns.
- The SW, OUTH, BOOT pin to each components, keep shortest wiring and minimum impedance.
- There is thermal PAD at the back of package. Solder the board GND for thermal PAD.
- Set the gate resistor of FET (M1) to 0 Ω. If resistor is connected, M1 OFF timing is delayed in M1 parasitic capacity and gate resistor, and the penetrating current flows to the internal transistor of M1 and SW. The penetrating current might worsen the efficiency or detect OCP.
- To reduce noise, consider the board layout in the shortest wiring and minimum impedance for Boost loop (D2 →CVOUT→DGND→M2→D2) and Buck loop (VCC→RCS→M1→D1→DGND→GND→CIN→VCC).
- The ringing of Low-side FET can be suppressed by R_G, but there is a concern that efficiency might worsen when R_G increases. When using R_G, decide the resistance value after full evaluation.
- When PWM min pulse width satisfies the following formula, please do not connect a capacitor to LED1 to LED4 pins. It might misdetect LED short protection. When the connection of the capacitor is necessary for noise measures, please refer to us.

$$t_{MIN} \leq \frac{10}{f_{OSC}}$$

t_{MIN} : PWM min pulse width f_{OSC} : DCDC frequency target

- Wire both ends of R_{CS1} and R_{CS2} (Red line of below figure) most shortly. If a wiring is long, it may lead to false detection of OCP by an inductance.

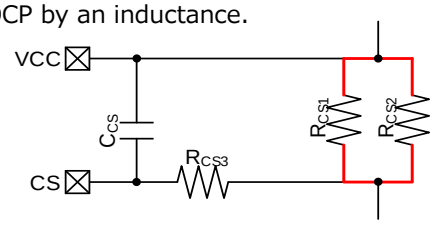


Figure 17. The Case of R_{CS} Parallel

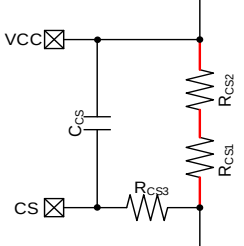


Figure 18. The case of R_{CS} Series

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PCB Board External Components List (Buck-Boost Application)

Serial No.	Component Name	Component Value	Product Name	Manufacturer
1	C_{IN1}	10 µF	GCM32EC71H106KA03	murata
2	C_{IN2}	-	-	-
3	C_{IN3}	-	-	-
4	R_{CS1}	150 mΩ	MCR100 Series	Rohm
5	R_{CS2}	150 mΩ	MCR100 Series	Rohm
6	R_{CS3}	Short	-	-
7	C_{CS}	-	-	-
8	C_{SS}	0.1 µF	GCM155R71H104KE37	murata
9	C_{PC1}	0.01 µF	GCM155R71H103KA40	murata
10	R_{PC1}	5.1 kΩ	MCR03 Series	Rohm
11	R_{RT1}	27 kΩ	MCR03 Series	Rohm
12	R_{FL1}	100 kΩ	MCR03 Series	Rohm
13	R_{FL2}	100 kΩ	MCR03 Series	Rohm
14	C_{VREG}	2.2 µF	GCM188C71A225KE01	murata
15	C_{BOOT}	0.1 µF	GCM155R71H104KE37	murata
16	R_{BOOT}	Short	-	-
17	L1	22 µH	CLF10060NIT-220M-D	TDK
18	M1	-	RSS070N05	Rohm
19	M2	-	RSS070N05	-
20	D1	-	RB050L-40	Rohm
21	D2	-	RB050L-40	Rohm
22	C_{VOUT1}	10 µF	GCM32EC71H106KA03	murata
23	C_{VOUT2}	10 µF	GCM32EC71H106KA03	murata
24	C_{VOUT3}	10 µF	GCM32EC71H106KA03	murata
25	C_{VOUT4}	10 µF	GCM32EC71H106KA03	murata
26	R_{OVP1}	20 kΩ	MCR03 Series	Rohm
27	R_{OVP2}	360 kΩ	MCR03 Series	Rohm
28	R_{ISET1}	100 kΩ	MCR03 Series	Rohm
29	R_G	0 kΩ	-	-

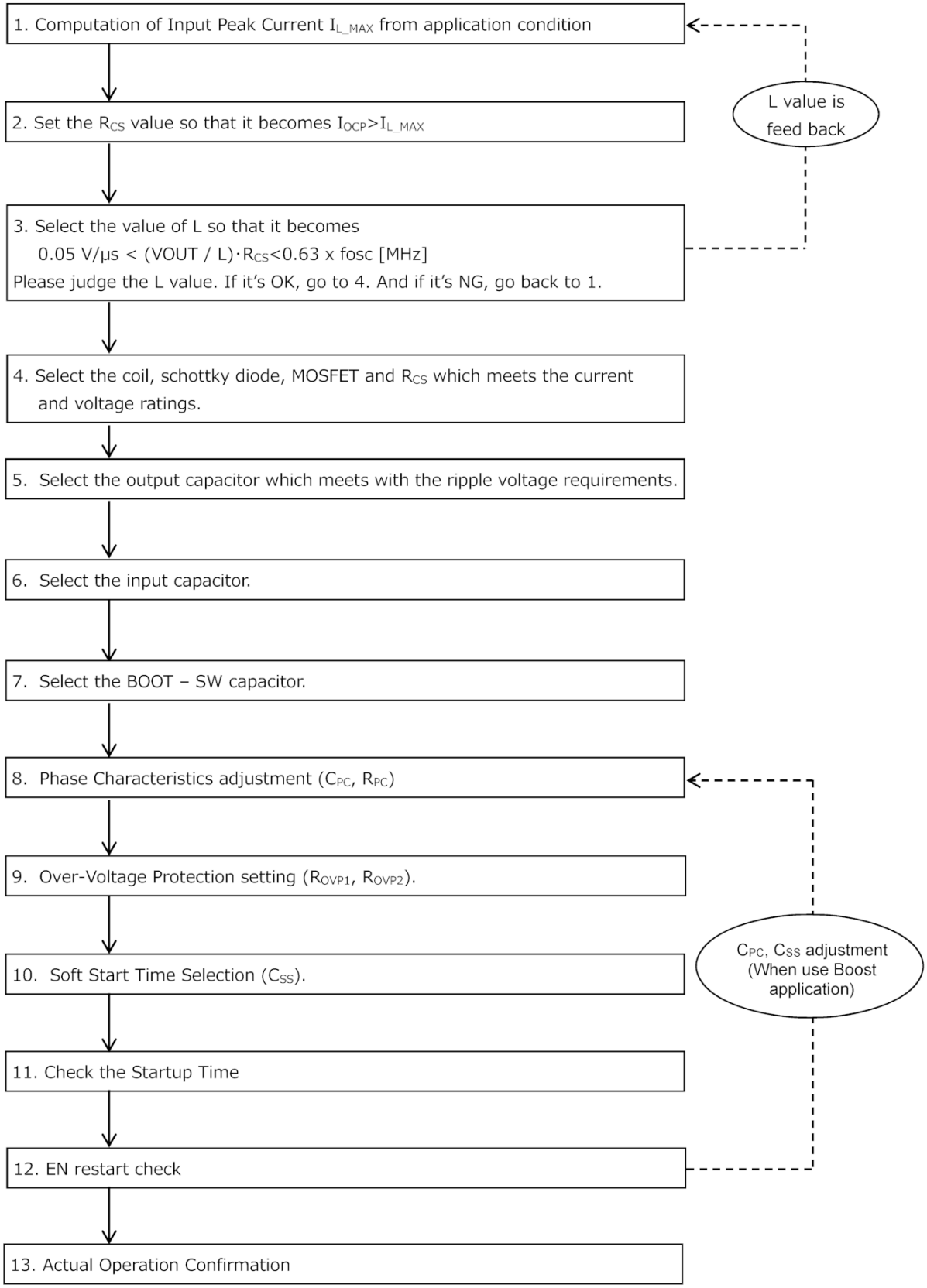
* The above components are modified according to operating conditions and load to be used.

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Selection of Components Externally Connected

Select the external components following the steps below.

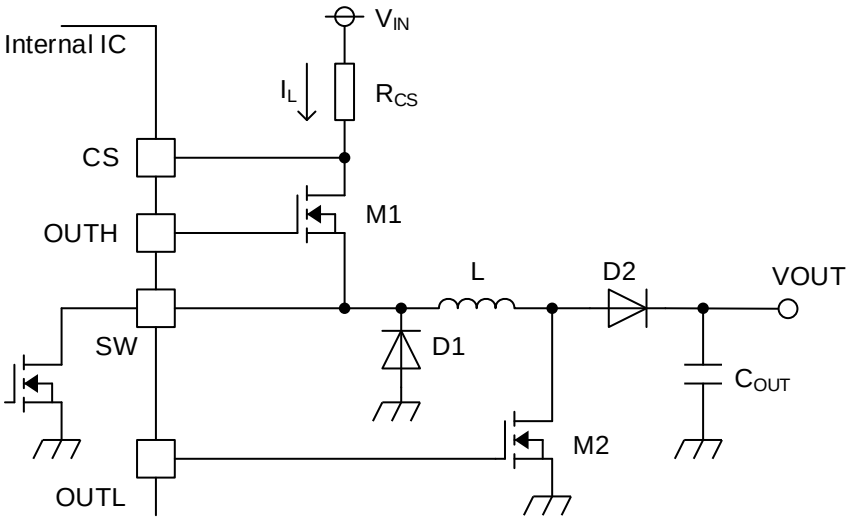


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Selection of Components Externally Connected - continued

1. Derivation of Maximum Input Leak Current I_{L_MAX}



Output Application Circuit Diagram (Buck-Boost Application)

(1) Maximum Output Voltage ($VOUT_{_MAX}$) Computation
Consider the Vf variation and number of LED connection in series for $VOUT_{_MAX}$ derivation

$$VOUT_{_MAX} = (Vf + \Delta Vf) \times N + 1.1$$

where:

$VOUT_{_MAX}$	is the maximum output voltage.
V_f	is the LED Vf voltage.
ΔV_f	is the LED Vf voltage variation.
N	is the LED series number.

(2) Maximum Output Current I_{OUT_MAX} Computation

$$I_{OUT_MAX} = I_{LED} \times 1.05 \times M$$

where:

I_{OUT_MAX}	is the maximum output current.
I_{LED}	is the output current per channel.
M	is the LED parallel number.

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1. Derivation of Maximum Input Leak Current I_{L_MAX} - continued

(3) Maximum Input Peak Current I_{L_MAX} Computation

$$I_{L_MAX} = I_{L_AVG} + \frac{1}{2}\Delta I_L$$

where:

I_{L_MAX} is the maximum input current.
I_{L_AVG} is the maximum input average current.
ΔI_L is the coil current amplification.

(In case of Boost Application)

$$I_{L_AVG} = VOUT_{_MAX} \times \frac{I_{OUT_MAX}}{\eta \times VCC}$$

$$\Delta I_L = \frac{VCC}{L} \times \frac{1}{f_{OSC}} \times \frac{VOUT_{_MAX} - VCC}{VOUT_{_MAX}}$$

(In case of Buck-Boost application)

$$I_{L_AVG} = (VCC + VOUT_{_MAX}) \times \frac{I_{OUT_MAX}}{\eta \times VCC}$$

$$\Delta I_L = \frac{VCC}{L} \times \frac{1}{f_{OSC}} \times \frac{VOUT_{_MAX}}{VCC + V_{OUT_MAX}}$$

(In case of Buck application)

$$I_{L_AVG} = I_{OUT_MAX} / \eta$$

$$\Delta I_L = \frac{VOUT}{L} \times \frac{1}{f_{OSC}} \times \frac{VCC - VOUT_{_MAX}}{VCC}$$

where:

VCC is the supply voltage.
η is the efficiency.
f_{OSC} is the DC/DC oscillation frequency.
L is the coil value.

- The worst case for VCC is minimum, so the minimum value should be applied in the equation.
- BD81A44EFV-M / BD81A44MUV-M adopts the current mode DC/DC converter control and is appropriately designed for coil value. The abovementioned value is recommended according to efficiency and stability. If choose the L values outside this recommended range, it not to be guaranteed the stable continuous operation. For example, it may cause irregular switching waveform.
- η (efficiency) is around 80 %.

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Selection of Components Externally Connected - continued

2. Setting of Over Current Protection Value (I_{OCP})

$$I_{OCP} = \frac{V_{OCP_MIN}}{R_{CS}} > I_{L_MAX} \quad [A]$$

where:

I_{OCP_MIN} is the overcurrent protection detect voltage.
V_{OCP_MIN} is the overcurrent protection detect voltage (0.18 V).
R_{CS} is the current detect resistance.
I_{L_MAX} is the maximum input peak current.

R_{CS} should be selected by the above equation.

3. Selection of Inductor

In order to achieve stable operation of the current mode DC/DC converter, it is recommended adjusting the L value within the range indicated below.

$$0.05 < \frac{VOUT \times R_{CS}}{L \times 10^6} < \frac{0.63 \times f_{OSC}}{10^6} \quad [V/\mu s]$$

where:

$VOUT$ is the DC/DC converter output voltage.
R_{CS} is the current detect resistance.
L is the coil value.
f_{OSC} is the DC/DC oscillation frequency.

Consider the deviation of L value and set with enough margins.

It is more stable by reducing the value of $\frac{VOUT \times R_{CS}}{L \times 10^6}$, however it slows down the response time.

Also, the following equation should be satisfied during coil selection in case it is used in VCC = 5 V or less.

$$L < \frac{12 \times VCC \times VCC \times \eta}{VOUT \times I_{LED} \times M \times f_{OSC}}$$

where:

L is the coil value.
VCC is the supply voltage.
η is the efficiency.
$VOUT$ is the DC/DC converter output voltage.
I_{LED} is the LED current per channel.
f_{OSC} is the DC/DC oscillation frequency.
M is the LED parallel number.

LED intensity may drop when a coil which does not satisfy the above is chosen.

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Selection of Components Externally Connected - continued

4. Selection of Voltage/Current Ratings of Coil (L), Diode (D1, D2), FET (M1, M2), $R_{CS,}$ and C_{OUT}

	Current Rating	Voltage Rating	Heat Loss
Coil L	> I_{L_MAX}	-	-
Diode D1	> I_{OCP}	> $VCC_{_MAX}$	-
Diode D2	> I_{OCP}	> V_{OVP_MAX}	-
FET M1	> I_{OCP}	> $VCC_{_MAX}$	-
FET M2	> I_{OCP}	> V_{OVP_MAX}	-
R_{CS}	-	-	> I_{OCP}^2 x R_{CS}
C_{OUT}	-	> V_{OVP_MAX}	-

Consider deviation of external parts and set with enough margins.
In order to achieve fast switching, choose the FET's with smaller gate-capacitance.

5. Setting of Output Capacitor

Select the output capacitor C_{OUT} based on the requirements of the ripple voltage VOUTpp.

$$VOUTpp = \frac{20 \times I_{LED} \times M}{f_{OSC} \times C_{VOUT} \times \eta} + \Delta I_L \times R_{ESR} \quad [V]$$

where:

$VOUTpp$	is the VOUT ripple voltage.
I_{LED}	is the LED current per channel.
M	is the LED parallel number.
f_{OSC}	is the DC/DC oscillation frequency.
C_{VOUT}	is the VOUT capacity.
η	is the efficiency.
ΔI_L	is the coil current amplification.
R_{ESR}	is the equivalent series resistance of output capacitor $C_{OUT.}$

The actual VOUT ripple voltage is affected by PCB layout and external components characteristics. Therefore, check with the actual machine, and design a capacity with enough margins to fit in allowable ripple voltage.
The maximum value of C_{OUT} that can be set is 500 µF.

6. Selection of Input Capacitor

An input capacitor which is 10 µF or more with low ESR ceramic capacitor is recommended. An input capacitor which is not recommended may cause large ripple voltage at the input and hence lead to malfunction of the IC.

7. Selection of BOOT - SW Capacitor

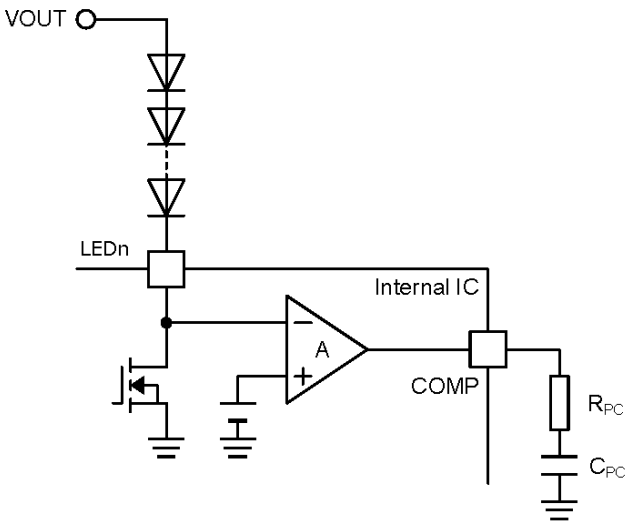
When using the Buck-Boost application or Buck application, insert 0.1 µF capacitor between the BOOT pin and the SW pin.

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Selection of Components Externally Connected - continued

8. Setting of Phase Compensation Circuit



COMP Pin Application Schematic(n = 1 to 4)

Stability Condition of Application

The stability in LED voltage feedback system is achieved when the following conditions are met.

(1) When gain is 1 (0 dB), the phase delay is 150° or less (or simply, phase margin is 30° or more).

(2) When gain is 1 (0 dB), the frequency (Unity Gain Frequency) is 1/10 or less of switching frequency.

To assure stability based on phase margin adjustment is setting the Phase-lead fz close to unity gain frequency. In addition, the Phase-lag fp1 is decided based on C_{OUT} and output impedance R_L.
The respective formulas are as follows.

Phase-lead $fz = 1/(2\pi R_{PC} C_{PC})$ [Hz]

Phase-lag $fp1 = 1/(2\pi R_L C_{OUT})$ [Hz]

* The output impedance that is calculated in $R_L = VOUT/I_{OUT}$

To make a good result, set fz between 1 kHz to 10 kHz. Substitute the value in the maximum load for R_L. Further, this setting is easily obtained, and the adjustment with the actual machine may be necessary because it is not strictly calculated. In case of mass production design, thorough confirmation with the actual machine is necessary because these characteristics can change based on board layout, load condition and etc.

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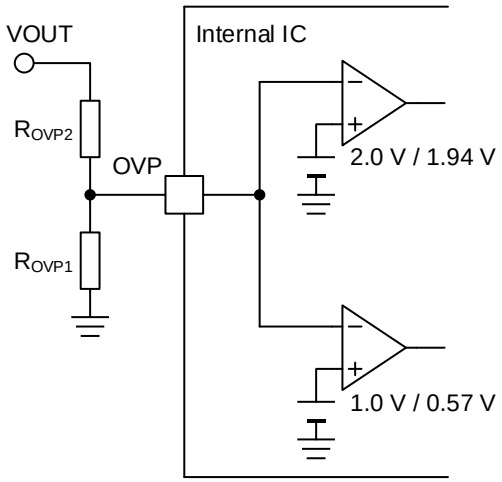
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Selection of Components Externally Connected - continued

9. Setting of Over Voltage Protection (OVP)

Over voltage protection (OVP) is set from the external resistance R_{OVP1}, R_{OVP2}.

The setting described below is important in the either boost, buck and buck-boost applications.



OVP Application Circuit

The OVP pin detects the over voltage when it is 2.0 V (Typ) or more and stops the DC/DC switching. In addition, it detects the open condition when the OVP pin is at 2.0 V (Typ) or more and the LED1 to LED4 pins voltage is at 0.3 V (Typ) or less, and the circuit is latched to OFF (Refer to Protection Feature). In preventing error in detection of OPEN, it is necessary that the resistor divide voltage of the maximum value of output voltage shall be less than the minimum value of OPEN detection voltage.

Set the R_{OVP1}, R_{OVP2} in such a way the formula shown below can be met.

$$VOUT(Max) \times \frac{R_{OVP1}}{(R_{OVP1}+R_{OVP2})} < V_{OVPopen}(Min) \cdots\cdots (1)$$

where:

$VOUT$ is the DC/DC output voltage.

$V_{OVPopen}$ is the OVP pin open detection voltage.

Example 1: When Vf = 3.2 V±0.3 V LED is used in 8 series

$$VOUT(Max) = 1.1(LED\ control\ voltage\ Max) + (3.2 + 0.3) \times 8 = 29.1 \quad [V]$$

Open Detection OVP Pin Voltage $V_{OVPopen}(Min) = 1.9 \quad [V]$

If R_{OVP1} = 20 kΩ, set by R_{OVP2} > 286.3 kΩ from (1).

Example 2: When Vf = 3.2 V±0.3 V LED is used in 3series

$$VOUT(Max) = 1.1(LED\ control\ voltage\ Max) + (3.2 + 0.3) \times 3 = 11.6 \quad [V]$$

Open Detection OVP Pin Voltage $V_{OVPopen}(Min) = 1.9 \quad [V]$

If R_{OVP1} = 20 kΩ, set by R_{OVP2} > 102.1 kΩ from (1).

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9. Setting of Over Voltage Protection (OVP) - continued

<Attention at the OVP Voltage Setting>

At the boost application, it is decided whether pre-boost works by initial value of the OVP pin voltage. When it does not perform pre-boost, be careful because startup time may become long.

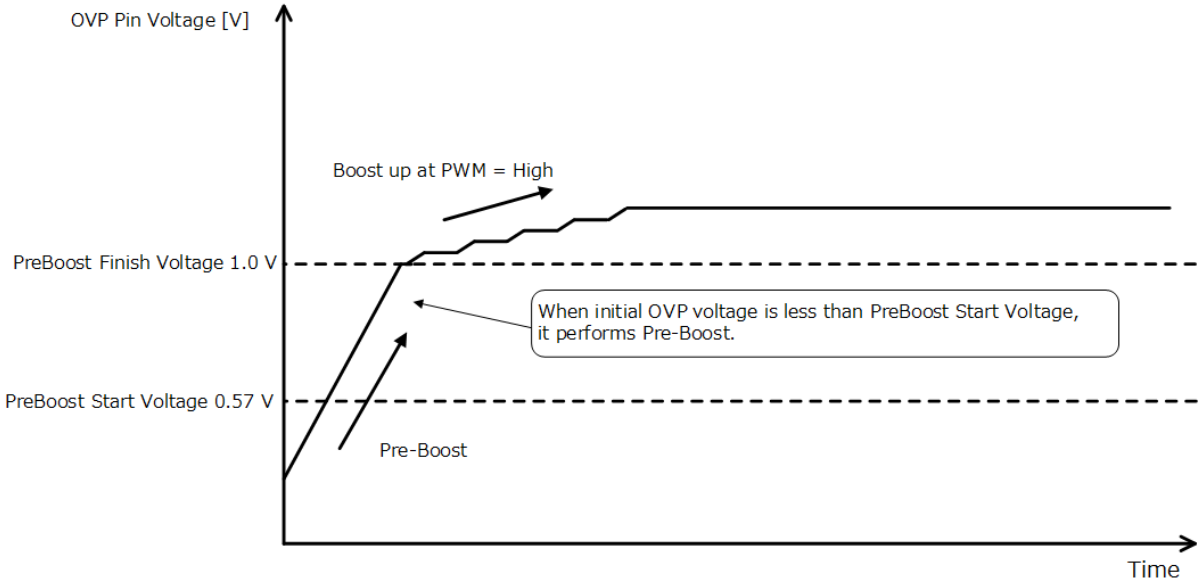


Figure 19. With Pre-boost

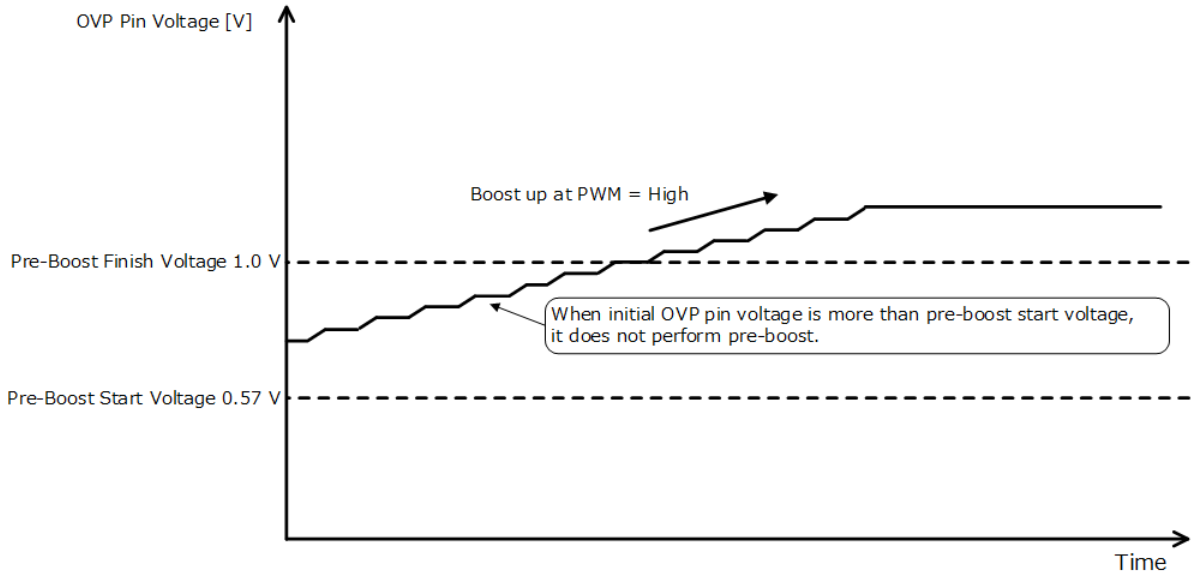


Figure 20. Without Pre-boost

At the buckboost or buck application, initial OVP voltage is less than pre-boost start voltage by VDISC function, it always performs pre-boost.

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Selection of Components Externally Connected - continued

10. Setting of Soft Start Time

The soft start circuit is necessary to prevent increase of the coil current and overshoot of the output during the start-up. A capacitance in the range of 0.047 μF to 0.47 μF is recommended. A capacitance less than 0.047 μF may cause overshoot at the output voltage. On the other hand, a capacitance more than 0.47 μF may cause massive reverse current through the parasitic elements when power supply is OFF and may damage the IC.

Soft start time t_{SS} (Typ).

$$t_{SS} = C_{SS} \times 3.3 / (5 \times 10^{-6}) \quad [s]$$

where:

C_{SS} is the Capacitance at the SS pin.

11. Confirmation of Start-up Time

If the PWM duty is smaller at start-up, the start-up time becomes longer. It is effective to reduce the C_{PC} value to shorten start-up time, however, confirmation of the phase margin is necessary. PWM duty and data of start-up time in typical 2 conditions are shown below.

Condition 1 (Boost)

VCC = 12 V, VOUT = 30 V (assume 8 LED's series), R_{RT} = 27 kΩ (f_{OSC} = 300 kHz), R_{ISET} = 100 kΩ (I_{LED} = 50 mA), C_{PC} = 0.01 μF, R_{PC} = 5.1 kΩ, C_{SS} = 0.1 μF, R_{OVP1} =2 0 kΩ, R_{OVP2} = 360 kΩ

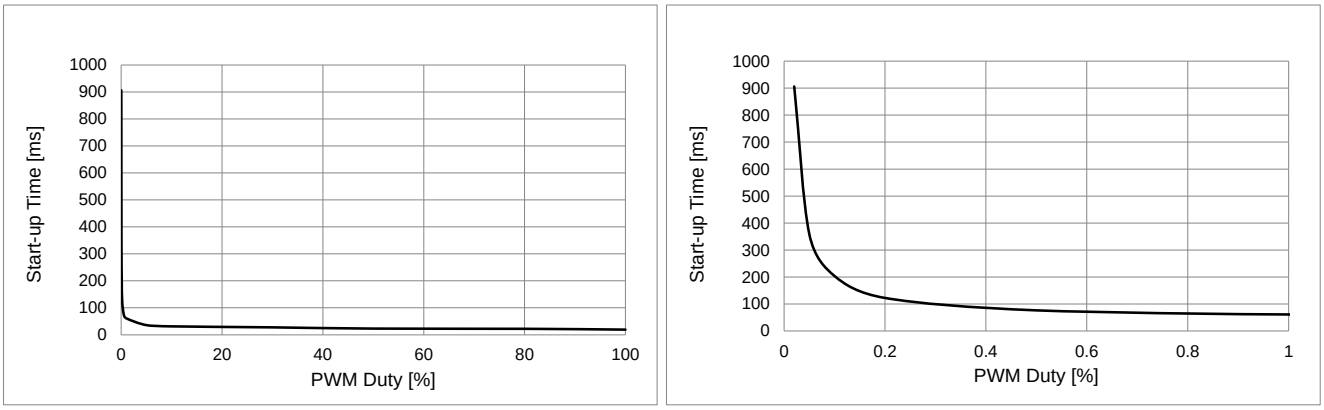


Figure 21. Start-up Time(Boost) vs PWM Duty

Condition 2 (Buck-Boost)

VCC = 12 V, VOUT = 20 V (assume 5 LED's series), R_{RT}= 27 kΩ (f_{OSC} = 300 kHz), R_{ISET} = 100 kΩ (I_{LED} = 50 mA), C_{PC} = 0.01 μF, R_{PC} = 5.1 kΩ, C_{SS} = 0.1 μF, R_{OVP1} = 30 kΩ, R_{OVP2} = 360 kΩ

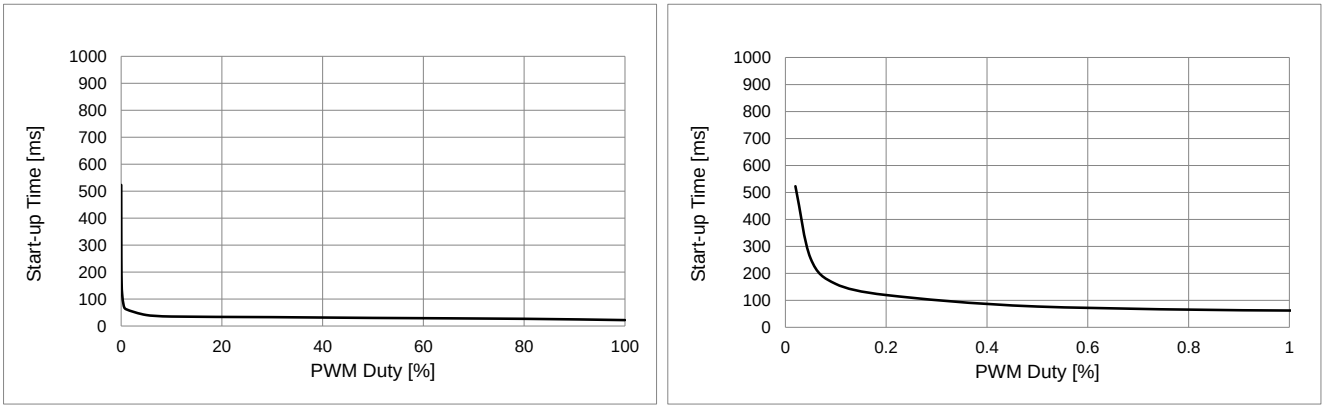


Figure 22. Start-up Time(Buck-Boost) vs PWM Duty

The above are reference data. Always confirm by machine operation because the actual start-up time depends on layout pattern, component constant, and component characteristics.

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Selection of Components Externally Connected – continued

12. EN Restart Check

When it starts in the state that an electric charge remains in Vout including the case of the EN restart, It may become the SCP detection condition. Set the condition according to applications.

When use the Buck-Boost or Buck application.
Connect the VOUT and VDISC pin and set EN = Low time to satisfy the below equation.

$$t_{DISC} = \frac{3 \times VOUT \times C_{OUT}}{4 \times I_{DISC}} < EN\ Low\ Time \quad [s]$$

Regarding t_{DISC} details, please refer to Output Voltage Discharge Circuit (VOUT Discharge Function).

When use the Boost application.
Adjust C_{SS} and C_{PC} value to satisfy the below equation. If C_{PC} value is changed, phase margin will changed, and if C_{SS} value is changed, start up time is changed. Please verifying by actual measurements.

$$t1 = \left(\frac{0.4+2.7\times n-VCC}{0.4+2.7\times n} \times \frac{1}{f_{OSC}\times R_{RT}\times 1.38\times 10^{-10}} + 1.56\right) \times \frac{C_{PC}}{(0.46\times Duty)} \quad [s]$$

$$t2 = C_{SS} \times 6.1 \times 10^5 + 29791/f_{OSC} \quad [s]$$

Adjust C_{PC} and C_{SS} value with $t1 < t2$.
Where:

n is the LED series number.
VCC is the supply voltage.
f_{OSC} is the DC/DC oscillation frequency.
R_{RT} is the RT resistence.
C_{PC} is the COMP capacitor.
$Duty$ is the PWM Duty.
C_{SS} is the Capacitance at the SS pin.

(Example) n = 7, VCC = 7 V, f_{OSC} = 300 kHz, R_{RT} = 27 kΩ, C_{PC} = 0.01 μF, C_{SS} = 0.1 μF, PWM Duty = 1 %

$$t1 = \left(\frac{0.4+2.7\times 7-7}{0.4+2.7\times 7} \times \frac{1}{300k\times 27k\times 1.38\times 10^{-10}} + 1.56\right) \times \frac{0.01}{(0.46\times 1)} = 0.0463 \quad [s]$$

$$t2 = 0.1\,\mu \times 6.1 \times 10^5 + 29791/300k = 0.1603 \quad [s]$$

In the case of this condition, it is no problem because "$t1 < t2$" is met.

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Selection of Components Externally Connected - continued

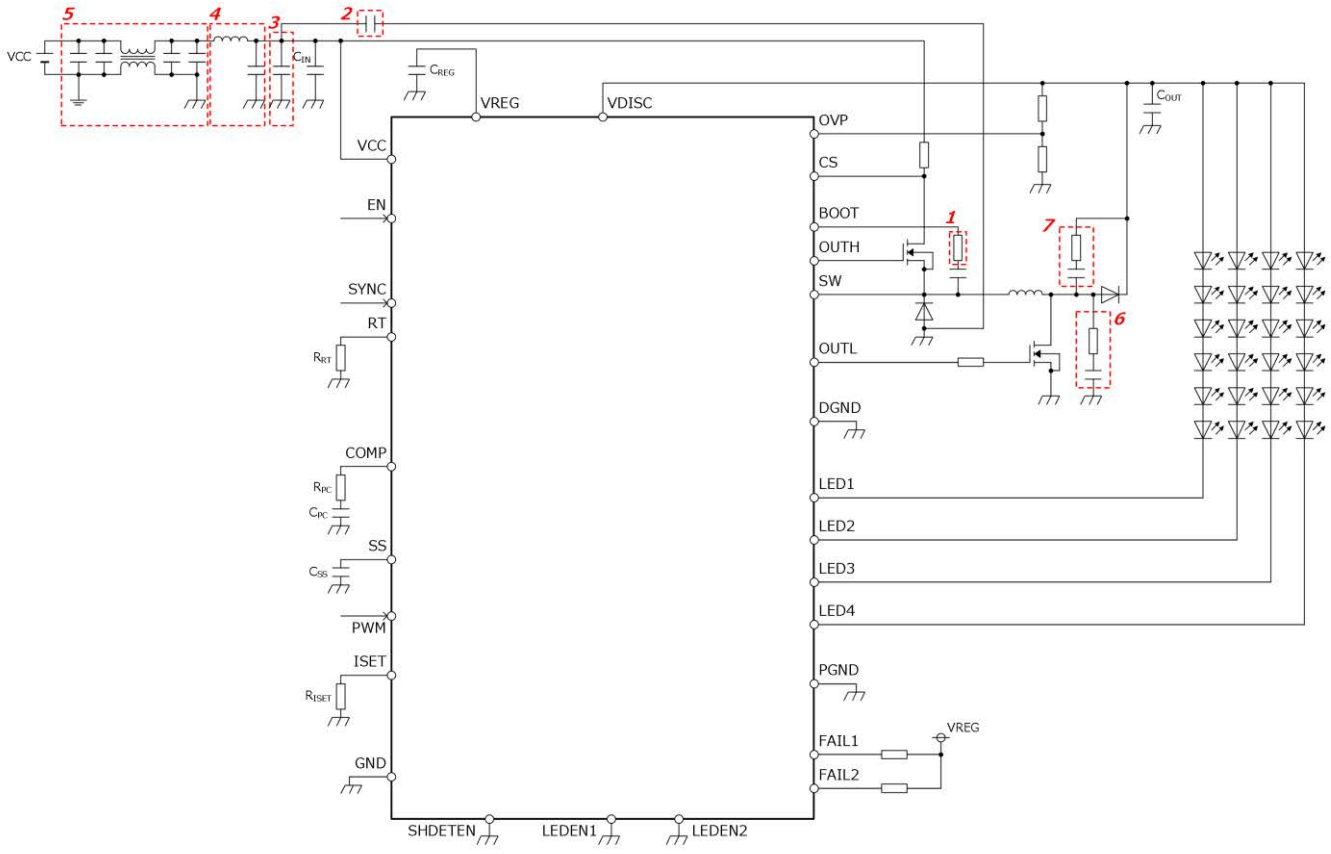
13. Confirmation of Actual Operation

Set up the external components value by procedures and attentions mentioned above. However, those settings above are not guaranteed because these are theoretically calculated and it does not include the external parts' variation or characteristics changing. The overall characteristics may change depend on power supply voltage, LED current, LED number, inductance, output capacitance, switching frequency, and PCB layout. We strongly recommend verifying your design by taking the actual measurements.

Additional parts for EMC

The example of EMC countermeasure components is shown in the chart below.

1. The resistance for adjusting Slew Rate of high side FET
2. The capacitor for reducing current loop noise of high side FET.
3. The capacitor for reducing noise of high frequency on power line.
4. The low pass filter for reducing noise of power line.
5. The common mode filter for reducing noise of power line.
6. The snubber circuit for reducing noise of high frequency of low side FET.
7. The snubber circuit for reducing ringing of low side FET switching.



Application Circuit Reference Example (Including EMC Countermeasure Components)

It is basically non-recommended to connect a capacitor to the LED1 to LED4 pins. Please refer to PCB Application Circuit. When the connection of the capacitor is necessary for noise measures, please refer to us.

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Precautions on PCB Layout

The layout pattern greatly affects the efficiency and ripple characteristics. Therefore, it is necessary to examine carefully when designing. As show in the figure below, Buck-Boost DC/DC converter has two loops; “Loop1” and “Loop2”. The parts in each loop have to be set as near as possible to each other. (For example, GND of C_{OUT} and DGND should be very near, GND of C_{IN} and GND of D1 should be very near and so on.)

Moreover, the wirings of each loop should be as low impedance as possible.

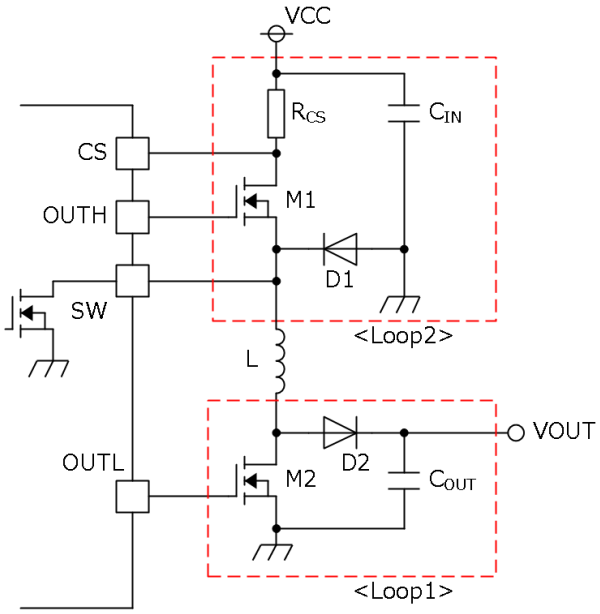


Figure 23. Circuit of DC/DC Block

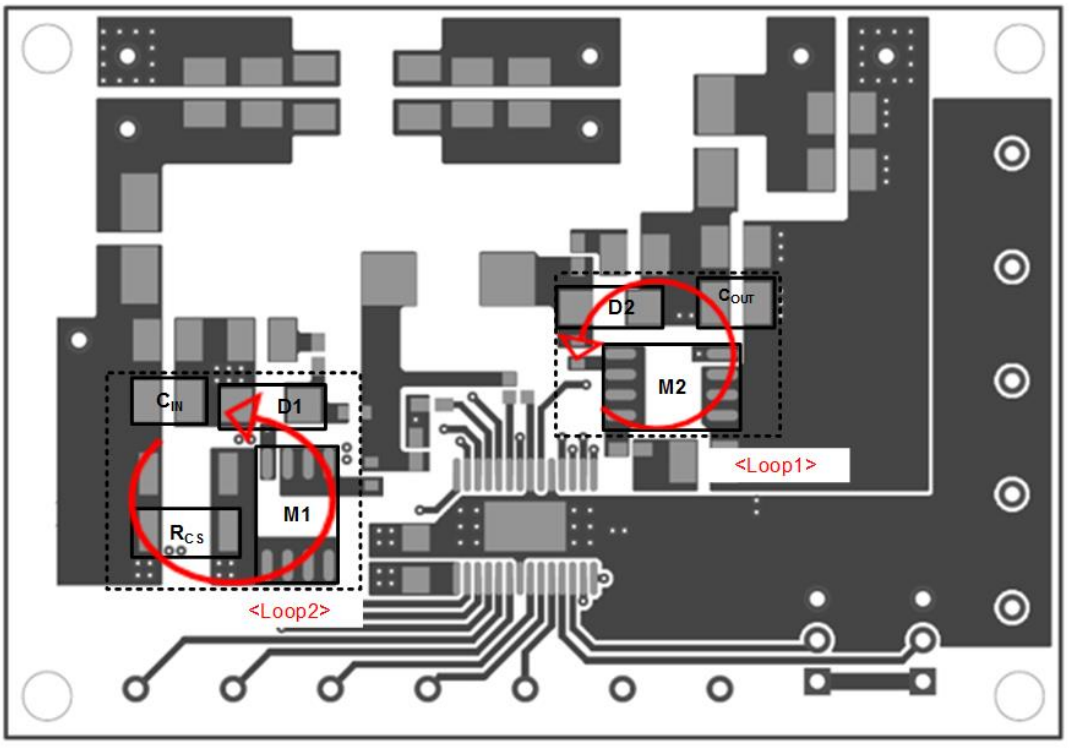


Figure 24. BD81A44EFV-M PCB TOP-layer

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Calculation Example of Power Consumption (Case of Buck-Boost application)

$$P_C = I_{CC} \times VCC \quad \cdots (1) \text{ Circuit Power}$$
$$+ C_{ISS1} \times V_{VREG} \times f_{OSC} \times V_{VREG} \quad \cdots (2) \text{ External Boost FET Power}$$
$$+ C_{ISS2} \times V_{VREG} \times f_{OSC} \times V_{VREG} \quad \cdots (3) \text{ External Buck FET Power}$$
$$+ \{V_{LED} \times M + \Delta Vf \times N \times (M-1)\} \times I_{LED} \quad \cdots (4) \text{ Current Driver Power}$$

where:

P_C	is the IC power consumption.
I_{CC}	is the circuit current.
VCC	is the supply voltage.
C_{ISS1}	is the External boost FET gate capacity.
C_{ISS2}	is the External buck FET gate capacity.
V_{VREG}	is the VREG voltage.
f_{OSC}	is the switching frequency.
V_{LED}	is the LED control voltage.
I_{LED}	is the LED output current.
M	is the LED parallel number.
ΔVf	is the LED Vf tolerance of each strings.
N	is the LED series number.

<Sample Calculation>

I_{CC} = 10 mA, VCC = 12 V, C_{ISS1} = 2000 pF, C_{ISS2} = 2000 pF, V_{VREG} = 5 V, f_{OSC} = 2200 kHz, V_{LED} = 1 V, I_{LED} = 50 mA, M = 4, ΔVf = 0.1 V, N = 5

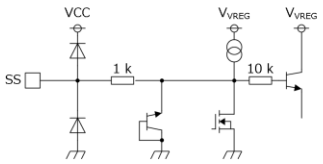
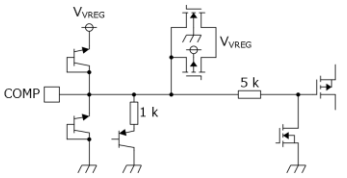
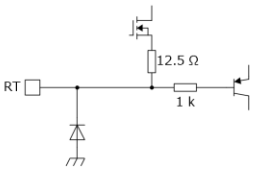
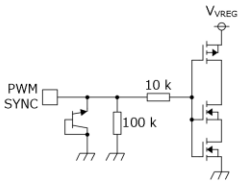
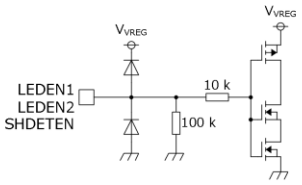
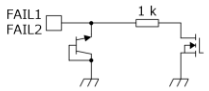
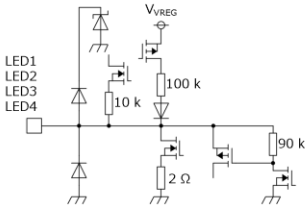
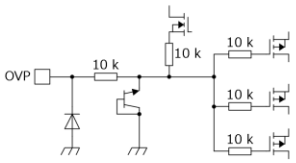
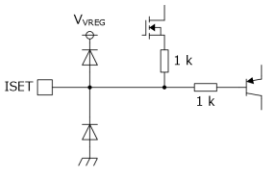
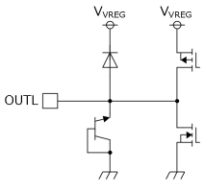
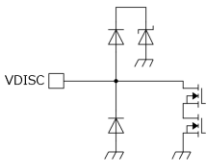
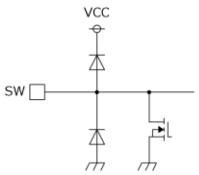
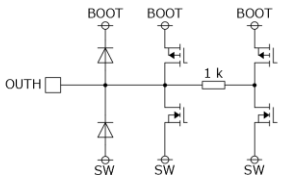
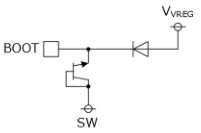
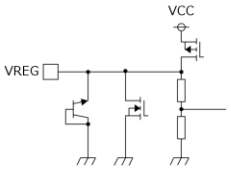
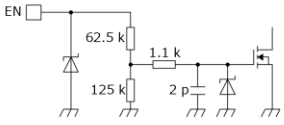
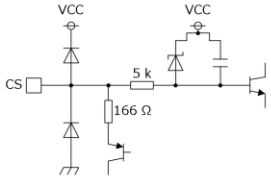
$$P_C = 10\ mA \times 12\ V$$
$$+ 2000\ pF \times 5\ V \times 2200\ kHz \times 5\ V$$
$$+ 2000\ pF \times 5\ V \times 2200\ kHz \times 5\ V$$
$$+ \{1.0 \times 4 + 0.1 \times 5 \times (4-1)\} \times 50\ mA = 0.615 \quad [W]$$

The above is a simple calculation and the value may differ from the actual value.

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I/O Equivalence Circuit

SS	COMP	RT
		
SYNC, PWM	**SHDETEN, LEDEN1, LEDEN2**	**FAIL1, FAIL2**
		
LED1, LED2, LED3, LED4	**OVP**	**ISET**
		
OUTL	**VDISC**	**SW**
		
OUTH	**BOOT**	**VREG**
		
EN	**CS**	
		

*All values are Typ value

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Operational Notes

1. Reverse Connection of Power Supply
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage
   Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes - continued

9. Unused Input Pins

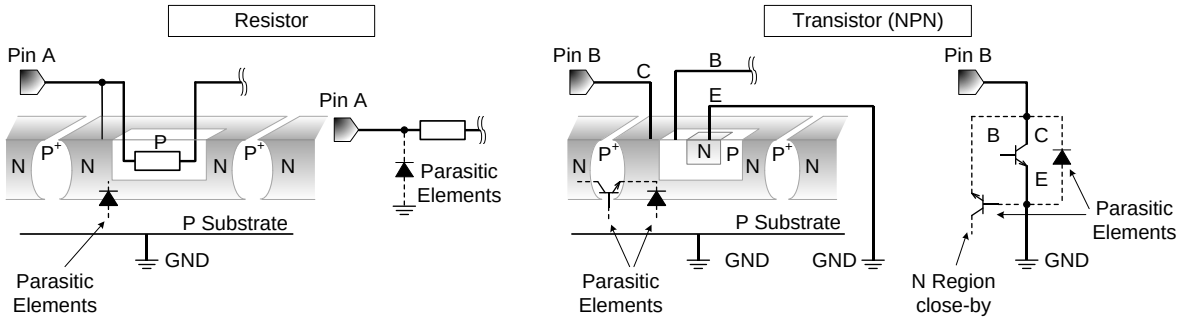
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause



these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

Figure 25. Example of monolithic IC structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

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Operational Notes - continued

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

B D 8 1 A 4 4 E F V	-	M E 2

Package
EFV: HTSSOP-B28

Product Rank
M: for Automotive
Packaging and forming specification
E2: Embossed carrier tape

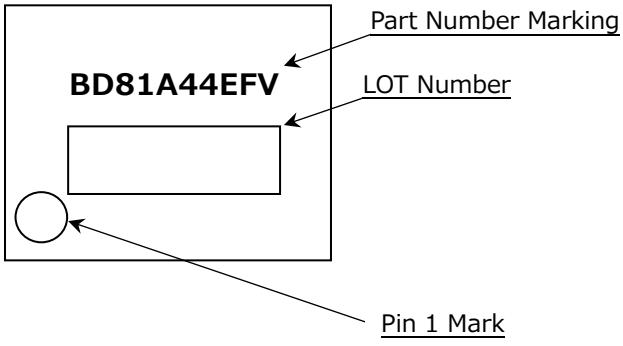
B D 8 1 A 4 4 M U V	-	M E 2

Package
MUV: VQFN28SV5050

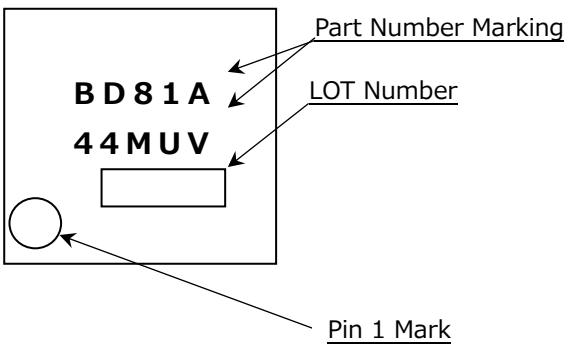
Product Rank
M: for Automotive
Packaging and forming specification
E2: Embossed carrier tape

Marking Diagram

HTSSOP-B28 (TOP VIEW)



VQFN28SV5050 (TOP VIEW)



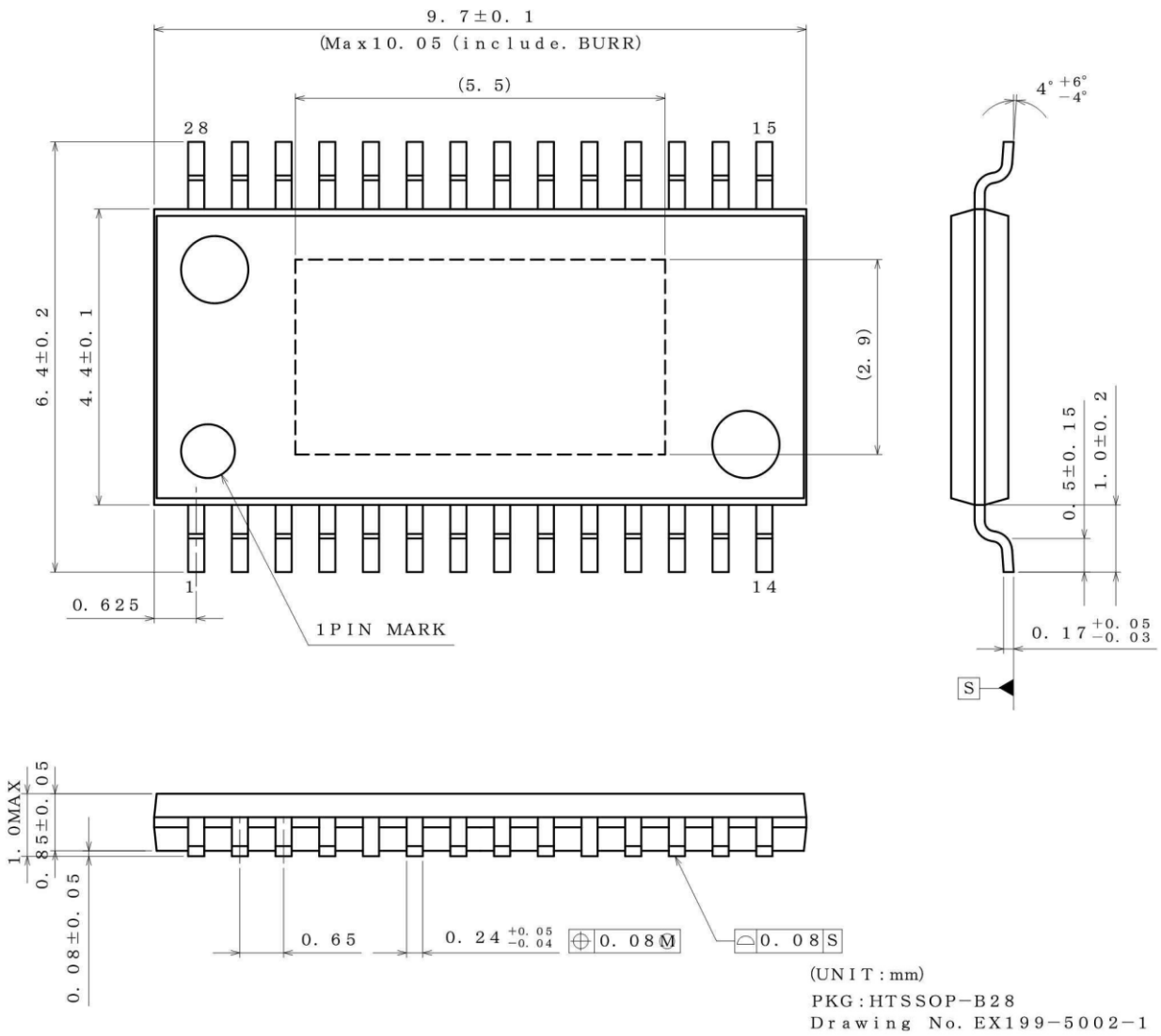
Marking	Package	Orderable Part Number
BD81A44EFV	HTSSOP-B28	BD81A44EFV-ME2
BD81A44MUV	VQFN28SV5050	BD81A44MUV-ME2

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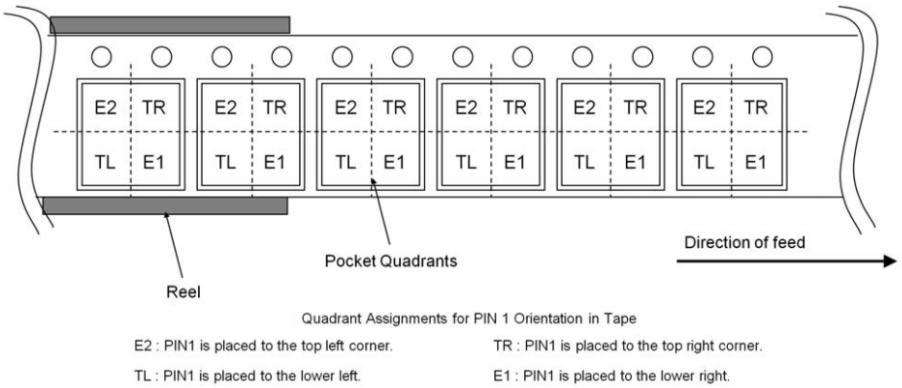
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Physical Dimension and Packing Information

Package Name	HTSSOP-B28



Packing Information	
Packing Form	Embossed carrier tape
Quantity	2500 pcs
Direction of feed	E2



Quadrant Assignments for PIN 1 Orientation in Tape

E2 : PIN1 is placed to the top left corner. TR : PIN1 is placed to the top right corner.

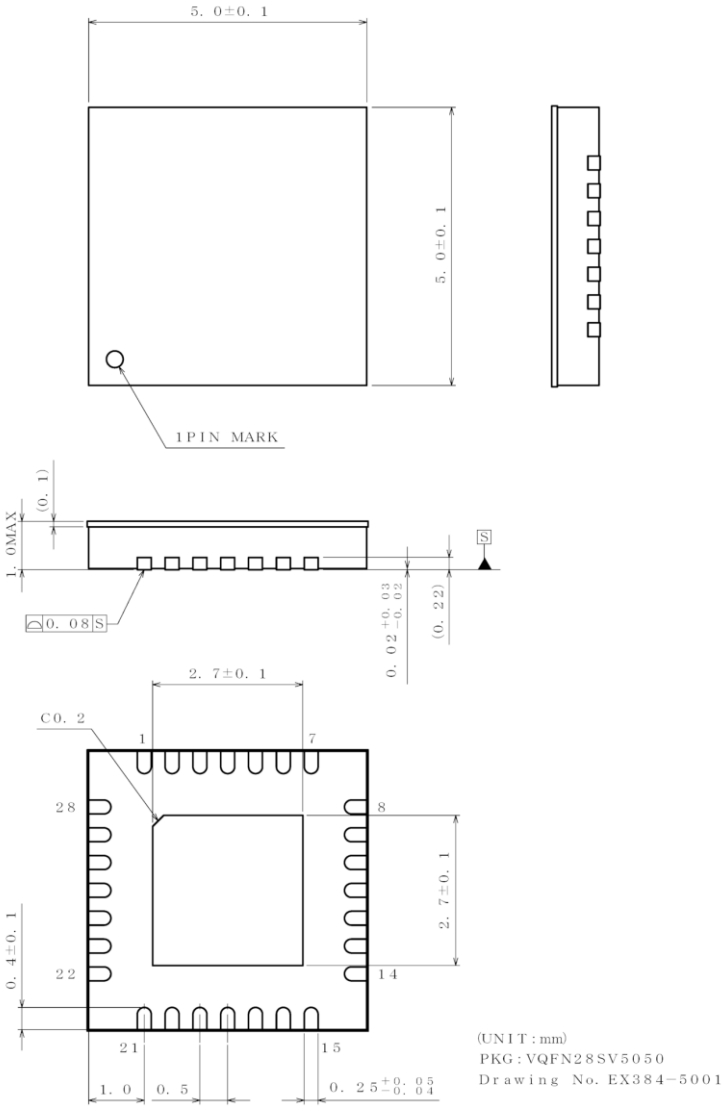
TL : PIN1 is placed to the lower left. E1 : PIN1 is placed to the lower right.

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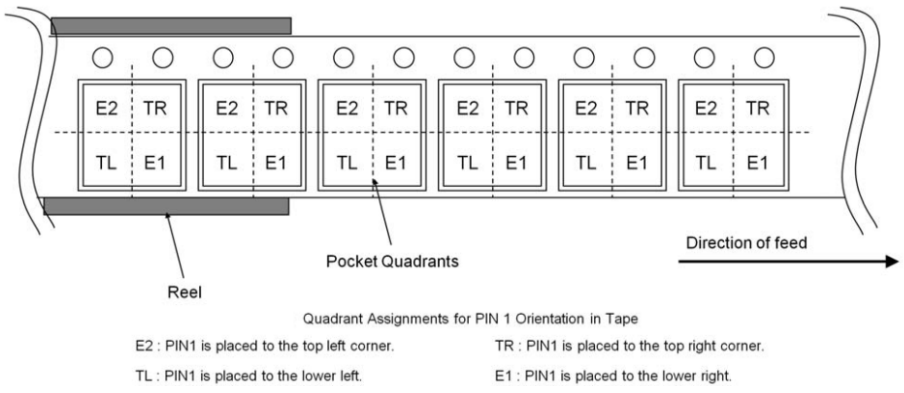
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Physical Dimension and Packing Information - continued

Package Name	VQFN28SV5050



Packing Information	
Packing Form	Embossed carrier tape
Quantity	2500 pcs
Direction of feed	E2



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Revision History

Date	Revision	Details
13.Jan.2016	001	New Release
26.Apr.2016	002	P.9 Absolute Maximum Ratings PWM, SYNC and EN terminal. Before : -0.3 to +7 < VCC After : -0.3 to +7 P.10 Thermal Resistance 2 internal layers / Copper Pattern, Bottom / Copper Pattern Before : 74.2mm2(Square) After : 74.2mm x 74.2mm P.29 I/O Equivalence Circuit Change RT, OUTL, OUTH and EN terminal.
19.Oct.2016	003	P.12 Change the PWM Frequency Limit Max value 15kHz to 20kHz.
25.Oct.2017	004	P.1 General Description Change to “Light modulation (10,000:1@100Hz dimming function) is possible by PWM input.” P.1 Features Change to “10,000:1 PWM dimming @100Hz”. P.12 PWM Minimum Pulse Width, Conditions Change to “fPWM=100Hz to 20kHz”. P.12 PWM Frequency, Min Change to “0.1kHz”.
29.Aug.2019	005	P.1 Add ○This product is protected by U.S. Patent No.7,235,954, No.7,541,785, No.7,944,189. P.5 Add <Caution of Large LED Current Setting> P.8 Add “(7) DC/DC Switching Control at Over Voltage Output (LSDET)” P.8 Add “(8) PWM Pulse and DC/DC Switching” P.18 1. Add sentence,“When VOVP at the time of the start is 0.57V or less, pre-boost function is effective.” P.29 Add “<Attention at the OVP Voltage Setting>”.All pages change the format to BD81A74MUV-M, BD81A74EFV-M.

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Revision History - continued

Date	Revision	Details
17.Oct.2019	006	P.1 Features Change “Spread Spectrum Function” to “10,000:1 PWM dimming @100Hz”.
11.Sep.2020	007	Format update Formula update Added Figure and calculation. Added the following sentence to the description of "PCB Application Circuit Diagram" When PWM min pulse width satisfies the following formula, please do not connect a capacitor to LED1 to LED4 pins. It might misdetect LED short protection. When the connection of the capacitor is necessary for noise measures, please refer to us. $t_{MIN} \leq 10/f_{OSC}$ t_{MIN} : PWM min pulse width f_{OSC} : DCDC frequency target Change about "Selection of Components Externally Connected"/"Setting of Over Current Protection Value (I_{OCP})" (Before) V_{OCP_MIN} is the overcurrent protection detect voltage (0.17 V). (After) V_{OCP_MIN} is the overcurrent protection detect voltage (0.18 V). Added the following sentence to "Selection of Components Externally Connected"/"Confirmation of Actual Operation" It is basically non-recommended to connect a capacitor to the LED1 to LED4 pins. Please refer to PCB Application Circuit. When the connection of the capacitor is necessary for noise measures, please refer to us.
12.Feb.2021	008	P.7 Figure 4 X axis name Before : R_{RT} [Ω] After : R_{RT} [kΩ]

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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