MP2452

1A, 36V, 1MHz Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP2452 is a high frequency (1MHz) step-down switching regulator with integrated internal high-side high voltage power MOSFET. It provides up to 1A highly efficient output current with current mode control for fast loop response.

The wide 3.3V to 36V input range accommodates a variety of step-down applications in automotive input environment. A 3μA shutdown mode quiescent current allows use in battery-powered applications.

High power conversion efficiency over a wide load range is achieved by scaling down the switching frequency at light load condition to reduce the switching and gate driving losses.

Frequency fold-back helps prevent inductor current runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation.

The MP2452 is available in the 2mm x 3mm QFN8 package.

FEATURES

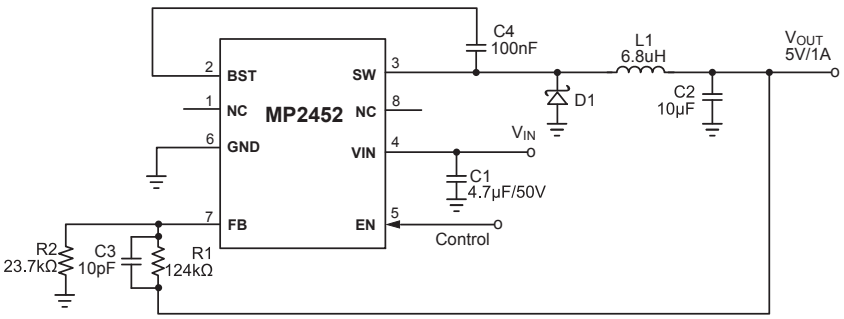
- 1A Continuous Load Current
- 130 μA Operating Quiescent Current
- Wide 3.3V to 36V Operating Input Range
- 500 mΩ Internal Power MOSFET
- 1MHz fixed Switching Frequency
- Internally compensated
- Stable with Ceramic Output Capacitors
- Internal Soft-Start
- > 90% Efficiency
- +0.794V FB Reference Voltage
- Output Adjustable from +0.794V to 33V
- 3μA Low Shutdown Supply Current
- 2mm x 3mm QFN8 Package

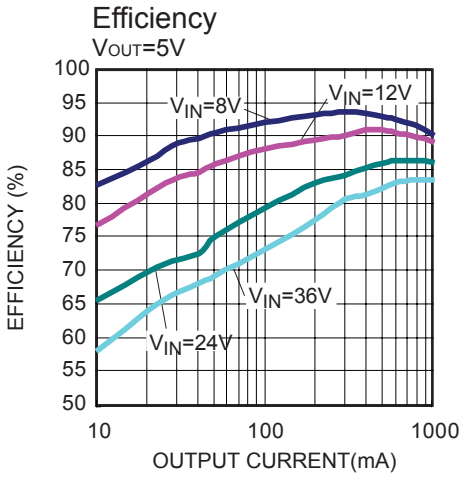
APPLICATIONS

- High Voltage Power Conversion
- Automotive Systems
- Industrial Power Systems
- Distributed Power Systems
- Battery Powered Systems

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TYPICAL APPLICATION





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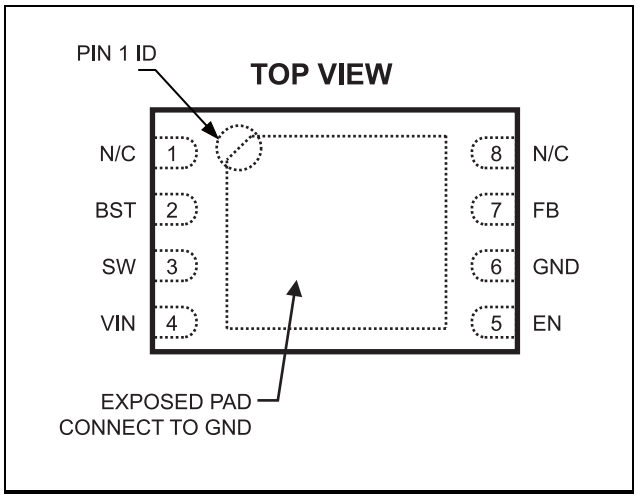
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ORDERING INFORMATION

Part Number*	Package	Top Marking	Temperature
MP2452DD	QFN8(2mm x 3mm)	5F	–40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP2452DD–Z).
For RoHS compliant packaging, add suffix –LF (e.g. MP2452DD–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage (V_{IN}).....–0.3V to 40V
Switch Voltage (V_{SW}).....–0.3V to V_{IN}+0.3V
BST to SW .....-0.3 to 5.0V
All Other Pins .....–0.3V to 5.0V
Continuous Power Dissipation (T_A = +25°C) (2)
.....2.3W
Junction Temperature .....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to 150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} .....3.3V to 36V
Output Voltage V_{OUT}.....+0.794V to 33V
Operating Temperature..... –40°C to +85°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN8(2mmx3mm) .....55 ..... 12 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_A= 25°C, unless otherwise noted.

Parameter	Condition	Min	Typ	Max	Units
Feedback Voltage	4.0V < V_{IN} < 36V	0.778	0.794	0.810	V
	3.3V < V_{IN} < 4.0V	0.770	0.794	0.818	V
Upper Switch On Resistance	V_{BST}-V_{SW}=5V		500		mΩ
Upper Switch Leakage	V_{EN} = 0V, V_{SW} = 0V		0.1	1	μA
Current Limit		1.2	1.5		A
VIN UVLO Up Threshold		2.7	3.0	3.2	V
VIN UVLO Hysteresis			0.4		V
Soft-start time	FB from 0 to 0.794V		0.5		ms
Oscillator Frequency		800	1000	1200	kHz
Minimum Switch On Time			100		ns
Shutdown Supply Current	V_{EN} = 0V		3	15	μA
Average Quiescent Supply Current	No load, Not switching, V_{FB}=0.9		130		μA
	No load, Switching		220		μA
Thermal Shutdown			150		°C
Enable Up Threshold		1.2	1.5	1.8	V
Enable Threshold Hysteresis			0.3		V

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PIN FUNCTIONS

Pin #	Name	Description
2	BST	Bootstrap. This is the positive power supply for the internal floating high side MOSFET driver. Connect a bypass capacitor between this pin and SW pin.
6	GND, EXPOSED PAD	Ground. Connected GND as close as possible to the output capacitor avoiding the high current switch paths. Connect exposed pad to GND plane
7	FB	Feedback. This is the input to the error amplifier. An external resistive divider connected between the output and GND is compared to the internal +0.794V reference to set the regulation voltage.
5	EN	Enable input. Pulling this pin below the specified threshold shuts the chip down. Pulling it above the specified threshold enables the chip. Floating this pin shuts the chip down.
4	VIN	Input Supply. This supplies power to all the internal control circuitry, both BS regulators and the high side switch. Connect a decoupling capacitor to ground close to this pin as possible to reduce switching spikes.
3	SW	Switch node. This is the output from the high-side switch. Connect a low V_F Schottky diode to ground close to this pin as possible to reduce switching spikes.
1, 8	N/C	No connect.

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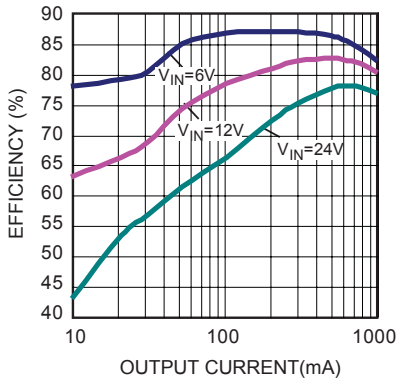
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TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, C1 = 4.7µF, C2 = 10µF, L = 6.8µH and T_A = +25°C, unless otherwise noted.

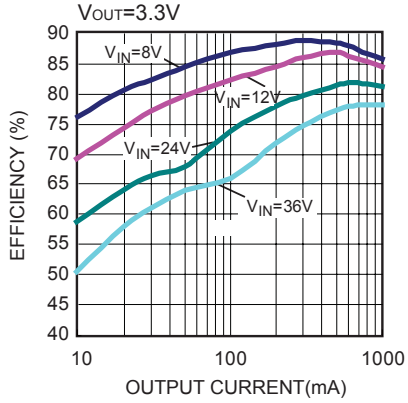
Efficiency

V_{OUT}=2.5V

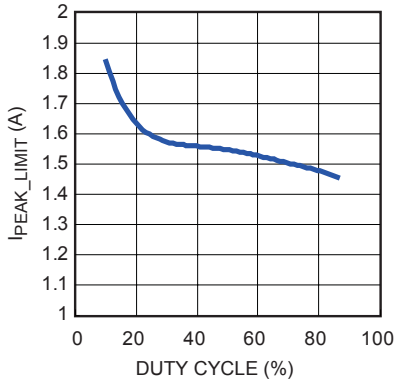


Efficiency

V_{OUT}=3.3V

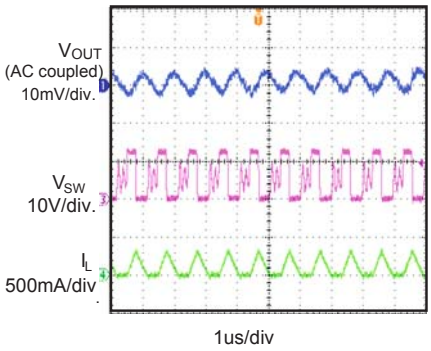


Current Limit vs. Duty Cycle



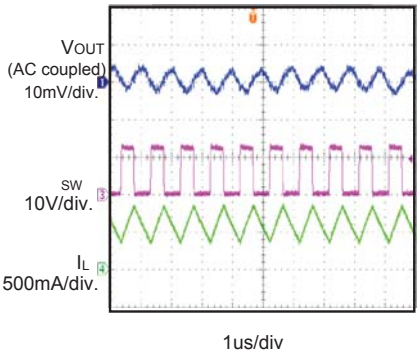
Steady State

V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0.1A



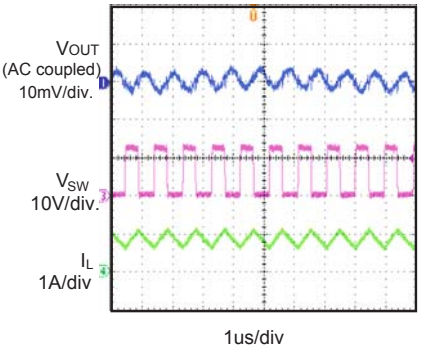
Steady State

V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0.6A



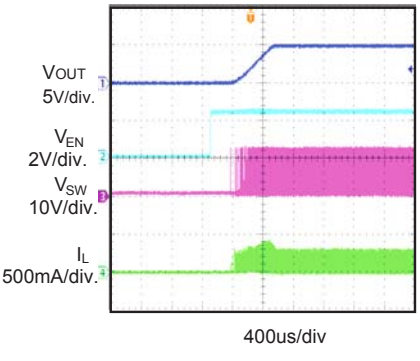
Steady State

V_{IN}=12V,V_{OUT}=5V,I_{OUT}=1A



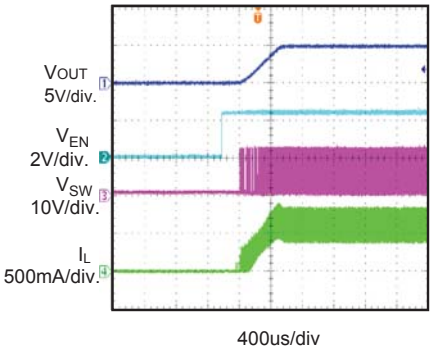
Startup Through EN

V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0.1A



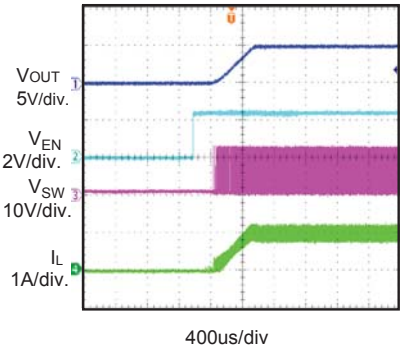
Startup Through EN

V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0.6A



Startup Through EN

V_{IN}=12V,V_{OUT}=5V,I_{OUT}=1A



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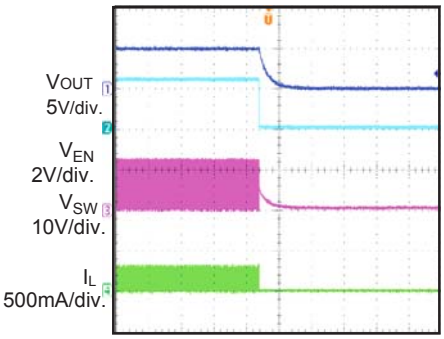
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, C1 = 4.7µF, C2 = 10µF, L = 6.8µH and T_A = +25°C, unless otherwise noted.

Shutdown Through EN

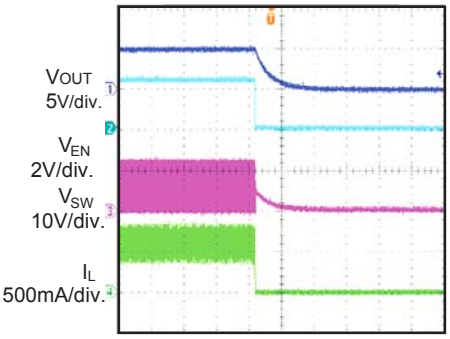
V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0.1A



2ms/div

Shutdown Through EN

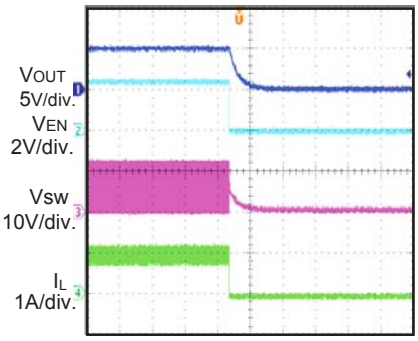
V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0.6A



200us/div

Shutdown Through EN

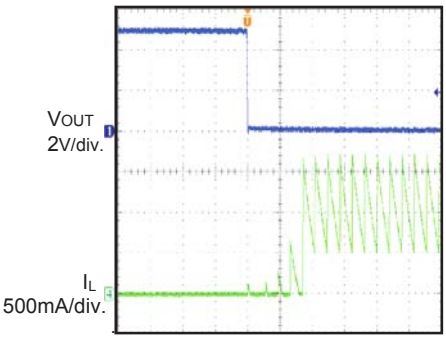
V_{IN}=12V,V_{OUT}=5V,I_{OUT}=1A



200us/div

Short Circuit Entry

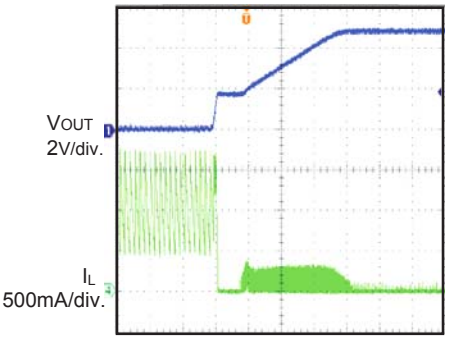
I_{OUT}=0A to Short



40us/div

Short Circuit Recovery

I_{OUT}= Short to 0A



100us/div

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FUNCTION BLOCK DIAGRAM

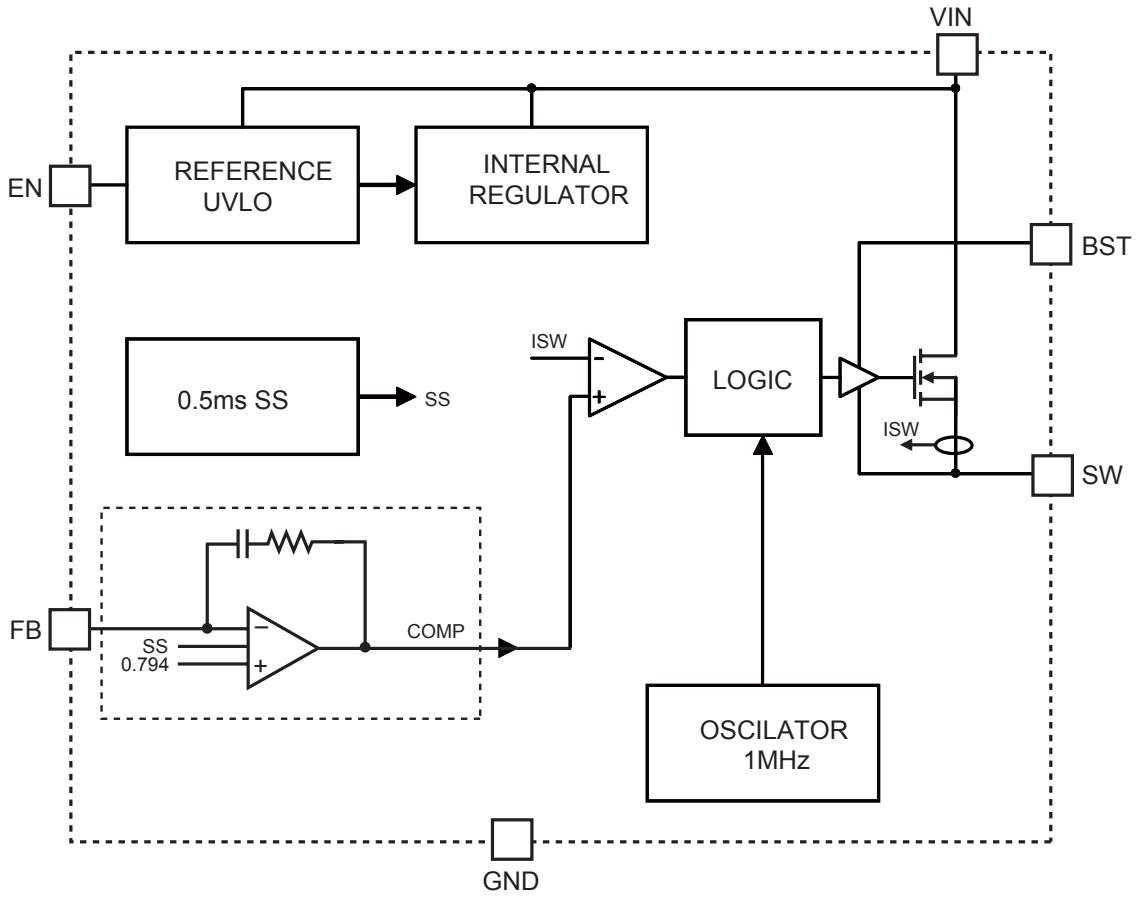


Figure 1—Function Block Diagram

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OPERATION

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The MP2452 is a 1MHz, non-synchronous, step-down switching regulator with integrated internal high-side high voltage power MOSFET. It provides internally compensated single 1A output with current mode control. It features wide input voltage range, internal soft-start control, and precision current limit. Its very low operational quiescent current suits it for battery powered applications.

PWM Control

At moderate to high output current, the MP2452 operates in a fixed frequency, peak current control mode to regulate the output voltage. A PWM cycle is initiated by the internal clock. The power MOSFET is turned on and remains on until its current reaches the value set by COMP voltage. When the power switch is off, it remains off for at least 100ns before the next cycle starts
If, in one PWM period, the current in the power MOSFET does not reach COMP set current value, the power MOSFET remains on, saving a turn-off operation.

Pulse Skipping Mode

At light load condition, the MP2452 goes into pulse skipping mode to improve light load efficiency. Pulse skipping decision is based on its internal COMP voltage. If COMP is lower than the internal sleep threshold, a PAUSE command is generated to block the turn-on clock pulse so the power MOSFET is not commanded ON subsequently, saving gate driving and switching losses. This PAUSE command also puts the whole chip into sleep mode, consuming very low quiescent current to further improve the light load efficiency.

When COMP voltage is higher than the sleep threshold, the PAUSE signal is reset so the chip is back into normal PWM operation. Every time when the PAUSE changes states from low to high, a turn-on signal is generated right away, turning on the power MOSFET.

Error Amplifier

The Error amplifier is composed of an internal OP-AMP with an R-C feedback network connected between its output node (internal COMP node) and its negative input node (FB). When FB is lower than its internal reference voltage (REF), the COMP output is then driven higher by the OP-AMP, causing higher switch peak current output hence more energy delivered to the output. Vise versus.

When connecting to the FB pin, normally there is a voltage divider composed of R_1 and R_2 where R_2 is between FB and GND while R_1 is between the voltage output node and FB. R_1 serves also to control the gain of the error amplifier along with the internal compensation R-C network.

Internal Regulator

Most of the internal circuitries are powered on by the 2.6V internal regulator. This regulator takes VIN input and operates in the full VIN range. When VIN is greater than 3.0V, the output of the regulator is in full regulation. When VIN is lower, the output degrades.

Enable Control

The MP2452 has a dedicated enable control pin EN. When VIN>UVLO, the chip can be enabled and disabled by EN pin. This is a HIGH effective logic. Its trailing threshold is a consistent 1.2V. Its rising threshold is about 300mV higher. When floating, EN pin is internally pulled down to GND so the chip is disabled.

When EN is pulled down to 0V, the chip is put into the lowest shutdown current mode. When EN is higher than zero but lower than its rising threshold, the chip is still in shutdown mode but the shutdown current increases slightly.

Under Voltage Lockout (UVLO)

VIN Under voltage lockout (UVLO) is implemented to protect the chip from operating at insufficient supply voltage. The UVLO rising threshold is about 3.0V while its trailing threshold is a consistent 2.6V.

Internal Soft-start

Reference type soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V at a slow pace set by the soft-start time. When it is lower than the internal reference REF, SS overrides the REF so the error amplifier uses SS instead of REF as the reference. When SS is higher than REF, REF gains the control back.

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SS is also associated with FB. Though SS can be much lower than FB, it can only be slightly higher than FB. If somehow FB is brought down, SS follows to track FB. This function is designed to accommodate the short-circuit recovery situation. When a short-circuit is removed, the SS ramps up as if it is a fresh soft-start process. This prevents output voltage overshoot.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from thermally running away. When the silicon die temperature is higher than its upper threshold, it shuts down the whole chip. When the temperature is lower than its lower threshold, thermal shutdown is gone so the chip is enabled again.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection. This UVLO's rising threshold is about 2.4V with a hysteresis of about 300mV. During this UVLO, the SS voltage of the controller is reset to zero. When the UVLO is removed, the controller follows soft-start process.

The bootstrap capacitor is charged and regulated to about 5V by the dedicated internal bootstrap regulator. When the voltage between BST and SW nodes is lower than its regulation, a PMOS pass transistor connected from VIN to BST is turned on. The charging current path is from VIN, BST and then to SW. External circuit should provide enough voltage headroom to facilitate the charging.

As long as VIN is sufficiently higher than SW, the bootstrap capacitor can be charged. When the power MOSFET is ON, VIN is about equal to SW so the bootstrap capacitor cannot be charged. When the external free wheeling diode is on, VIN to SW difference is the largest so it is the best period to charge. When there is no current in the inductor, SW equals to the output voltage VOUT so the difference between VIN and VOUT can be used to charge the bootstrap capacitor.

At higher duty cycle operation condition, the time period available to the bootstrap charging is less so the bootstrap capacitor may not be charged sufficiently.

In case the external circuit has not sufficient voltage and time to charge the bootstrap capacitor, extra external circuitry can be used to ensure the bootstrap voltage in normal operation region.

The floating driver's UVLO is not communicated to the controller.

The DC quiescent current of the floating driver is about 20uA. Make sure the bleeding current at SW node is at least higher than this number.

Current Comparator and Current Limit

The power MOSFET current is accurately sensed via a current sense MOSFET. It is then fed to the high speed current comparator for the current mode control purpose. The current comparator takes this sensed current as one of its inputs. When the power MOSFET is turned on, the comparator is first blanked till the end of the turn-on transition to dodge the noise. Then, the comparator compares the power switch current with COMP voltage. When the sensed current is higher than COMP voltage, the comparator outputs low, turning off the power MOSFET. The maximum current of the internal power MOSFET is internally limited cycle by cycle.

Startup and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents and then the internal regulator is enabled. The regulator provides stable supply for the rest circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET OFF for about 50us to blank the startup glitches. When the internal soft-start block is enabled, it first holds its SS output low to ensure the rest circuitries are ready and then slowly ramps up.

Three events shut down the chip: EN low, VIN low, thermal shutdown. In the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. COMP voltage and the internal supply rail are pulled down then. The floating driver is not subject to this shutdown command but its charging path is disabled.

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APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to FB pin. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = V_{OUT} \frac{R2}{R1 + R2}$$

Thus the output voltage is:

$$V_{OUT} = V_{FB} \frac{(R1 + R2)}{R2}$$

The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor.

Choose R1 around 124kΩ for optimal transient response. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.794V} - 1}$$

Table 1—Resistor Selection vs. Output Voltage Setting

V_{OUT}	R1	R2
0.8V	124kΩ (1%)	NS
1.2V	124kΩ (1%)	243kΩ (1%)
3.3V	124kΩ (1%)	39.2kΩ (1%)
5V	124kΩ (1%)	23.7kΩ (1%)

Inductor

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current.

Generally, a good rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum load current. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L1 = \frac{V_{OUT}}{f_S \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_S is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_S \times L1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where I_{LOAD} is the load current.

Table 2 lists a number of suitable inductors from various manufacturers. The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI requirement.

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Table 2—Inductor Selection Guide

Part Number	Inductance (µH)	Max DCR (Ω)	Current Rating (A)	Dimensions L x W x H (mm^3)
Wurth Electronics				
744062003	3.3	0.032	2.8	6.8x6.8x2.3
7447789004	4.7	0.035	2.9	7.3x7.3x3.2
7447789006	6.8	0.044	2.5	7.3x7.3x3.2
744065100	10	0.053	3	10x10x2.8
744066150	15	0.05	3.2	10x10x3.8
TOKO				
D73CB-#636CY-3R3M	3.3	0.035	2.26	7.6x7.6x3.5
DS75LC-B1047AS -4R7N	4.7	0.026	3.5	7.6x7.6x5.0
DS75LC-B1047AS-6R8N	6.8	0.036	2.9	7.6x7.6x5.0
DS75LC-B1047AS -100M	10	0.053	2.3	7.6x7.6x5.0
DS85LC-B1000AS-150M	15	0.077	2.1	8.4x8.3x5.0

Input Capacitor

The input capacitor (C1) can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1µF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system.

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Compensation Components

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause system unstable. A good rule of thumb is to set the crossover frequency to approximately one-tenth of the switching frequency. If an electrolytic capacitor is used, the loop bandwidth is no higher than 1/4 of the ESR zero frequency (f_{ESR}). f_{ESR} is given by:

$$f_{ESR} = \frac{1}{2\pi \times C2 \times R_{ESR}}$$

The Table 3 lists the typical values of compensation components for some standard output voltages with various output capacitors (ceramic) and inductors. The values of the compensation components have been optimized for fast transient responses and good stability at given conditions.

Table 3—Compensation Values for Typical Output Voltage/Capacitor Combinations

V_{OUT} (V)	L (μH)	C2 (μF)	R2 (kΩ)	C3 (pF)
1.2	3.3	10	243	6.8
2.5	4.7	10	57.6	6.8
3.3	4.7	10	39.2	10
5	6.8	10	23.7	10
12	10~15	10	8.87	10

Note:

With the compensation, the control loop has the bandwidth at about 1/10 switching frequency and the phase margin higher than 45 degree.

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator. In below cases, an external BST diode is recommended from the 5V to BST pin:

- There is a 5V rail available in the system;
- V_{IN} is no greater than 5V;
- V_{OUT} is between 3.3V and 5V;

This diode is also recommended for high duty cycle operation (when V_{OUT} / V_{IN} > 65%) applications.

The bootstrap diode can be a low cost one such as IN4148 or BAT54.

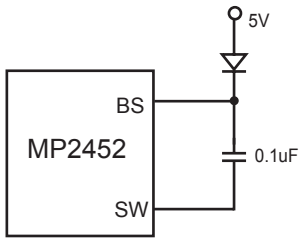


Figure 2—External Bootstrap Diode

At no load or light load, the converter may operate in pulse skipping mode in order to maintain the output voltage in regulation. Thus there is less time to refresh the BS voltage. In order to have enough gate voltage under such operating conditions, the difference of V_{IN} –V_{OUT} should be greater than 3V. For example, if the V_{OUT} is set to 3.3V, the V_{IN} needs to be higher than 3.3V+3V=6.3V to maintain enough BS voltage at no load or light load. To meet this requirement, EN pin can be used to program the input UVLO voltage to Vout+3V.

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TYPICAL APPLICATION CIRCUITS

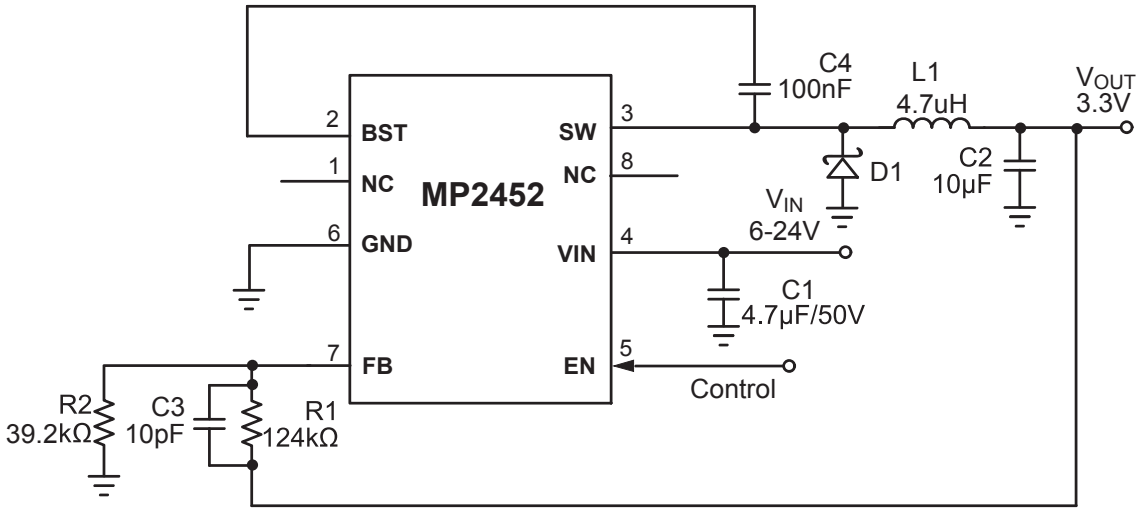


Figure 3—3.3V Output Typical Application Schematic

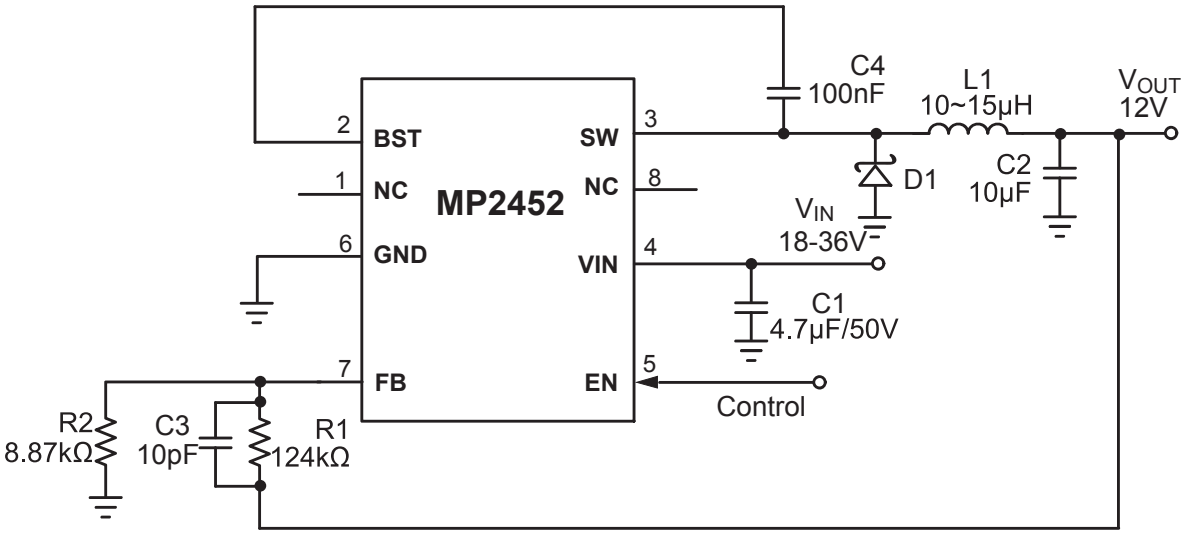


Figure 4—12V Output Typical Application Schematic

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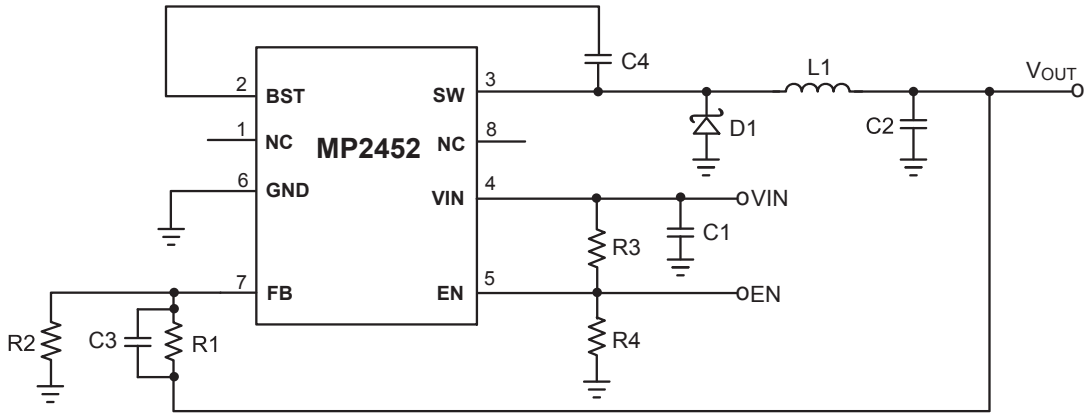
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PCB LAYOUT

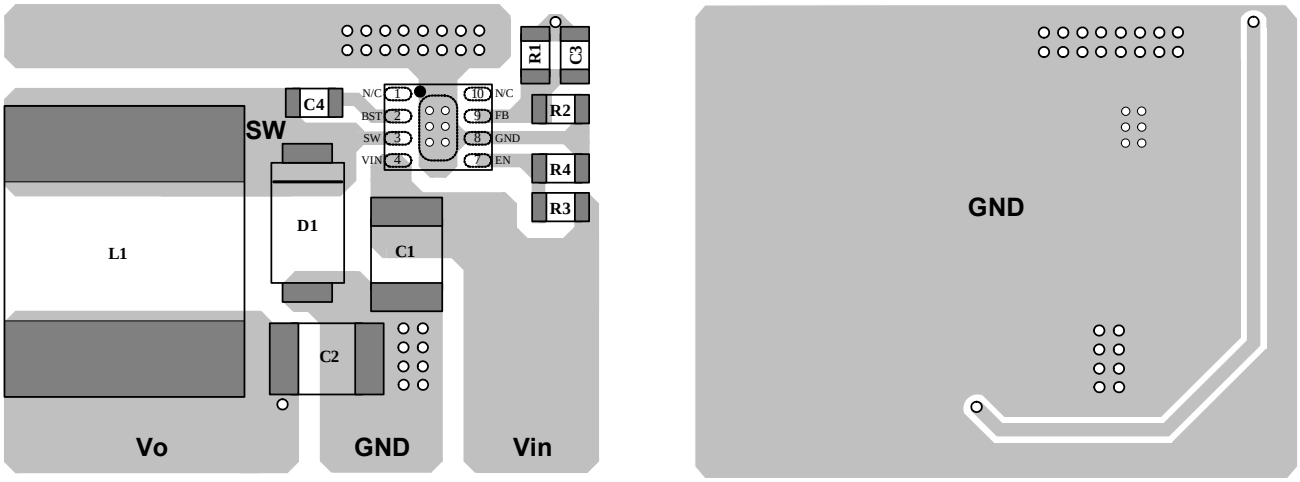
PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance.

If change is necessary, please follow these guidelines and take figure 5 for reference.

1) Keep the path of switching current short and minimize the loop area formed by Input cap, high-side MOSFET and external switching diode.
2) Bypass ceramic capacitors are suggested to be put close to the Vin Pin.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) Route SW away from sensitive analog areas such as FB.
5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.



MP2452 Typical Application Circuit



Top Layer **Bottom Layer**

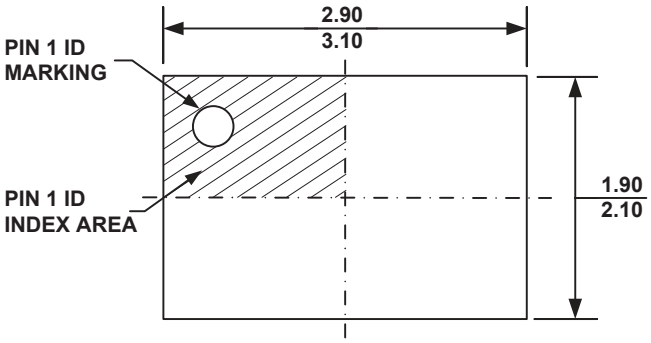
Figure 5—Typical Application Circuit and PCB Layout Guide (Double Layers)

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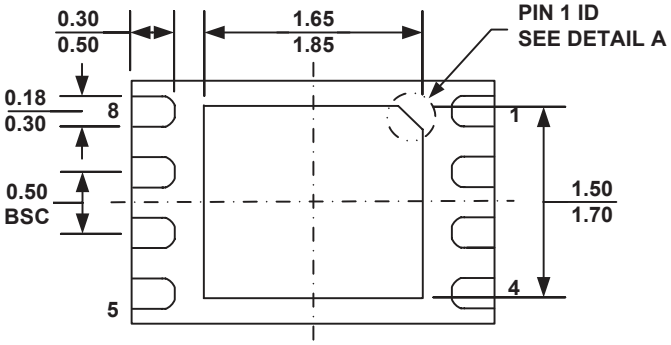
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PACKAGE INFORMATION

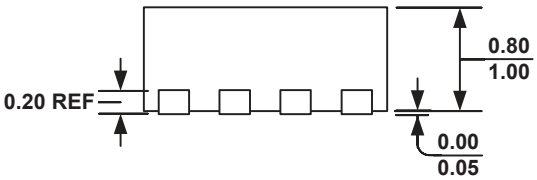
QFN (2mm x 3mm)



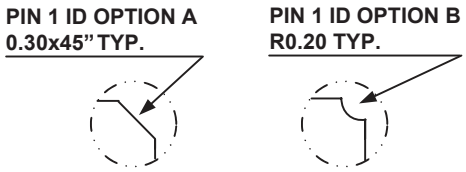
TOP VIEW



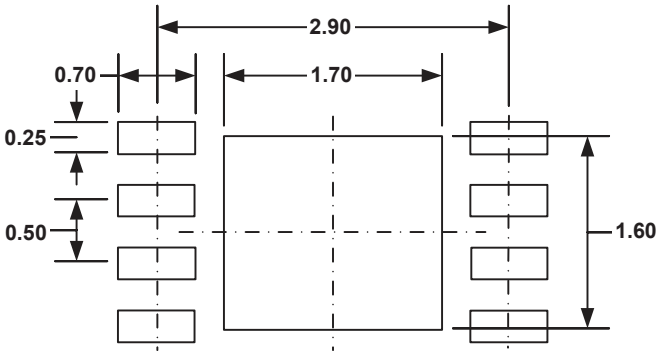
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VCED-2.
5) DRAWING IS NOT TO SCALE.

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