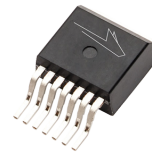
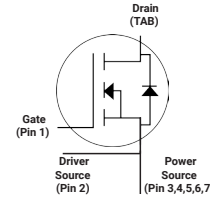


# C3M0025065J1

Silicon Carbide Power MOSFET  
C3M™ MOSFET Technology  
N-Channel Enhancement Mode



TO-263-7L XL



Package Types: TO-263-7L XL  
PN's: C3M0025065J1

## Features

- 3<sup>rd</sup> generation SiC MOSFET technology
- Optimized package with separate driver source pin
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery ( $Q_{rr}$ )
- Halogen free, RoHS compliant

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## Typical Applications

- Datacenter and telecom power supplies
- EV battery chargers
- High voltage DC/DC converters
- Energy storage systems
- Solar inverters

## Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

## Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	$V_{DS}$			650	V	$T_c = 25^\circ\text{C}$	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19		Transient	
Operational Gate-Source Voltage	$V_{GS op}$		-4/15			Static	Note 1
DC Continuous Drain Current	$I_D$			80	A	$V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}, T_J \leq 150^\circ\text{C}$	Fig. 19
				59		$V_{GS} = 15\text{ V}, T_c = 100^\circ\text{C}, T_J \leq 150^\circ\text{C}$	Note 2
Pulsed Drain Current	$I_{DM}$			251		$t_{pmax}$ limited by $T_{Jmax}$ $V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}$	Fig. 22
Power Dissipation	$P_D$			271	W	$T_c = 25^\circ\text{C}, T_J = 150^\circ\text{C}$	Fig. 20
Operating Junction Temperature	$T_J$			-40 to +175	$^\circ\text{C}$		
Case and Storage Temperature	$T_c, T_{stg}$			-40 to 150			
Solder Temperature	$T_L$			260		According to JEDEC J-STD-020	

Note (1): Recommended turn-on gate voltage is 15V with  $\pm 5\%$  regulation tolerance, see Application Note PRD-04814 for additional details

Note (2): Verified by design


**Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  Unless Otherwise Specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.3	3.6	V	$V_{DS} = V_{GS}, I_D = 9.22\text{ mA}$	Fig. 11
			2.0			$V_{DS} = V_{GS}, I_D = 9.22\text{ mA}, T_J = 150^\circ\text{C}$	
Zero Gate Voltage Drain Current	$I_{DSS}$		1	50	$\mu\text{A}$	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	
Gate-Source Leakage Current	$I_{GSS}$		10	250	nA	$V_{GS} = 15\text{ V}, V_{DS} = 0\text{ V}$	
Drain-Source On-State Resistance	$R_{DS(on)}$		25	34	m $\Omega$	$V_{GS} = 15\text{ V}, I_D = 33.5\text{ A}$	Fig. 4, 5, 6
			30			$V_{GS} = 15\text{ V}, I_D = 33.5\text{ A}, T_J = 150^\circ\text{C}$	
Transconductance	$g_{fs}$		25		S	$V_{DS} = 20\text{ V}, I_{DS} = 33.5\text{ A}$	Fig. 7
			24			$V_{DS} = 20\text{ V}, I_{DS} = 33.5\text{ A}, T_J = 150^\circ\text{C}$	
Input Capacitance	$C_{iss}$		2980		pF	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ V to } 400\text{ V}$ $F = 1\text{ Mhz}$ $V_{AC} = 25\text{ mV}$	Fig. 17, 18
Output Capacitance	$C_{oss}$		178				
Reverse Transfer Capacitance	$C_{rss}$		12				
Effective Output Capacitance (Energy Related)	$C_{o(er)}$		236			$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ V to } 400\text{ V}$	Note: 3
Effective Output Capacitance (Time Related)	$C_{o(tr)}$		340				Note: 3
$C_{oss}$ Stored Energy	$E_{oss}$		19		$\mu\text{J}$	$V_{DS} = 400\text{ V}, F = 1\text{ Mhz}$	Fig. 16
Turn-On Switching Energy (Body Diode)	$E_{ON}$		116		$\mu\text{J}$	$V_{DS} = 400\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}, I_D = 33.5\text{ A},$ $R_{G(ext)} = 2.5\text{ }\Omega, L = 59\text{ }\mu\text{H}, T_J = 25^\circ\text{C}$ FWD = Internal Body Diode of MOSFET	Fig. 25
Turn-Off Switching Energy (Body Diode)	$E_{OFF}$		59				
Turn-On Delay Time	$t_{d(on)}$		13		ns	$V_{DD} = 400\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}$ $I_D = 33.5\text{ A}, R_{G(ext)} = 2.5\text{ }\Omega, L = 59\text{ }\mu\text{H}$ Timing Relative to $V_{DS}$ Inductive Load	Fig. 26
Rise Time	$t_r$		20				
Turn-Off Delay Time	$t_{d(off)}$		25				
Fall Time	$t_f$		9				
Internal Gate Resistance	$R_{G(int)}$		1.3		$\Omega$	$F = 1\text{ Mhz}, V_{AC} = 25\text{ mV}$	
Gate to Source Charge	$Q_{gs}$		35		nC	$V_{DS} = 400\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}$ $I_D = 33.5\text{ A}$ Per IEC60747-8-4 pg 21	Fig. 12
Gate to Drain Charge	$Q_{gd}$		31				
Total Gate Charge	$Q_g$		109				

Note (3):  $C_{o(er)}$ , a lumped capacitance that gives same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400 V.

$C_{o(tr)}$ , a lumped capacitance that gives same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400 V.



## Reverse Diode Characteristics ( $T_c = 25\text{ }^\circ\text{C}$ Unless Otherwise Specified)

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Note
Diode Forward Voltage	$V_{SD}$	5.0		V	$V_{GS} = -4\text{ V}, I_{SD} = 16.8\text{ A}, T_J = 25\text{ }^\circ\text{C}$	Fig. 8, 9, 10
		4.5			$V_{GS} = -4\text{ V}, I_{SD} = 16.8\text{ A}, T_J = 150\text{ }^\circ\text{C}$	
Continuous Diode Forward Current	$I_S$		45	A	$V_{GS} = -4\text{ V}, T_c = 25\text{ }^\circ\text{C}$	
Diode Pulse Current	$I_{S, \text{pulse}}$		251		$V_{GS} = -4\text{ V}$ , Pulse Width $t_p$ Limited by $T_{Jmax}$	
Reverse Recovery Time	$t_{rr}$	13		ns	$V_{GS} = -4\text{ V}, I_{SD} = 33.5\text{ A}, V_R = 400\text{ V}$ $\text{dif}/\text{dt} = 5665\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	
Reverse Recovery Charge	$Q_{rr}$	274		nC		
Peak Reverse Recovery Current	$I_{rrm}$	37		A		
Reverse Recovery Time	$t_{rr}$	16		ns	$V_{GS} = -4\text{ V}, I_{SD} = 33.5\text{ A}, V_R = 400\text{ V}$ $\text{dif}/\text{dt} = 1630\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	
Reverse Recovery Charge	$Q_{rr}$	164		nC		
Peak Reverse Recovery Current	$I_{rrm}$	17		A		

## Thermal Characteristics

Parameter	Symbol	Typ.	Unit	Test Conditions	Note
Thermal Resistance from Junction to Case	$R_{\theta JC}$	0.46	$^\circ\text{C}/\text{W}$		Fig. 21
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	40			

Typical Performance

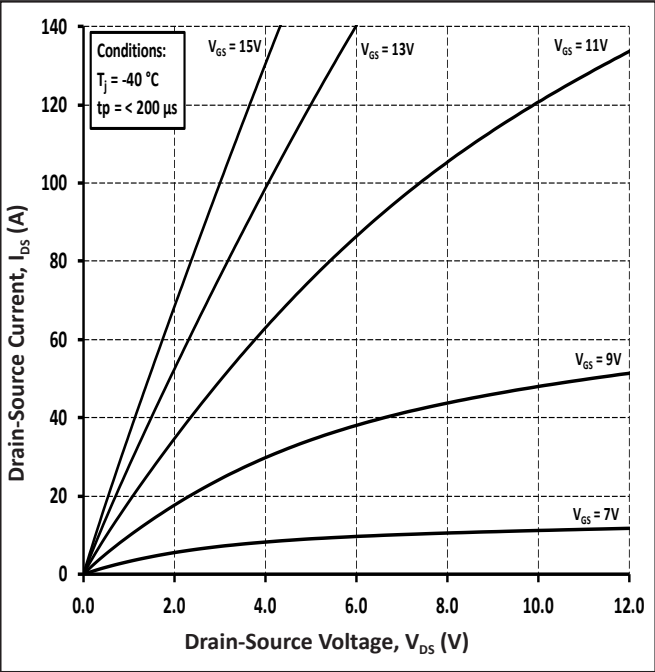


Figure 1. Output Characteristics  $T_j = -40\text{ }^{\circ}\text{C}$

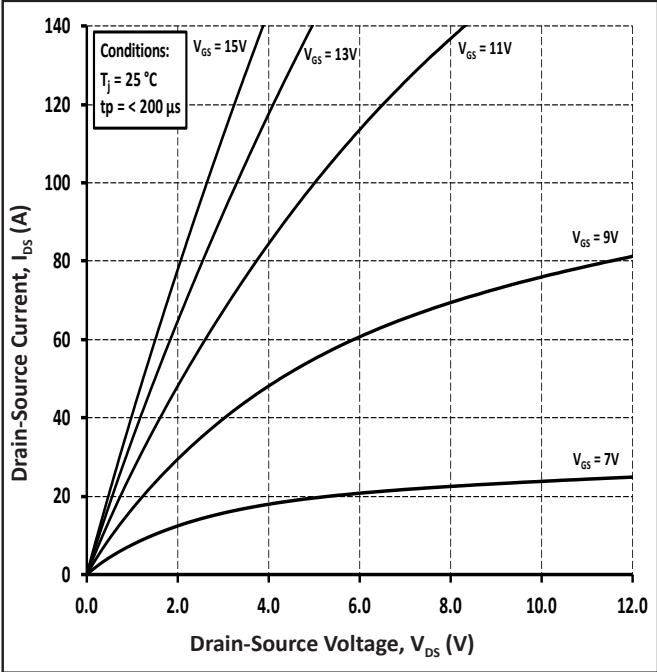


Figure 2. Output Characteristics  $T_j = 25\text{ }^{\circ}\text{C}$

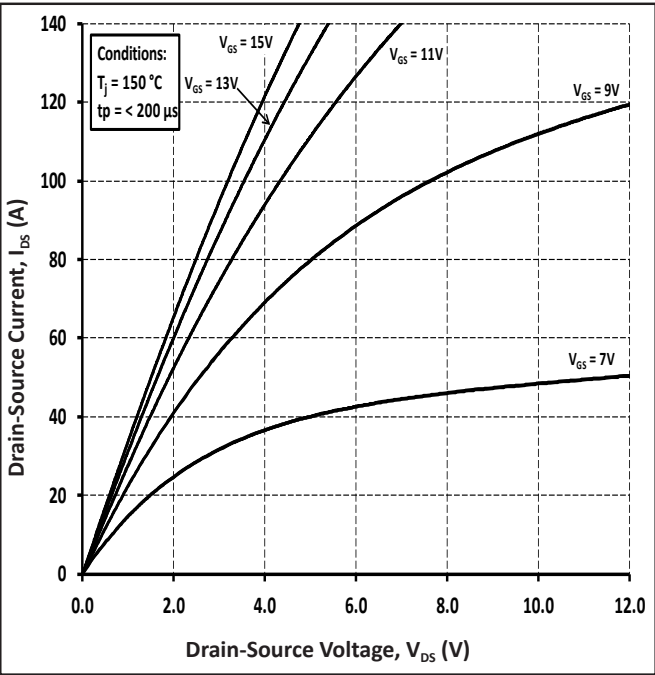


Figure 3. Output Characteristics  $T_j = 150\text{ }^{\circ}\text{C}$

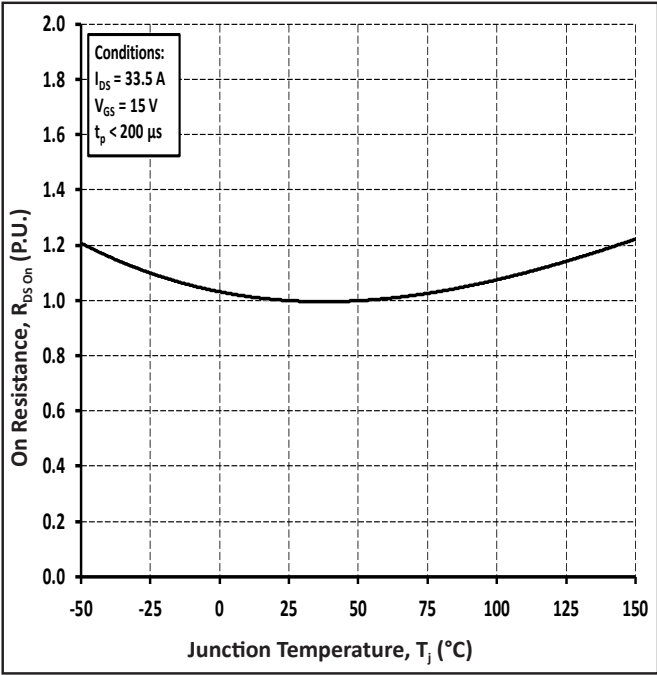


Figure 4. Normalized On-Resistance vs Temperature

Typical Performance

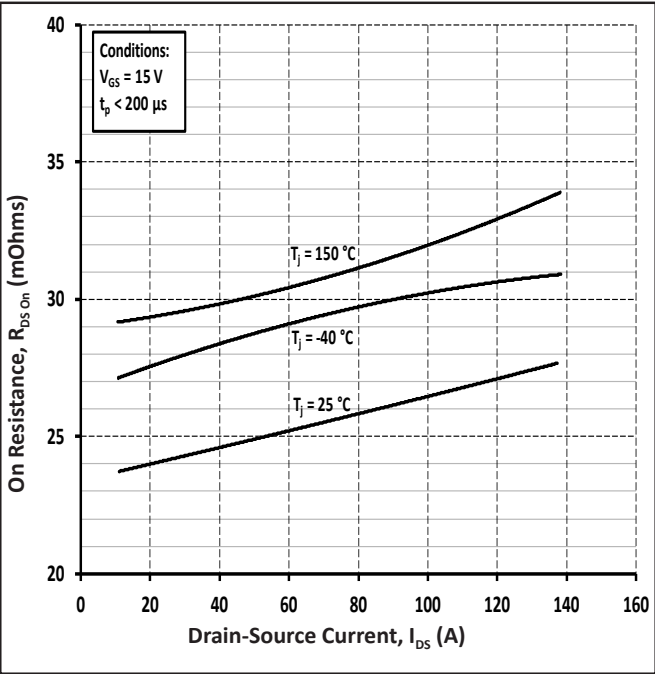


Figure 5. On-Resistance vs Drain Current for Various Temperatures

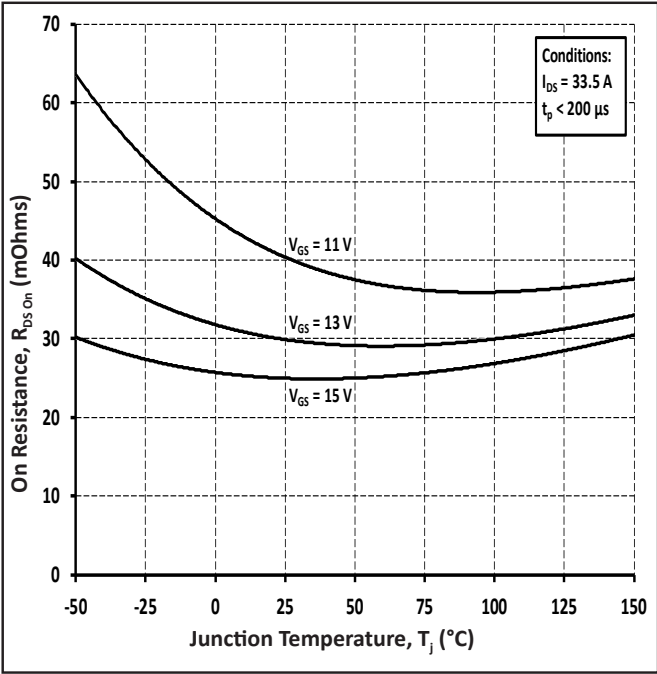


Figure 6. On-Resistance vs Temperature for Various Gate Voltage

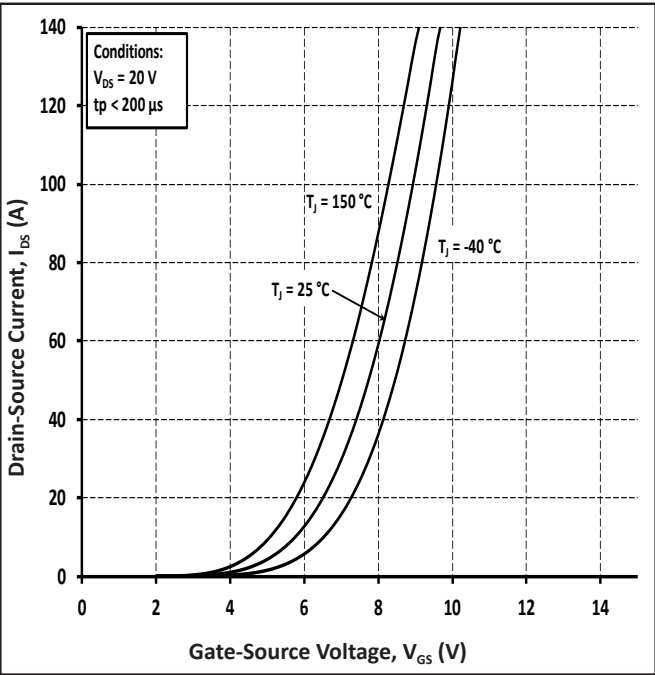


Figure 7. Transfer Characteristic for Various Junction Temperatures

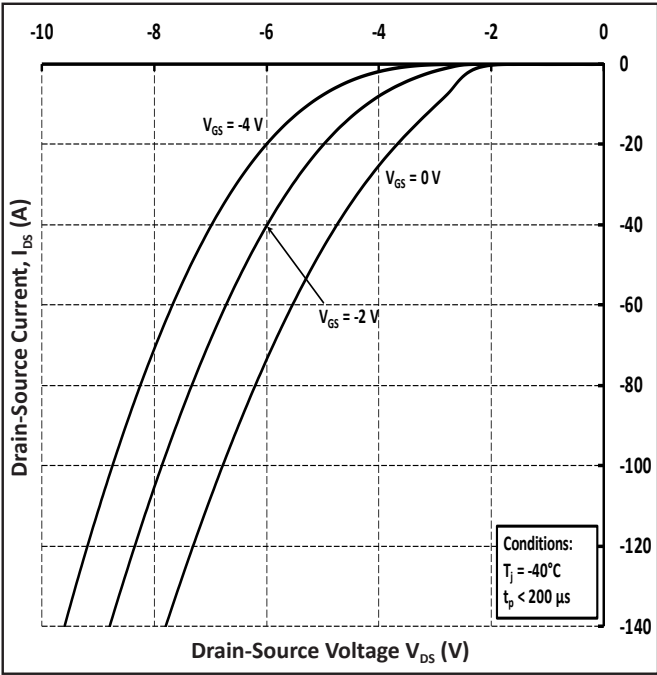


Figure 8. Body Diode Characteristic at -40 °C

Typical Performance

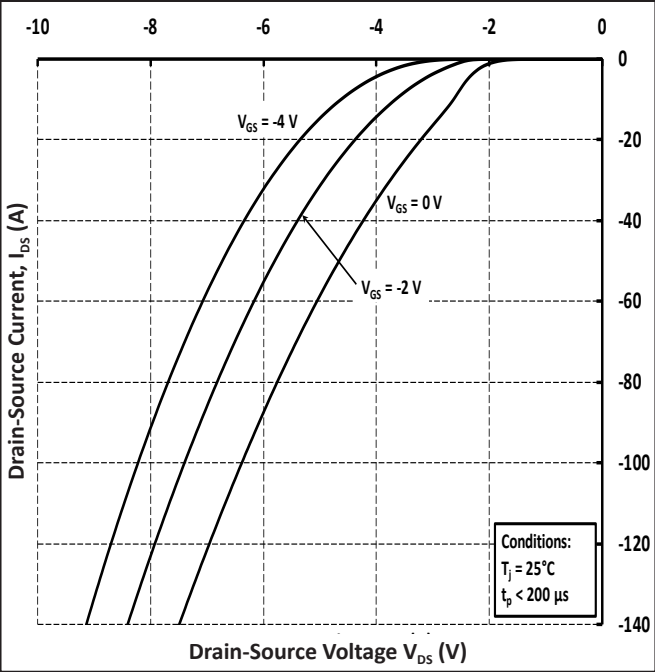


Figure 9. Body Diode Characteristic at 25 °C

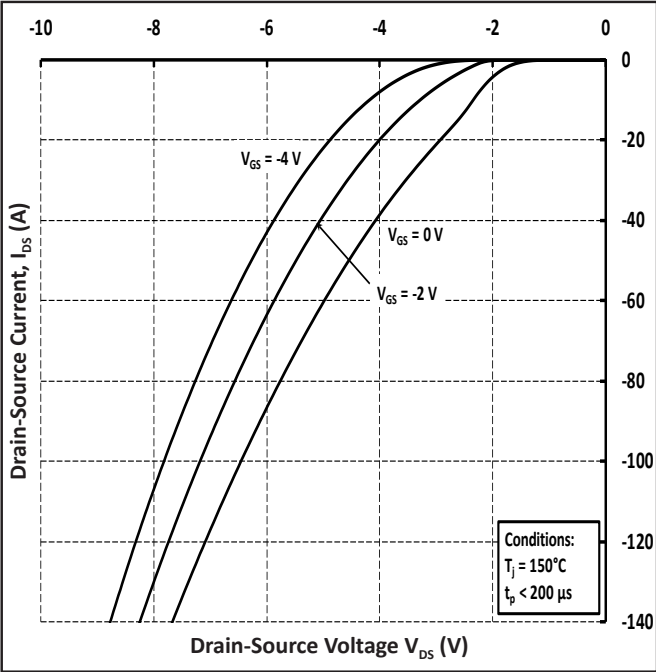


Figure 10. Body Diode Characteristic at 150 °C

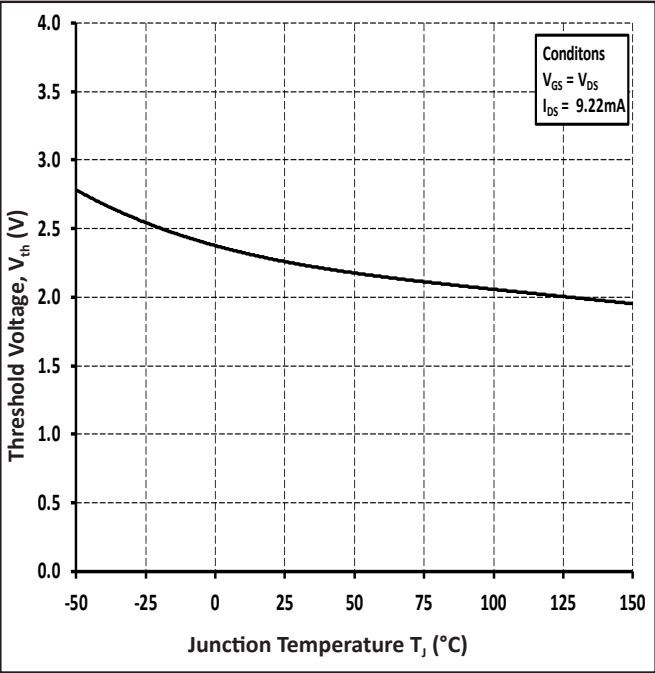


Figure 11. Threshold Voltage vs Temperature

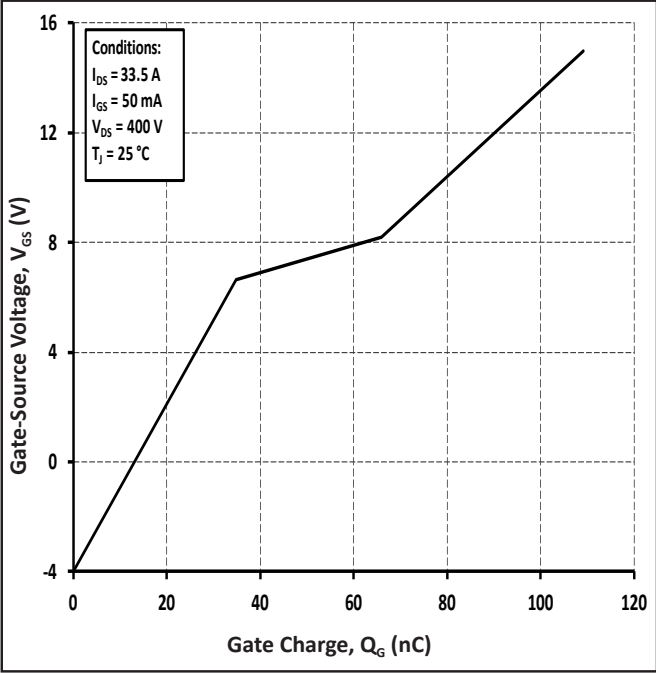


Figure 12. Gate Charge Characteristic

Typical Performance

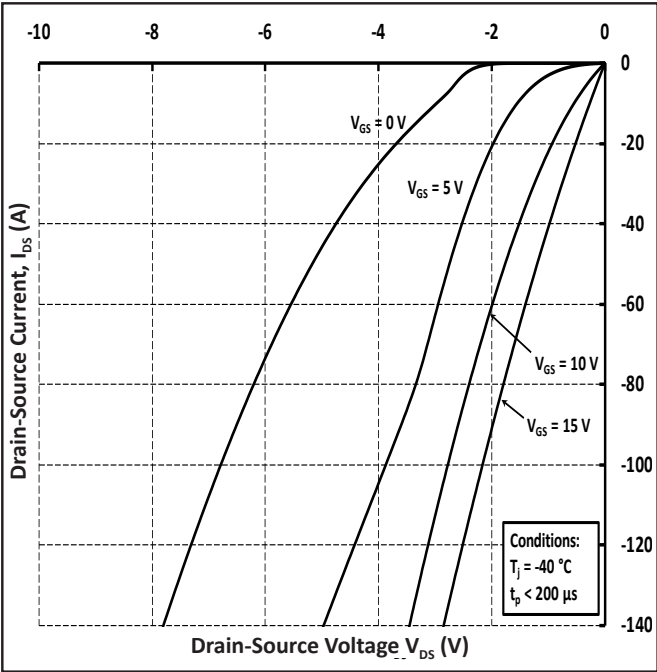


Figure 13. 3<sup>rd</sup> Quadrant Characteristic at  $-40\text{ }^{\circ}\text{C}$

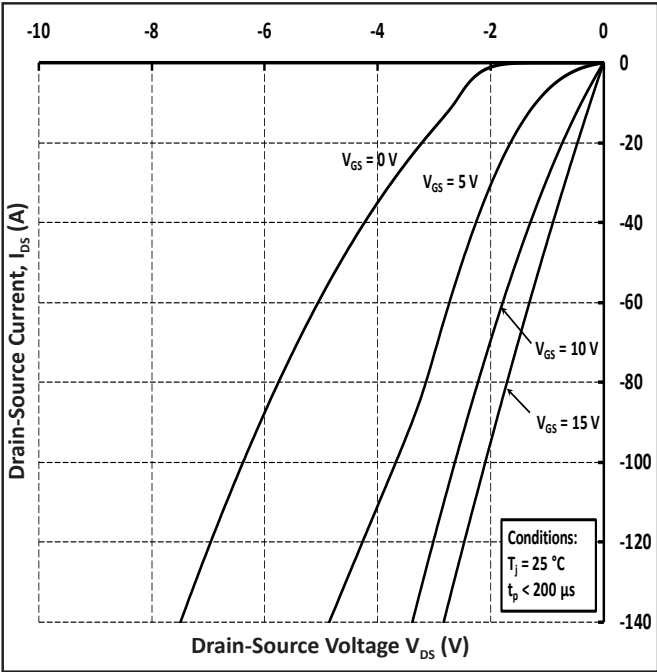


Figure 14. 3<sup>rd</sup> Quadrant Characteristic at  $25\text{ }^{\circ}\text{C}$

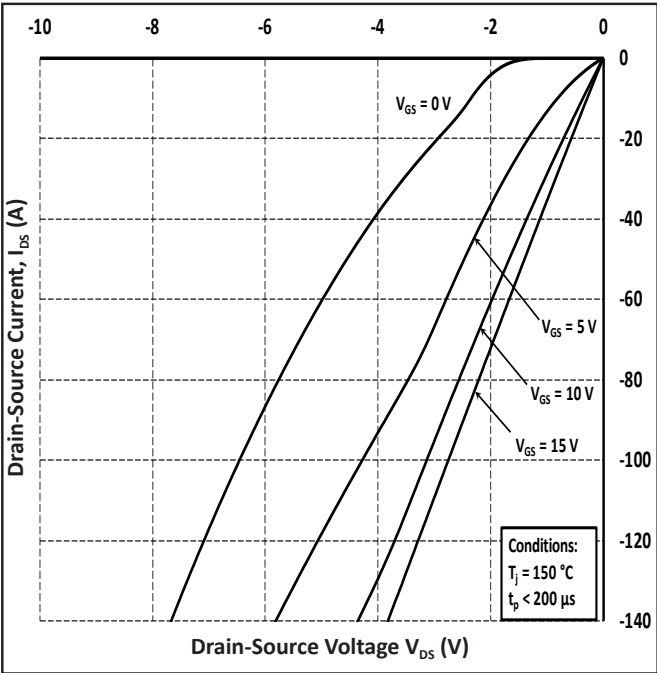


Figure 15. 3<sup>rd</sup> Quadrant Characteristic at  $150\text{ }^{\circ}\text{C}$

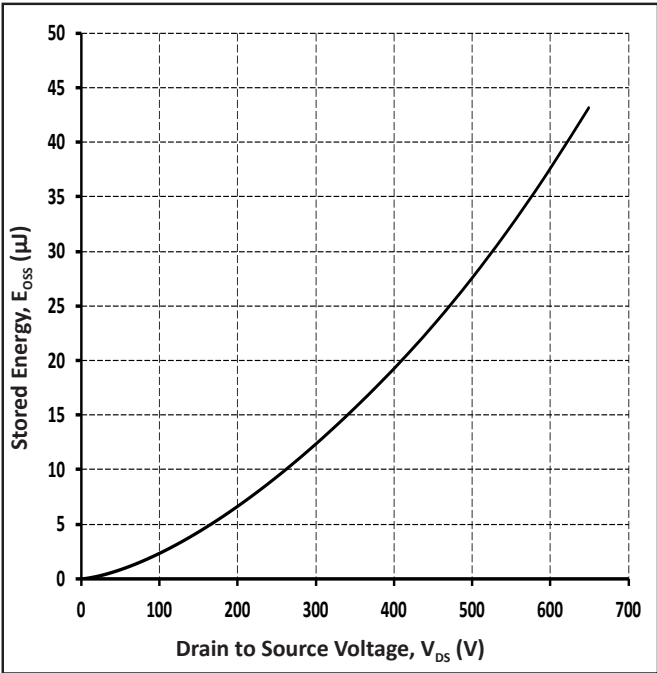


Figure 16. Output Capacitor Stored Energy



## Typical Performance

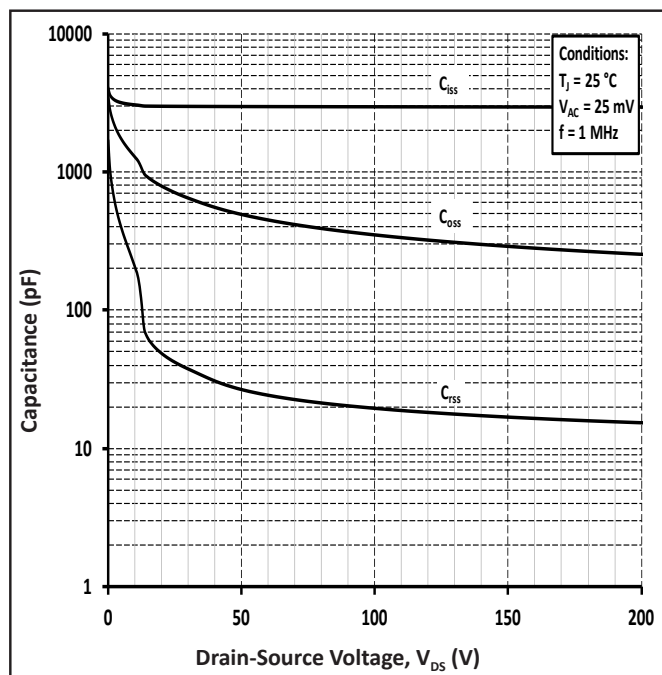


Figure 17. Capacitances vs Drain-Source Voltage (0-200 V)

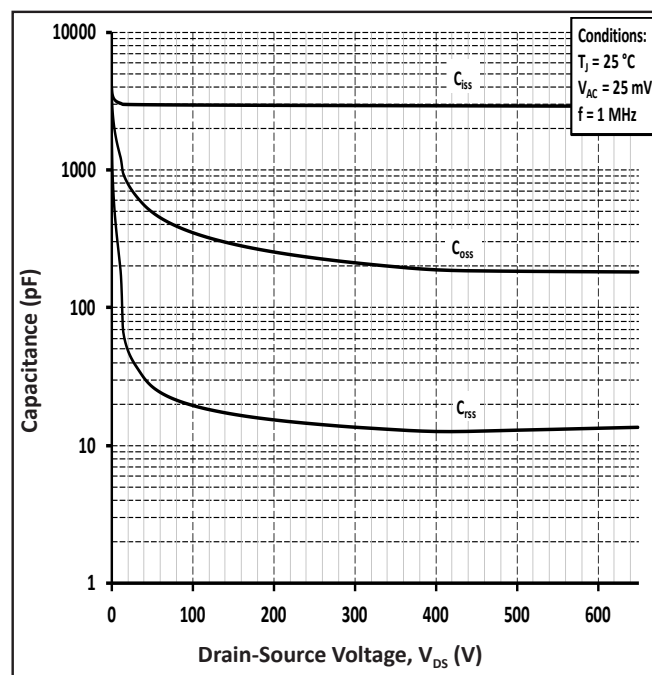


Figure 18. Capacitances vs Drain-Source Voltage (0-600 V)

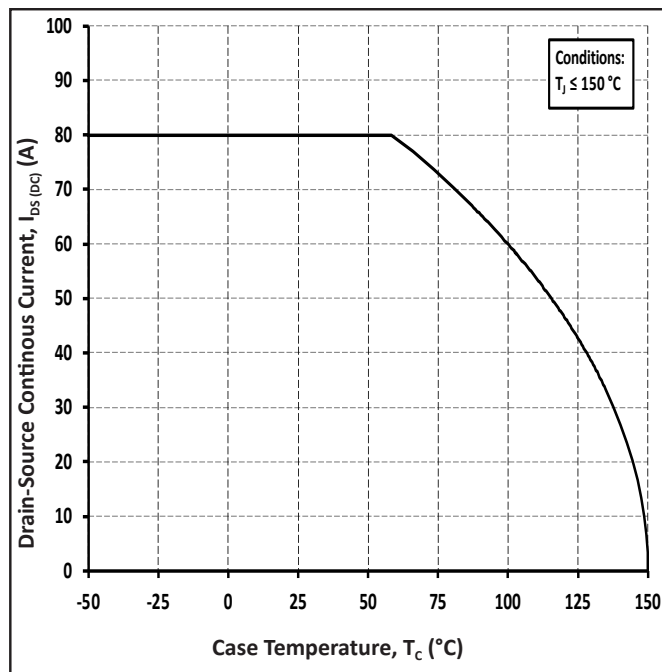


Figure 19. Continuous Drain Current Derating vs Case Temperature

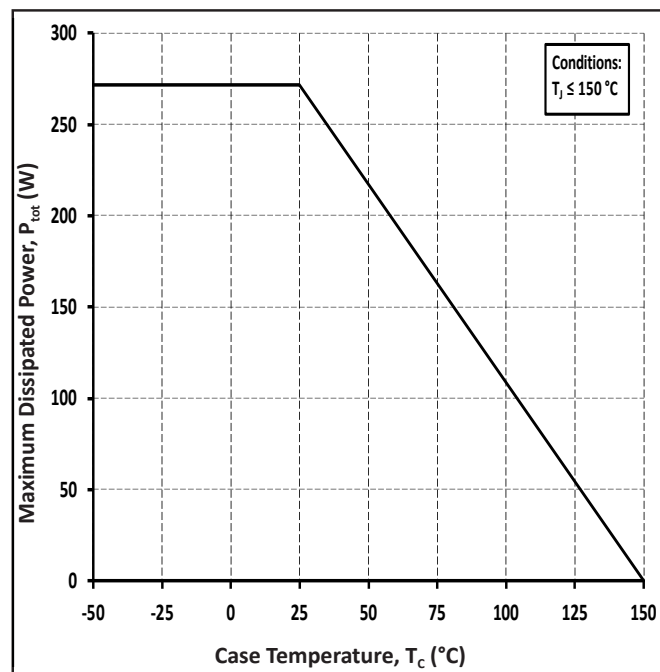


Figure 20. Maximum Power Dissipation Derating vs Case Temperature



## Typical Performance

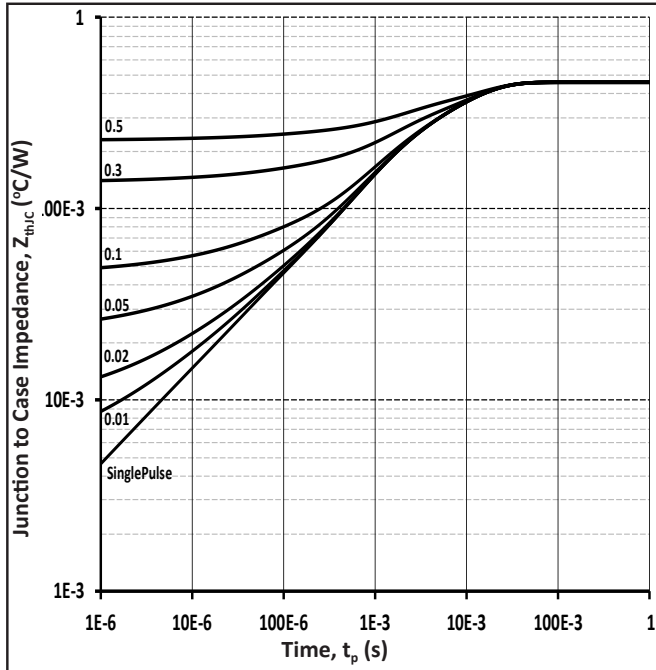


Figure 21. Transient Thermal Impedance (Junction - Case)

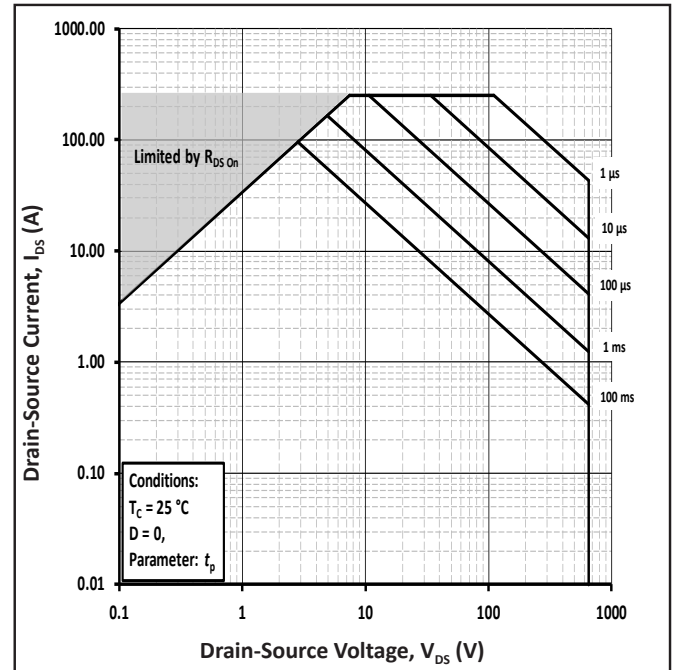


Figure 22. Safe Operating Area

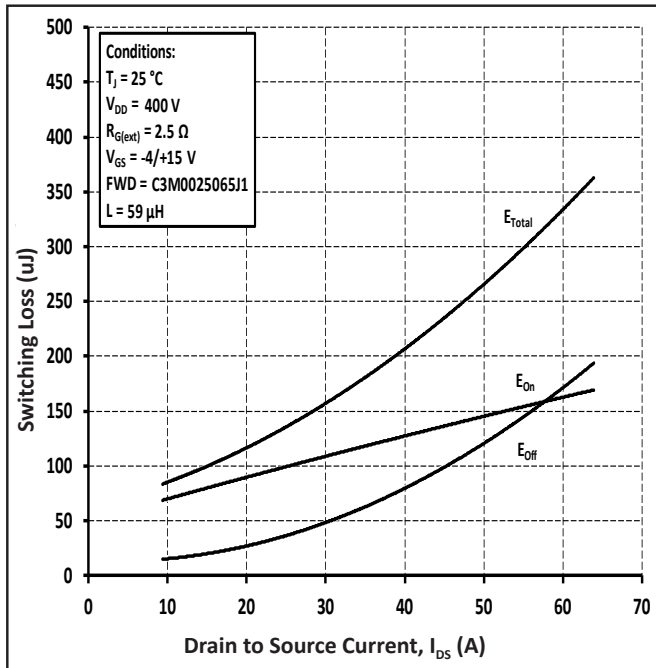


Figure 23. Clamped Inductive Switching Energy vs Drain Current ( $V_{DD} = 400 \text{ V}$ )

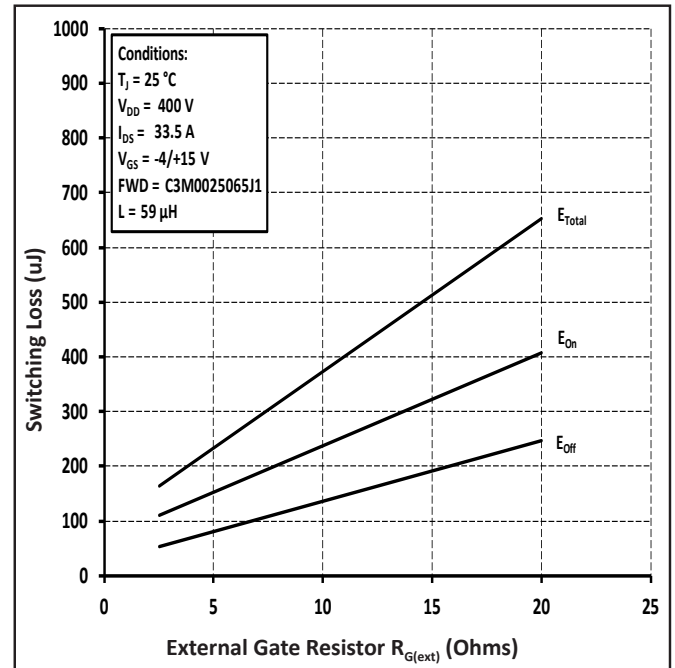


Figure 24. Clamped Inductive Switching Energy vs  $R_{G(ext)}$

Typical Performance

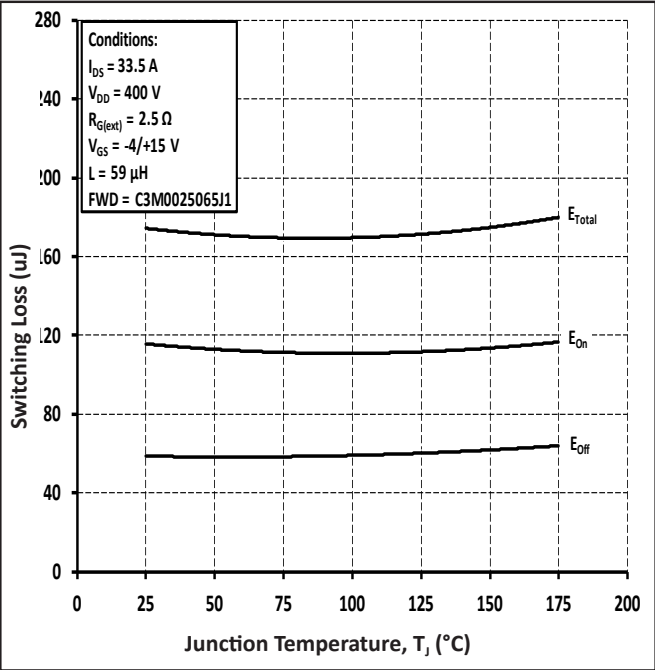


Figure 25. Clamped Inductive Switching Energy vs Temperature

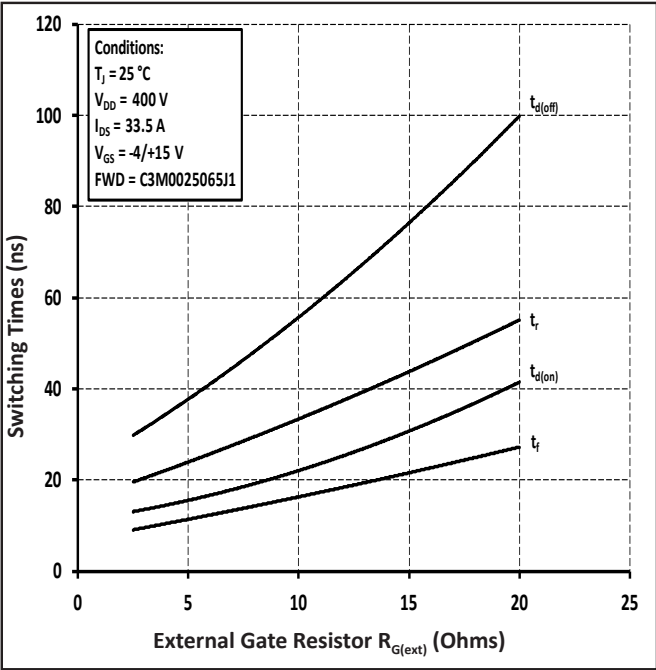


Figure 26. Switching Times vs  $R_{G(ext)}$

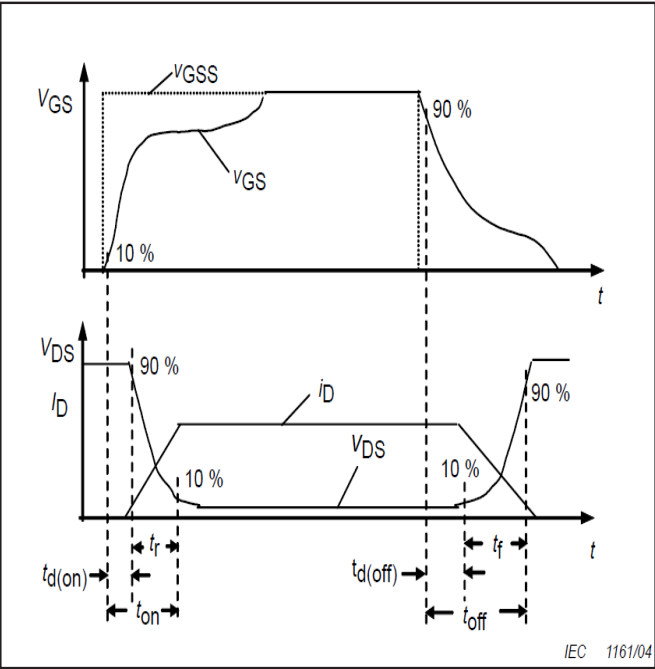


Figure 27. Switching Times Definition

## Test Circuit Schematic

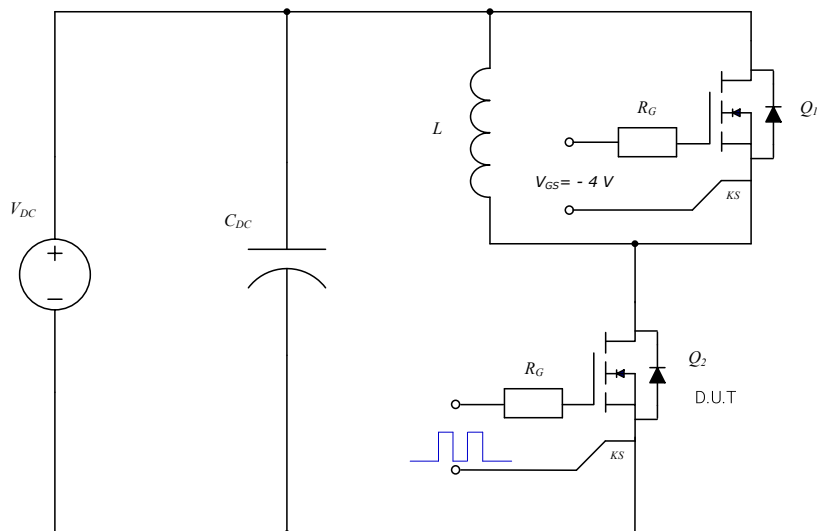
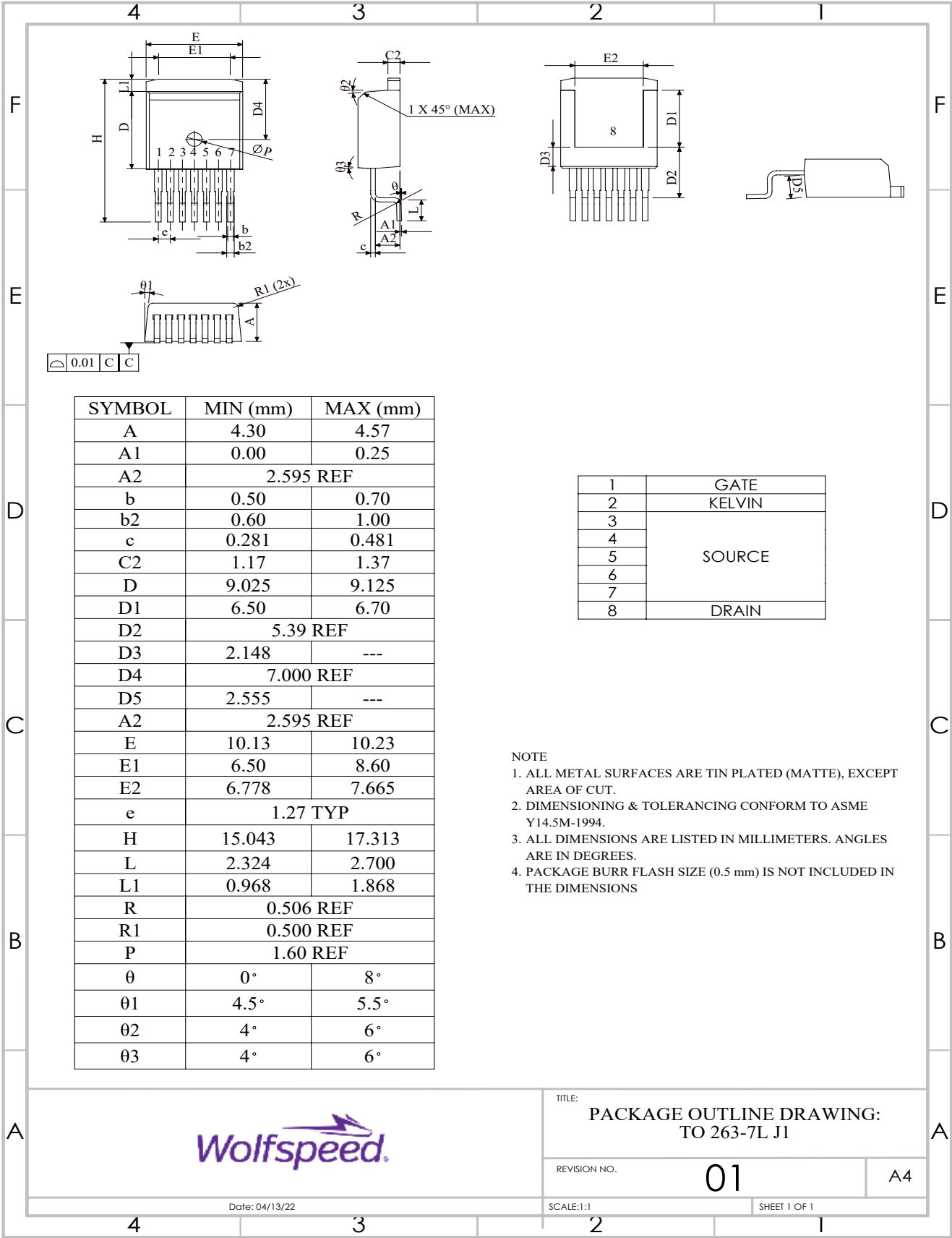


Figure 28. Clamped Inductive Switching Waveform Test Circuit

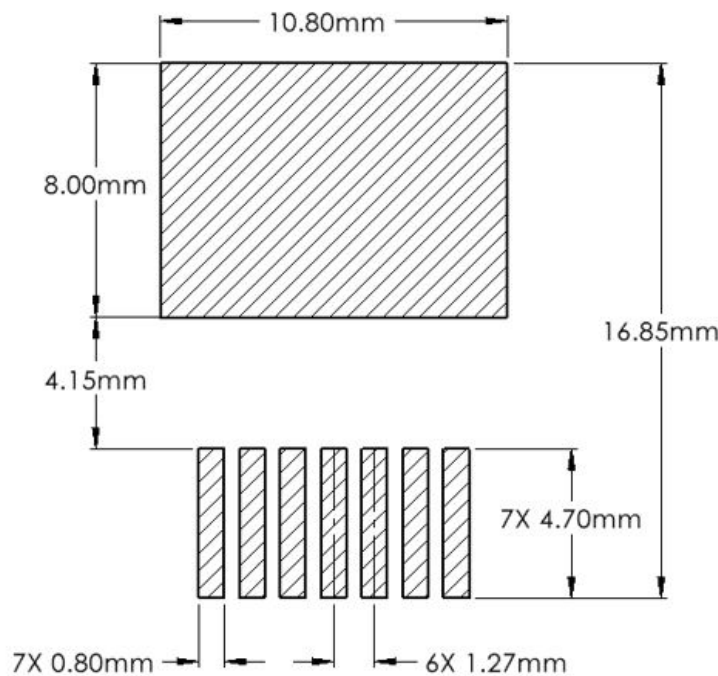
Note (4): Turn-off and Turn-on switching energy and timing values measured using SiC MOSFET Body Diode as shown above.

Package Dimensions

Package: TO-263-7L XL



Recommended Solder Pad Layout



Revision History

Current Revision	Date of Release	Description of Changes
0	October-2021	Initial Release
1	January-2024	Updated Wolfspeed branding, package drawing, package image, solder pad layout, added Rev history
2	December - 2024	Legal Disclaimer Updated



## Notes & Disclaimer

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