

MOSFETs Silicon P-Channel MOS (U-MOSVI)

# SSM3J353F

#### 1. Applications

· Power Management Switches

#### 2. Features

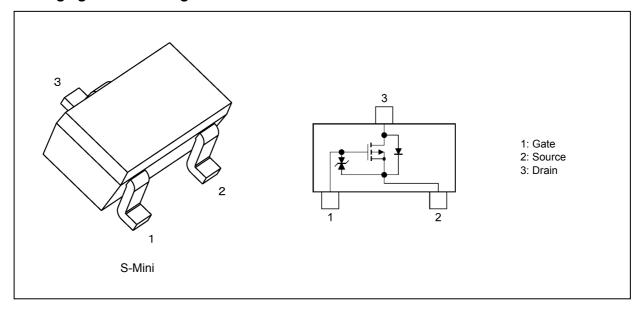
- (1) 4.0 V gate drive voltage.
- (2) Low drain-source on-resistance

:  $R_{DS(ON)} = 274 \text{ m}\Omega \text{ (max) } (@V_{GS} = -4.0 \text{ V}, I_D = -0.5 \text{ A})$ 

 $R_{DS(ON)}$  = 232 m $\Omega$  (max) (@V\_{GS} = -4.5 V,  $I_D$  = -0.5 A)

 $R_{DS(ON)}$  = 150 m $\Omega$  (max) (@V<sub>GS</sub> = -10 V, I<sub>D</sub> = -2.0 A)

#### 3. Packaging and Pin Assignment





## 4. Absolute Maximum Ratings (Note) (Unless otherwise specified, Ta = 25 °C)

Char	acteristics		Symbol	Rating	Unit
Drain-source voltage			$V_{DSS}$	-30	V
Gate-source voltage	'		$V_{GSS}$	-25 / +20	
Drain current (DC)		(Note 1)	$I_D$	-2.0	Α
Drain current (pulsed)		(Note 1), (Note 2)	$I_{DP}$	-4.0	
Power dissipation	'	(Note 3)	$P_D$	600	mW
Power dissipation	t ≤ 1s	(Note 3)		1200	
Channel temperature			T <sub>ch</sub>	150	°C
Storage temperature			T <sub>stg</sub>	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

- Note 1: Ensure that the channel temperature does not exceed 150 °C.
- Note 2: Repetitive rating; pulse width limited by maximum channel temperature.
- Note 3: Device mounted on a 25.4 mm × 25.4 mm × 1.6 mm FR4 glass epoxy board (Cu pad: 645 mm<sup>2</sup>)
- Note: This transistor is sensitive to electrostatic discharge and should be handled with care.
- Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.
- Note: The channel-to-ambient thermal resistance, R<sub>th(ch-a)</sub>, and the drain power dissipation, P<sub>D</sub>, vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.



#### 5. Electrical Characteristics

#### 5.1. Static Characteristics (Unless otherwise specified, T<sub>a</sub> = 25 °C)

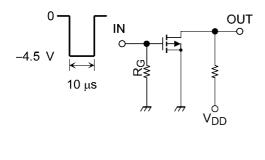
Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current		I <sub>GSS</sub>	V <sub>GS</sub> = ±16 V	_	_	±1	μΑ
Drain cut-off current		I <sub>DSS</sub>	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}$	_	_	-1	
Drain-source breakdown voltage		V <sub>(BR)DSS</sub>	I <sub>D</sub> = -1 mA, V <sub>GS</sub> = 0 V	-30	_	_	V
Drain-source breakdown voltage	(Note 1)	V <sub>(BR)DSX</sub>	I <sub>D</sub> = -1 mA, V <sub>GS</sub> = 8 V	-22	_	_	
Gate threshold voltage		V <sub>th</sub>	$V_{DS} = V_{GS}$ , $I_{D} = -0.25$ mA	-1.0	_	-2.2	
Drain-source on-resistance	(Note 2)	R <sub>DS(ON)</sub>	I <sub>D</sub> = -0.5 A, V <sub>GS</sub> = -4.0 V	_	198	274	mΩ
			I <sub>D</sub> = -0.5 A, V <sub>GS</sub> = -4.5 V	_	176	232	
			I <sub>D</sub> = -2.0 A, V <sub>GS</sub> = -10 V	_	125	150	
Forward transfer admittance	(Note 2)	Y <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1.0 A	_	2.6	_	S

Note 1: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

# 5.2. Dynamic Characteristics (Unless otherwise specified, T<sub>a</sub> = 25 °C)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -15 V, V <sub>GS</sub> = 0 V,	_	159	_	pF
Reverse transfer capacitance	C <sub>rss</sub>	f = 1 MHz	_	23		
Output capacitance	C <sub>oss</sub>		_	30	_	
Switching time (turn-on time)	t <sub>on</sub>	$V_{DS} = -15 \text{ V}, I_{D} = -1.0 \text{ A},$	_	30	_	ns
Switching time (turn-off time)	t <sub>off</sub>	$V_{GS}$ = 0 to -4.5 V, $R_{G}$ = 15 $\Omega$	_	34		

## 5.3. Switching Time Test Circuit



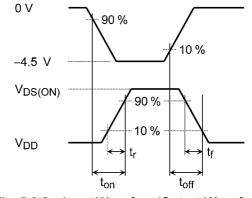


Fig. 5.3.1 Switching Time Test Circuit

Fig. 5.3.2 Input Waveform/Output Waveform

### 5.4. Gate Charge Characteristics (Unless otherwise specified, Ta = 25 °C)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Total gate charge (gate-source plus gate-drain)		V <sub>DD</sub> = -15 V, I <sub>D</sub> = -2.0 A,	_	3.4	_	nC
Gate-source charge 1	Q <sub>gs1</sub>	V <sub>GS</sub> = -4.5 V	_	1.5	_	
Gate-drain charge	Q <sub>gd</sub>		_	1.4	_	

## 5.5. Source-Drain Characteristics (Unless otherwise specified, T<sub>a</sub> = 25 °C)

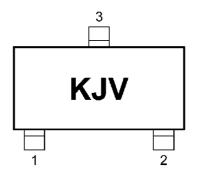
Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Diode forward voltage	(Note 1)	$V_{DSF}$	$I_D = 2.0 \text{ A}, V_{GS} = 0 \text{ V}$	_	0.9	1.2	V

Note 1: Pulse measurement.

Note 2: Pulse measurement.



# 6. Marking





#### 7. Characteristics Curves (Note)

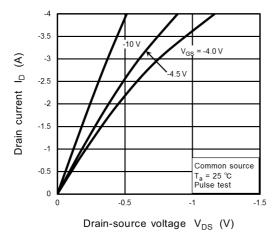


Fig. 7.1 I<sub>D</sub> - V<sub>DS</sub>

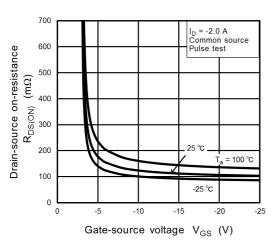


Fig. 7.3  $R_{DS(ON)} - V_{GS}$ 

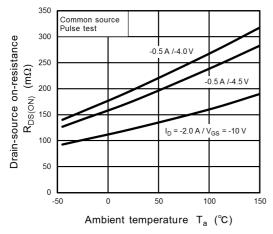


Fig. 7.5  $R_{DS(ON)}$  -  $T_a$ 

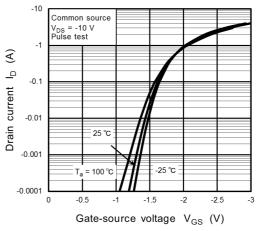


Fig. 7.2 I<sub>D</sub> - V<sub>GS</sub>

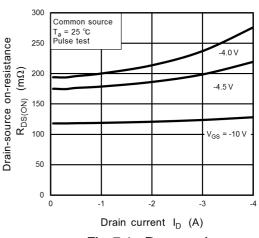


Fig. 7.4 R<sub>DS(ON)</sub> - I<sub>D</sub>

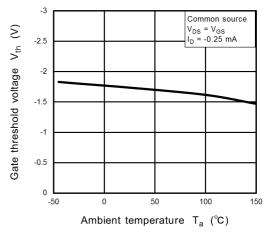


Fig. 7.6 V<sub>th</sub> - T<sub>a</sub>

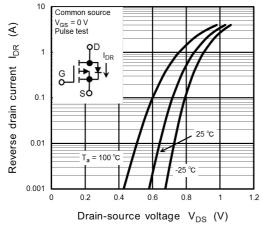


Fig. 7.7 IDR - VDS

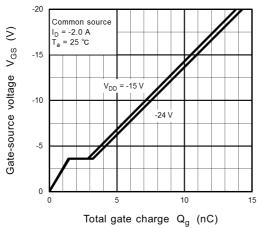


Fig. 7.9 Dynamic Input Characteristics

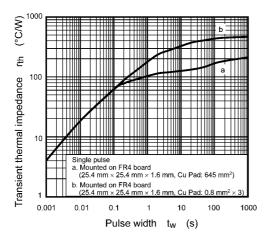


Fig. 7.11 rth - tw

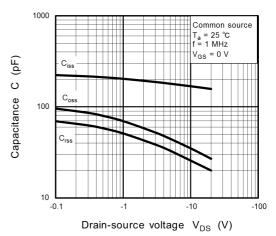


Fig. 7.8 C - V<sub>DS</sub>

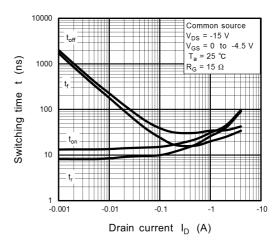


Fig. 7.10 t-I<sub>D</sub>

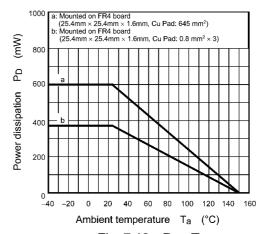


Fig. 7.12 P<sub>D</sub> - T<sub>a</sub>

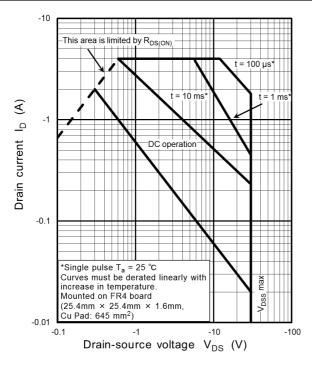


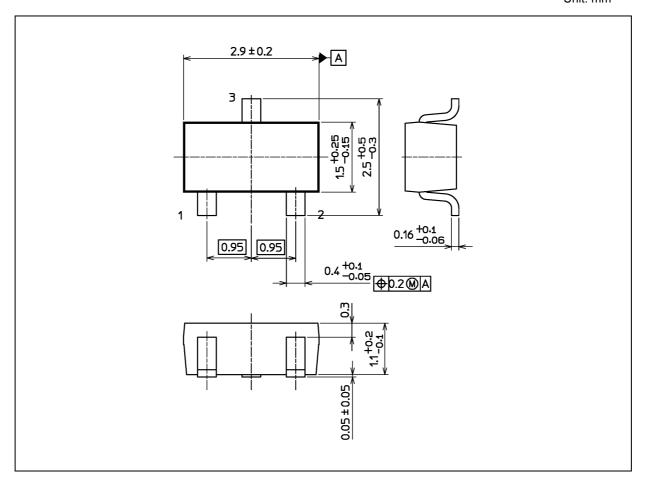
Fig. 7.13 Safe Operationg Area

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



# **Package Dimensions**

Unit: mm



Weight: 12 mg (typ.)

	Package Name(s)
Nickname: S-Mini	



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