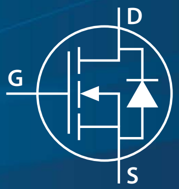
EPC2019 – Enhancement Mode Power Transistor

V_{DS} , 200 V
$R_{DS(on)}$, 42 mΩ max
I_D , 8.5 A



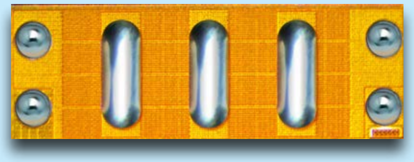
EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

APPLICATION NOTES:

- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source
- Questions: **Ask a GaN Expert**



EPC2019 eGaN® FETs are supplied only in passivated die form with solder bars
Die size: 2.77 x 0.95 mm

Applications

- High Speed DC-DC conversion
- Class-D Audio
- High Frequency Hard-Switching and Soft-Switching Circuits

Benefits

- Ultra High Efficiency
- Ultra Low $R_{DS(on)}$
- Ultra Low Q_G
- Ultra Small Footprint

Maximum Ratings

	PARAMETER	VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	200	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	240	
I_D	Continuous (T_A = 25˚C, $R_{\theta JA}$ = 18°C/W)	8.5	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	45	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics

	PARAMETER	TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.7	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	7.5	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	72	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Static Characteristics (T_J = 25˚C unless otherwise stated)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 125 µA	200			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 160 V		1	100	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.001	2.5	mA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		1	100	µA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1.5 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 7 A		22	42	mΩ
V_{SD}	Source-Drain Forward Voltage#	I_S = 0.5 A, V_{GS} = 0 V		2.0		V

Defined by design. Not subject to production test.

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 100 V		254	288	pF
C_{RSS}	Reverse Transfer Capacitance			1.3		
C_{OSS}	Output Capacitance			135	163	
$C_{OSS(ER)}$	Effective Output Capacitance,Energy Related (Note 2)	V_{GS} = 0 V, V_{DS} = 0 to 100 V		156		
$C_{OSS(TR)}$	Effective Output Capacitance,Time Related (Note 3)			201		
R_G	Gate Resistance			0.4		Ω
Q_G	Total Gate Charge	V_{GS} = 5 V, V_{DS} = 100 V, I_D = 7 A		2.4	2.9	nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 100 V, I_D = 7 A		0.8		
Q_{GD}	Gate-to-Drain Charge			0.6		
$Q_{G(TH)}$	Gate Charge at Threshold			0.6		
Q_{OSS}	Output Charge	V_{GS} = 0 V, V_{DS} = 100 V		20	24	
Q_{RR}	Source-Drain Recovery Charge			0		

All measurements were done with substrate connected to source.
Defined by design. Not subject to production test.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

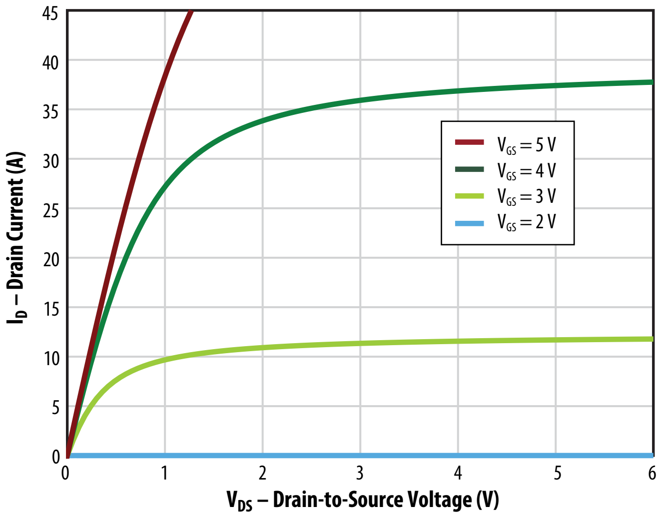


Figure 2: Typical Transfer Characteristics

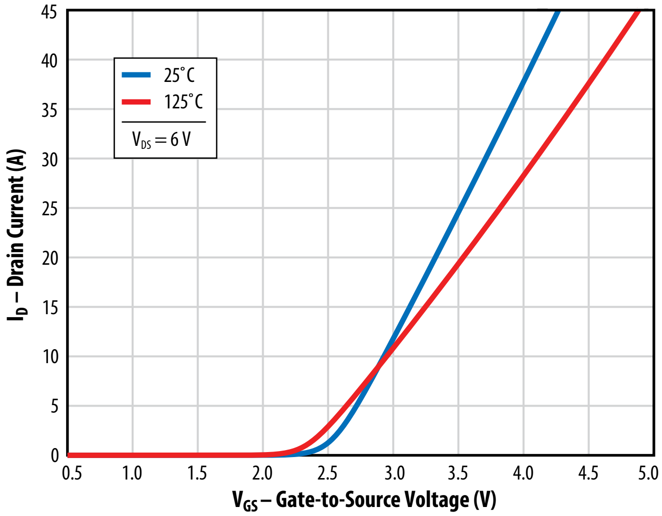


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

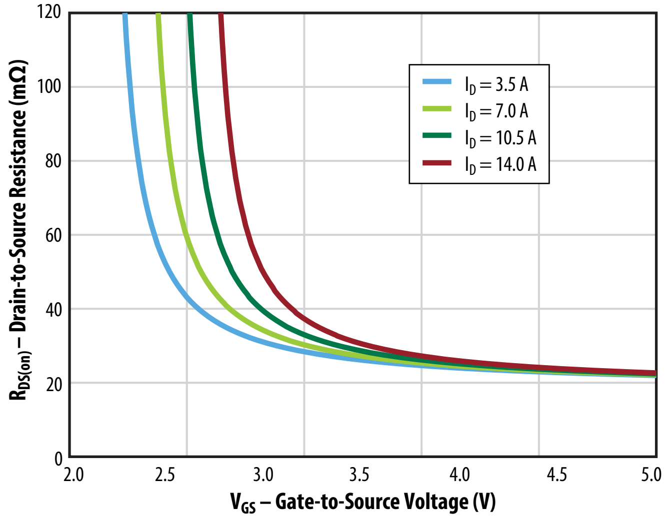


Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

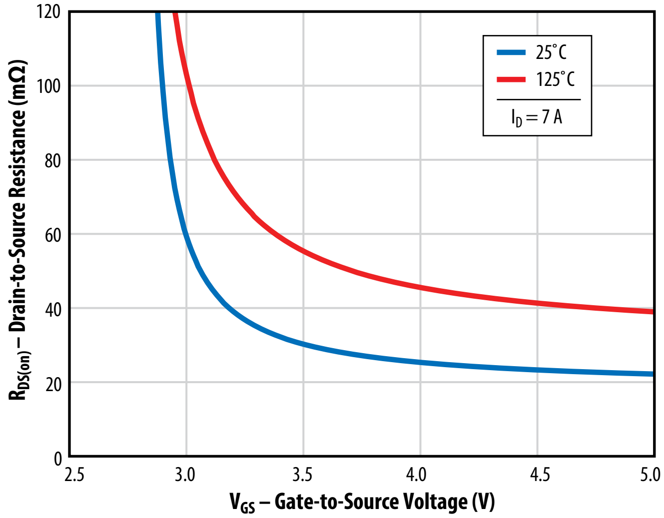


Figure 5a: Typical Capacitance (Linear Scale)

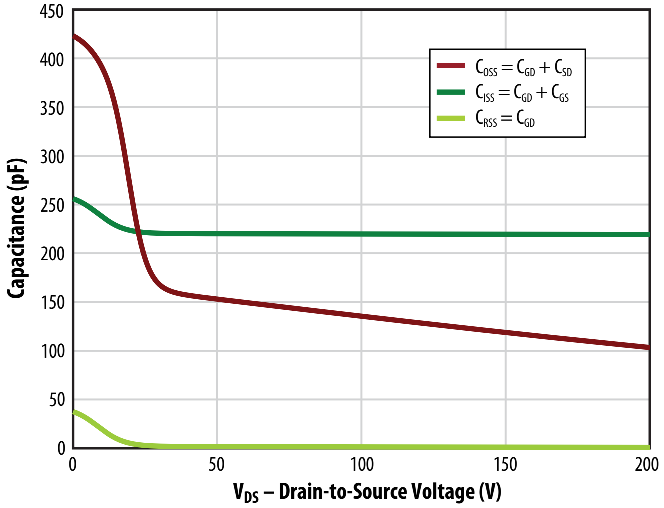


Figure 5b: Typical Capacitance (Log Scale)

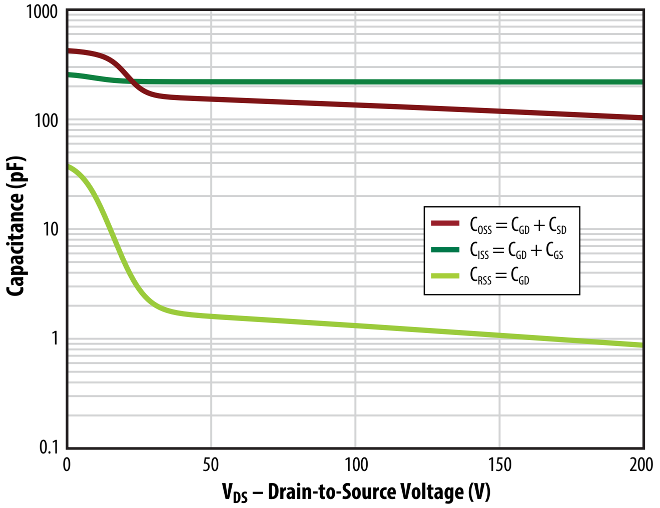


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

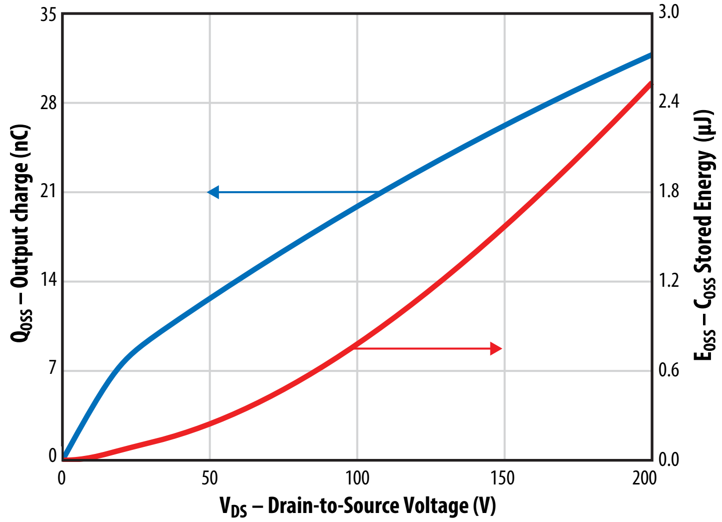


Figure 7: Typical Gate Charge

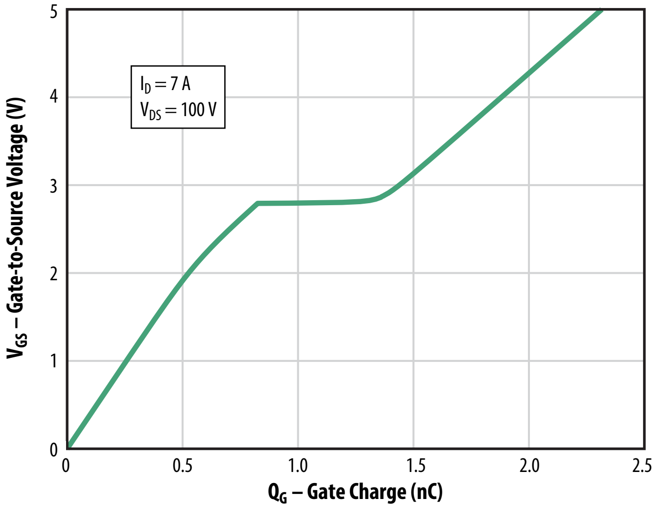
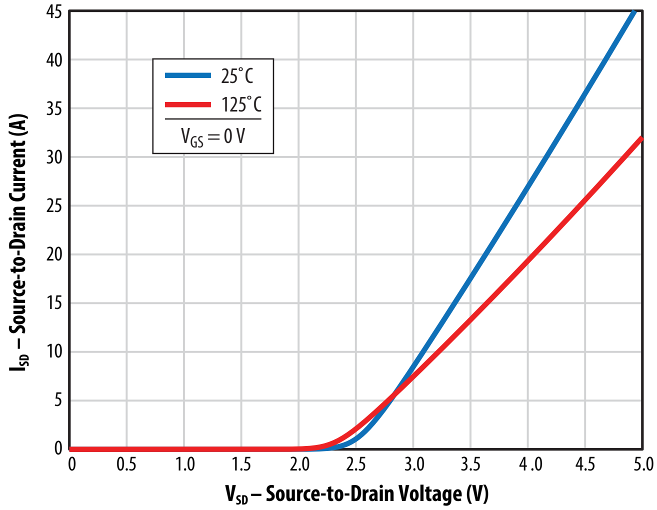


Figure 8: Reverse Drain-Source Characteristics



Note: Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0 V for OFF.

Figure 9: Normalized On-State Resistance vs. Temperature

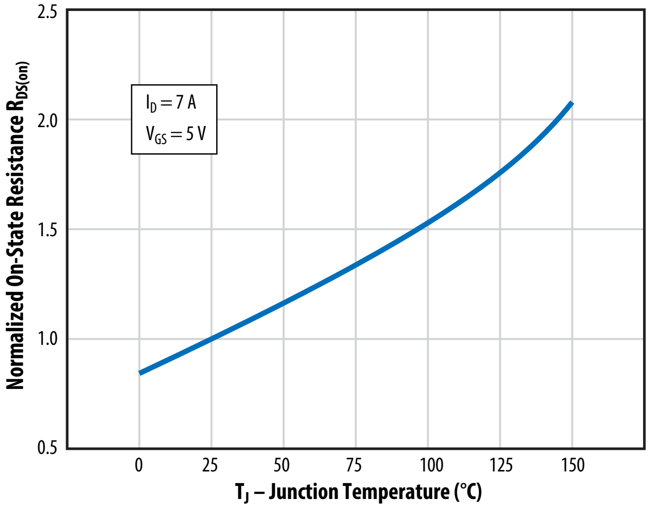


Figure 10: Normalized Threshold Voltage vs. Temperature

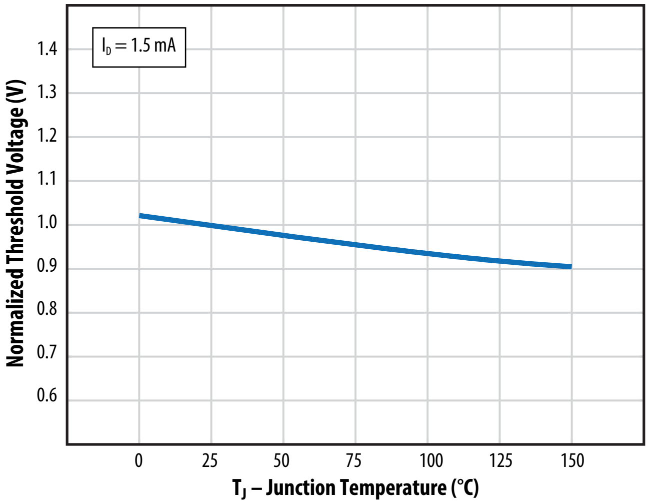
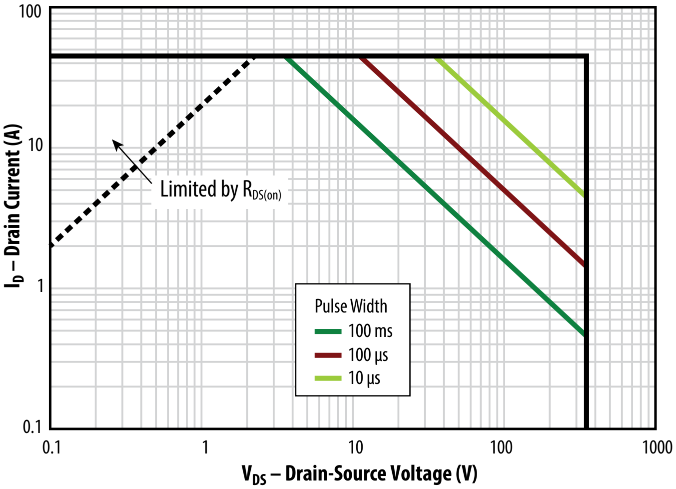
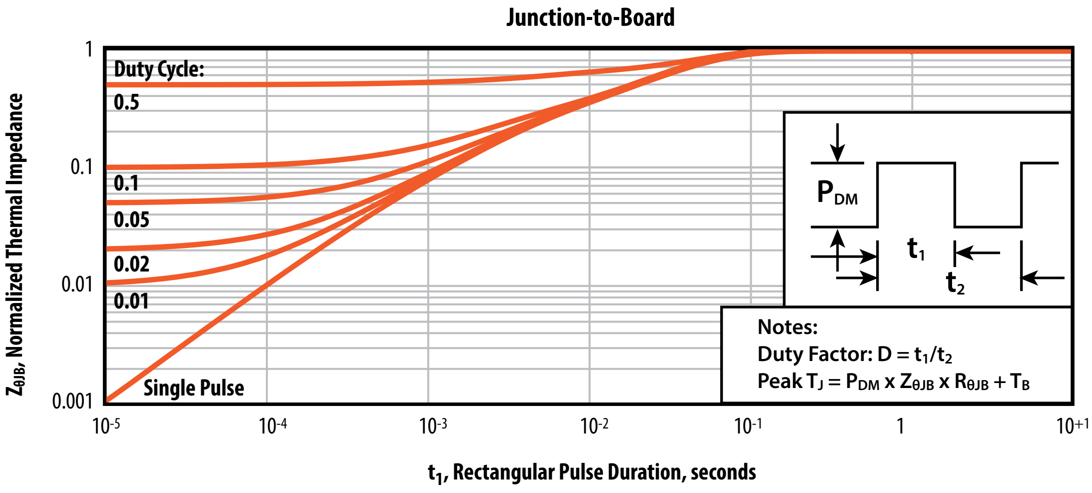


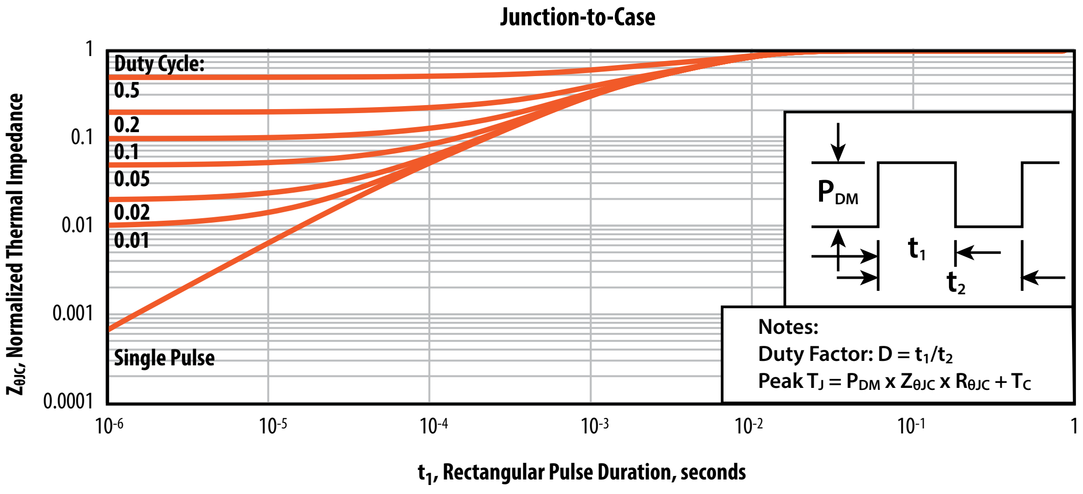
Figure 11: Safe Operating Area



T_J = Max Rated, T_C = +25°C, Single Pulse

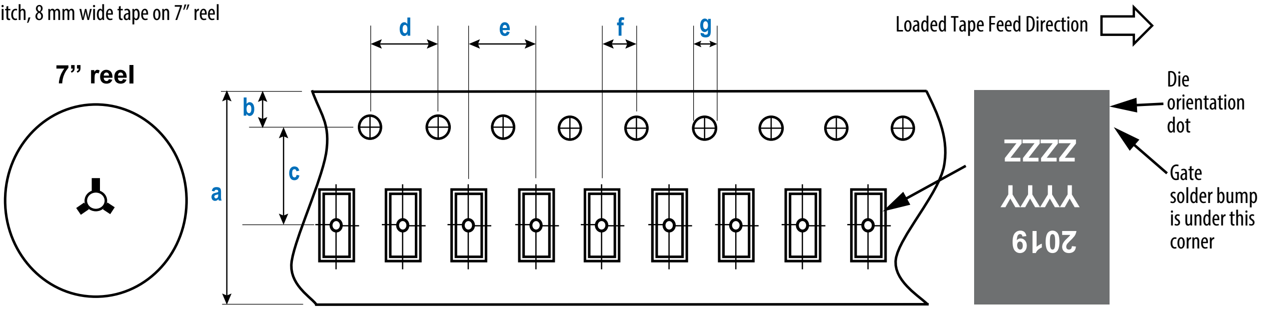
Figure 12: Transient Thermal Response Curves





TAPE AND REEL CONFIGURATION

4 mm pitch, 8 mm wide tape on 7” reel



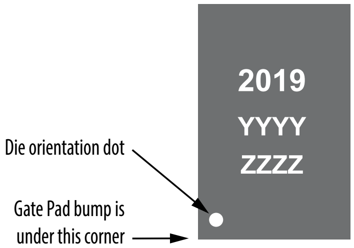
Die is placed into pocket
solder bar side down
(face side down)

	Dimension (mm)		
EPC2019 (Note 1)	**Target**	**MIN**	**MAX**
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (Note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.40	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

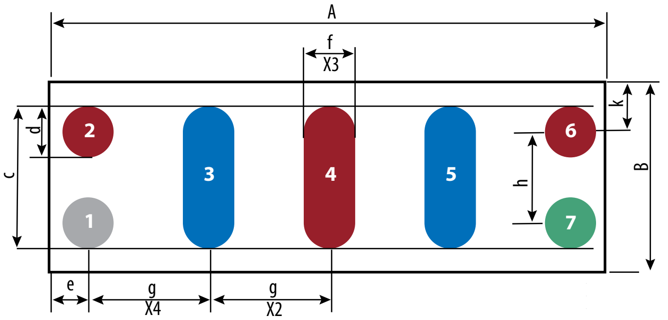
DIE MARKINGS



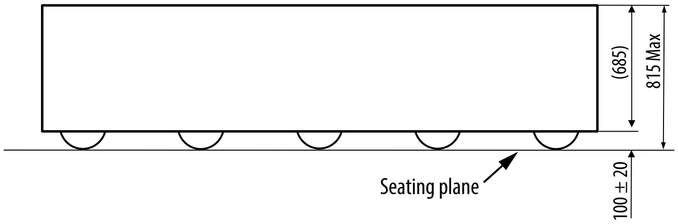
Part Number	Laser Markings		
	Part # Marking Line 1	**Lot_Date Code Marking Line 2**	**Lot_Date Code Marking Line 3**
EPC2019	2019	YYYY	ZZZZ

DIE OUTLINE

Solder Bar View



Side View



DIM	MICROMETERS		
	MIN	**Nominal**	**MAX**
A	2736	2766	2796
B	920	950	980
c	697	700	703
d	247	250	253
e	168	183	198
f	245	250	255
g	600	600	600
h	450	450	450
i	235	250	265

Pad no.1 is Gate;

Pad no. 3, 5 are Drain;

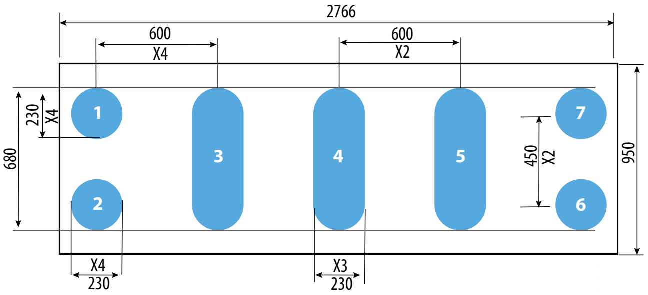
Pad no. 2, 4, 6 are Source;

Pad no. 7 is Substrate.*

*Substrate pin should be connected to Source

RECOMMENDED LAND PATTERN

(measurements in µm)



The land pattern is solder mask defined.

Pad no. 1 is Gate

Pad no. 3, 5 are Drain

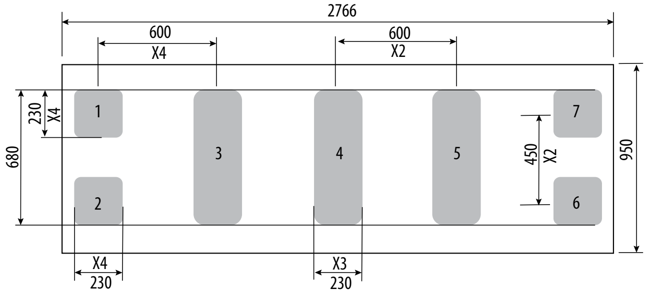
Pad no. 2, 4, 6 are Source

Pad no. 7 is Substrate*

*Substrate pin should be connected to Source

RECOMMENDED STENCIL DRAWING

(units in µm)



Recommended stencil should be 4 mil (100 µm) thick, must be laser cut , opening per drawing. The corner has a radius of R60.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content

Additional Resources Available

- Assembly resources available at: https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx
- Library of Altium footprints for production FETs and ICs: https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip
  (for preliminary device Altium footprints, contact EPC)

Note: This datasheet is representative of lots with date code of 2131 or later.

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change without notice.
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