

4-Bit Bi-directional Level Shifter for open-drain and Push-Pull Application

Features

- Fully Symmetric Supply Voltage
- 1.1V to 3.6V on A Port and B Port
- High-Speed with 24 Mb/s Data Rate for push-pull application
- High-Speed with 2 Mb/s Data Rate for open-drain application
- No Direction-Control Signal Needed
- Low Bit-to-Bit Skew
- Non-preferential Power-up Sequencing
- ESD protection exceeds 8000V HBM per JESD22-A114
- Integrated 10 kΩ Pull-up Resistors
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](https://www.diodes.com/quality/product-definitions/) or your local Diodes representative.
- Packaging (Pb-free & Green):
 - 14-pin, TSSOP (L)
 - 14-pin, 3.5x3.5 mm TQFN (ZB)
 - 12-pin, CSP (GA)

<https://www.diodes.com/quality/product-definitions/>

Applications

- I2C, SMBus, MDIO
- Low Voltage ASIC Level Translation
- Mobile Phones, PDAs, Camera

Block Diagram

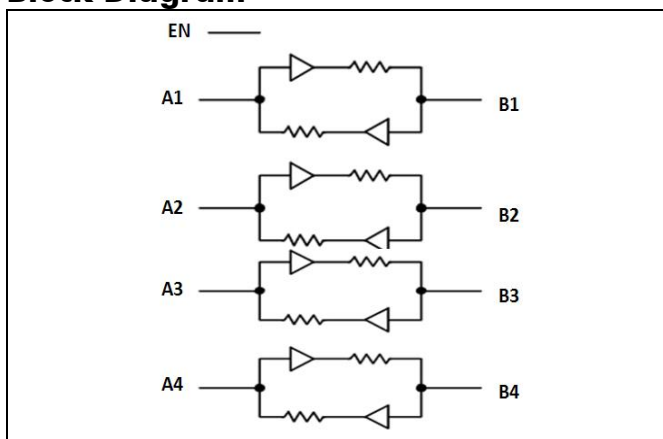
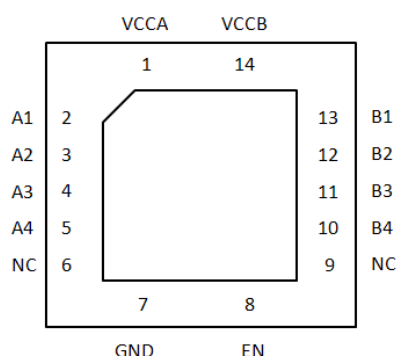


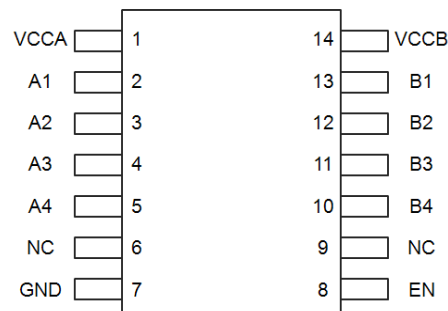
Figure 1: Block Diagram

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

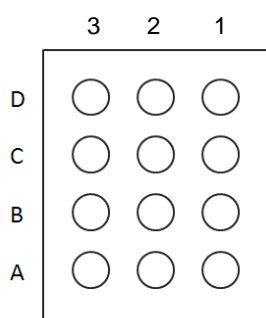
Pin Configuration



TQFN3.5x3.5-14 (Top View)



TSSOP-14 (Top View)



CSP-12 (Top View)

Pin Description

Pin No TSSOP	Pin No TQFN	Pin No CSP	Pin Name	Type	Description
1	1	B2	V _{CCA}	Power	A port supply voltage. $1.1\text{V} \leq V_{CCA} \leq 3.6\text{V}$
2	2	A3	A1	I/O	Input/output A1. Referenced to V _{CCA} .
3	3	B3	A2	I/O	Input/output A2. Referenced to V _{CCA}
4	4	C3	A3	I/O	Input/output A3. Referenced to V _{CCA}
5	5	D3	A4	I/O	Input/output A4. Referenced to V _{CCA}
7	7	D2	GND	GND	Ground.
8	8	C2	EN	Input	Output enable (active High). Pull EN low to place all outputs in 3-state mode.
10	10	D1	B4	I/O	Input/output B4. Referenced to V _{CCB}
11	11	C1	B3	I/O	Input/output B3. Referenced to V _{CCB}
12	12	B1	B2	I/O	Input/output B2. Referenced to V _{CCB}
13	13	A1	B1	I/O	Input/output B1. Referenced to V _{CCB}
14	14	A2	V _{CCB}	Power	B port supply voltage. $1.1\text{V} \leq V_{CCB} \leq 3.6\text{V}$
6, 9	6, 9	/	NC	NC	Not Connect

Maximum Ratings

Storage Temperature	-65°C to +150°C
DC Supply Voltage Port B	-0.3V to +5.5V
DC Supply Voltage Port A	-0.3V to +5.5V
Vi(A) referenced DC Input / Output Voltage	-0.3V to +5.5V
Vi(B) referenced DC Input / Output Voltage	-0.3V to +5.5V
Enable Control Pin DC Input Voltage	-0.3V to +5.5V
Short Circuit duration (I/O to GND)	40mA

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V _{CCA}	V _{CCA} Positive DC Supply Voltage	1.1	-	3.6	V
V _{CCB}	V _{CCB} Positive DC Supply Voltage	1.1	-	3.6	V
V _{EN}	Enable Control Pin Voltage	0	-	3.6	V
V _{IO}	I/O Pin Voltage	0	-	3.6	V
Δt/ΔV	Input Transition Rise or Fall Time	-	-	10	ns/V
T _A	Operating Temperature Range	-40	-	+85	°C

DC Electrical Characteristics

Unless otherwise specified, -40°C ≤ T_A ≤ 85°C, 1.1V ≤ V_{CC} ≤ 3.6V

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{IHB}	B port Input HIGH Voltage	2.3V ≤ V _{CC(B)} ≤ 3.6V	V _{CCB} - 0.4	-	-	V
		1.5V ≤ V _{CC(B)} < 2.3V	V _{CCB} - 0.2			V
		1.1V ≤ V _{CC(B)} < 1.5V	V _{CCB} - 0.1			V
V _{ILB}	B port Input LOW Voltage			-	0.15	V
V _{IHA}	A port Input HIGH Voltage	2.3V ≤ V _{CC(A)} ≤ 3.6V	V _{CCA} - 0.4			V
		1.5V ≤ V _{CC(A)} < 2.3V	V _{CCA} - 0.2			V
		1.1V ≤ V _{CC(A)} < 1.5V	V _{CCA} - 0.1			V
V _{ILA}	A port Input LOW Voltage	-	-	-	0.15	V
V _{IH(EN)}	Control Pin Input HIGH Voltage	1.5V < V _{CC(A)} ≤ 3.6V	0.65*V _{CCA}	-	-	V
		1.1V ≤ V _{CC(A)} ≤ 1.5V	0.6*V _{CCA}			V
V _{IL(EN)}	Control Pin Input LOW Voltage	1.5V < V _{CC(A)} ≤ 3.6V	-	-	0.35*V _{CCA}	V
		1.1V ≤ V _{CC(A)} ≤ 1.5V			0.2*V _{CCA}	V
V _{OHB}	B port Output HIGH Voltage	B port source current = -20 μA	0.8*V _{CCB}	-	-	V
V _{OLB}	B port Output LOW Voltage	B port sink current = 1 mA	-	-	0.4	V
V _{OHA}	A port Output HIGH Voltage	A port source current = -20 μA	0.8*V _{CCA}	-	-	V
V _{OLA}	A port Output LOW Voltage	A port sink current = 1 mA	-	-	0.4	V
I _{CCB}	V _{CCB} Supply Current	V _I = V _{CCI} ; I _O = 0A; EN = Low or High	V _{CC(A)} = 1.1V to 3.6V, V _{CC(B)} = 1.1V to 3.6V	-	1.0	3 μA
			V _{CC(A)} = 1.1V, V _{CC(B)} = 1.8V	-	0.6	2 μA
			V _{CC(A)} = 1.8V, V _{CC(B)} = 3.3V	-	0.7	2 μA
			V _{CC(A)} = 3.6V, V _{CC(B)} = 0V	-		1 μA
			V _{CC(A)} = 0V, V _{CC(B)} = 3.6V	-		1 μA
I _{CCA}	V _{CCA} Supply Current	V _I = V _{CCI} ; I _O = 0A; EN = Low or High	V _{CC(A)} = 1.1V to 3.6V, V _{CC(B)} = 1.1V to 3.6V	-	0.2	1 μA
			V _{CC(A)} = 3.6V, V _{CC(B)} = 0V	-	-	1 μA
			V _{CC(A)} = 0V, V _{CC(B)} = 3.6V	-	-	1 μA

PI4ULS3V204

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{OZ}	I/O Tri-state Output Mode Leakage Current	-	-	0.1	1.0	μA
I_{I-EN}	Control pin leakage Current	$V_I = V_{CC1}$ or GND	-	-	1	μA
R_{PU}	Pull-Up Resistors I/O A and B	-	-	10	-	$k\Omega$
C_i	EN	$V_{CC(A)} = 3.3V, V_{CC(B)} = 3.3V$	-	-	0.5	pF
C_{iO}	A port	$V_{CC(A)} = 3.3V, V_{CC(B)} = 3.3V$	-	-	5	pF
	B port	$V_{CC(A)} = 3.3V, V_{CC(B)} = 3.3V$	-	-	5	pF

Note: All units are production tested at $T_A = +25^\circ C$. Limits over the operating temperature range are guaranteed by design.

Typical values are for $V_{CCB} = +2.8V$, $V_{CCA} = +1.8V$ and $T_A = +25^\circ C$.

AC Electrical Characteristics

Timing Characteristics – Rail-to-Rail Driving Configuration (I/O test circuits of Figures 2, 3 and 7, $C_{LOAD} = 15\text{ pF}$, driver output impedance $\leq 50\Omega$, $R_{LOAD} = 1\text{ M}\Omega$, $T_A = -40^\circ C$ to $85^\circ C$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{CCA} = 1.2V \pm 0.1V$, $V_{CCB} = 1.8V \pm 0.15V$						
t_{RB}	B port Rise Time	-			20	nS
t_{FB}	B port Fall Time	-			25	nS
t_{RA}	A port Rise Time	-			20	nS
t_{FA}	A port Fall Time	-			20	nS
t_{EN}	Enable Time	-			200	nS
t_{DIS}	Disable Time	-			200	nS
$t_{PHL-A-B}$	Propagation Delay (Driving A)	-			9	nS
$t_{PLH-A-B}$		-			11	nS
$t_{PHL-B-A}$	Propagation Delay (Driving B)	-			9	nS
$t_{PLH-B-A}$		-			10	nS
t_{PPSKEW}	Part-to-Part Skew	-			1	nS
MDR	Maximum Data Rate	-			20	Mbps
$V_{CCA} = 1.2V \pm 0.1V$, $V_{CCB} = 2.5V \pm 0.2V$						
t_{RB}	B port Rise Time	-			12	nS
t_{FB}	B port Fall Time	-			14	nS
t_{RA}	A port Rise Time	-			20	nS
t_{FA}	A port Fall Time	-			25	nS
t_{EN}	Enable Time	-			200	nS
t_{DIS}	Disable Time	-			200	nS
$t_{PHL-A-B}$	Propagation Delay (Driving A)	-			9	nS
$t_{PLH-A-B}$		-			11	nS
$t_{PHL-B-A}$	Propagation Delay (Driving B)	-			9	nS
$t_{PLH-B-A}$		-			10	nS
t_{PPSKEW}	Part-to-Part Skew	-			1	nS
MDR	Maximum Data Rate	-			20	Mbps
$V_{CCA} = 1.2V \pm 0.1V$, $V_{CCB} = 3.3V \pm 0.3V$						
t_{RB}	B port Rise Time	-			12	nS
t_{FB}	B port Fall Time	-			18	nS
t_{RA}	A port Rise Time	-			16	nS
t_{FA}	A port Fall Time	-			30	nS
t_{EN}	Enable Time	-			200	nS
t_{DIS}	Disable Time	-			200	nS
$t_{PHL-A-B}$	Propagation Delay (Driving A)	-			8	nS
$t_{PLH-A-B}$		-			11	nS

PI4ULS3V204

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{PHL-B-A}$	Propagation Delay (Driving B)	-			8	nS
$t_{PLH-B-A}$		-			10	nS
t_{PPSKEW}	Part-to-Part Skew	-			1	nS
MDR	Maximum Data Rate	-			20	Mbps
$V_{CCA} = 1.8V \pm 0.15V$, $V_{CCB} = 1.2V \pm 0.1V$						
t_{RB}	B port Rise Time	-			25	nS
t_{FB}	B port Fall Time	-			25	nS
t_{RA}	A port Rise Time	-			14	nS
t_{FA}	A port Fall Time	-			25	nS
t_{EN}	Enable Time	-			200	nS
t_{DIS}	Disable Time	-			200	nS
$t_{PHL-A-B}$	Propagation Delay (Driving A)	-			10	nS
$t_{PLH-A-B}$		-			15	nS
$t_{PHL-B-A}$	Propagation Delay (Driving B)	-			12	nS
$t_{PLH-B-A}$		-			12	nS
t_{PPSKEW}	Part-to-Part Skew	-			1	nS
MDR	Maximum Data Rate	-			20	Mbps
$V_{CCA} = 1.8V \pm 0.15V$, $V_{CCB} = 2.5V \pm 0.2V$						
t_{RB}	B port Rise Time	-			8	nS
t_{FB}	B port Fall Time	-			8	nS
t_{RA}	A port Rise Time	-			6	nS
t_{FA}	A port Fall Time	-			12	nS
t_{EN}	Enable Time	-			200	nS
t_{DIS}	Disable Time	-			150	nS
$t_{PHL-A-B}$	Propagation Delay (Driving A)	-			5	nS
$t_{PLH-A-B}$		-			4	nS
$t_{PHL-B-A}$	Propagation Delay (Driving B)	-			4	nS
$t_{PLH-B-A}$		-			4	nS
t_{PPSKEW}	Part-to-Part Skew	-			1	nS
MDR	Maximum Data Rate	-			24	Mbps
$V_{CCA} = 1.8V \pm 0.15V$, $V_{CCB} = 3.3V \pm 0.3V$						
t_{RB}	B port Rise Time	-			8	nS
t_{FB}	B port Fall Time	-			8	nS
t_{RA}	A port Rise Time	-			4	nS
t_{FA}	A port Fall Time	-			10	nS
t_{EN}	Enable Time	-			180	nS
t_{DIS}	Disable Time	-			120	nS
$t_{PHL-A-B}$	Propagation Delay (Driving A)	-			6	nS
$t_{PLH-A-B}$		-			4	nS
$t_{PHL-B-A}$	Propagation Delay (Driving B)	-			4	nS
$t_{PLH-B-A}$		-			4	nS
t_{PPSKEW}	Part-to-Part Skew	-			1	nS
MDR	Maximum Data Rate	-			24	Mbps

PI4ULS3V204

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{CCA} = 2.5V \pm 0.2V$, $V_{CCB} = 1.2V \pm 0.1V$						
t_{RB}	B port Rise Time	-			25	nS
t_{FB}	B port Fall Time	-			30	nS
t_{RA}	A port Rise Time	-			12	nS
t_{FA}	A port Fall Time	-			30	nS
t_{EN}	Enable Time	-			200	nS
t_{DIS}	Disable Time	-			180	nS
$t_{PHL-A-B}$	Propagation Delay (Driving A)	-			10	nS
$t_{PLH-A-B}$		-			14	nS
$t_{PHL-B-A}$	Propagation Delay (Driving B)	-			20	nS
$t_{PLH-B-A}$		-			12	nS
t_{PPSKEW}	Part-to-Part Skew	-			1	nS
MDR	Maximum Data Rate	-			20	Mbps
$V_{CCA} = 2.5V \pm 0.2V$, $V_{CCB} = 1.8V \pm 0.15V$						
t_{RB}	B port Rise Time	-			8	nS
t_{FB}	B port Fall Time	-			9	nS
t_{RA}	A port Rise Time	-			9	nS
t_{FA}	A port Fall Time	-			9	nS
t_{EN}	Enable Time	-			200	nS
t_{DIS}	Disable Time	-			120	nS
$t_{PHL-A-B}$	Propagation Delay (Driving A)	-			3	nS
$t_{PLH-A-B}$		-			2	nS
$t_{PHL-B-A}$	Propagation Delay (Driving B)	-			5	nS
$t_{PLH-B-A}$		-			5	nS
t_{PPSKEW}	Part-to-Part Skew	-			1	nS
MDR	Maximum Data Rate	-			24	Mbps
$V_{CCA} = 2.5V \pm 0.2V$, $V_{CCB} = 3.3V \pm 0.3V$						
t_{RB}	B port Rise Time	-			7	nS
t_{FB}	B port Fall Time	-			8	nS
t_{RA}	A port Rise Time	-			4	nS
t_{FA}	A port Fall Time	-			10	nS
t_{EN}	Enable Time	-			200	nS
t_{DIS}	Disable Time	-			120	nS
$t_{PHL-A-B}$	Propagation Delay (Driving A)	-			3	nS
$t_{PLH-A-B}$		-			5	nS
$t_{PHL-B-A}$	Propagation Delay (Driving B)	-			4	nS
$t_{PLH-B-A}$		-			4	nS
t_{PPSKEW}	Part-to-Part Skew	-			1	nS
MDR	Maximum Data Rate	-			24	Mbps
$V_{CCA} = 3.3V \pm 0.3V$, $V_{CCB} = 1.2V \pm 0.1V$						
t_{RB}	B port Rise Time	-			26	nS
t_{FB}	B port Fall Time	-			32	nS
t_{RA}	A port Rise Time	-			12	nS
t_{FA}	A port Fall Time	-			40	nS
t_{EN}	Enable Time	-			120	nS
t_{DIS}	Disable Time	-			300	nS
$t_{PHL-A-B}$	Propagation Delay	-			10	nS

PI4ULS3V204

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{PLH-A-B}$	(Driving A)	-			14	nS
$t_{PHL-B-A}$	Propagation Delay (Driving B)	-			25	nS
$t_{PLH-B-A}$		-			12	nS
t_{PPSKEW}	Part-to-Part Skew	-			1	nS
MDR	Maximum Data Rate	-			20	Mbps
$V_{CCA} = 3.3V \pm 0.3V, V_{CCB} = 1.8V \pm 0.15V$						
t_{RB}	B port Rise Time	-			6	nS
t_{FB}	B port Fall Time	-			11	nS
t_{RA}	A port Rise Time	-			6	nS
t_{FA}	A port Fall Time	-			7	nS
t_{EN}	Enable Time	-			120	nS
t_{DIS}	Disable Time	-			200	nS
$t_{PHL-A-B}$	Propagation Delay (Driving A)	-			4	nS
$t_{PLH-A-B}$		-			4	nS
$t_{PHL-B-A}$	Propagation Delay (Driving B)	-			5	nS
$t_{PLH-B-A}$		-			5	nS
t_{PPSKEW}	Part-to-Part Skew	-			1	nS
MDR	Maximum Data Rate	-			24	Mbps
$V_{CCA} = 3.3V \pm 0.3V, V_{CCB} = 2.5V \pm 0.2V$						
t_{RB}	B port Rise Time	-			6	nS
t_{FB}	B port Fall Time	-			10	nS
t_{RA}	A port Rise Time	-			6	nS
t_{FA}	A port Fall Time	-			7	nS
t_{EN}	Enable Time	-			120	nS
t_{DIS}	Disable Time	-			200	nS
$t_{PHL-A-B}$	Propagation Delay (Driving A)	-			4	nS
$t_{PLH-A-B}$		-			4	nS
$t_{PHL-B-A}$	Propagation Delay (Driving B)	-			4	nS
$t_{PLH-B-A}$		-			4	nS
t_{PPSKEW}	Part-to-Part Skew	-			1	nS
MDR	Maximum Data Rate	-			24	Mbps

Timing Characteristics – Open Drain Driving Configuration
 $(1.1 \leq V_{CCA} \leq V_{CCB} \leq 3.6V, T_A = -40^\circ C \text{ to } 85^\circ C)$

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{RB}	B port Rise Time	-	-	-	300	nS
t_{FB}	B port Fall Time	-	-	-	30	nS
t_{RA}	A port Rise Time	-	-	-	300	nS
t_{FA}	A port Fall Time	-	-	-	30	nS
$t_{PHL-A-B}$	Propagation Delay (Driving A)	-	-	-	20	nS
$t_{PLH-A-B}$		-	-	-	260	nS
$t_{PHL-B-A}$	Propagation Delay (Driving B)	-	-	-	20	nS
$t_{PLH-B-A}$		-	-	-	260	nS
t_{PPSKEW}	Part-to-Part Skew	-	-	-	1	nS
MDR	Maximum Data Rate	-	2	-	-	Mbps

Test Circuits

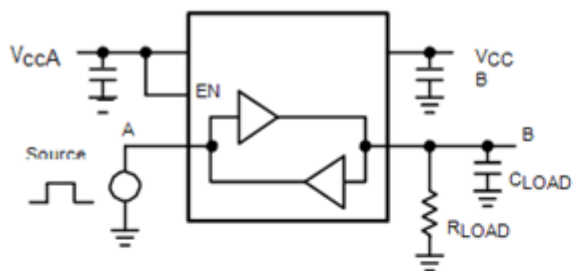


Figure 2. Rail-to-Rail Driving A

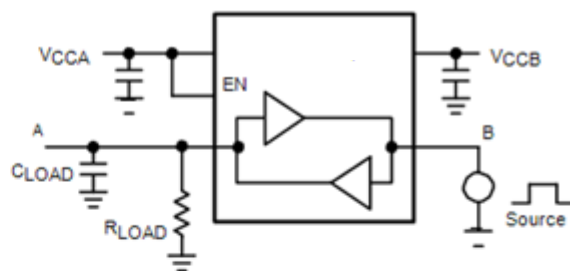


Figure 3. Rail-to-Rail Driving B

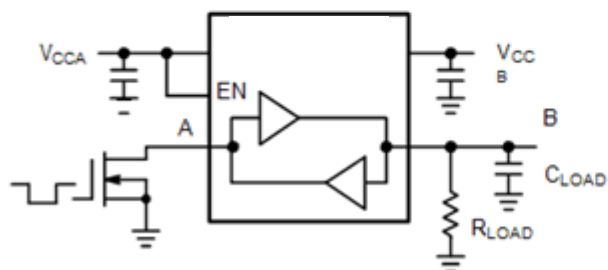


Figure 4. Open-Drain Driving A

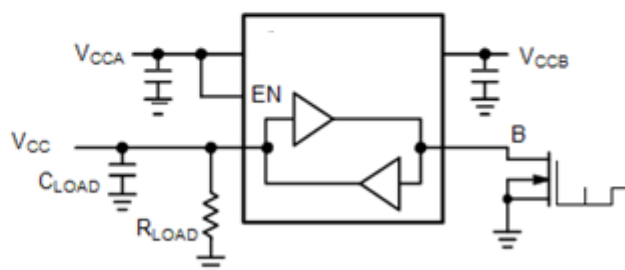


Figure 5. Open-Drain Driving B

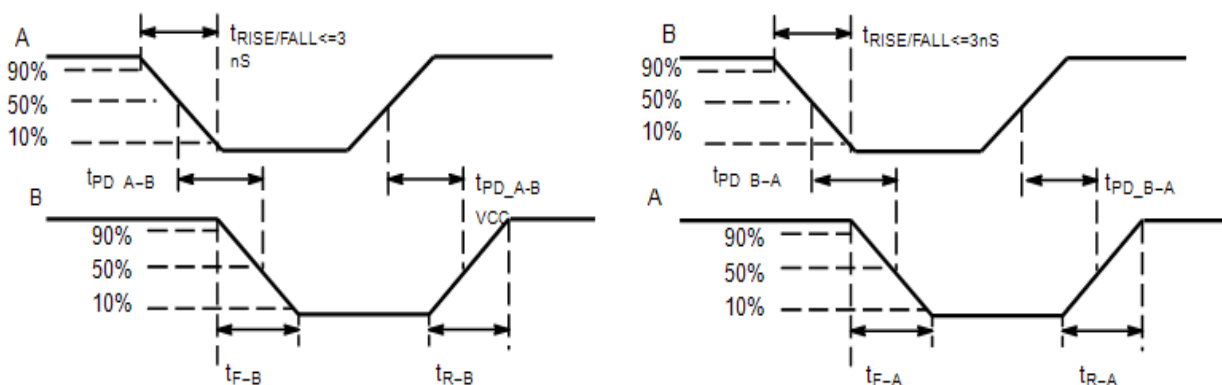
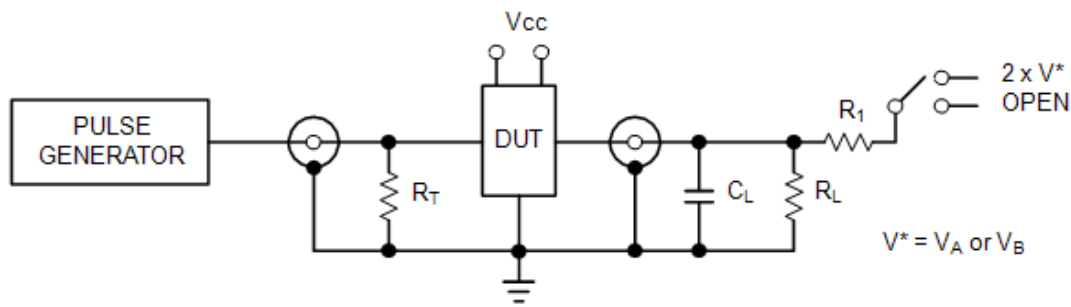


Figure 6. Definition of Timing Specification Parameters



Test	Switch
t_{PZH}, t_{PHZ}	Open
t_{PZL}, t_{PLZ}	$2 \times V^*$

$C_L = 15 \text{ pF}$ or equivalent (Includes jig and probe capacitance)
 $R_L = R_1 = 50 \text{ k}\Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)
 $V^* = V_A$ or V_B for A or B measurements, respectively.

Figure 7. Test Circuit for Enable/Disable Time Measurement

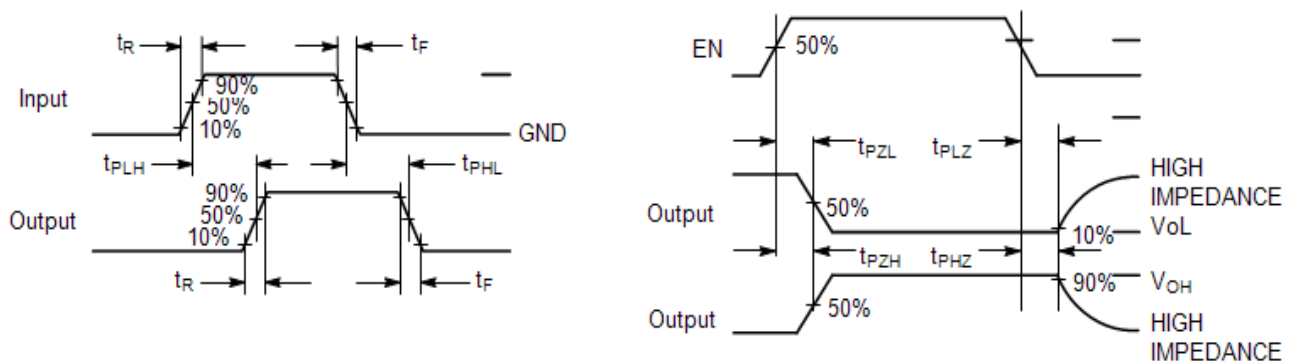


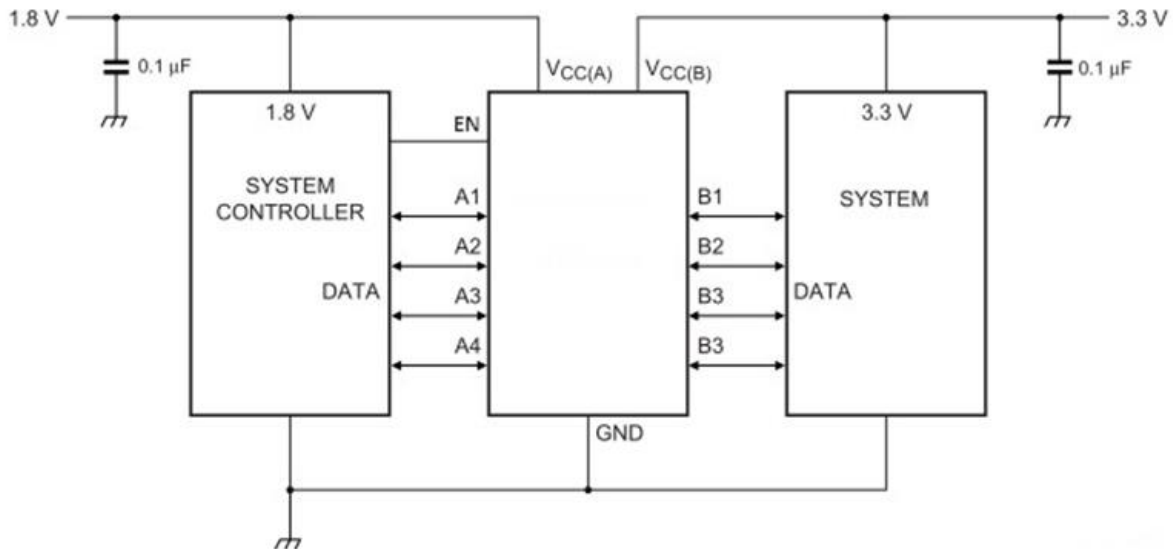
Figure 8. Timing Definitions for Propagation Delays and Enable/Disable Measurement

Functional Description

The PI4ULS3V204 is a 4-bit configurable dual-supply bidirectional auto sensing translator that does not require a directional control pin. The A and B ports are designed to track two different power supply rails, V_{CCA} and V_{CCB} respectively. Both the V_{CCA} and V_{CCB} supply rails are configurable from 1.1 V to 3.6V. This allows voltage logic signals on the V_{CCA} side to be translated into lower, higher or equal value voltage logic signals on the V_{CCB} side, and vice-versa.

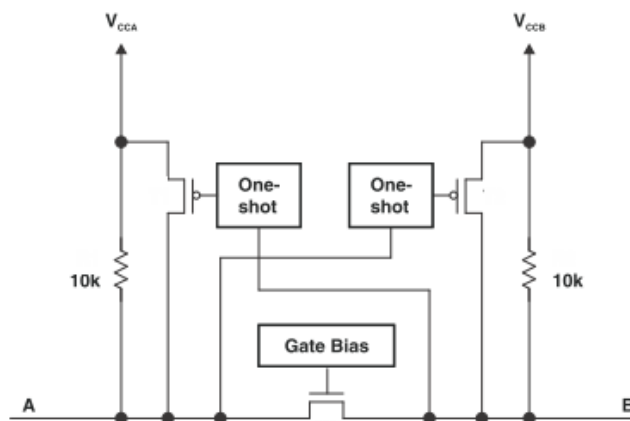
The translator has integrated $10 \text{ k}\Omega$ pull-up resistors on the I/O lines. The integrated pull-up resistors are used to pull-up the I/O lines to either V_{CCA} or V_{CCB} . The PI4ULS3V204 is an excellent match for open-drain applications such as the I²C communication bus.

Application Information



Level Translator Architecture

The PI4ULS3V204 auto sense translator provides bidirectional voltage level shifting to transfer data in multiple supply voltage systems. This device has two supply voltages, V_{CCA} and V_{CCB} , which set the logic levels on the input and output sides of the translator. When used to transfer data from A port to B port, input signals referenced to the V_{CCA} supply are translated to output signals with a logic level matched to V_{CCB} . In a similar manner, translation shifts input signals with a logic level compatible to V_{CCB} to an output signal matched to V_{CCA} . The PI4ULS3V204 consists of two bidirectional channels that independently determine the direction of the data flow without requiring a directional pin. The one-shot circuits are used to detect the rising or falling input signals. In addition, the one shots decrease the rise and fall time of the output signal for high-to-low and low-to-high transitions. Each input/output channel has an internal 10 k Ω pull-up resistors. The magnitude of the pull-up resistors can be reduced by connecting external resistors in parallel to the internal 10 k Ω resistors.



Input Driver Requirements

The rise (t_R) and fall (t_F) timing parameters of the open drain outputs depend on the magnitude of the pull-up resistors. In-addition, the propagation times (t_{PD}), skew (t_{PSKEW}) and maximum data rate depend on the impedance of the device that is connected to the translator. The timing parameters listed in the data sheet assume that the output impedance of the drivers connected to the translator is less than 50 k Ω .

Enable Input (EN)


The PI4ULS3V204 has an Enable pin (EN) that provides tri-state operation at the I/O pins. Driving the Enable pin to a low logic level minimizes the power consumption of the device and drives the I/O V_{CCB} and I/O V_{CCA} pins to a high impedance state. Normal translation operation occurs when the EN pin is equal to a logic high signal. The EN pin is referenced to the V_{CCA} supply and has overvoltage tolerant protection.

Power Supply Guidelines

During normal operation, supply voltage V_{CCA} can be greater than, less than or equal to V_{CCB} . The sequencing of the power supplies will not damage the device during the power up operation. For optimal performance, 0.01 μ F to 0.1 μ F decoupling capacitors should be used on the V_{CCA} and V_{CCB} power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces.

Part Marking

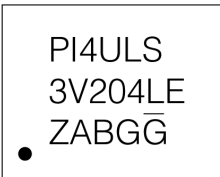
ZB Package



PI4ULS
3V204ZBE
ZYYWWJG

Z: Die Rev
YYWW: Date Code (Year & Workweek)
J: Assembly Site Code
G: Wafer Fab Site Code

L Package



PI4ULS
3V204LE
ZABG \bar{G}

Z: Die Rev
AB: Date Code (Year & Workweek)
G: Assembly Site Code
G: Wafer Fab Site Code
The Bar above 2nd "G" means Cu wire

GA Package

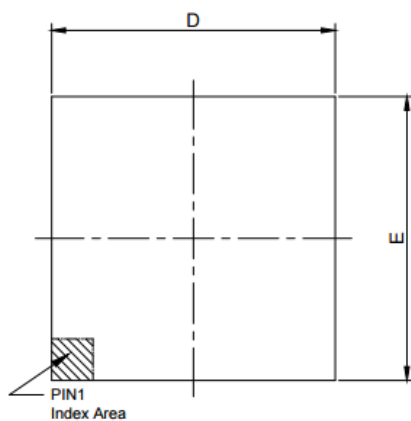


PI4ULS
3V204GAE
ZYYWWXX

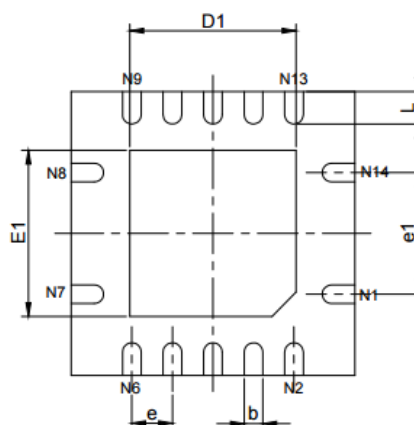
Z: Die Rev
YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

PI4ULS3V204

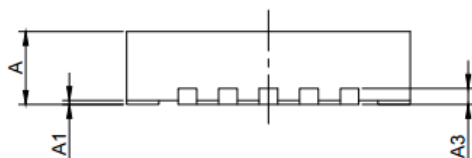
**Packaging Mechanical:
14-TQFN (ZB)**



TOP VIEW



BOTTOM VIEW



SIDE VIEW

PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.80	0.90
A1	0.00	0.05
A3	0.20 REF	
D	3.42	3.58
E	3.42	3.58
D1	1.95	2.15
E1	1.95	2.15
b	0.20	0.30
e	0.50 TYP	
e1	1.50 TYP	
L	0.32	0.48

Note:
1. Ref: JEDEC MO-288B



DATE: 06/18/13

DESCRIPTION: 14-Pin, TQFN, 3.5x3.5

PACKAGE CODE: ZB (ZB14)

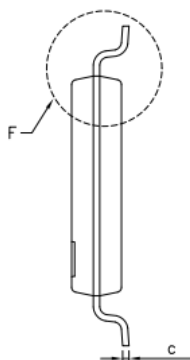
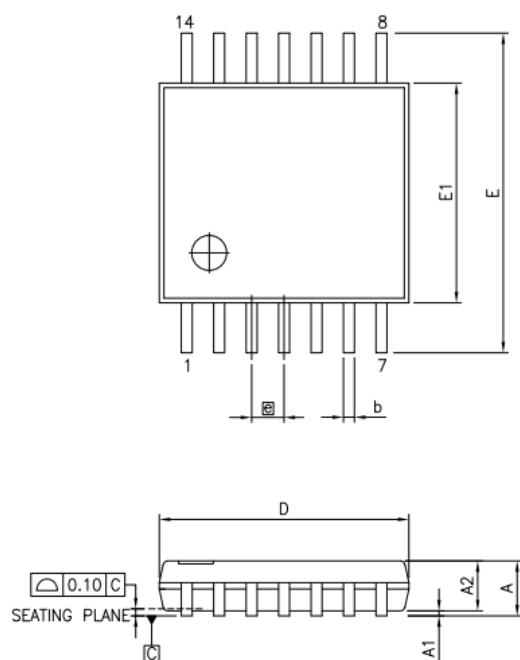
DOCUMENT CONTROL #: PD-2154

REVISION: --

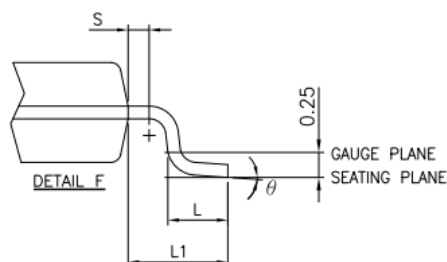
13-0193

PI4ULS3V204

14-TSSOP (L)



SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
c	0.09	—	0.20
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	—	—
θ	0°	—	8°



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
2. JEDEC MO-153F
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

16-0060



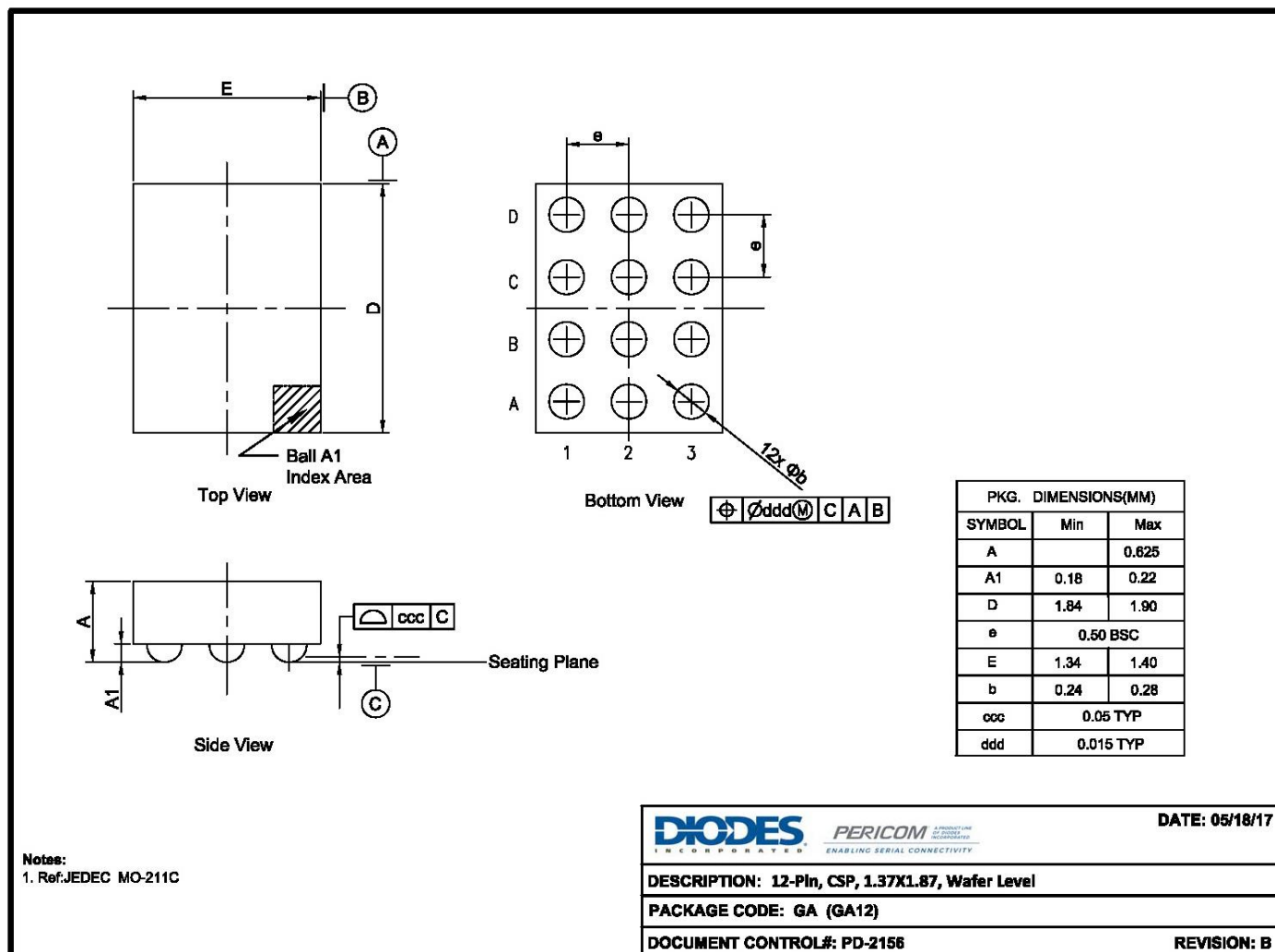
DATE: 03/24/16

DESCRIPTION: 14-Pin, 173mIl Wide TSSOP

PACKAGE CODE: L (L14)

DOCUMENT CONTROL #: PD-1309

REVISION: E

PI4ULS3V204
12-CSP (GA)


17-0369

For latest package info.

 please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>
Ordering Information

Part Number	Package Code	Package Description
PI4ULS3V204LEX	L	14-Pin, 173 mil Wide (TSSOP)
PI4ULS3V204ZBEX	ZB	14-Pin, 3.5x3.5 (TQFN)
PI4ULS3V204GAEX	GA	12-Pin, 1.37x1.87, Wafer Level (CSP)
PI4ULS3V204ZBEX-13R	ZB	14-Pin, 3.5x3.5 (TQFN), Pin 1 orientation is Top Left

Notes:

- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
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- E = Pb-free and Green
- X suffix = Tape/Reel
- For packaging detail, go to our website at: <https://www.diodes.com/assets/MediaList-Attachments/Diodes-Package-Information.pdf>

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