To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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H7P1002DL, H7P1002DS

Silicon P Channel MOS FET
High Speed Power Switching

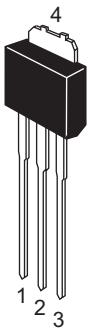
REJ03G1601-0100
Rev.1.00
Nov 16, 2007

Features

- Low on-resistance
  $R_{DS(on)}$ = 85 mΩ typ.
- Low drive current
- 4.5 V gate drive device can driven from 5 V source

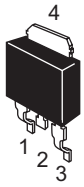
Outline

RENESAS Package code: PRSS0004ZD-B
(Package name: DPAK (L)-(2))

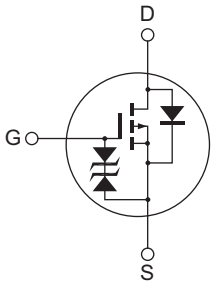


H7P0601DL

RENESAS Package code: PRSS0004ZD-C
(Package name: DPAK (S))



H7P0601DS



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Rating	Unit
Drain to source voltage	V_{DSS}	–100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–15	A
Drain peak current	$I_{D\ (pulse)}$ Note1	–60	A
Body-drain diode reverse drain current	I_{DR}	–15	A
Avalanche current	I_{AP} Note3	–12	A
Avalanche energy	E_{AR} Note3	14.4	mJ
Channel dissipation	Pch Note2	30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. Value at Tc = 25°C
3. Value at Tch = 25°C, Rg ≥ 50 Ω

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Electrical Characteristics

(Ta = 25°C)

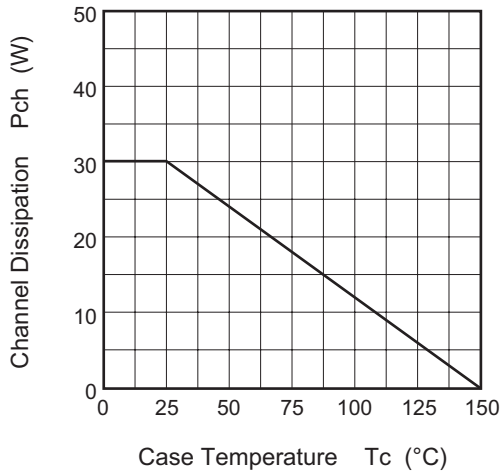
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–100	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –100 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.5	V	I_D = –1 mA, V_{DS} = –10 V Note4
Static drain to source on state resistance	$R_{DS(on)}$	—	85	105	mΩ	I_D = –7.5 A, V_{GS} = –10 V Note4
		—	105	150	mΩ	I_D = –7.5 A, V_{GS} = –4.5 V Note4
Forward transfer admittance	$\|y_{fs}\|$	7.2	12	—	S	I_D = –7.5 A, V_{DS} = –10 V Note4
Input capacitance	Ciss	—	2600	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	190	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	120	—	pF	f = 1 MHz
Total gate charge	Qg	—	45	—	nC	V_{DD} = –50 V
Gate to source charge	Qgs	—	6.5	—	nC	V_{GS} = –10 V
Gate to drain charge	Qgd	—	9.0	—	nC	I_D = –15 A
Turn-on delay time	$t_{d(on)}$	—	23	—	ns	V_{GS} = –10 V, I_D = –7.5 A
Rise time	t_r	—	45	—	ns	R_L = 4.0 Ω
Turn-off delay time	$t_{d(off)}$	—	80	—	ns	Rg = 4.7 Ω
Fall time	t_f	—	13	—	ns	
Body-drain diode forward voltage	V_{DF}	—	–0.91	—	V	I_F = –15 A, V_{GS} = 0
Body-drain diode reverse recovery time	t_{rr}	—	50	—	ns	I_F = –15 A, V_{GS} = 0 di_F/dt = 100 A/µs

Note: 4. Pulse test

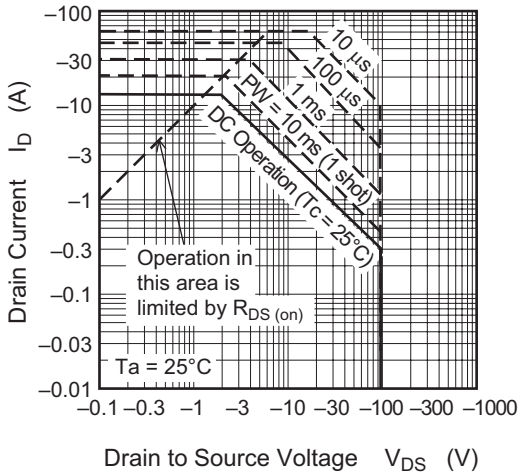
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Main Characteristics

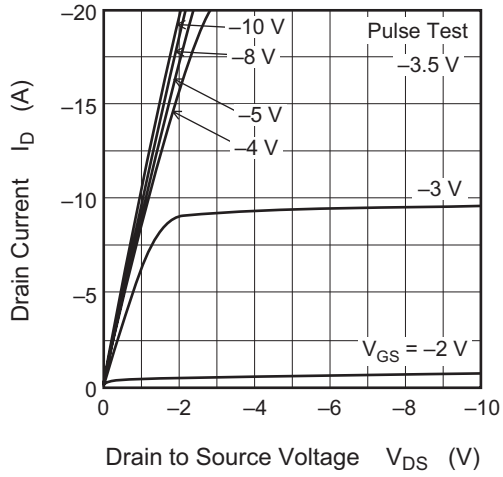
Power vs. Temperature Derating



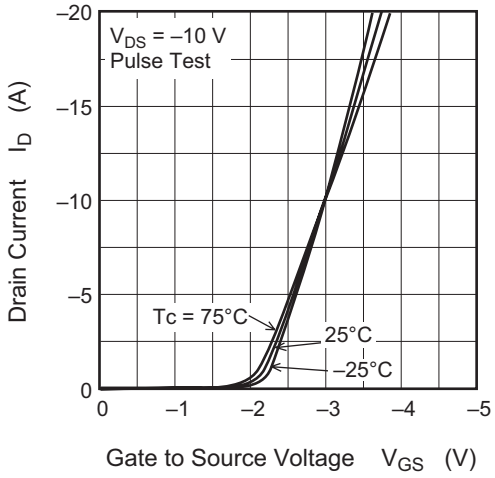
Maximum Safe Operation Area



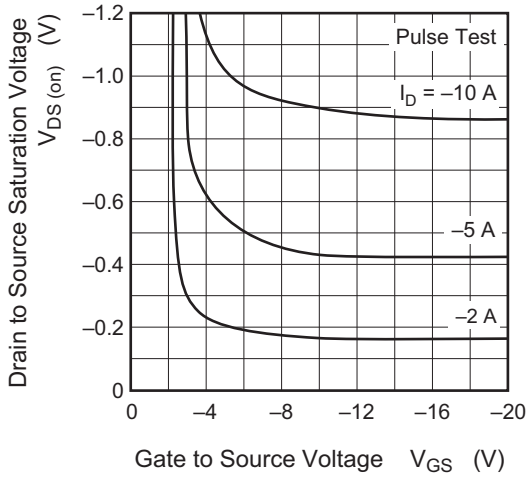
Typical Output Characteristics



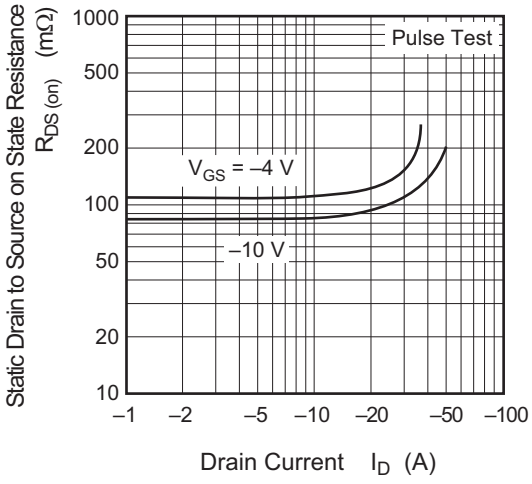
Typical Transfer Characteristics



Drain to Source Saturation Voltage vs. Gate to Source Voltage

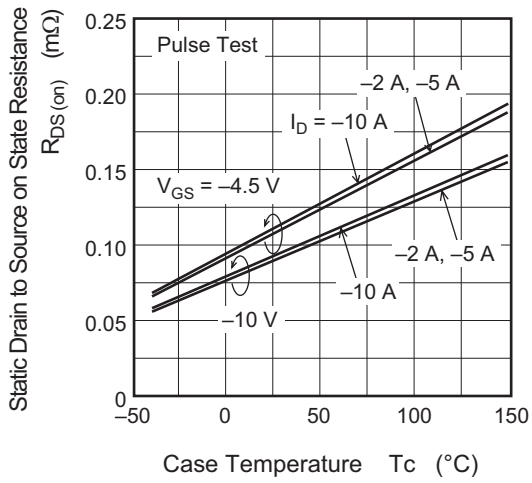


Static Drain to Source on State Resistance vs. Drain Current

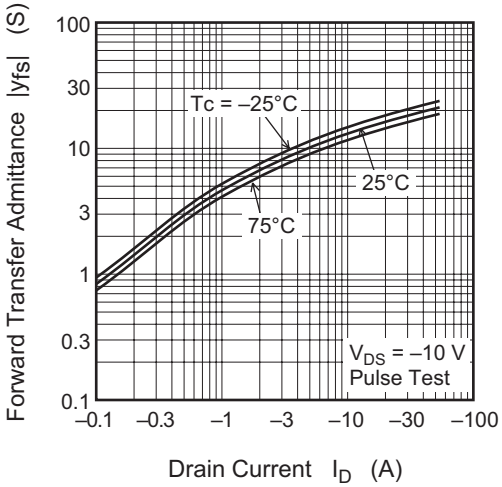


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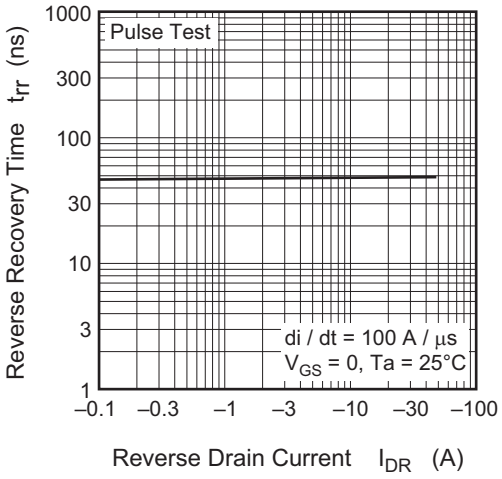
Static Drain to Source on State Resistance vs. Temperature



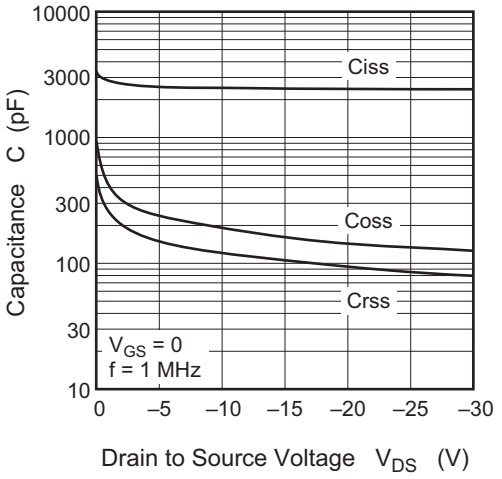
Forward Transfer Admittance vs. Drain Current



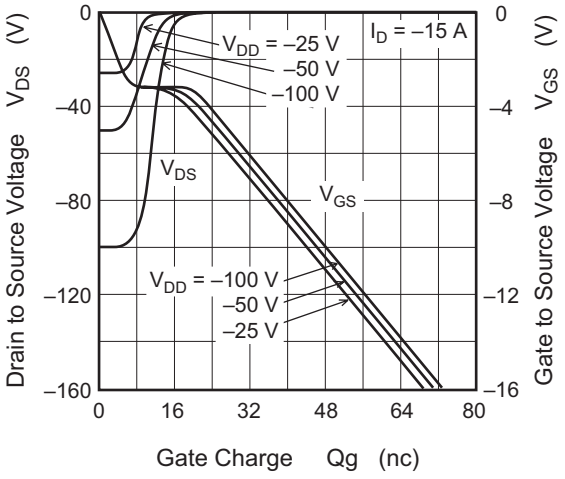
Body-Drain Diode Reverse Recovery Time



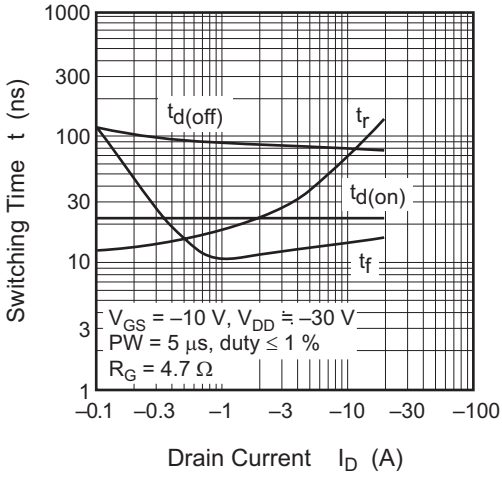
Typical Capacitance vs. Drain to Source Voltage



Dynamic Input Characteristics

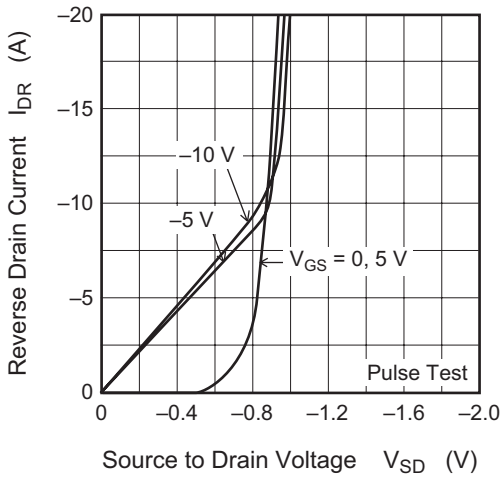


Switching Characteristics

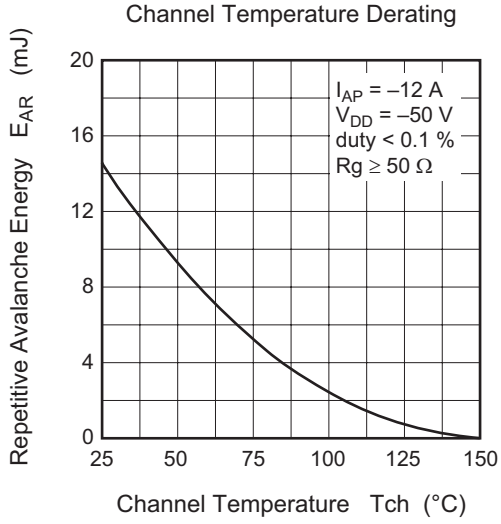


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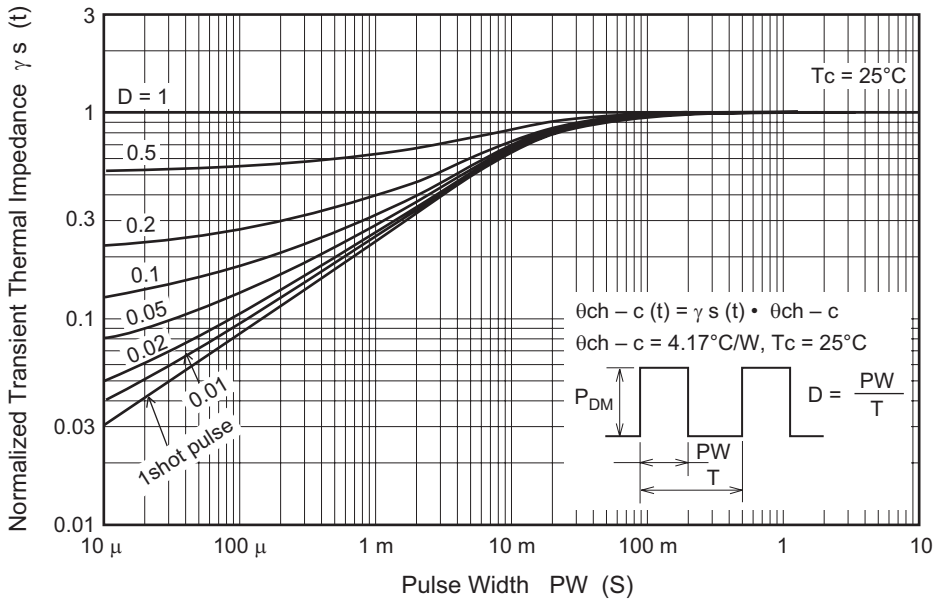
Reverse Drain Current vs. Source to Drain Voltage



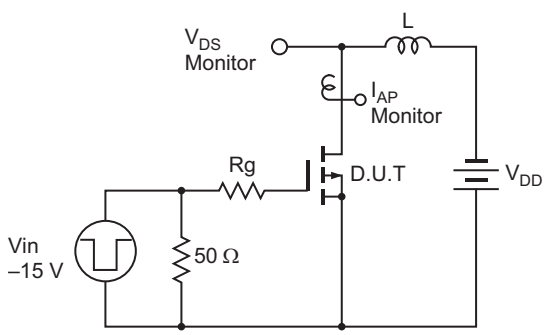
Maximum Avalanche Energy vs. Channel Temperature Derating



Normalized Transient Thermal Impedance vs. Pulse Width

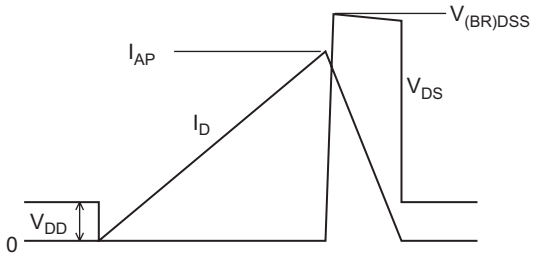


Avalanche Test Circuit



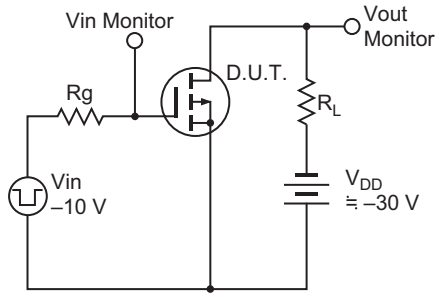
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

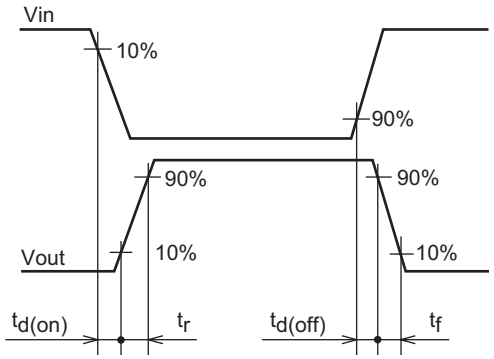


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Switching Time Test Circuit



Waveform



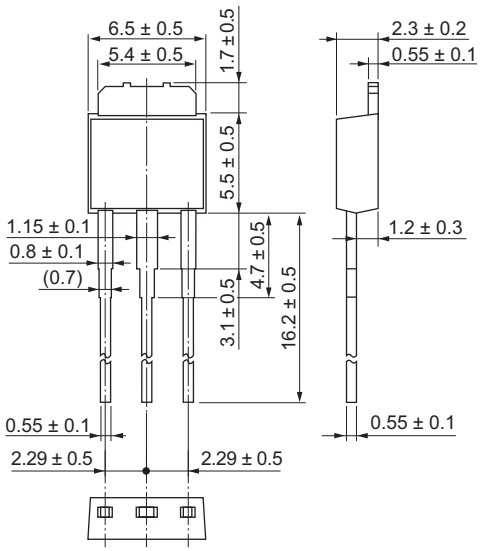
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Package Dimensions

• H7P1002DL

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
DPAK(L)-(2)	—	PRSS0004ZD-B	DPAK(L)-(2) / DPAK(L)-(2)V	0.42g

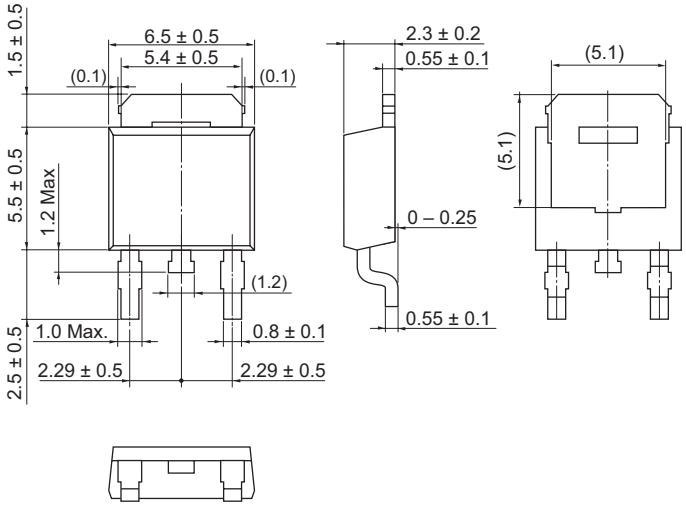
Unit: mm



• H7P1002DS

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
DPAK(S)	SC-63	PRSS0004ZD-C	DPAK(S) / DPAK(S)V	0.28g

Unit: mm



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H7P1002DL-E	3200 pcs	Hold Box, Radial Taping
H7P1002DSTL-E	3000 pcs	Taping

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