NCP81174

4/3/2-Phase Synchronous Buck Controller with Power Saving Mode and PWM VID Interface

The NCP81174 is a general−purpose up to four−phase synchronous buck controller. It combines differential voltage sensing, differential phase current sensing, and PWM VID interface to provide accurate regulated power for the computer or graphic controllers. It can receive power saving command (PSI) from processors and operates in single−phase diode emulation mode to obtain high efficiency in light load. Dual−edge multiphase PWM modulation ensures a fast transient response with minimum possible capacitors.

Features

- Output Voltage up to 2.0 V with PWM VID Interface
- Support 1.8 V and 3.3 V VID interface
- Remote Differential Output Voltage Sense
- Differential Current Sense For Each Phase
- 200 kHz − 1000 kHz Switching Frequency
- Power Saving Interface (PSI)
- Power Good Output
- Thermally Compensated Current Monitoring
- Over Current Protection
- Fast Transient Response
- 5 V V_{CC} Shunt Regulator
- Latched OVP and UVP Protections
- QFN−32, 5 x 5 mm, 0.5 mm Pitch Package
- This is a Pb−Free Device

Typical Applications

- GPU and CPU Power
- Graphics Card Applications
- Desktop and Notebook Applications

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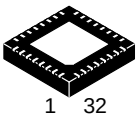
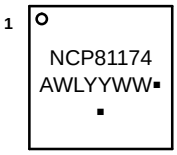


QFN32
MW SUFFIX
CASE 488AM

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NCP81174MNTXG	QFN32 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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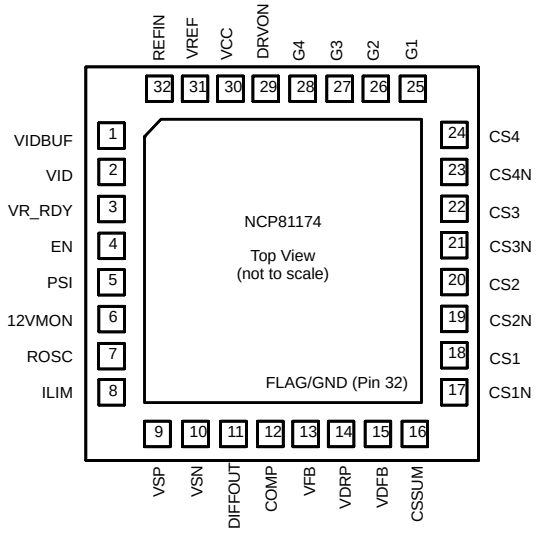

Figure 1. Pinout

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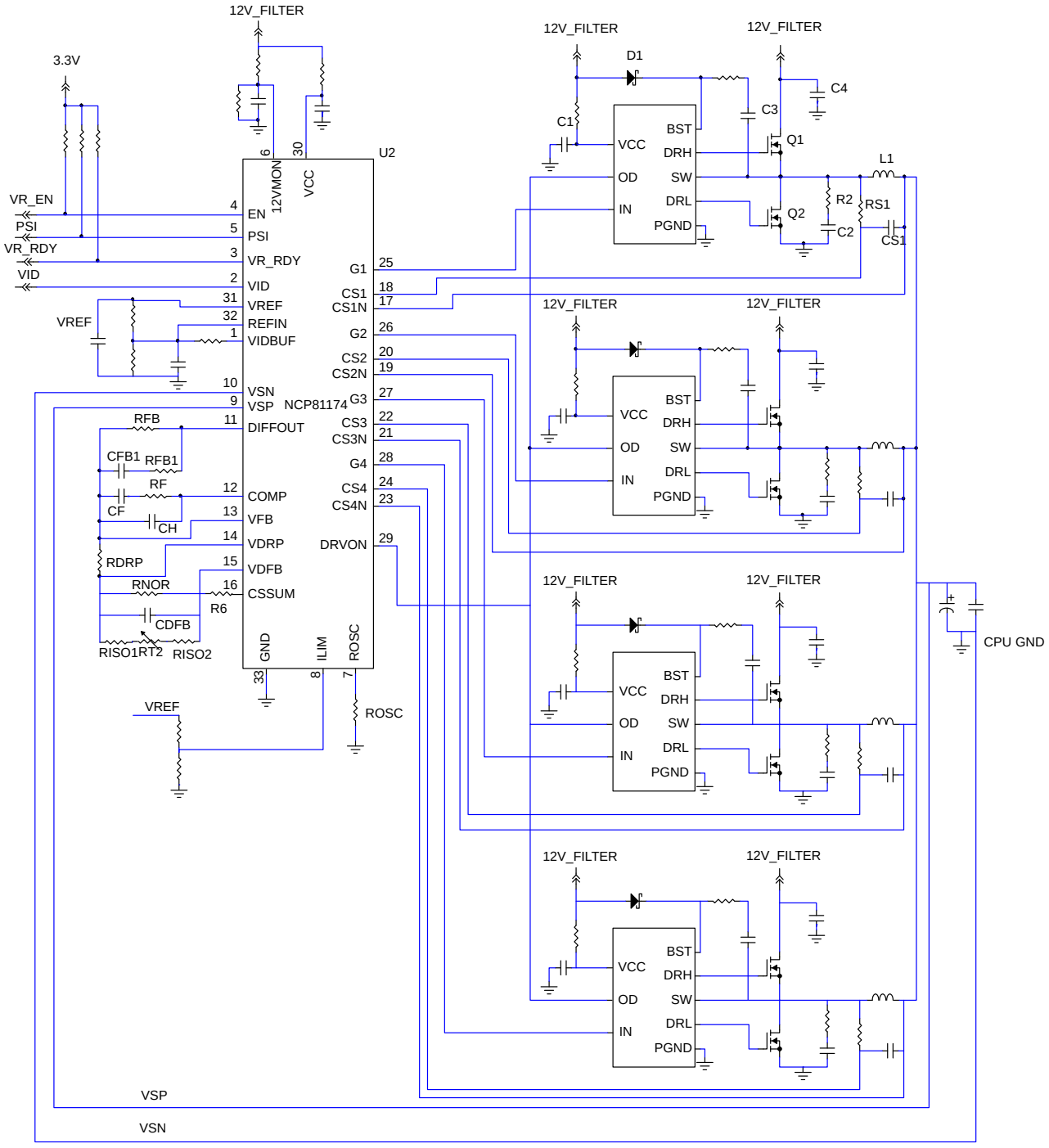

Figure 2. Typical Four Phase Application Circuit with PWM−VID Interface

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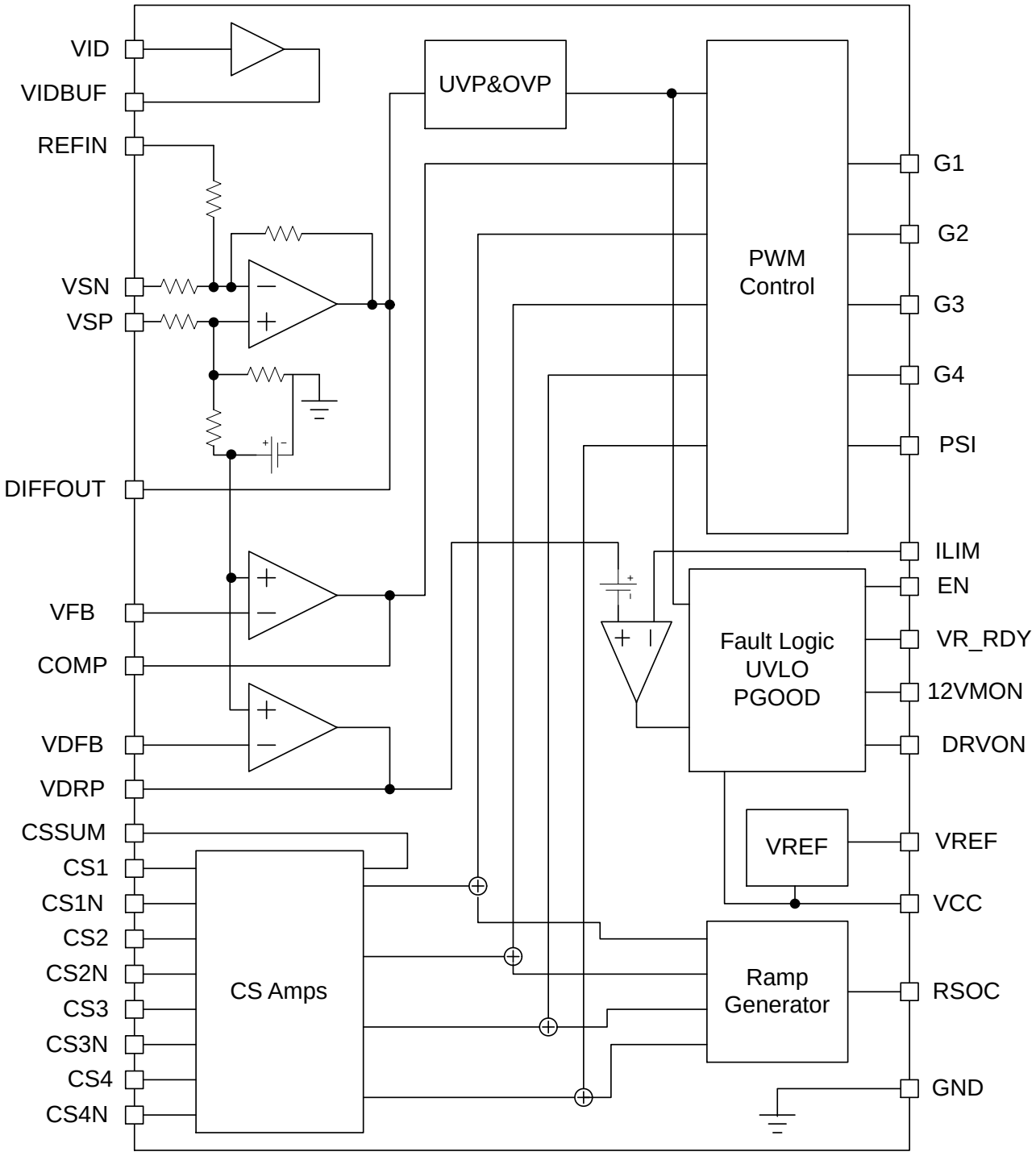

Figure 3. Functional Block Diagram

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PIN DESCRIPTION

Pin	Name	Description
1	VIDBUF	VID PWM pulse output from an internal buffer.
2	VID	Voltage ID from processor.
3	VR_RDY	Power good indicator.
4	EN	Chip enable.
5	PSI	Power saving control. Three levels.
6	12VMON	12 V input power rail monitor. It is a divided down voltage from the input power rail, should be kept to less than 4 V at all time.
7	ROSC	A resistance from this pin to ground programs the oscillator frequency.
8	ILIM	Over current shutdown threshold setting.
9	VSP	Non−inverting input to the internal differential remote sense amplifier.
10	VSN	Inverting input to the internal differential remote sense amplifier.
11	DIFFOUT	Output of the differential remote voltage sense amplifier.
12	COMP	Output of the compensation amplifier.
13	VFB	Inverting input of the compensation error amplifier
14	VDRP	Voltage signal proportional to the total current.
15	VDFB	Current summing amplifier inverting input
16	CSSUM	Current summing output signal
17	CS1N	Inverting input to current sense amplifier, phase 1.
18	CS1	Non−inverting input to current sense amplifier, phase 1.
19	CS2N	Inverting input to current sense amplifier, phase 2.
20	CS2	Non−inverting input to current sense amplifier, phase 2.
21	CS3N	Inverting input to current sense amplifier, phase 3.
22	CS3	Non−inverting input to current sense amplifier, phase 3.
23	CS4N	Inverting input to current sense amplifier, phase 4.
24	CS4	Non−inverting input to current sense amplifier, phase 4.
25	G1	Phase 1 PWM output, 3 levels.
26	G2	Phase 2 PWM output, 3 levels.
27	G3	Phase 3 PWM output, 3 levels.
28	G4	Phase 4 PWM output, 3 levels.
29	DRVON	Gate driver enable.
30	VCC	Power supply for the chip. NCP81174 has a built−in 5 V shunt regulator, allowing it to connect to the external 12 V supply through a resistor. Do not connect a 5 V supply to VCC directly.
31	VREF	2.0 V output reference voltage. A 10 nF ceramic capacitor is recommended to connect this pin to ground.
32	REFIN	Reference voltage input for output voltage regulation.
33	FLAG	Thermal pad and analog ground, connected to system ground.

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MAXIMUM RATINGS

ELECTRICAL INFORMATION

Pin Symbol	VMAX	VMIN	ISOURCE	ISINK
COMP	5.5 V	−0.3 V	10 mA	10 mA
VDRP	5.5 V	−0.3 V	5 mA	5 mA
VSP	5.5 V	GND – 300 mV	1 mA	1 mA
VSN	GND + 300 mV	GND – 300 mV	1 mA	1 mA
DIFFOUT	5.5 V	−0.3 V	20 mA	20 mA
VR_RDY	5.5 V	−0.3 V	N/A	20 mA
VCC	7.0 V	−0.3 V	N/A	10 mA
ROSC	5.5 V	−0.3 V	1 mA	N/A
PWMVID	5.5 V	−0.3 V (−2 V, <50 ns)		
All Other Pins	5.5 V	−0.3 V		

*All signals referenced to AGND unless otherwise noted.

THERMAL INFORMATION

Rating	Symbol	Value	Unit
Thermal Characteristic, QFN Package (Note 1)	R_{thja}	48.5	°C/W
Junction Temperature Range (Note 2)	T_J	−40 to 125	°C
Operating Ambient Temperature Range	T_A	0 to 100	°C
Maximum Storage Temperature Range	T_{STG}	−55 to +150	°C
Moisture Sensitivity Level, QFN Package	MSL	1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*The maximum package power dissipation must be observed.
1. JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM.
2. JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM.

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ELECTRICAL CHARACTERISTICS

(V_{VCC} = 5 V, V_{REFIN} = 1.0 V, V_{PSI} = 3.3 V, typical values are referenced to T_A = 25°C, Min and Max values are referenced to T_A from 0°C to 100°C. unless other noted.)

Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE						
System Input Voltage Range		V_{SYS}	7.0		20	V
SUPPLY CURRENT						
DC Supply Current	Vsys = 13.2 V, Rshunt = 150			54	60	mA
UVLO Turn−On Current				30	35	mA
VCC UVLO Rising				4.9	5.2	V
VCC UVLO Falling			3.8	4.1		V
VCC Quiescent Current	no switching, PS0 no switching, PS1/PS2	I_{CC}	− −	46 46	− −	mA mA
SWITCHING FREQUENCY						
PS0 Switching Frequency Range		F_{sw}	200		1000	kHz
Switching Frequency Accuracy					10	%
ROSC Output Voltage				2.0	2.05	V
VOLTAGE REFERENCE						
VREF Reference Voltage	I_{REF} = 1 mA	V_{VREF}	1.98	2.0	2.02	V
PWM MODULATION						
Minimum On Time (Note 3)	Fsw = 800 kHz		−	30	−	ns
0% Duty Cycle	COMP voltage when the PWM outputs remain HI		−	1.3	−	V
100% Duty Cycle	COMP voltage when the PWM outputs remain HI		−	2.3	−	V
PWM Phase Angle Error	Between adjacent phases		−15		15	°
VOLTAGE ERROR AMPLIFIER						
Open−Loop DC Gain (Note 3)				100		dB
Unity Gain Bandwidth (Note 3)				10		MHz
Slew Rate (Note 3)				5		V/μs
COMP Voltage Swing	I_{COMP}(source) = 2 mA		3.5	−	−	V
	I_{COMP}(sink) = 0.2 mA		−	−	50	mV
Non−inverting Voltage Range (Note 3)			0	1.3	3	V
Input Bias Current			−50	0	50	nA
Input Offset Voltage (Note 3)	VSP = VSN = 1.0 V		−1.0		1.0	mV
CURRENT−SENSE AMPLIFIER						
Input Bias Current	CSx = CSxN = 1.0 V		−200	0	200	nA
Input Offset Voltage (Note 3)			−1.0		1.0	mV
Common Mode Input Range (Note 3)			−0.3		2.0	V
Differential Mode Input Range			−120		120	mV
Closed−Loop DC Gain (Note 3)	0 V < CSx − CSxN < 0.1 V		5.7	6.0	6.3	V/V
−3dB Gain Bandwidth (Note 3)				10		MHz
Current Sharing Offset			−2.5	−	2.5	mV

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3. Guaranteed by design, may not be tested.

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ELECTRICAL CHARACTERISTICS

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Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
CURRENT SUMMING AMPLIFIER						
Current Sense Input to CSSUM DC Gain	−60 mV < CSx − CSxN < 60 mV			−3.93		V/V
Current Sense Input to CSSUM −3 dB Bandwidth (Note 3)	CL = 10 pF to GND, RL = 10 kΩ to GND			4		MHz
CSSUM Output Slew Rate (Note 3)				4		V/μs
CSSUM Summing Amp Output Offset (Note 3)			−15	0	15	mV
Maximum CSSUM Output Voltage			3.0			V
Minimum CSSUM Output Voltage					0.3	V
Output Source Current (Note 3)			1	–	–	mA
Output Sink Current (Note 3)			1	–	–	mA
DROOP AMPLIFIER VDRP						
Input Bias Current (Note 3)			−200		200	nA
Input Offset Voltage (Note 3)	VSP = VSN = 1.1 V		−4.0		4.0	mV
Open Loop DC Gain (Note 3)	CL = 20 pF to GND including ESD RL = 1 kΩ to GND		–	100		dB
Open Loop Unity Gain Bandwidth (Note 3)	CL = 20 pF to GND including ESD RL = 1 kΩ to GND		–	10	–	MHz
Maximum Output Voltage	I_{SOURCE} = 4.0 mA		3	–	–	V
Minimum Output Voltage	I_{SINK} = 1.0 mA		–	–	1	V
Output source current (Note 3)	Vout = 3.0 V		4	–	–	mA
Output sink current (Note 3)	Vout = 1.0 V		1	–	–	mA
REMOTE VOLTAGE DIFFERENTIAL SENSE AMPLIFIER						
Input Bias Current (Note 3)	VSN = 0 V			30		μA
VSP Input Pull down Resistance	DRVON = low DRVON = high			1.5 17		kΩ
VSP Input Bias Voltage (Note 3)	DRVON = low DRVON = high			0.09 0.66		V
Input Voltage Range (Note 3)			−0.3	–	3.0	V
3dB Bandwidth (Note 3)	CL = 80 pF to GND, RL = 10 kΩ to GND		–	10	–	MHz
Closed Loop DC gain	VSP −VSN = 0.5 to 1.3 V		0.98	1.0	1.025	V/V
Maximum Output Voltage	I_{SOURCE} = 2 mA		3.0	–	–	V
Minimum Output Voltage	I_{SINK} = 2 mA		–	–	0.5	V
Output source current (Note 3)	Vout = 3 V		2.0	–	–	mA
Output sink current (Note 3)	Vout = 0.5 V		2.0	–	–	mA
DRVON						
Output High Voltage	Sourcing 500 μA		3.0	–	–	V
Output Low Voltage	Sinking 500 μA		–	–	0.7	V
Rise Time	CL (PCB) = 20 pF, ΔVo = 10% to 90%		–	20	–	ns

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ELECTRICAL CHARACTERISTICS

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Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
DRVON						
Fall Time	CL (PCB) = 20pF, ΔVo = 10% to 90%		−	20	−	ns
ENABLE						
Enable Threshold	EN rising		−	1.1	1.15	V
	EN falling		0.95	1.0		
EN 3.3V IO Detection Threshold	EN rising			2.5	2.55	V
	EN falling		2.35	2.4		
EN Input Bias Current	External 1k pull−up to 3.3 V		−	−	1.0	μA
POWER SAVE INPUT						
PSI High Threshold (3.3 V input logic), Refer to Table 1	Rising Falling	$V_{highPSI_3.3V}$	 2.05	2.4 2.2	2.55	V
PSI High Threshold (1.8 V input logic), Refer to Table 2	Rising Falling	$V_{highPSI_1.8V}$	 1.05	1.4 1.2	1.55	V
PSI Low Threshold	Rising Falling	V_{lowPSI}	 0.5	0.8 0.6	0.95	V
PSI Input Bias Current (Note 3)			−	−	1.0	μA
PWM OUTPUTS						
Output High Voltage	Sourcing 500 μA		3.0	−	−	V
Mid Output Voltage			1.4	1.5	1.6	V
Output Low Voltage	Sinking 500 μA		−	−	0.7	V
Rise Time	CL (PCB) = 50 pF, ΔVo = 10% to 90%		−	10	15	ns
Fall Time	CL (PCB) = 50 pF, ΔVo = 10% to 90%		−	10	15	ns
4/3/2 PHASE DETECTION						
Gate Pin Source Current			−	80	−	uA
Gate Pin Threshold Voltage			210	240	265	mV
Phase Detect Timer			−	20	27	μs
VR_RDY – STARTUP						
Vout Startup Delay	Measured from EN to Vout Start up from 0 V			1.3		ms
VR_RDY Startup Delay	Measured from EN to VR_RDY assertion			1.9		ms
VR_RDY Shutdown Delay	Measured from EN to VR_RDY de−assertion			200	350	ns
VR_RDY Low Voltage	I_{VR_RDY}= 10 mA (sink)		−	−	0.4	V
VR_RDY Leakage Current	VR_RDY = 5 V		−	−	0.2	μA
PROTECTION – OCP, OVP, UVP						
Current Limit ILIM to VDRP Gain			0.95	1.0	1.05	V/V
Current Limit ILIM to VDRP Gain in PSI				0.25		V/V

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ELECTRICAL CHARACTERISTICS

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Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
PROTECTION – OCP, OVP, UVP						
Current Limit ILIM Input Range			0		2.0	V
Under Voltage Protection (UVP) Threshold	Relative to REFIN Voltage			50%		REFIN
Under Voltage Protection (UVP) Delay				5		μs
Over Voltage Protection (OVP) Threshold	Relative to REFIN Voltage			150%		REFIN
Over Voltage Protection (OVP) Threshold Clamping Voltage				2		V
Over Voltage Protection (OVP) Delay				5		us
12VMON						
12VMON Rising				0.94	1.0	V
12VMON Falling			0.65	0.87		V
12VMON Range (Note 3)					4.0	V
PWM−VID BUFFER						
Buffer Output Rise Time		T_r		3.0		ns
Buffer Output Fall Time		T_f		3.0		ns
Rising and Falling Edge Delay (Note 3)	$\Delta T = \lvert T_r - T_f \rvert$	ΔT			0.5	ns
Propagation Delay	$T_{pd} = T_{pHL} = T_{pLH}$	T_{pd}		8.0		ns
Propagation Delay Error (Note 3)	$\Delta T_{pd} = T_{pHL} - T_{pLH}$	ΔT_{pd}			0.5	ns
REFIN						
REFIN Discharge Switch ON−Resistance	I_{REFIN} (sink) = 2 mA			6.0		Ω
REFIN Discharge Time (Note 3)	Measured from EN assertion			100		μs

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DETAILED DESCRIPTION

General

The NCP81174, a 4/3/2−phase synchronous buck controller with PWM VID interface in a QFN−32 package, provides a compact−footprint power management solution for new generation computing and graphic processors. It receives power saving input (PSI) from processors and operates in 1−phase forced PWM or diode emulation mode to obtain high efficiency in light−load conditions. It can either receive PWMVID from the processor to achieve dynamic voltage control or locally set the reference from an internal precise 2 V regulator. Operating in high switching frequency up to 1 MHz allows employing small size inductor and capacitors. Introduction of dual−edge current mode multi−phase control results in fast transient response and good dynamic current balance.

Power Operation Modes

The NCP81174 has three power operation modes corresponding to PSI levels as shown in Table 1 and 2. The chip is compatible to different I/O systems. If the upstream controller has a 3.3 V or higher I/O interface, the configuration would follow Table 1, the ENABLE signal needs to be higher than 2.5 V to turn on the chip; If the upstream controller has a 1.8 V I/O interface, the configuration would follow Table 2, the ENABLE signal needs to be higher than 1.1 V only to turn on the chip. The operation mode can be changed on the fly.

Table 1. POWER SAVING INTERFACE (PSI) CONFIGURATIONS (3.3 V I/O, EN > 2.5 V)

PSI Level	Power Mode	Phase Configuration
High (PSI ≥ 2.4 V)	PS0	Full Phase, FCCM
Intermediate (0.8V < PSI < 2.4 V)	PS1	1−Phase, FCCM
Low (PSI ≤ 0.8 V)	PS2	1−Phase, Auto CCM/DCM

Table 2. POWER SAVING INTERFACE (PSI) CONFIGURATIONS (1.8 V I/O, 2.5 V > EN > 1.1 V)

PSI Level	Power Mode	Phase Configuration
High (PSI ≥ 1.4 V)	PS0	Full Phase, FCCM
Intermediate (0.8 V < PSI < 1.4 V)	PS1	1−Phase, FCCM
Low (PSI ≤ 0.8 V)	PS2	1−Phase, Auto CCM/DCM

Remote Voltage Sense

A true differential amplifier allows the NCP81174 to measure Vcore voltage feedback with respect to the Vcore ground reference point by connecting the Vcore reference point to VSP, and the Vcore ground reference point to VSN. This configuration keeps ground potential differences between the local controller ground and the Vcore ground reference point from affecting regulation of Vcore between Vcore and Vcore ground reference points. The remote sensing amplifier also subtracts the REFIN (DAC) voltage, thereby producing an unamplified output error voltage at the DIFFOUT pin. This output also has a 1.3 V bias voltage as the floating ground to allow both positive and negative error voltages.

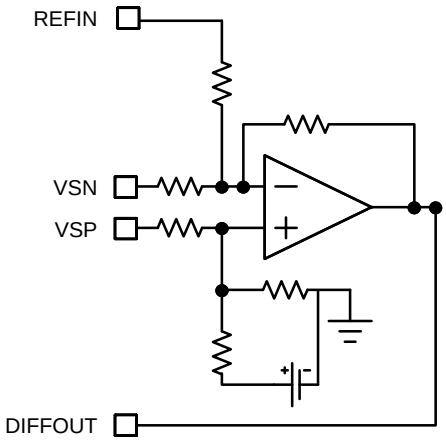

Figure 4. Voltage Remote Sense

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Switching Frequency

The Rosc pin provides a 2.0 V reference voltage. The resistor connected to this pin will sink current from the pin to ground. This current is internally mirrored into a capacitor to create an oscillator. The period is proportional to the resistance and the frequency is inversely proportional to the total resistance. The total resistance may be estimated by equation 1. This equation is valid for the individual phase frequency in multi−phase mode PS0 and single phase mode PS1. In PS2, the frequency will be close to set frequency in CCM and scaled down with load current in DCM operation.

$$Rosc \cong 20947 \cdot F_{SW}^{-1.1262} \quad \text{(eq. 1)}$$

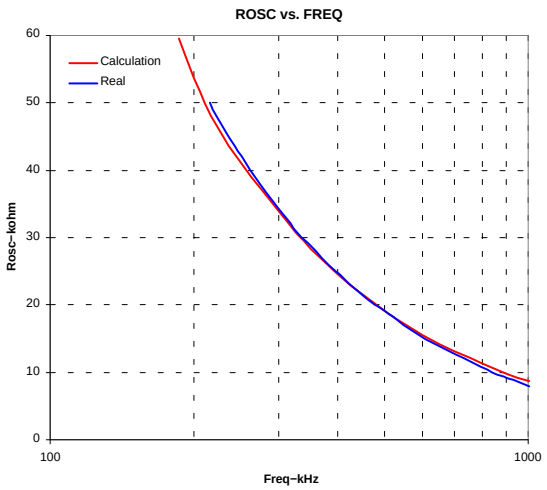

Figure 5. ROSC vs. Frequency

PWM VID

The NCP81174 receives the PWMVID signal from the upstream controller for the Vcore regulation. The signal is decoded internally and passed to the VID buffer output (VIDBUF), where the duty cycle is converted to a corresponding signal between 0 V and 2 V. The VIDBUF high level is derived from a precise 2.0 V reference voltage. The VIDBUF signal is then filtered through the external low pass filter constructed by R_REFADJ and C_REFIN. The filtered output is connected to the REFIN pin. The REFIN is the voltage reference of the Vcore regulator. The output voltage maximum, minimum, and also boot voltage can be calculated with below equations.

$$V_{max} = Vref \cdot \frac{R_VREF2}{R_{VREF2} + (R_VREF1 \parallel R_REFADJ)} \quad \text{(eq. 2)}$$

$$V_{min} = Vref \cdot \frac{R_VREF2 \parallel R_REFADJ}{R_{VREF1} + (R_VREF2 \parallel R_REFADJ)} \quad \text{(eq. 3)}$$

$$V_{boot} = \frac{V_{max} + V_{min}}{2} \quad \text{(eq. 4)}$$

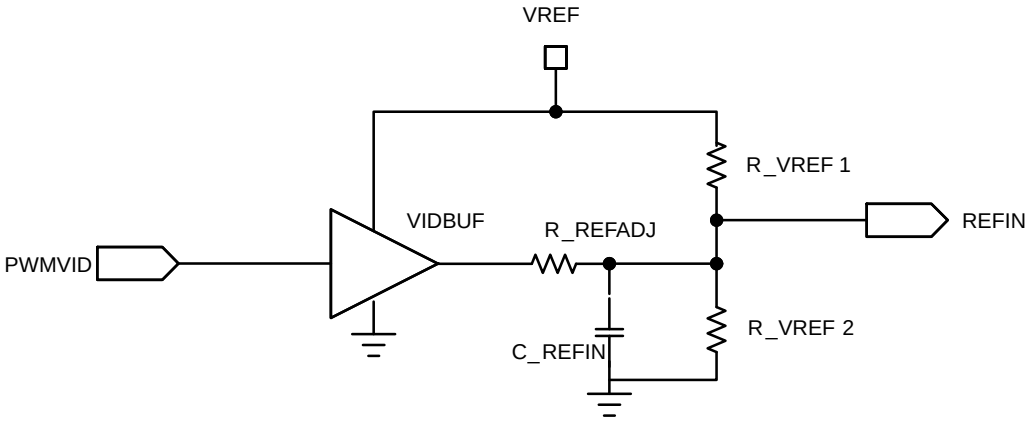

Figure 6. PWM VID Interface

The NCP81174 can decode both 1.8 V and 3.3 V PWMVID output levels. If the EN voltage input is more than 2.5 V, a 3.3 V PWMVID I/O is identified. If EN voltage is above 1.1 V (Overall chip enable threshold) but less than 2.5 V, a 1.8 V PWMVID I/O is assumed.

Soft Start

The NCP81174 has an internal controlled soft start function. The output starts to ramp up following a system reset period after the device is enabled. The device is able to

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start up smoothly under an output pre−biased condition without discharging the output before ramping up.

Before the output soft start begins, an internal switch will be turned on to discharge the external filter cap C_REFIN connected to the REFIN pin to reset the DAC setting, the typical on resistance of the switch is around 6 Ωs. After the discharging, internal switch will be turned off to allow external C_REFIN cap to recharge. After 100 μs, the output voltage ramps up with a fixed slew rate of 1.3 mV/μS.

The circuit can be set to start from either all the phases when the input power rails are all available or from phase 1 when only one input power rail is available by presetting the power mode from PSI pin (See Power Operation Modes).

5V Shunt Regulator

The NCP81174 has an internal shunt regulator to generate 5 V from the external power supply (e.g. 12 V). It is recommended to connect three 0603 resistors (450 Ω each) in parallel from a 12 V power supply to the VCC pin.

Thermal Compensation Amplifier with VDRP and VDFB pins

Thermal compensation amplifier is an internal amplifier in the path of droop current feedback for additional adjustment of the gain of summing current and temperature compensation. The way thermal compensation is implemented separately ensures minimum interference to the voltage loop compensation network.

PWM Comparators with Hysteresis and 3rd state of PWM Outputs

Four PWM comparators receive an error signal at their non−inverting input and one of the triangle waves at its inverting input. The output of each comparator generates the PWM outputs G1, G2, G3 and G4.

During the steady state operation, the duty cycle will center on the valley of the triangle waveform, with steady state duty cycle calculated by Vout/Vin. During a transient event, both high and low comparator output transitions shift phase to the points where the error signal intersects the down and up ramp of the triangle wave.

PWM signals vary between high and low in all phase operation or forced PWM mode. In power saving mode (PS2), PWM signals vary between high and mid level to allow diode emulation.

2/3/4 Phase Operation

Besides 4−phase, the part can be configured to run in 2 or 3−phase mode. In 2−phase mode, phase 1 and 3 should be used to drive the external gate drivers, gate outputs G2 and G4 should be grounded. In 3−phase mode, gate output G4 should be grounded. The current sense inputs of the unused channels should be connected to the Vcore output.

Differential Current Sense Amplifiers and Summing Amplifier

Four differential amplifiers are provided to sense the output current of each phase. The inputs of each current sense amplifier must be connected across the current sensing element of the phase controlled by the corresponding gate output (G1, G2, G3, or G4). If a phase is unused, the differential inputs to that phase's current sense amplifier must be shorted together and connected to the output.

A voltage is generated across the current sense element (such as an inductor or sense resistor) by the current flowing in that phase. The outputs of four current amplifiers are fed into a summing amplifier to have a summed−up output (CSSUM). Signal of CSSUM combines information of total current of all phases in operation. The gain from the total sense current input to CSSUM (A_{CSSUM}) is ~3.93.

The output of the current sense amplifiers are used to control three functions. First, the output controls the adaptive voltage positioning, where the output voltage is actively controlled according to the output current. Second, the output signal is fed to the current limit circuit. This again is the summed current of all phases in operation. Finally, the individual phase current is connected to the PWM comparator. In this way current balance is accomplished.

Undervoltage Lockout (VCC UVLO) and 12VMON

VCC is constantly monitored for undervoltage lockout (UVLO). Line input (normally 12V) is monitored for undervoltage lockout through 12VMON pin by connecting an appropriate resistor divider from line input to the 12VMON input. The setting of the resistor divider should make the 12VMON voltage less than 4 V at all time. During power-up, both VCC and 12VMON will be monitored. Only after they exceed their individual UVLO thresholds, the full circuit will be activated and ready for soft start if the enable pin is also valid. Both UVLO comparators have hysteresis to avoid chattering. The second function of 12VMON pin is to provide feed-forward input voltage information in PS2 mode, see Power Operation Mode section.

Over Current Protection and Under Voltage Protection

A programmable overcurrent function is incorporated within the IC. The inverting input of the comparator is connected to the ILIM pin. The voltage at this pin (0~2 V) sets the maximum output current the converter can produce. The VREF pin provides a convenient and accurate reference voltage from which a resistor divider can create the overcurrent setpoint voltage. Although not actually disabled, tying the ILIM pin directly to the VREF pin sets the limit above useful levels − effectively disabling overcurrent shutdown. The comparator non−inverting input is the summed current information from the current sense amplifier. The overcurrent event will set PWM low for the rest of the cycle when the current information exceeds the voltage at the ILIM pin. If the overcurrent continuously happens and the output will eventually hit the Under Voltage Protection (UVP) limit and it will be a latched event. The UVP limit is set to 50% below the REFIN voltage. The PWM outputs will stay at mid state until the V_{CC} voltage is removed and re−applied, or the ENABLE input is brought low and then high.

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Over Voltage Protection

An output voltage monitor is incorporated. During normal operation, if the output voltage is 50% over the REFIN, the VR_RDY goes low, the DRVON signal remains high, and PWM outputs are set low. The limit will be clamped to 2 V if 50% over REFIN creates a voltage above the 2 V. The outputs will remain disabled until the V_{CC} voltage is removed and reapplied, or the ENABLE input is brought low and then high.

DESIGN METHODOLOGY

Programming the Current Limit

The VREF pin provides a 2.0 V reference voltage which is divided down with a resistor divider (RLIM1/RLIM2) and fed into the current limit pin ILIM. The current limit function is based on the total sensed current of all phases multiplied by a controlled gain (Acssum*Adrp). DCR sensed inductor current is a function of the winding temperature. If not using thermal compensation, the best approach is to set the maximum current limit based on expected average maximum temperature of the inductor windings,

$$DCR_{Tmax} = DCR_{25} \cdot (1 + 0.00393 \cdot (T_{max} - 25)) \quad \text{(eq. 5)}$$

For multiphase controller, the ripple current can be calculated as,

$$I_{PP} = \frac{(V_{in} - N \cdot V_{out}) \cdot V_{out}}{L \cdot F_{SW} \cdot V_{in}} \quad \text{(eq. 6)}$$

Therefore calculate the current limit voltage as below,

$$V_{LIMI} \cong A_{CSSUM} \cdot A_{DRP} \cdot DCR_{TMAX} \cdot \left(I_{MIN_OCP} \cdot + 0.5 \cdot I_{PP}\right) \quad \text{(eq. 7)}$$

$$V_{LIMIT} \cong A_{CSSUm} \cdot A_{DRP} \cdot DCR_{TMAX} \cdot \left(I_{MIN_OCP} \cdot + 0.5 \cdot \frac{(V_{in} - N \cdot V_{out}) \cdot V_{out}}{L \cdot F_{SW} \cdot V_{in}}\right)$$

In Equation 7, A_{CSSUM} and A_{DRP} are the gain of current summing amplifier and droop amplifier.

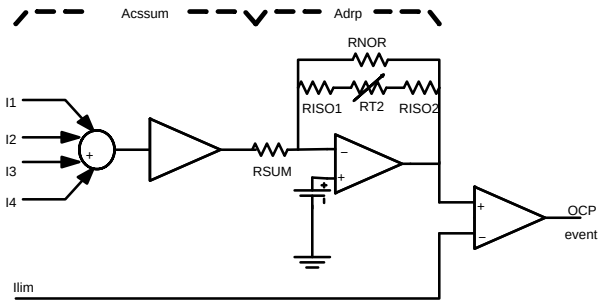

Figure 7. ACSSUM and ADRP

As introduced before, V_{LIMIT} comes from a resistor divider connected to VREF, thus

$$V_{LIMIT} = 2\ V \cdot \frac{R_{LIM2}}{R_{LIM2} + R_{LIM2}} \cdot COEpsi \quad \text{(eq. 8)}$$

$$A_{CSSUM} \sim = -3.93$$

$$A_{DRP} = -\frac{R_{NOR} \cdot \left(R_{ISO1} + R_{ISO2} + R_{T2}\right)}{\left(R_{NOR} + R_{ISO1} + R_{ISO2} + R_{T2}\right) \cdot R_{SUM}} \quad \text{(eq. 9)}$$

RISO1 and RISO2 are in series with R_{T2} , the NTC temperature sense resistor placed near inductor. RSUM is the resistor connecting between pin VDFB and pin CSSUM. In PS0 mode, the current limit follows the Equation 10; In PS1 or PS2, the current limit calculation follows Equation 11, COEpsi is a coefficient for the current limiting related in power saving mode PS1, PS2. COEpsi value is one over the original phase count N. Refer to the PSI and phase shedding section for more details.

$$I_{LIMIT}(normal) \cong \frac{\frac{2\ V \cdot R_{LIM2}}{R_{LIM1} + R_{LIM2}}}{3.93 \cdot \frac{R_{NOR} \cdot (R_{ISO1} + R_{ISO2} + R_{T2})}{(R_{NOR} \cdot R_{ISO1} + R_{ISO2} + R_{T2}) \cdot R_{SUM}} \cdot DCR_{25^\circ} \cdot (1 + 0.00393 \cdot (T_{inductor} - 25))} - 0.5 \cdot \frac{(V_{in} - V_{out}) \cdot V_{out}}{L \cdot F_{SW} \cdot V_{in}} \quad \text{(eq. 10)}$$

$$I_{LIMIT}(normal) \cong \frac{\frac{2\ V \cdot R_{LIM2}}{R_{LIM1} + R_{LIM2}} \cdot COEpsi}{3.93 \cdot \frac{R_{NOR} \cdot (R_{ISO1} + R_{ISO2} + R_{T2})}{(R_{NOR} \cdot R_{ISO1} + R_{ISO2} + R_{T2}) \cdot R_{SUM}} \cdot DCR_{25^\circ} \cdot \left(1 + 0.00393 \cdot \left(T_{inductor} - 25\right)\right)} - 0.5 \cdot \frac{\left(V_{in} - V_{out}\right) \cdot V_{out}}{L \cdot F_{SW} \cdot V_{in}} \quad \text{(eq. 11)}$$

N is the number of phases involved in the circuit.

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Inductor Current Sensing Compensation

The NCP81174 uses the inductor current sensing method. An RC filter is selected to cancel out the impedance from inductor and recover the current information through the inductor's DCR. This is done by matching the RC time constant of the sensing filter to the L/DCR time constant. The first cut approach is to use a 0.1 uF capacitor for C and then solve for R.

$$R_{sense}(T) = \frac{L}{0.1 \cdot \mu F \cdot DCR_{25C} \cdot (1 + 0.00393 \cdot (T - 25))} \quad \text{(eq. 12)}$$

Because the inductor value is a function of load and inductor temperature final selection of R is best done experimentally on the bench by monitoring the VDRP pin and performing a step load test on the actual solution.

Compensation and Output Filter Design

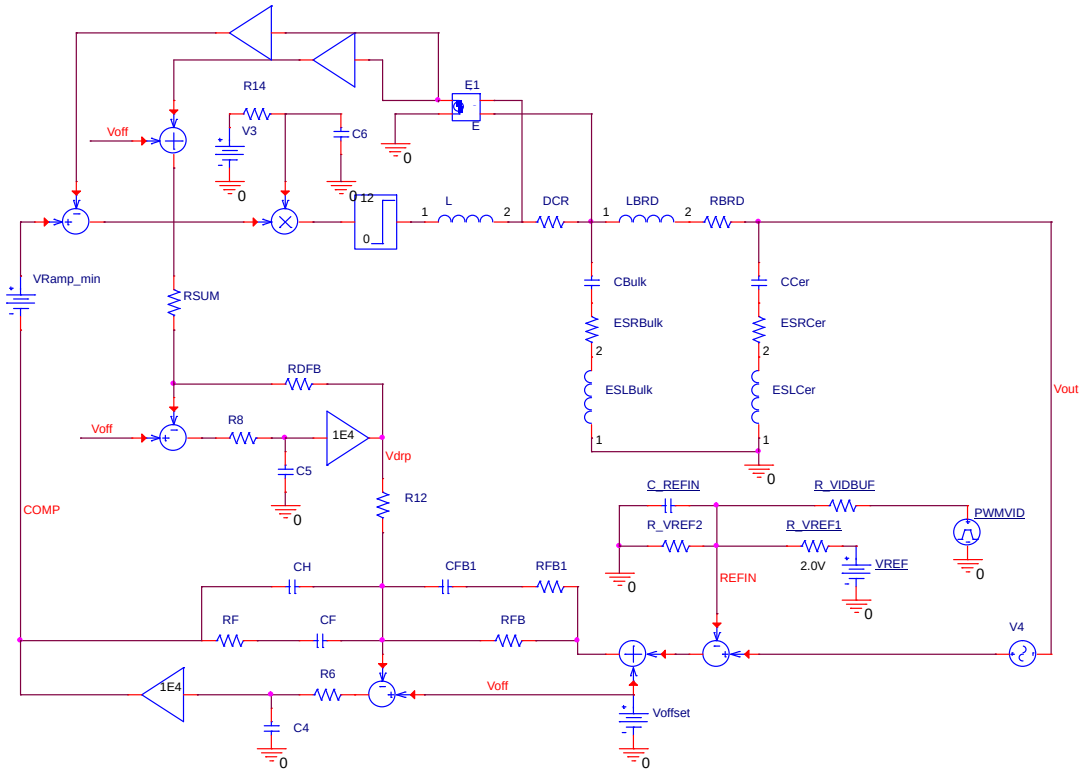

Figure 8. System Average Model

A simple state average model shown in Figure 8 can be used to assist the system design and determine a stable solution.

The goal is to compensate the system such that the resulting gain generates constant output impedance from DC up to the frequency where the ceramic takes over holding the impedance below the target output impedance. By matching the following equations a good set of starting compensation values can be found for a typical mixed bulk and ceramic capacitor type output filter.

$$\frac{1}{2\pi \cdot CF \cdot RF} = \frac{1}{2\pi \cdot (RBRD + ESRBulk) \cdot CBulk} \quad \text{(eq. 13)}$$

$$\frac{1}{2\pi \cdot CFB1 \cdot (RFB1 + RFB)} = \frac{1}{2\pi \cdot CCer \cdot (RBRD + ESRBulk)} \quad \text{(eq. 14)}$$

Droop Injection and Thermal Compensation

The VDRP signal is generated by summing the sensed output currents for each phase. A droop amplifier is added to adjust the total gain to approximately eight. VDRP is

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externally summed into the feedback network by the resistor RDRP. This introduces an offset which is proportional to the output current thereby forcing a controlled, resistive output impedance.

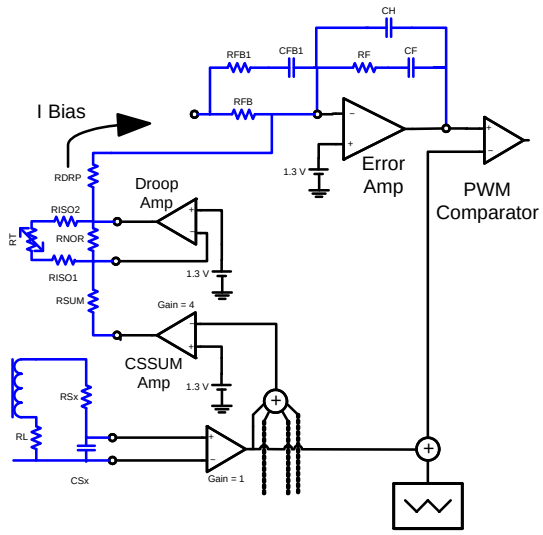

Figure 9. Droop Injection and Thermal Compensation

RDRP determines the target output impedance by the basic equation:

$$\frac{V_{out}}{I_{out}} = Z_{out} = \frac{R_{FB} \cdot DCR \cdot A_{CCSUM} \cdot A_{DRP}}{R_{DRP}} \quad \text{(eq. 15)}$$

$$R_{DRP} = \frac{R_{FB} \cdot DCR \cdot A_{CSSUM} \cdot A_{DRP}}{Z_{out}} \quad \text{(eq. 16)}$$

The value of the inductor's DCR is a function of temperature according to Equation 17:

$$DCR(T) = DCR_{25C} \cdot (1 + 0.00393 \cdot (T - 25)) \quad \text{(eq. 17)}$$

Actual DCR increases by temperature. The system can be thermally compensated to cancel this effect to a great degree by adding an NTC in parallel with RNOR to reduce the droop gain as the temperature increases. The NTC device is nonlinear. Putting a resistor in series with the NTC helps make the device appear more linear with temperature. The series resistor is split and inserted on both sides of the NTC to reduce noise injection into the feedback loop. The recommended total value for RISO1 plus RISO2 is approximately 1.0 kΩ.

The output impedance varies with inductor temperature by the equation:

$$Z_{out}(T) = \frac{R_{FB} \cdot DCR_{25C} \cdot (1 + 0.00393 \cdot (T - 25)) \cdot A_{CSSUM} \cdot A_{DRP}}{R_{DRP}} \quad \text{(eq. 18)}$$

By including the NTC RT2 and the series isolation resistors the new equation becomes:

$$Z_{out}(T) = \frac{R_{FB} \cdot DCR_{25C} \cdot (1 + 0.00393 \cdot (T - 25)) \cdot A_{CSSUM} \cdot \frac{R_{NOR} \cdot (R_{ISO1} + R_{ISO2} + R_{T2})}{(R_{NOR} + R_{ISO1} + R_{ISO2} + R_{T2}) \cdot R_{SUM}}}{R_{DRP}} \quad \text{(eq. 19)}$$

The typical equation of an NTC is based on a curve fit Equation 20:

$$RT2(T) = RT2_{25C} \cdot e^{\beta\left[\left(\frac{1}{273 + T}\right) - \left(\frac{1}{298}\right)\right]} \quad \text{(eq. 20)}$$

Figure 10 shows an example of the comparison of the compensated output impedance and uncompensated output impedance varying with temperature.

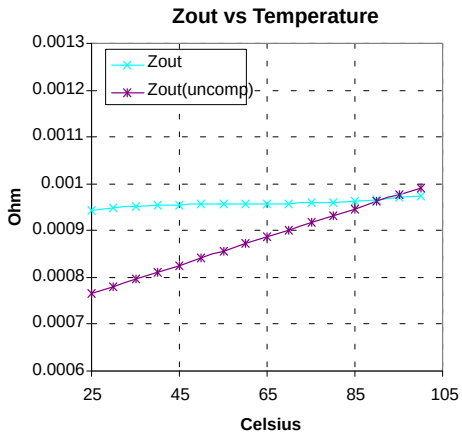

Figure 10. Zout vs. Temperature (10 kΩ NTC with a β value of 3740)

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SYSTEM TIMING DIAGRAM

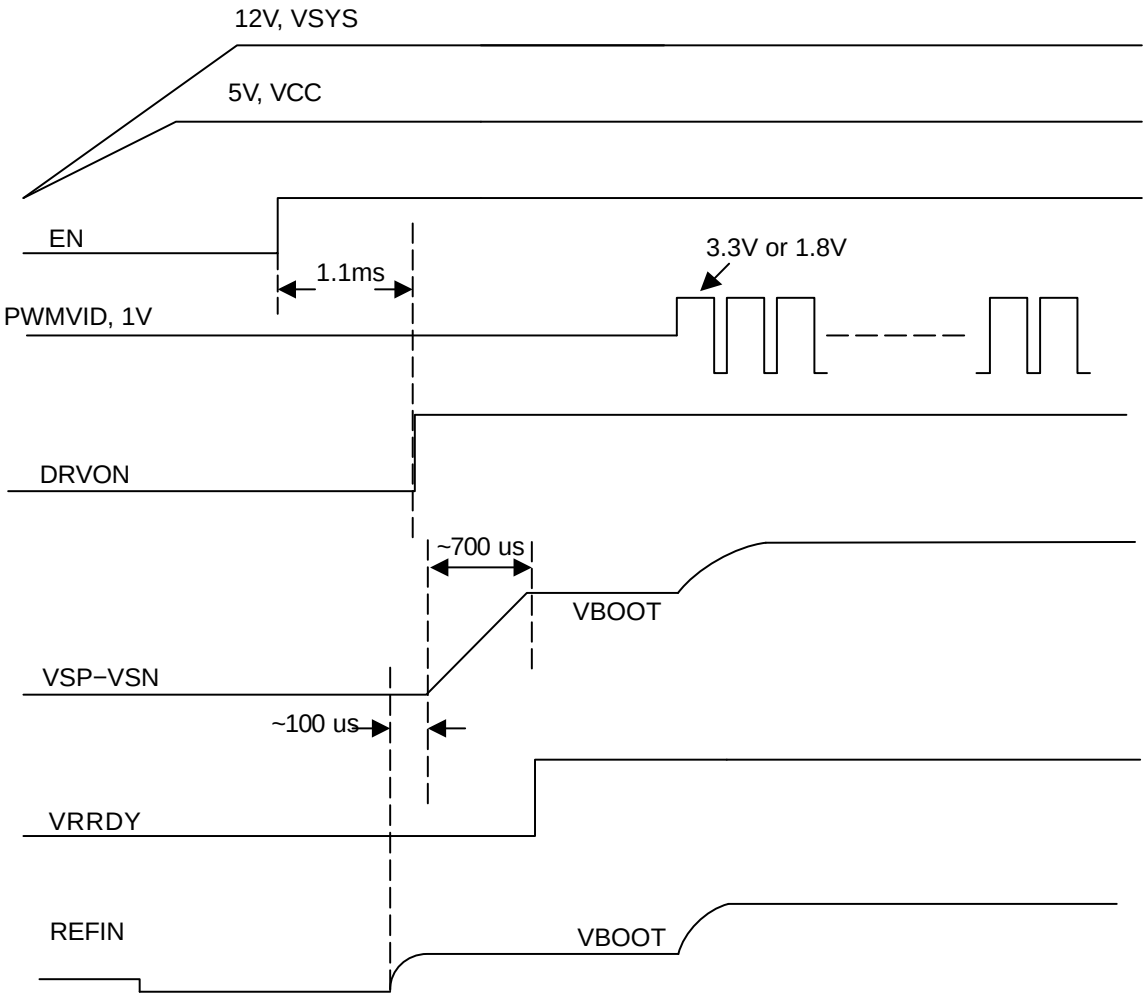

Figure 11. System Timing Diagram

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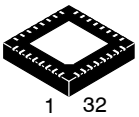
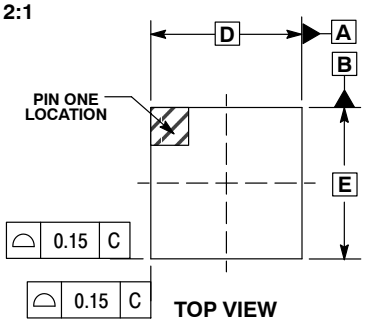
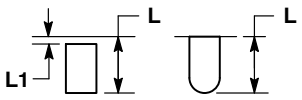
QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

DATE 23 OCT 2013

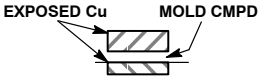


SCALE 2:1

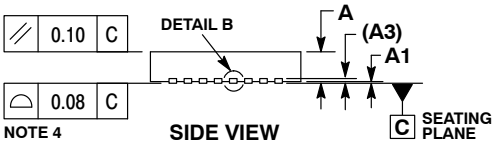




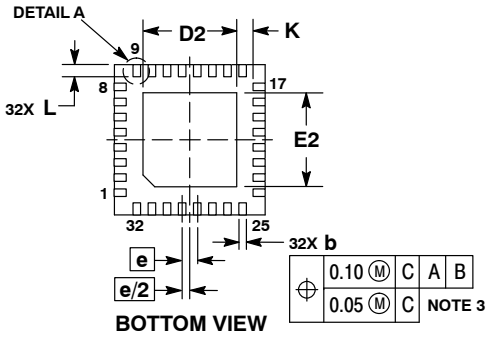
DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTION



SIDE VIEW

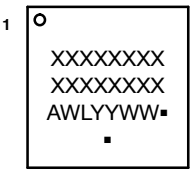


BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15

GENERIC MARKING DIAGRAM*

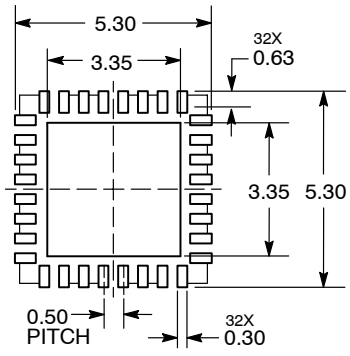


XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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