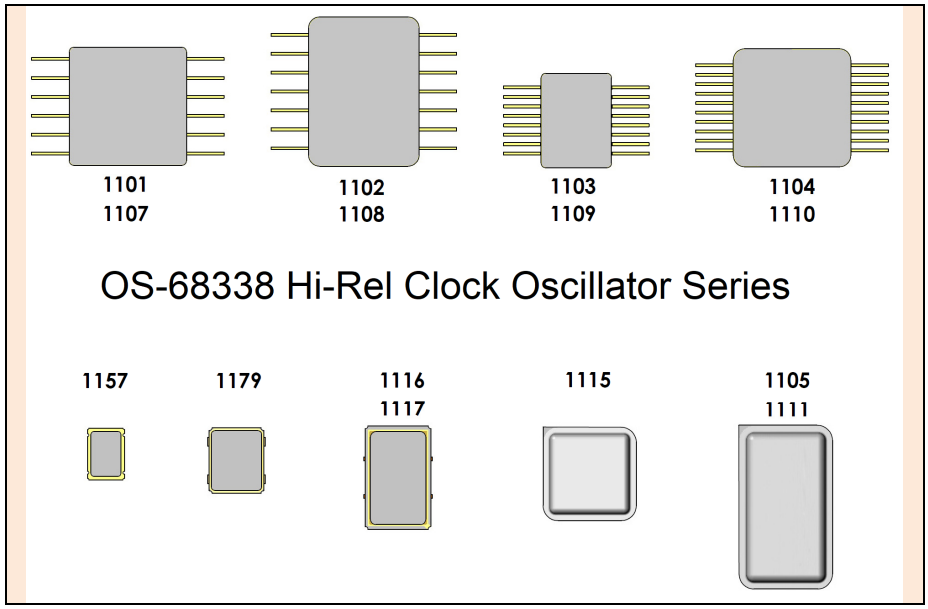
REV	DESCRIPTION	DATE	PREP	APPD
Q	CO-31668	12/4/20	SM	LT/DF



EXAMPLES SHOWN IN ACTUAL SIZE

MOUNT HOLLY SPRINGS, PA 17065

Oscillator Specification, Hybrid Clock

Hi-Rel Standard

THE RECORD OF APPROVAL FOR THIS DOCUMENT IS MAINTAINED ELECTRONICALLY WITHIN THE ERP SYSTEM

CODE IDENT NO	SIZE	DWG. NO.	REV
00136	A	OS-68338	Q

UNSPECIFIED TOLERANCES: N/A

1. SCOPE

1.1 General. This specification defines the design, assembly and functional evaluation of high reliability, hybrid clock oscillators produced by Vectron. Devices delivered to this specification represent the standardized Parts, Materials and Processes (PMP) Program developed, implemented and certified for advanced applications and extended environments.

1.2 Applications Overview. The designs represented by these products were primarily developed for the MIL-Aerospace community. The lesser Design Pedigrees and Screening Options imbedded within OS-68338 bridge the gap between Space and COTS hardware by providing custom hardware with measures of mechanical, assembly and reliability assurance needed for Military or Ruggedized COTS environments.

2. APPLICABLE DOCUMENTS

2.1 Specifications and Standards. The following specifications and standards form a part of this document to the extent specified herein. The issue currently in effect on the date of quotation will be the product baseline, unless otherwise specified. In the event of conflict between the texts of any references cited herein, the text of this document shall take precedence.

Military

MIL-PRF-55310	Oscillators, Crystal Controlled, General Specification For
MIL-PRF-38534	Hybrid Microcircuits, General Specification For

Standards

MIL-STD-202	Test Method Standard, Electronic and Electrical Component Parts
MIL-STD-883	Test Methods and Procedures for Microelectronics

Other

DOC007131	Test Specification, OS-68338 Hybrids, Hi-Rel Standard
QSP-90100	Quality Systems Manual, Vectron
DOC011627	Identification Common Documents, Materials and Processes, Hi-Rel XO
DOC203982	DPA Specification
QSP-91502	Procedure for Electrostatic Discharge Precautions
DOC208191	Enhanced Element Evaluation for Space Level Hybrid Oscillators

3. GENERAL REQUIREMENTS

3.1 Classification. All devices delivered to this specification are of hybrid technology conforming to Type 1, Class 2 of MIL-PRF-55310. Primarily developed as a Class S equivalent specification, options are imbedded within it to also produce Class B, Engineering Model and Ruggedized COTS devices. Devices carry a Class 2 ESDS classification per MIL-PRF-38534.

3.2 Item Identification. External packaging choices are of metal flatpacks, DIP's and ceramic with either TTL or ACMOS logic output. Unique Model Number Series' are utilized to identify device package configurations and output logic as listed in Table 1.

3.3 Absolute Maximum Ratings.

a. Supply Voltage Range (V_{CC}):	-0.5Vdc to +7.0Vdc
b. Storage Temperature Range (T_{STG}):	-65°C to +125°C
c. Junction Temperature (T_J):	+175°C
d. Lead Temperature (soldering, 10 seconds):	+300°C
e. Output Source/Sink Current:	±70 mA

3.4 Design, Parts, Materials and Processes, Assembly, Inspection and Test.

3.4.1 Design. The ruggedized designs implemented for these devices are proven in military and space applications under extreme environments. All designs (except 5x7mm) utilize a 4-point crystal mount. All designs (except 5x7mm and 7x9mm) use Established Reliability (MIL-ER) componentry. The 5x7mm models utilizes a 3-point crystal mount. When specified, radiation tolerant active devices up to 100krad (Si) (RHA level R) can be included without altering the device's internal topography.

3.4.1.1 Design and Configuration Stability. Barring changes to improve performance by reselecting passive chip component values to offset component tolerances, there will not be fundamental changes to the design or assembly or parts, materials and processes after first product delivery of that item without written approval from the procuring activity.

3.4.1.2 Environmental Integrity. Designs have passed the environmental qualification levels of MIL-PRF-55310. These designs have also passed extended dynamic levels of at least:

a. Sine Vibration: MIL-STD-202, Method 204, Condition G (30g pk.)
b. Random Vibration: MIL-STD-202, Method 214, Condition II-J (43.92g rms, three-minute duration in each of three mutually perpendicular directions)
c. Mechanical Shock: MIL-STD-202, Method 213, Condition F (1500g, 0.5ms)

3.4.2 Prohibited Parts, Materials and Processes. The items listed are prohibited for use in high reliability devices produced to this specification.

a. Gold metallization of package elements without a barrier metal.
b. Zinc chromate as a finish.
c. Cadmium, zinc, or pure tin external or internal to the device.
d. Plastic encapsulated semiconductor devices.
e. Ultrasonically cleaned electronic parts.
f. Heterojunction Bipolar Transistor (HBT) technology.
g. 'getter' materials

3.4.3 Assembly. Manufacturing utilizes standardized procedures, processes and verification methods to produce MIL-PRF-55310 Class S / MIL-PRF-38534 Class K equivalent devices. MIL-PRF-38534 Group B Option 1 in-line inspection is included on design pedigrees E, R and V to further verify lot pedigree. Devices are handled in accordance with Vectron document QSP-91502 (Procedure for Electrostatic Discharge Precautions). Element replacement will be as specified in MIL-PRF-38534, Rev L.

3.4.4 Inspection. The inspection requirements of MIL-PRF-55310 apply to all devices delivered to this document. Inspection conditions and standards are documented in accordance with the Quality Assurance, ISO-9001 and AS9100 derived, System of QSP-90100.

3.4.5 Test. The Screening test matrix of Table 5 is tailored for selectable-combination testing to eliminate costs associated with the development/maintenance of device-specific documentation packages while maintaining performance integrity.

3.4.6 Marking. Device marking shall be in accordance with the requirements of MIL-PRF-55310.

3.4.7 Ruggedized COTS Design Implementation. Design Pedigree "D" devices (see ¶ 5.2) use the same robust designs found in the other device pedigrees. They do not include the provisions of traceability or the Class-qualified componentry noted in paragraphs 3.4.3 and 4.1.

4. DETAIL REQUIREMENTS

4.1 Components

4.1.1 Crystals. Cultured quartz crystal resonators are used to provide the selected frequency for the devices. The optional use of Premium Q swept quartz can, because of its processing to remove impurities, be specified to minimize frequency drift when operating in radiation environments. In accordance with MIL-PRF-55310, the manufacturer has a documented crystal element evaluation program.

4.1.2 Passive Components

4.1.2.1 For Design Pedigree E, where available, resistors shall be Established Reliability, Failure Rate R (as a minimum) and capacitors shall be Failure Rate S. Where resistors and capacitors are not available as ER parts, and for all other passive components, the parts shall be from homogeneous manufacturing lots that have successfully completed the Enhanced Element Evaluation of DOC208191 which meets the requirements of Mil-PRF-38534 Revision L for Class K.

4.1.2.2 For Design Pedigrees R, V and X, where available, resistors shall be Established Reliability, Failure Rate R (as a minimum) and capacitors shall be Failure Rate S. Where resistors and capacitors are not available as ER parts, and for all other passive components, the parts shall be from homogeneous manufacturing lots that have successfully completed the Class K Element Evaluation of Mil-PRF-38534 Revision K for Class K.

4.1.2.3 For Design Pedigrees B and C, all passive elements shall comply with the Element Evaluation requirements of Mil-PRF-55310 Class B as a minimum.

4.1.2.4 For Design Pedigree D, the passive elements will be COTs level or higher.

4.1.2.5 When used, inductors will be open construction and may use up to 48-gauge wire.

4.1.3 Microcircuits.

4.1.3.1 For Design Pedigree E, the microcircuits shall be from homogeneous wafer lots that meet the Enhanced Element Evaluation requirements in DOC208191 and meet the requirements of Mil-PRF-38534 Revision L for Class K.

4.1.3.2 For Design Pedigree R, V and X, microcircuits shall be from homogeneous wafer lots that have successfully completed the MIL-PRF-38534, Revision K Lot Acceptance Tests for Class K.

4.1.3.3 For Design Pedigrees B and C, microcircuits are procured from wafer lots that have successfully completed the MIL-PRF-55310 Lot Acceptance Tests for Class B as a minimum.

4.1.3.4 For Design Pedigree D, microcircuits can be COTs level or higher.

4.1.4 Radiation. Microcircuits for Design Pedigrees E, R and V are certified to 100krad (Si) total ionizing dose (TID), RHA level R (2X minimum margin). NSC, as the original 54ACT designer, rates the SEU LET at >40 MeV and SEL at >120MeV for the FACT™ family (AN-932). Vectron has conducted additional SEE testing in 2008 to verify this performance since our lot wafer testing does not include these parameters and determinations. In addition, Vectron has conducted neutron displacement damage testing to confirm a tolerance of 6E11n/cm^2, 1MeV equivalent. Prompt dose (dose rate) testing of the 54ACT device shows that the part is immune to latch-up/burnout up to at least 1.39E10 rad(Si)/s and +125°C. The parts exhibited no transients at a dose rate of 1E8 rad(Si)/s. At dose rates up to 1.39E10, all parts recovered to pre-shot function and supply current within three to four microseconds.

4.1.5 Packages. Packages are procured that meet the construction, lead materials and finishes as specified in MIL-PRF-55310. All leads are Kovar with gold plating over a nickel underplate. Package lots are evaluated in accordance with the requirements of MIL-PRF-38534. Vectron will not perform Salt Spray testing as part of MIL-PRF-55310 Group C/Qualification. In accordance with MIL-PRF-55310, package evaluation results for salt atmosphere will be substituted for Salt Spray testing during MIL-PRF-55310 Group C/Qualification.

4.1. 6 Traceability and Homogeneity. All design pedigrees except option D have active device lots that are traceable to the manufacturer's individual wafer; all other elements and materials are traceable to their manufacturer and incoming inspection lots. Design pedigrees E, R, V and X have homogenous material. In addition, swept quartz crystals are traceable to the quartz bar and the processing details of the autoclave lot, as applicable. A production lot, as defined by Vectron, is all oscillators that have been kitted and assembled as a single group. After the initial kitting and assembly, this production lot may be divided into multiple sublots to facilitate alignment and test capacity.

4.2 Mechanical.

4.2.1 Package Outline. Table 1 links each Hi-Rel Standard Model Number of this specification to a corresponding package style. Mechanical Outline information of each package style is found in the referenced Figure.

4.2.2 Thermal Characteristics. The worst-case thermal characteristics of each package style are found in Table 4.

4.2.3 Lead Forming. When lead forming option is specified, the applicable leak test specified in screening will be performed after forming.

4.3 Electrical.

4.3.1 Input Power. Devices are available with an input voltage of either +5.0 Vdc (±10%) or +3.3 Vdc (±10%). Current is measured, no load, at maximum rated operating voltage.

4.3.2 Temperature Range. Operating range is -55°C to +125°C.

4.3.3 Frequency Tolerance. Initial accuracy at +23°C is ±15 ppm maximum. Frequency-Temperature Stability is ±50 ppm maximum from +23°C reference. Frequency-Voltage Tolerance is ±4 ppm maximum.

4.3.4 Frequency Aging. Aging limits, and when tested in accordance with MIL-PRF-55310 Group B inspection, shall not exceed ±1.5 ppm the first 30 days, ±5 ppm Year 1 and ±2 ppm per year thereafter.

4.3.4.1 Frequency Aging Duration Option. By customer request, the Aging test may be terminated after 15 days if the measured aging rate is less than half of the specified aging rate. This is a common method of expediting 30-Day Aging without incurring risk to the hardware and used quite successfully for numerous customers. It is based on the 'least squares fit' determinations of MIL-PRF-55310 paragraph 4.8.35. The 'half the time/half the spec' limit is generally conservative as roughly 2/3 of a unit's Aging deviation occurs within that period of time. Vectron's automated aging systems take about 6 data points per day, so a lot of data is available to do very accurate projections, much more data than what is required by MIL-PRF-55310. The delivered data would include the Aging plots projected to 30 days. If the units would not perform within that limit, then they would continue to full 30-Day term. Please advise by purchase order text if this may be an acceptable option to exercise as it assists in Production Test planning.

4.3.5 Operating Characteristics. Symmetrical square wave limits are dependent on the device frequency and are in accordance with Tables 2 and 2A. Waveform measurement points and logic limits are in accordance with MIL-PRF-55310. Start-up time is 10.0 msec. maximum.

4.3.6 Output Load. Standard TTL (6 or 10) and ACMOS (10kΩ, 15pF) test loads are in accordance with MIL-PRF-55310.

5. QUALITY ASSURANCE PROVISIONS AND VERIFICATION

5.1 Verification and Test. Device lots shall be tested prior to delivery in accordance with the applicable Screening Option letter as stated by the 15th character of the part number. Table 5 tests are conducted in the order shown and annotated on the appropriate process travelers and data sheets of the governing test procedure. For devices that require Screening Options that include MIL-PRF-55310 Group A testing, the Post-Burn-In Electrical Test and the Group A Electrical Test are combined into one operation.

5.1.1 Screening Options. The Screening Options, by letter, are summarized as:

- A Modified MIL-PRF-38534 Class K Screening
- B Modified MIL-PRF-55310 Class B Screening & Group A QCI
- C Modified MIL-PRF-55310 (Rev E) Class S Screening & Group A QCI
- D Modified MIL-PRF-38534 Class K Screening & 30-day Aging
- E Modified MIL-PRF-55310 Class B Screening & Groups A & B QCI
- F Modified MIL-PRF-55310 (Rev E) Class S Screening & Groups A & B QCI
- G Modified MIL-PRF-55310 Class B Screening & Post BI Nominal Electricals

S MIL-PRF-55310 (Rev F) Class S Screening & Groups A & B QCI
X Engineering Model (EM)

5.2 Optional Design, Test and Data Parameters. The following is a list of design, assembly, inspection and test options that can be selected or added by purchase order request.

a. Design Pedigree (choose one as the 5th character in the part number):
(E) Enhanced Element Evaluation (MIL-PRF-38534 Rev L for Class K components as specified in DOC208191), 100krad die, Premium Q Swept Quartz
(R) Hi-Rel design w/ 100krad Class K die, Premium Q Swept Quartz
(V) Hi-Rel design w/ 100krad Class K die, Non-Swept Quartz
(X) Hi-Rel design w/ Non-Swept Quartz, Class K die
(B) Hi-Rel design w/ Swept Quartz, Class B die
(C) Hi-Rel design w/ Non-Swept Quartz, Class B die
(D) Hi-Rel design w/ Non-Swept Quartz and commercial grade components
b. Input Voltage, **(A)** for 5.0V, **(B)** for 3.3V as the 14th character
c. Not Used
d. Radiographic Inspection
e. Group C Inspection: MIL-PRF-55310, Rev E (requires 8 destruct specimens)
f. Group C Inspection: MIL-PRF-55310, Rev F (requires 8 destruct specimens, includes Random Vibration, MIL-STD-883, Method 1014 Leak Test and Life Test)
g. Group C Inspection: In accordance with MIL-PRF-38534, Table C-Xc, Condition PI (requires 8 destruct specimens – 5 pc. Life, 3 pc. RGA). Subgroup 1 fine leak test to be performed per MIL-STD-202, Method 112, Condition C.
h. Internal Water-Vapor Content (RGA) samples and test performance
i. MTBF Reliability Calculations
j. Worst Case Circuit Analysis (unless otherwise specified, MIL-HDBK-1547)
k. Derating and Thermal Analysis (unless otherwise specified, MIL-HDBK-1547 with Tj Max = +105°C; Derated Maximum Operating Temp = Tj Max – ΔTj)
l. Process Identification Documentation (PID)
m. Customer Source Inspection (pre-crystal mount pre-cap, post-crystal mount pre-cap and final). Due to components being mounted underneath the crystal blank, the following model numbers should be considered for pre-crystal mount pre-cap inspection: 1103, 1109, 1115, 1116, 1117, 1119, 1157, 1167, 1177, 1187, 1179, 1189 and 1199.
n. Destruct Physical Analysis (DPA): MIL-STD-1580 with exceptions as specified in Vectron DOC203982. When ordering destruct specimens for DPA performance on 1157, 1167, 1177 or 1187 platforms, you must order separate destruct specimens for RGA testing and the balance of DPA due to the likelihood of crystal damage during the puncturing of the 5x7mm enclosure.
o. Qualification: In accordance with MIL-PRF-55310, Rev F Table IV (requires 16 destruct specimens).
p. Qualification: In accordance with EEE-INST-002, Section C4, Table 3, Level 1 or 2 (requires 11 destruct specimens)
q. High Resolution Digital Pre-Cap Photographs (20 Megapixels minimum for all devices except 1157, 1167, 1177 and 1187 which will use 10 Megapixels minimum).
r. Hot solder dip of leads with Sn63/Pb37 solder prior to shipping.
s. As Designed Parts, Materials and Processes List

5.2.1 NASA EEE-INST-002. A combination of Design Pedigree R, Option S Screening, and Qualification per EEE-INST-002, Section C4, Table 3, meet the requirements of Level 1 and Level 2 device reliability.

5.3 Test Conditions. Unless otherwise stated herein, inspections are performed in accordance with those specified in MIL-PRF-55310. Process travelers identify the applicable methods, conditions and procedures to be used. Examples of electrical test procedures that correspond to MIL-PRF-55310 requirements are shown in Table 3.

5.4 Deliverable Data. The manufacturer supplies the following data, as a minimum, with each lot of devices (except devices with Screening Option X):

a. Completed assembly and screening lot travelers and screening data, including radiographic images, rework history and Certificate of Conformance.
b. Electrical test variables data, identified by unique serial number.
c. Special items when required by purchase order such as Group C data and RGA data.
d. Traceability, component LAT, enclosure LAT and RLAT (if specifically requested on the purchase order).

5.5 Discrepant Material. All MRB authority resides with the procuring activity.

5.6 Failure Analysis. Any failure during Qualification or Group C Inspection will be evaluated for root cause. The customer will be notified after occurrence and upon completion of the evaluation.

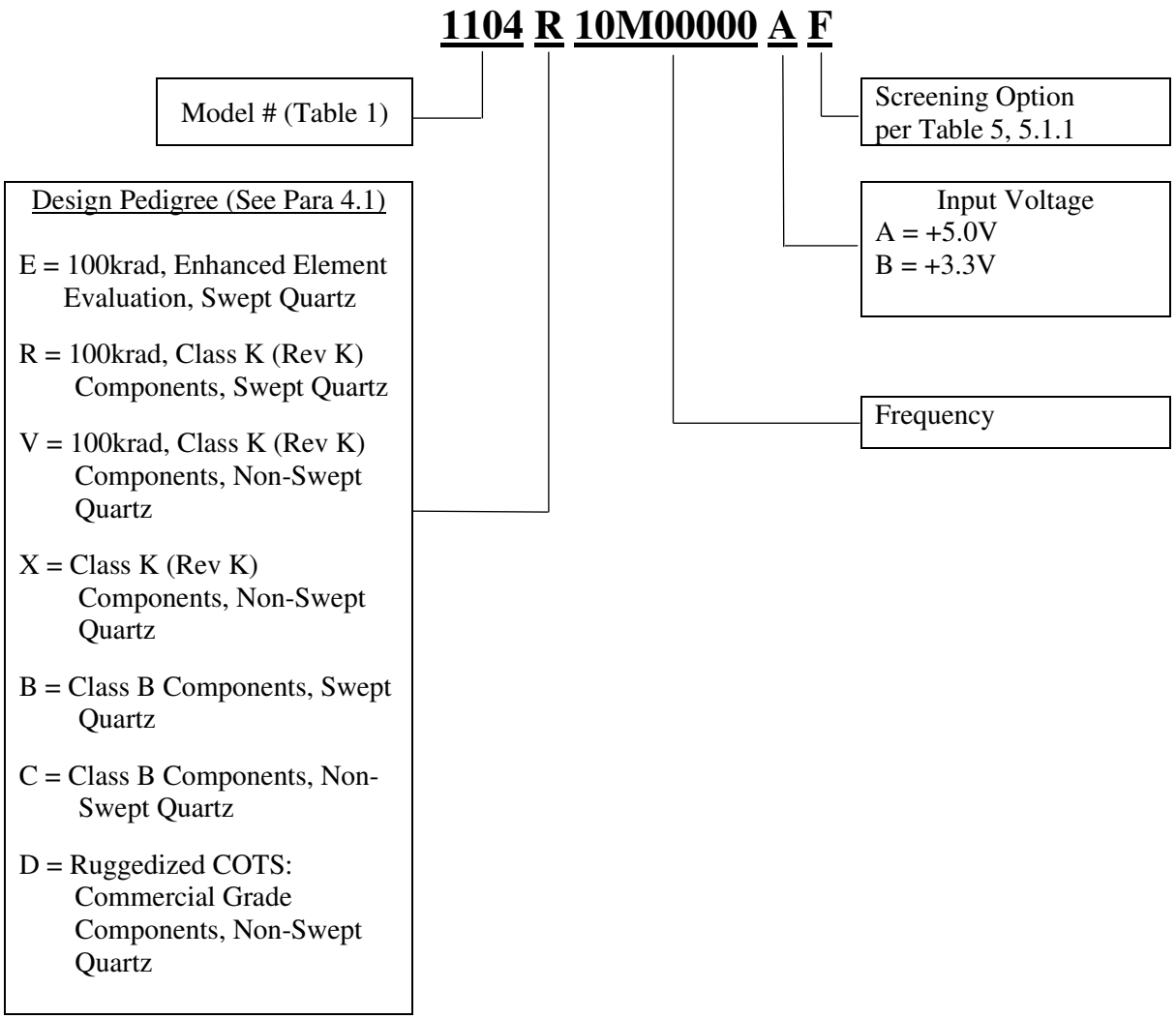
6. PREPARATION FOR DELIVERY

6.1 Packaging. Devices will be packaged in a manner that prevents handling and transit damage during shipping. Devices will be handled in accordance with MIL-STD-1686 for Class 1 devices.

7. ORDERING INFORMATION

7.1 Ordering Part Number. The ordering part number is made up of an alphanumeric series of 15 characters. Design-affected product options, identified by the parenthetic letter on the Optional Parameters list (¶ 5.2a and b), are included within the device part number.

The Part Number breakdown is described as:



7.1.1 Model Number. The device model number is the four (4) digit number assigned to a corresponding package and output combination per Table 1.

7.1.2 Design Pedigree. Class S variants correspond to either letter “E”, “R”, “V” or “X” and are described in paragraph 5.2a. Class B variants correspond to either letter “B” or “C” and are described in paragraph 5.2a. Ruggedized COTS, using commercial grade components, corresponds to letter “D”.

7.1.2.1 Input Voltage. Voltage is the 14th character, letters "A" representing +5.0V and "B" for +3.3V.

7.1.3 Output Frequency. The nominal output frequency is expressed in the format as specified in MIL-PRF-55310 utilizing eight (8) characters.

7.1.4 Screening Options. The 15th character is the Screening Option (letter A thru G, S or X) selected from Table 5.

7.2 Optional Design, Test and Data Parameters. Optional test and documentation requirements shall be specified by separate purchase order line items (as listed in ¶ 5.2c thru s).

HI-REL STANDARD MODEL #	PACKAGE	OUTPUT, Square Wave	PIN I/O 1/				MECHANICAL OUTLINE
			Vcc	Out	Gnd/ Case	E/D 2/	
1101	12 Lead Flatpack	ACMOS	12	7	6	na	FIGURE 1
1102	14 Lead Flatpack	ACMOS	14	8	7	na	FIGURE 2
1103	16 Lead Flatpack	ACMOS	8	10	9	na	FIGURE 3
1104	20 Lead Flatpack	ACMOS	13, 20	11	10	na	FIGURE 5
1105	14 Pin DIP	ACMOS	14	8	7	na	FIGURE 6
1115	4 pin ½ DIP	ACMOS	8	5	4	na	FIGURE 4
1116	J-lead SMT	ACMOS	4	3	2	1	FIGURE 7
1157 3/	4 pad 5 x 7mm	ACMOS	4	3	2	1	FIGURE 8
1119 4/	16 Lead Flatpack	ACMOS	8	10	9	na	FIGURE 9
1120 4/	20 Lead Flatpack	ACMOS	13, 20	11	10	na	FIGURE 10
1121 4/	12 Lead Flatpack	ACMOS	12	7	6	na	FIGURE 11
1122 4/	14 Lead Flatpack	ACMOS	14	8	7	na	FIGURE 12
1167	5 x 7mm, Straight Lead	ACMOS	4	3	2	1	FIGURE 13
1177	5 x 7mm, Inward Lead	ACMOS	4	3	2	1	FIGURE 14
1187	5 x 7mm, Outward Lead	ACMOS	4	3	2	1	FIGURE 15
1179	7 x 9mm, Straight Lead	ACMOS	4	3	2	1	FIGURE 16
1189	7 x 9mm, Inward Lead	ACMOS	4	3	2	1	FIGURE 17
1199	7 x 9mm, Outward Lead	ACMOS	4	3	2	1	FIGURE 18
1107	12 Lead Flatpack	TTL	12	7	6	na	FIGURE 1
1108	14 Lead Flatpack	TTL	14	8	7	na	FIGURE 2
1109	16 Lead Flatpack	TTL	8	10	9	na	FIGURE 3
1110	20 Lead Flatpack	TTL	13, 20	11	10	na	FIGURE 5
1111	14 Pin DIP	TTL	14	8	7	na	FIGURE 6
1117	J-lead SMT	TTL	4	3	2	1	FIGURE 7

1/. All unassigned pins have no internal connections or ties.
2/. A logic "1" (>+2.0V) or open on pin 1 will enable the output. A logic "0" (<+0.8V) will disable the output.
3/. Model 1157 replaces previous Model 1118.
4/. Models 1119 through 1122 are lead formed versions of Models 1101 through 1104. See Appendix A for recommended land patterns.

TABLE 1 - Item Identification and Package Outline

Frequency Range: 0.35 MHz to 100.0 MHz 3/ 4/								
Temperature Range: -55°C to +125°C								
Frequency Tolerance, Initial Accuracy @ +23°C: ±15 ppm max.								
Frequency-Temperature Stability from +23°C ref.: ±50 ppm max.								
Frequency-Voltage Tolerance: ±4 ppm max. (Vcc ±10%)								
Frequency Aging: ±1.5 ppm max. 1st 30 days, ±5 ppm max. Year 1, ±2 ppm max. Year 2+								
Start-up Time: 10.0 ms max.								
Frequency Range (MHz) 3/ 4/	Current (mA) (max. no load)		Models 1157 thru 1187 Only Current (mA) (max. no load)		Rise / Fall Times 1/ (ns max.)	Duty Cycle 1/ (%)		Fan-out (if TTL) 2/
	+5.5V	+3.63V	+5.5V	+3.63V		CMOS	TTL	
0.35 - 4.0	10	6	10	6	6	45 to 55	45 to 55	10
4.0 – 12.0	15	8	15	8	5	45 to 55	45 to 55	10
>12.0 – 24.0	15	10	15	10	5	45 to 55	40 to 60	10
>24.0 – 40.0	20	15	20	15	5	45 to 55	40 to 60	6
>40.0 – 65.0	35	20	40	25	5	45 to 55	40 to 60	6
>65.0 – 85.0	45	25	50	30	3	45 to 55	40 to 60	6
>85.0 – 100	55	30	N/A	35	3	40 to 60	40 to 60	6

1/. Waveform measurement points and logic limits are in accordance with MIL-PRF-55310.
2/. For +3.3V TTL option, R_L=160Ω for 10 TTL loads and R_L=270Ω for 6 TTL loads.
3/. Exception: Models 1157/1167/1177/1187 frequency range is 0.75 MHz to 100 MHz. Maximum frequency limit with +5.0V supply voltage is 85 MHz.
4/. Exception: Models 1179/1189/1199 maximum frequency limit is 70 MHz.

TABLE 2 - Electrical Performance Characteristics

OPERATION LISTING	REQUIREMENTS AND CONDITIONS
@ all Electrical Tests	
Input Current (no load)	MIL-PRF-55310, Para 4.8.5.1
Initial Accuracy @ Ref. Temp.	MIL-PRF-55310, Para 4.8.6
Output Logic Voltage Levels	MIL-PRF-55310, Para 4.8.21.3
Rise and Fall Times	MIL-PRF-55310, Para 4.8.22
Duty Cycle	MIL-PRF-55310, Para 4.8.23
@ Post Burn-In Electrical only	
Overvoltage Survivability	MIL-PRF-55310, Para 4.8.4
Initial Freq. – Temp. Accuracy	MIL-PRF-55310, Para 4.8.10.1
Freq. – Voltage Tolerance	MIL-PRF-55310, Para 4.8.14
Start-up Time (fast/slow start)	MIL-PRF-55310, Para 4.8.29

TABLE 3 - Electrical Test Parameters

Model #	Typical Thermal Resistance Junction to Case θ_{jc} (°C / W)	Δ Junction Temp. T_j (°C @ max. Icc) 1/	Typical Weight (Grams)
1101 / 1107 / 1121	30.77	9.31	3.0
1102 / 1108 / 1122	30.77	9.31	3.3
1103 / 1109 / 1119	27.88	8.44	1.4
1104 / 1110 / 1120	30.05	9.09	2.9
1105 / 1111	27.88	8.44	3.9
1115	29.92	9.05	2.2
1116 / 1117	31.62	9.57	1.2
1157 / 1167 / 1177 / 1187	12.84	3.53	0.2
1179/1189/1199	15.80	3.91	0.5

1/. Maximum operating power from Table 2 is used to calculate Δ Junction Temperatures.

TABLE 4 - Typical Thermal Characteristics and Weight

	Vcc=+5.0V			Vcc=+3.3V		
Frequency	Period Jitter 1 sigma (ps)	Phase Jitter (12kHz to 20MHz) (ps)	Period Jitter pk-pk (ps)	Period Jitter 1 sigma (ps)	Phase Jitter (12kHz to 20MHz) (ps)	Period Jitter pk-pk (ps)
1 MHz	8.5	8.0	60	20	11.3	150
24 MHz	6	0.22	48	10	0.33	85
40 MHz	5	0.16	40	8	0.25	70
80 MHz	5	0.08	40	6	0.14	45
100 MHz	4	0.08	32	5	0.14	40

Note: Period Jitter measured at +23C and Nominal Voltage using Wavecrest Model SIA-3000.

TABLE 4a – Typical Jitter Performance

OPN. NO.	OPERATION LISTING	REQUIREMENTS AND CONDITIONS	Option A	Option B	Option C	Option D	Option E	Option F	Option G	Option S	Option X
	SCREENING	MIL Class Similarity (MIL-PRF-55310, Class S/B or MIL-PRF-38534, Class K)	K 100%	B- 100%	S- 100%	K+ 100%	B 100%	S (Rev E) 100%	 100%	S (Rev F) 100%	EM 100%
1	Non-Destruct Bond Pull	MIL-STD-883, Meth 2023	X	NR	X	X	NR	X	NR	X	NR
2	Internal Visual	MIL-STD-883, Meth 2017 Class K, Meth 2032 Class K	X	X	X	X	X	X	X	X	X
3	Stabilization (Vacuum) Bake	MIL-STD-883, Meth 1008, Cond C, 150°C	X 48 hrs.	X 24 hrs.	X 48 hrs.	X 48 hrs.	X 24 hrs.	X 48 hrs.	X 24 hrs.	X 48 hrs.	X 24 hrs.
4	Random Vibration	MIL-STD-883, Meth 2026, Cond I-B, 15 mins in each axis	NR	NR	NR	NR	NR	NR	NR	X	NR
5	Thermal Shock	MIL-STD-883, Meth 1011, Cond A	NR	NR	X	NR	NR	X	NR	X	NR
6	Temperature Cycle	MIL-STD-883, Meth 1010, Cond. B (except Option S), 10 cycles min.	X	X	X	X	X	X	X	X Cond. C	NR
7	Constant Acceleration	MIL-STD-883, Meth 2001, Cond A, Y1 plane only, 5000 g's	X	X	X	X	X	X	X	X	NR
8	Particle Impact Noise Detection	MIL-STD-883, Meth 2020, Cond B (except Option S)	X	X	X	X	X	X	NR	X Cond. A	X
9	Electrical Testing, Pre Burn-In	Perform tests in Table 3. Nominal Vcc, nominal temperature	X	X	X	X	X	X	X	X	X
10	1st Burn-In	MIL-STD-883, Meth 1015, Cond B	X 160 hrs.	X 160 hrs.	X 240 hrs.	X 160 hrs.	X 160 hrs.	X 240 hrs.	X 160 hrs.	X 240 hrs.	NR
11	Electrical Testing, Intermediate	Perform tests in Table 3. Nominal Vcc, nominal temperature	X	NR	NR	X	NR	NR	NR	NR	NR
12	2nd Burn-In	MIL-STD-883, Meth 1015, Cond B	X 160 hrs.	NR	NR	X 160 hrs.	NR	NR	NR	NR	NR
13	Electrical Testing, Post Burn-In (Group A)	Perform tests in Table 3. Nominal Vcc & extremes, nominal temperature & extremes	X	X	X	X	X	X	X nom. Vcc	X	NR
14	Seal: Fine Leak Seal: Gross Leak	MIL-STD-202, Meth 112, Cond C (5×10^{-8} atm cc/sec max) MIL-STD-202, Meth 112, Cond D	X	X	X	X	X	X	X	NR	X
15	Seal: Fine Leak Seal: Gross Leak	MIL-STD-883, Meth 1014, Cond A2 or B1 MIL-STD-883, Meth 1014, Cond B2 or B3	NR	NR	NR	NR	NR	NR	NR	X	NR
16	Radiographic Inspection	MIL-STD-883, Meth 2012	X	AR	AR	X	AR	X	NR	X	NR
17	Solderability	MIL-STD-883, Meth 2003	1/	1/	1/	1/	1/	1/	1/	1/	NR
18	External Visual & Mechanical	MIL-STD-883, Meth 2009	X 2/	X 2/	X 2/	X 2/	X 2/	X 2/	X 2/	X 2/	X 2/
19	Aging, 30 Day 3/ (M55310 Group B)	MIL-PRF-55310, para. 4.8.35.1	NR	NR	NR	X	13 pcs.	X	NR	X	NR
20	Group C Inspection (optional)	See Para 5.2 herein for details of supplier recommended Group C Inspection options	5.2(g)	5.2(e)	5.2(e)	5.2(g)	5.2(e)	5.2(e)	5.2(e)	5.2(f)	NR

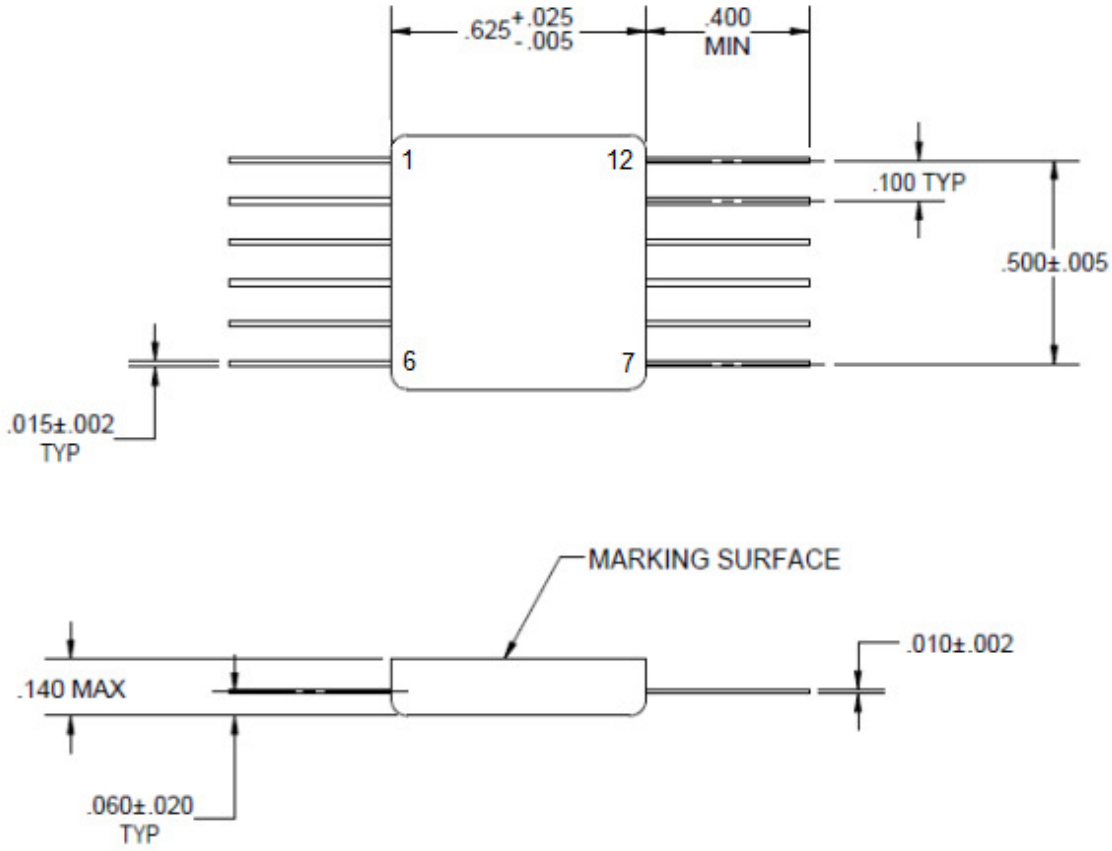
LEGEND: X = Required, NR = Not Required, AR = As Required

TABLE 5 - Test Matrix

1/ Performed at package LAT. Include LAT data sheet.

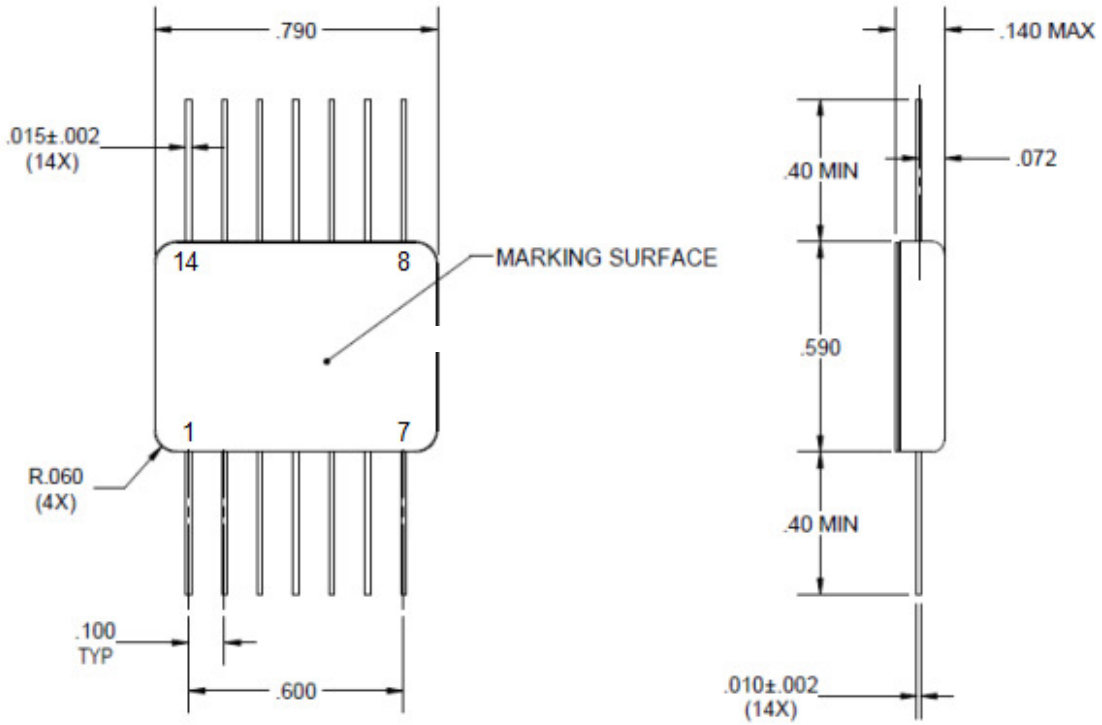
2/ When specified, RGA samples will be removed from the lot after completion of this operation. Use of Screening failures require customer concurrence.

3/ By customer request, the Aging test may be terminated after 15 days if the measured aging rate is less than one-half the specified aging rate, as described in paragraph 4.3.4.1 herein. Must be explicitly stated on the customer PO.



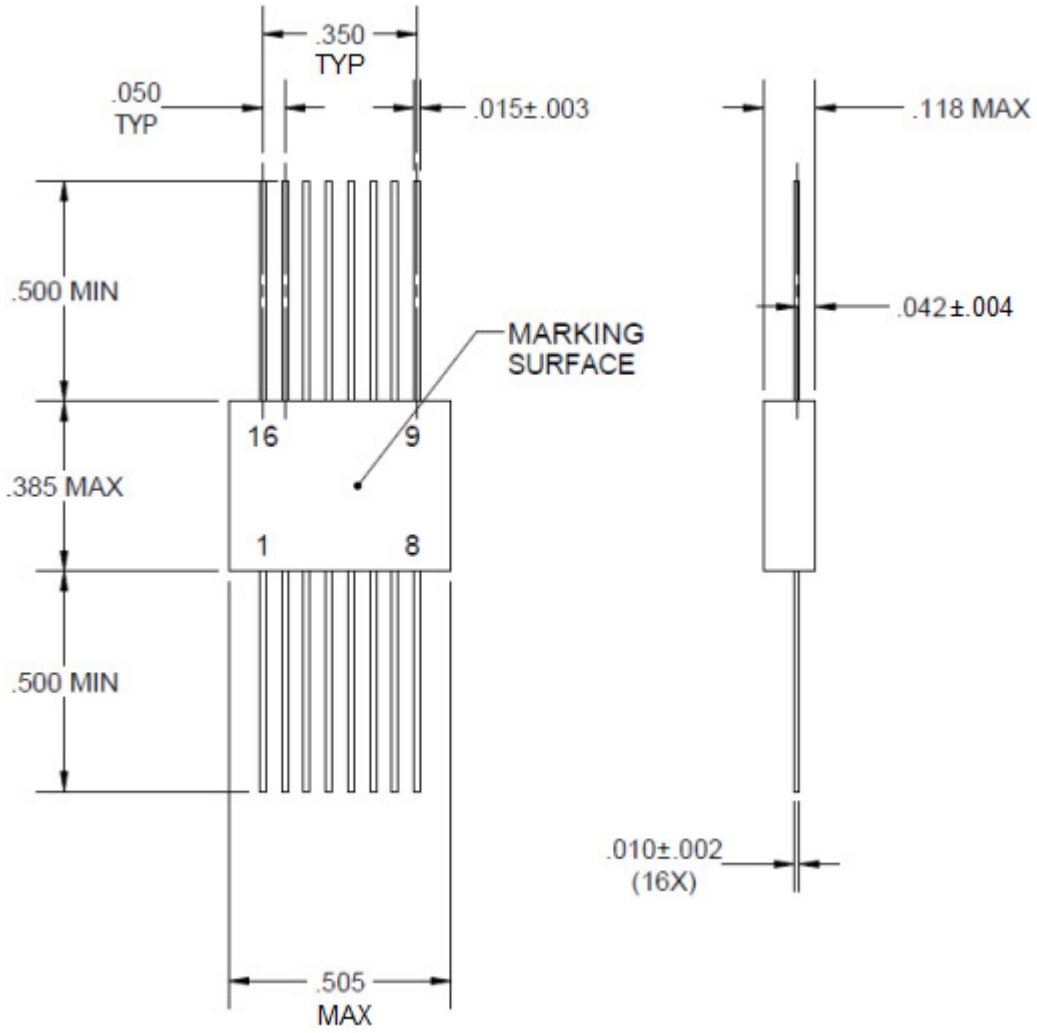
Pin	Function
6	GND/Case
7	Output
12	Vcc
All Others	No Internal Connection

FIGURE 1
Models 1101 & 1107 Package Outline



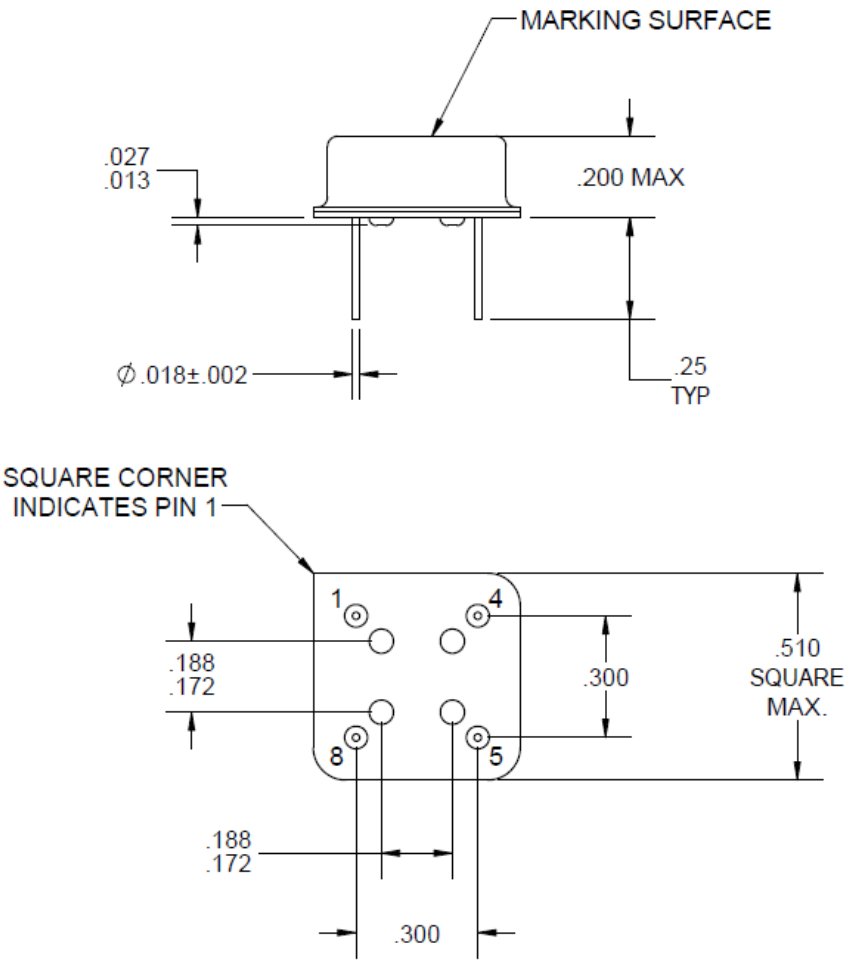
Pin	Function
7	GND/Case
8	Output
14	Vcc
All Others	No Internal Connection

FIGURE 2
Models 1102 & 1108 Package Outline
Tolerances: Unspecified = ±0.010”



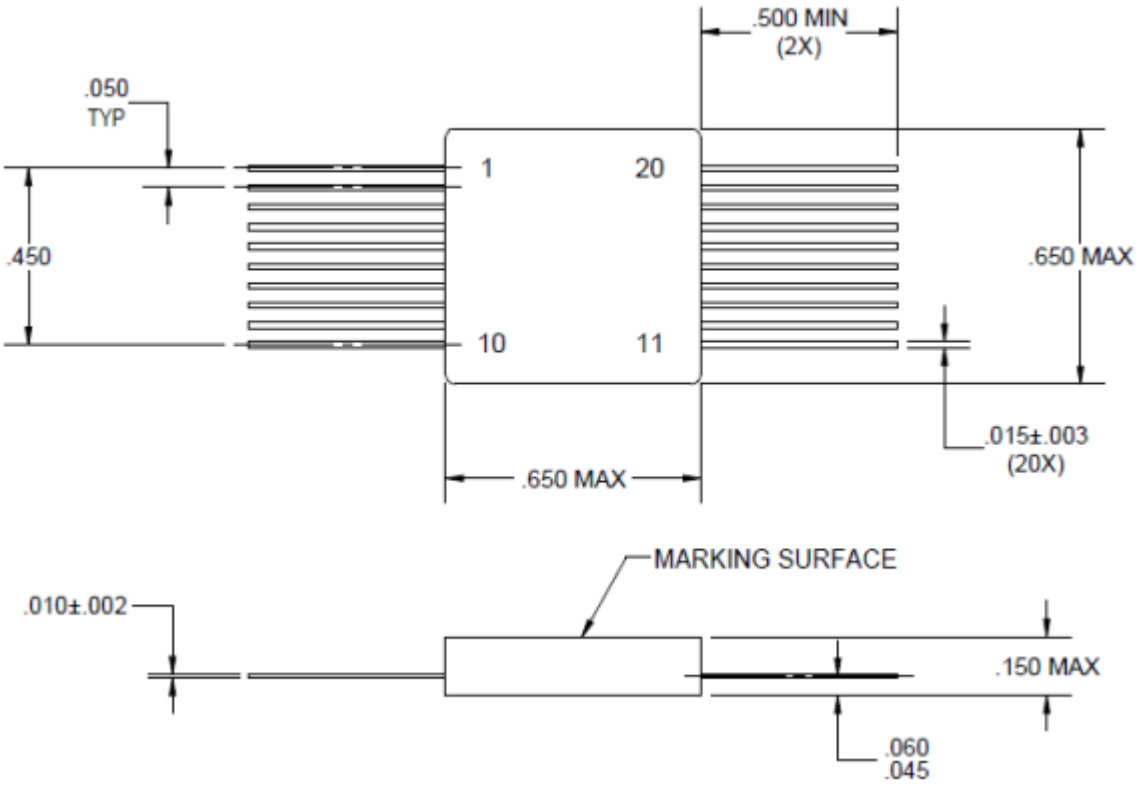
Pin	Function
9	GND/Case
10	Output
8	Vcc
All Others	No Internal Connection

FIGURE 3
Models 1103 & 1109 Package Outline



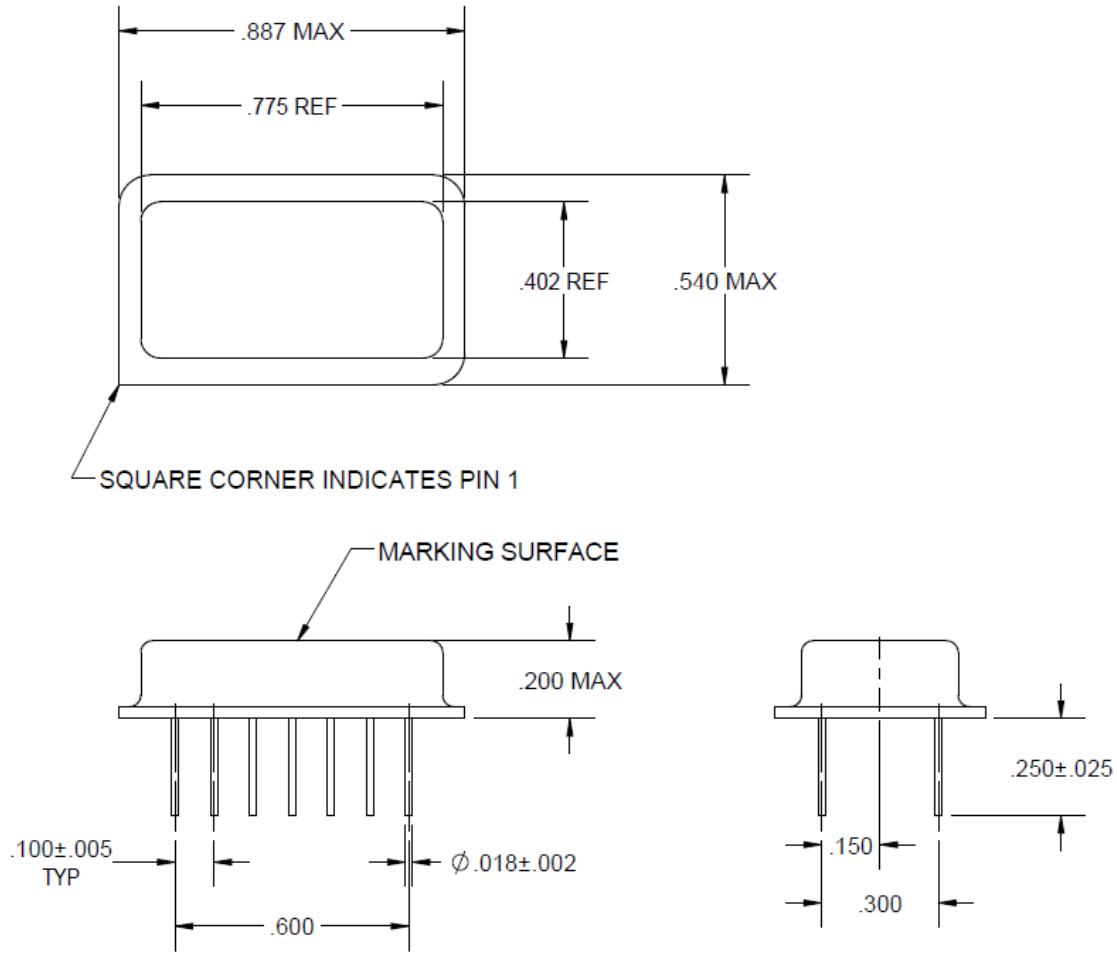
Pin	Function
4	GND/Case
5	Output
8	Vcc
All Others	No Internal Connection

FIGURE 4
Model 1115 Package Outline



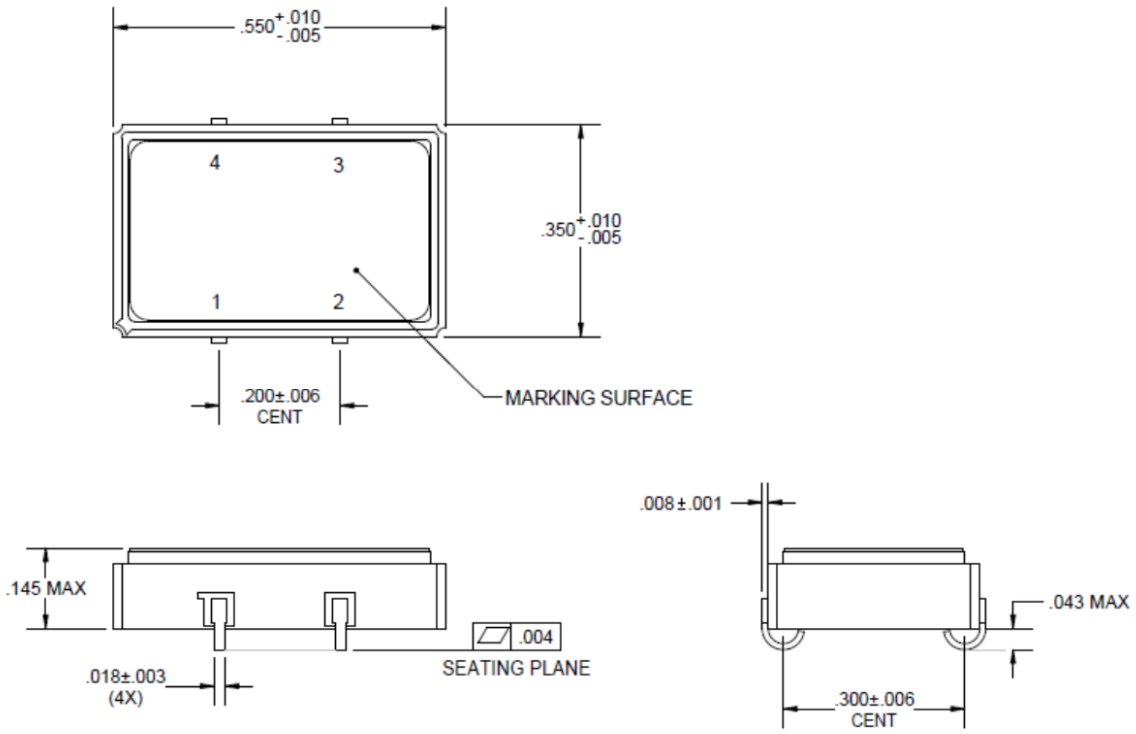
Pin	Function
10	GND/Case
11	Output
13, 20	Vcc
All Others	No Internal Connection

FIGURE 5
Model 1104 & 1110 Package Outline



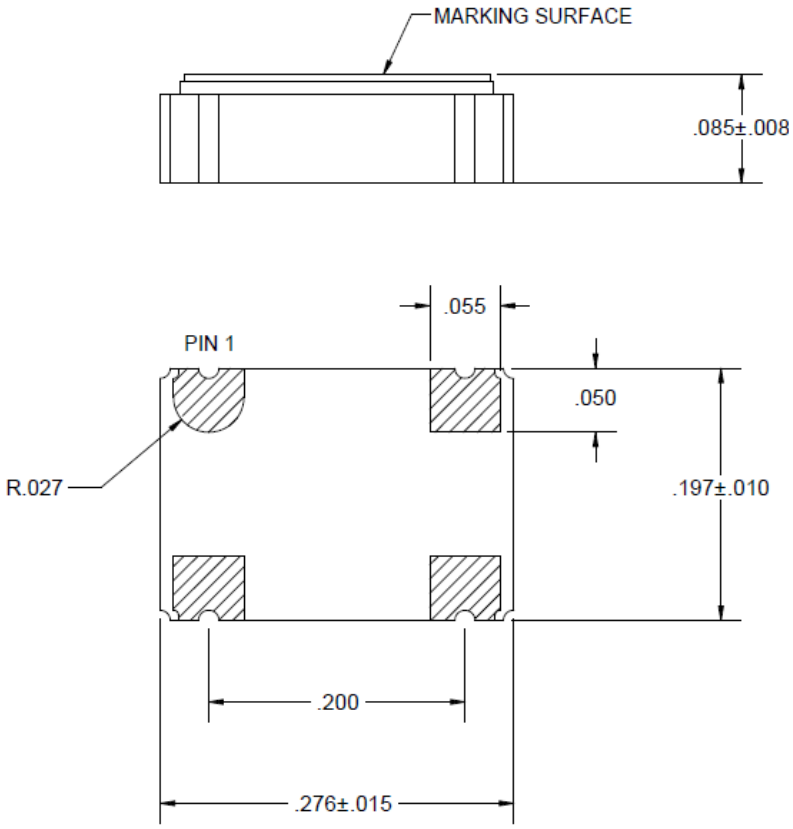
Pin	Function
7	GND/Case
8	Output
14	Vcc
All Others	No Internal Connection

FIGURE 6
Model 1105 & 1111 Package Outline



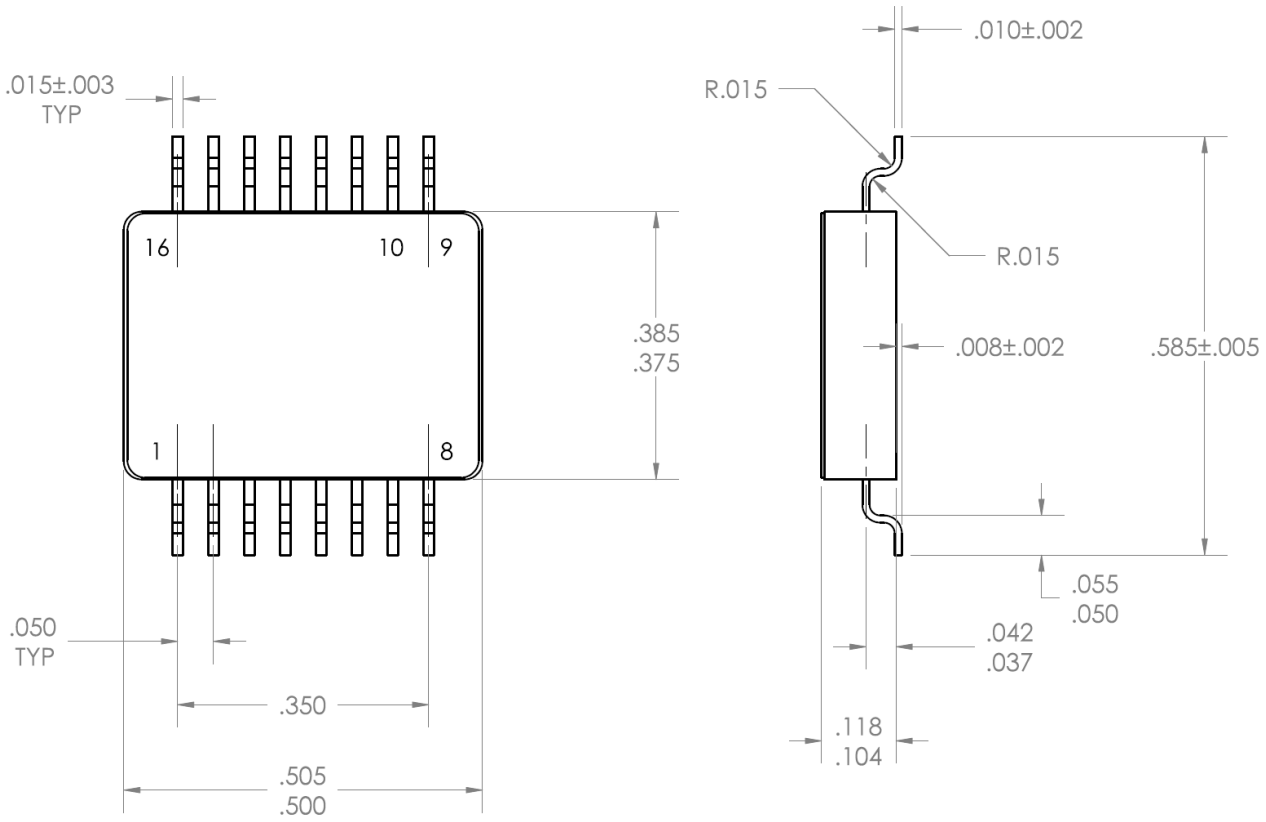
Pin	Function
1	Enable/Disable
2	GND/Case
3	Output
4	Vcc

FIGURE 7
Model 1116 & 1117 Package Outline



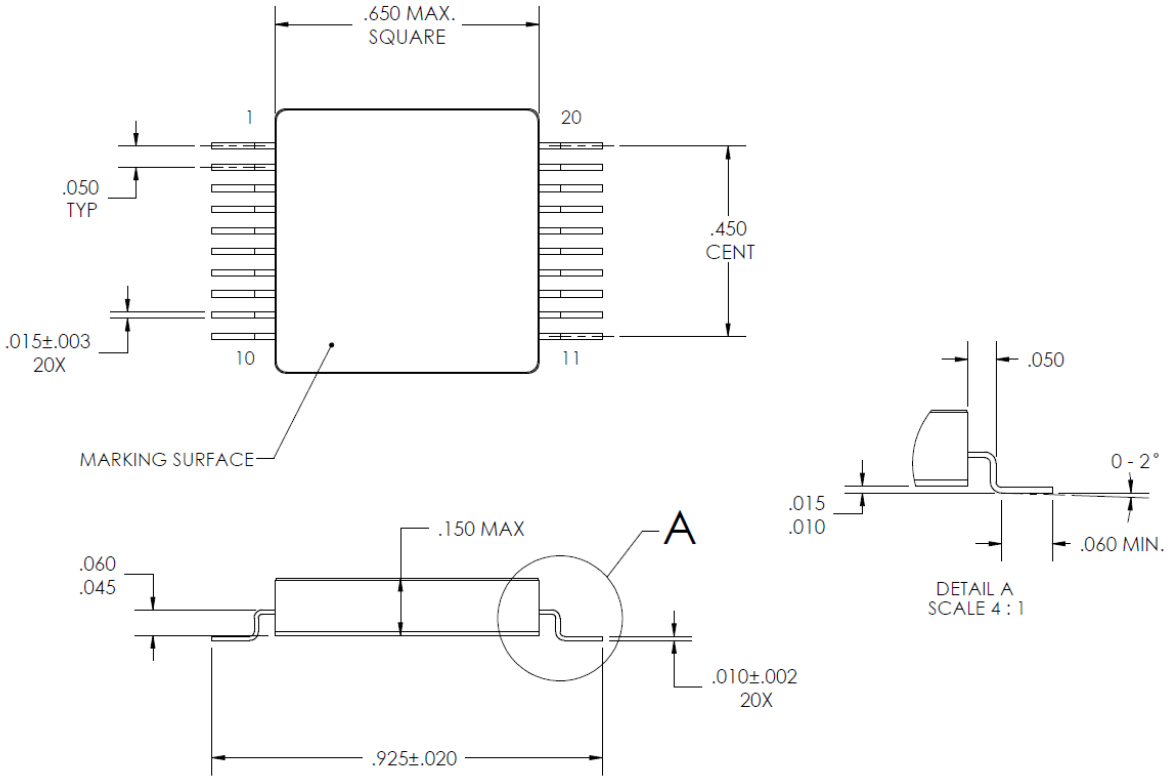
Pin	Function
1	Enable/Disable
2	GND/Case
3	Output
4	Vcc

FIGURE 8
Model 1157 Package Outline



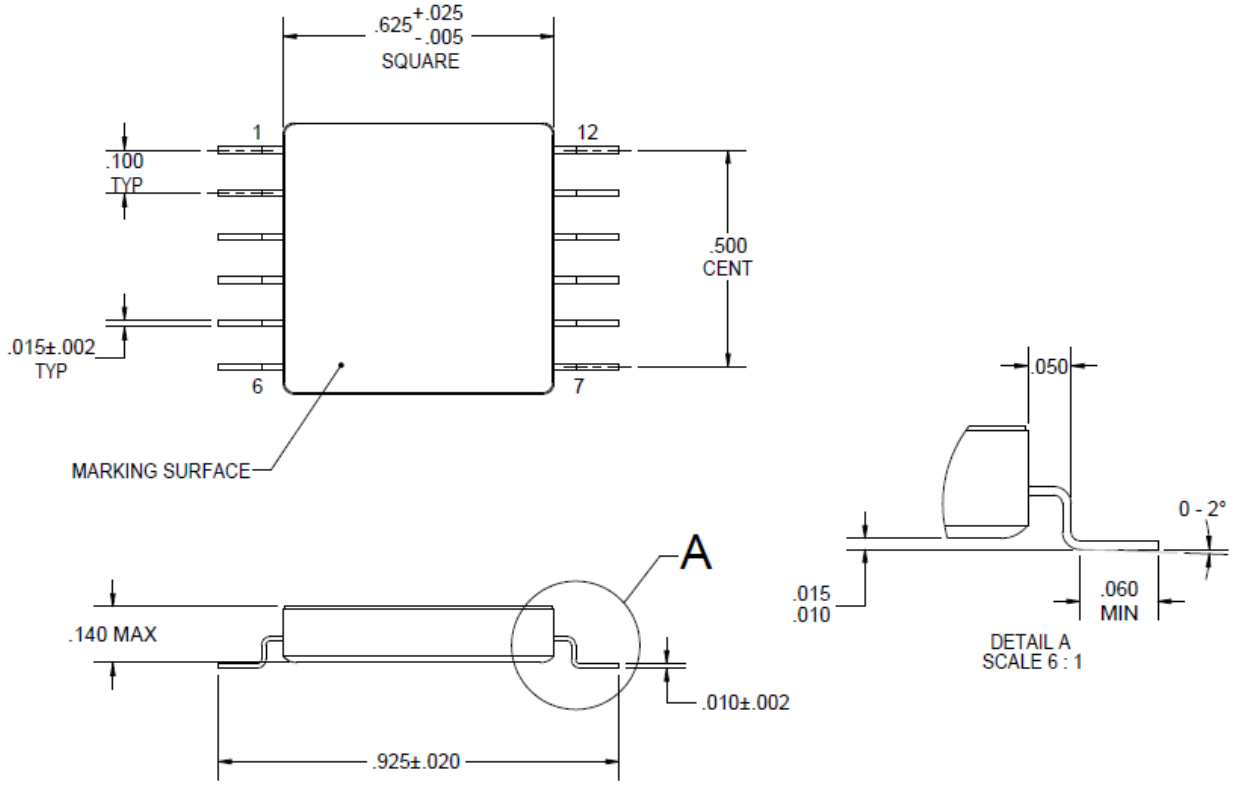
Pin	Function
9	GND/Case
10	Output
8	Vcc
All Others	No Internal Connection

FIGURE 9
Model 1119 Package Outline



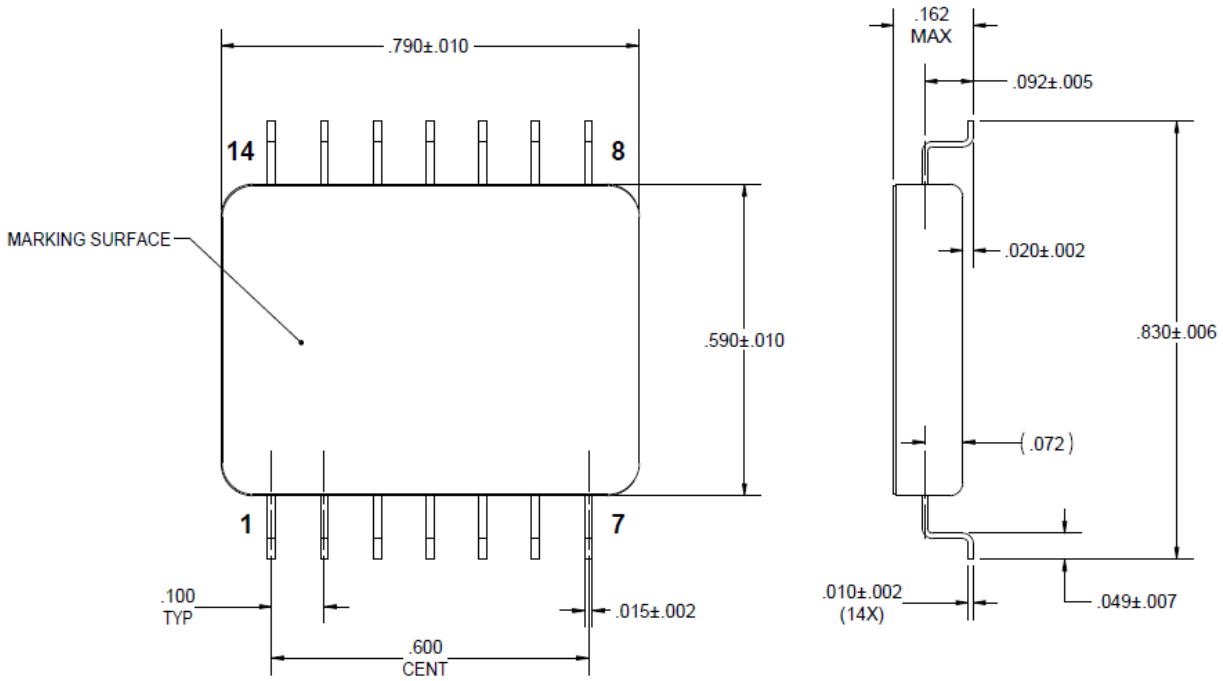
Pin	Function
10	GND/Case
11	Output
13, 20	Vcc
All Others	No Internal Connection

FIGURE 10
Model 1120 Package Outline



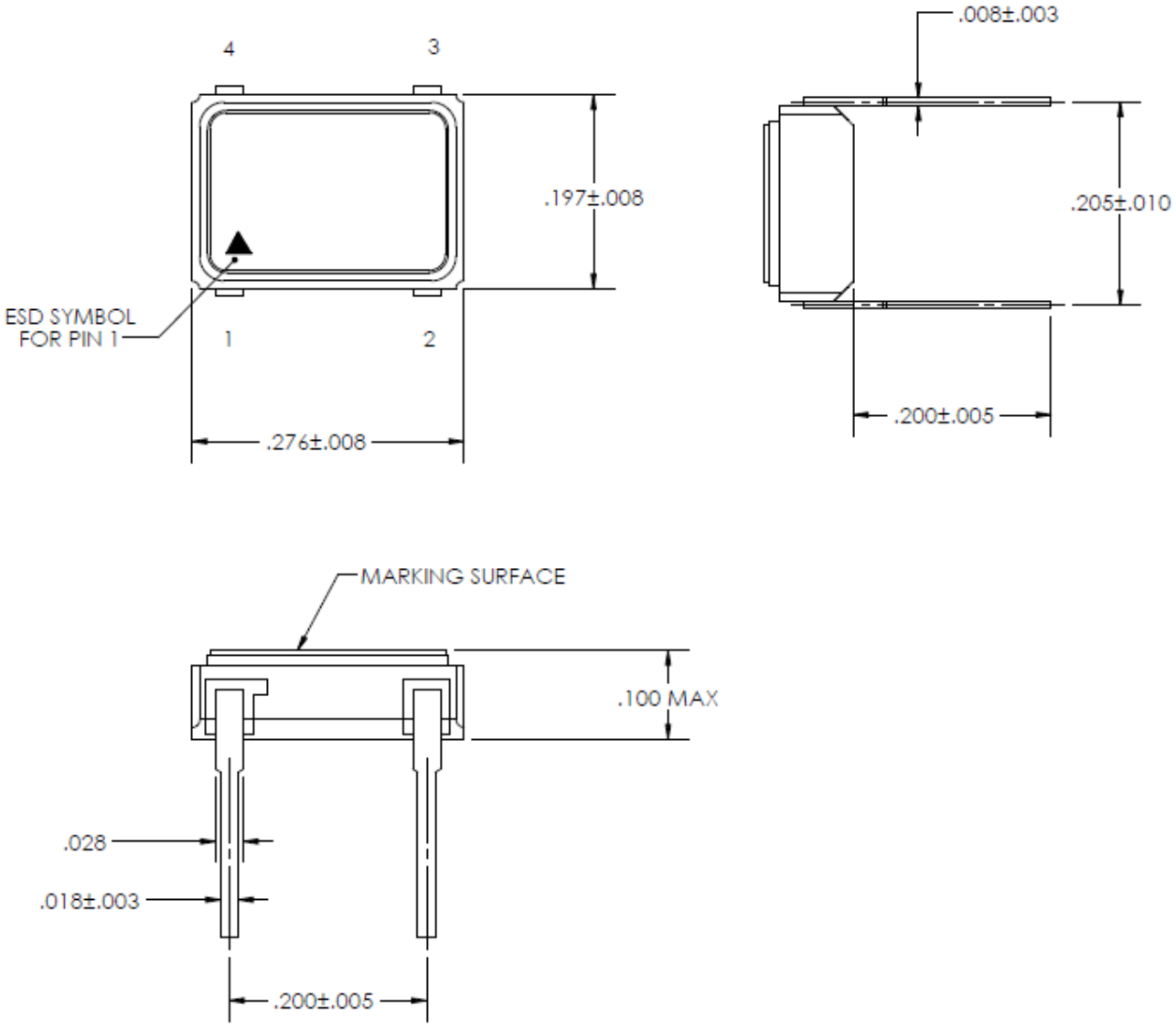
Pin	Function
6	GND/Case
7	Output
12	Vcc
All Others	No Internal Connection

FIGURE 11
Model 1121 Package Outline



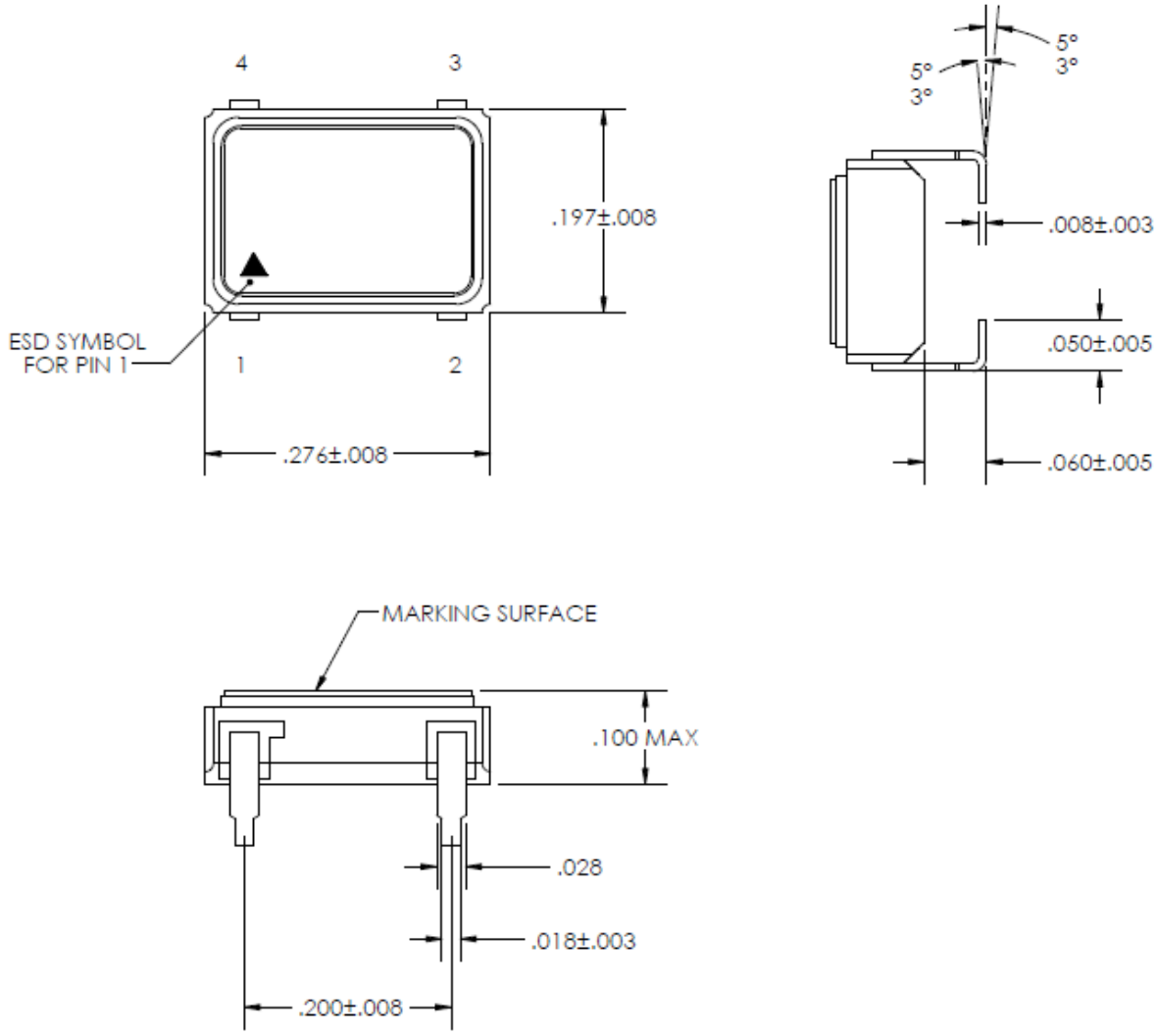
Pin	Function
7	GND/Case
8	Output
14	Vcc
All Others	No Internal Connection

FIGURE 12
Model 1122 Package Outline



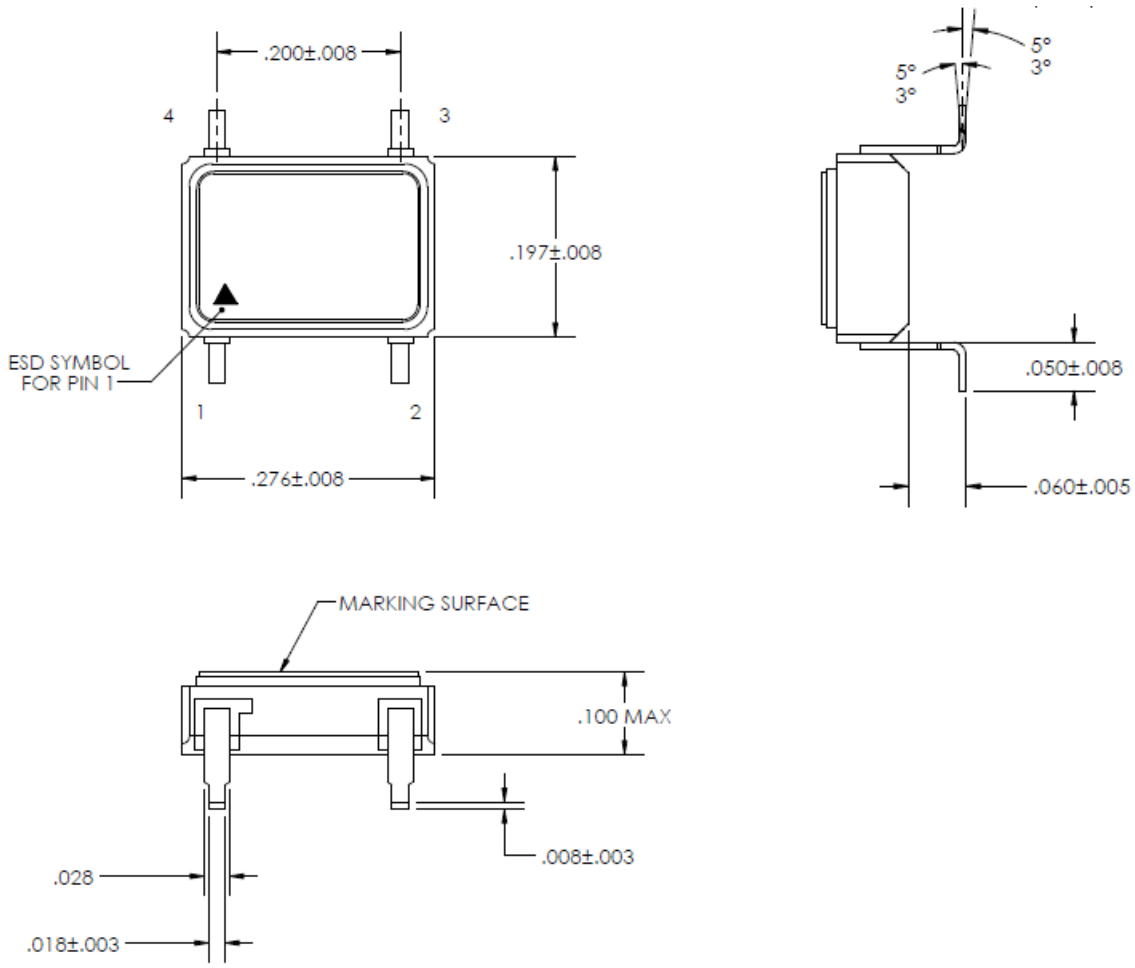
Pin	Function
1	Enable/Disable
2	GND/Case
3	Output
4	Vcc

FIGURE 13
Model 1167 Package Outline



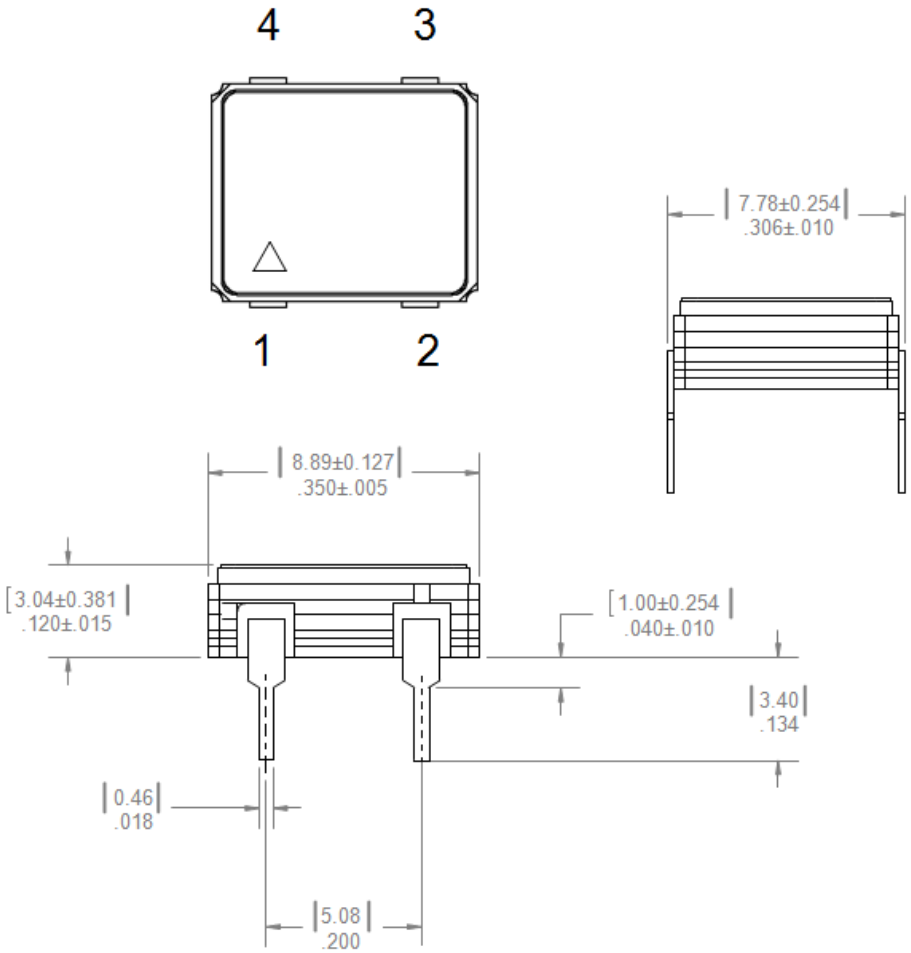
Pin	Function
1	Enable/Disable
2	GND/Case
3	Output
4	Vcc

FIGURE 14
Model 1177 Package Outline



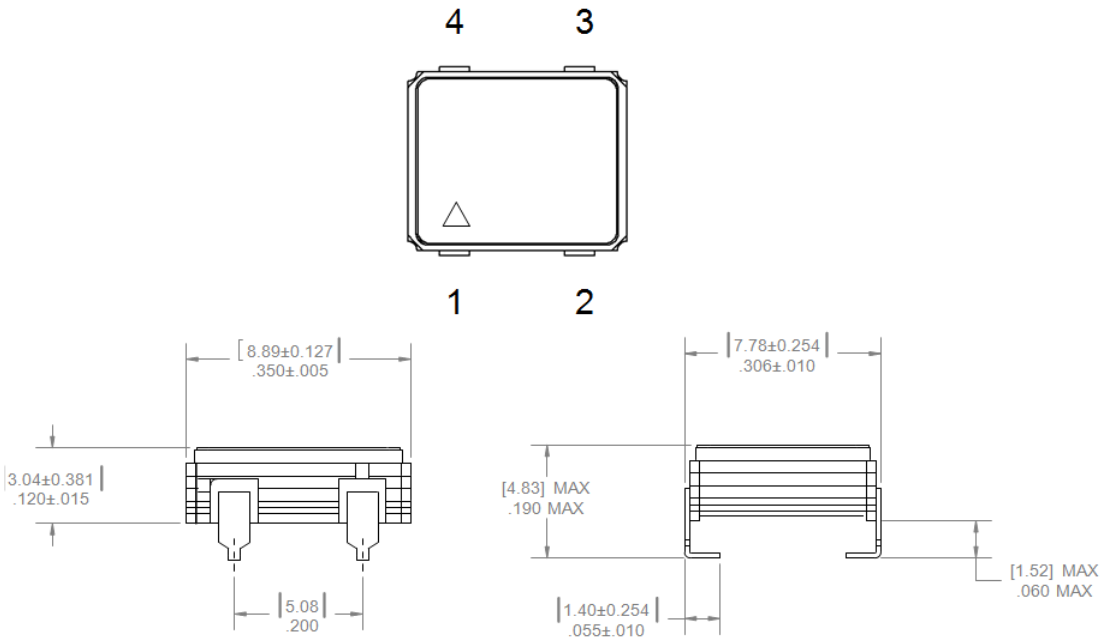
Pin	Function
1	Enable/Disable
2	GND/Case
3	Output
4	Vcc

FIGURE 15
Model 1187 Package Outline



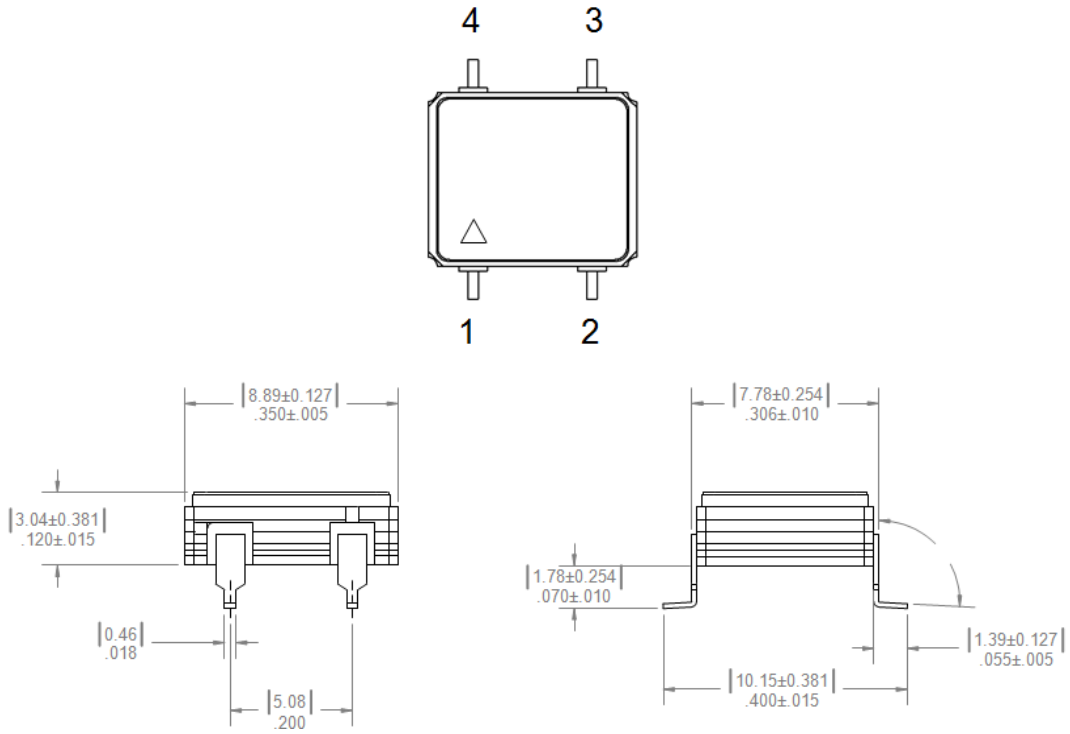
Pin	Function
1	Enable/Disable
2	GND
3	Out
4	Vcc

FIGURE 16
Model 1179 Package Outline



Pin	Function
1	Enable/Disable
2	GND
3	Out
4	Vcc

FIGURE 17
Model 1189 Package Outline

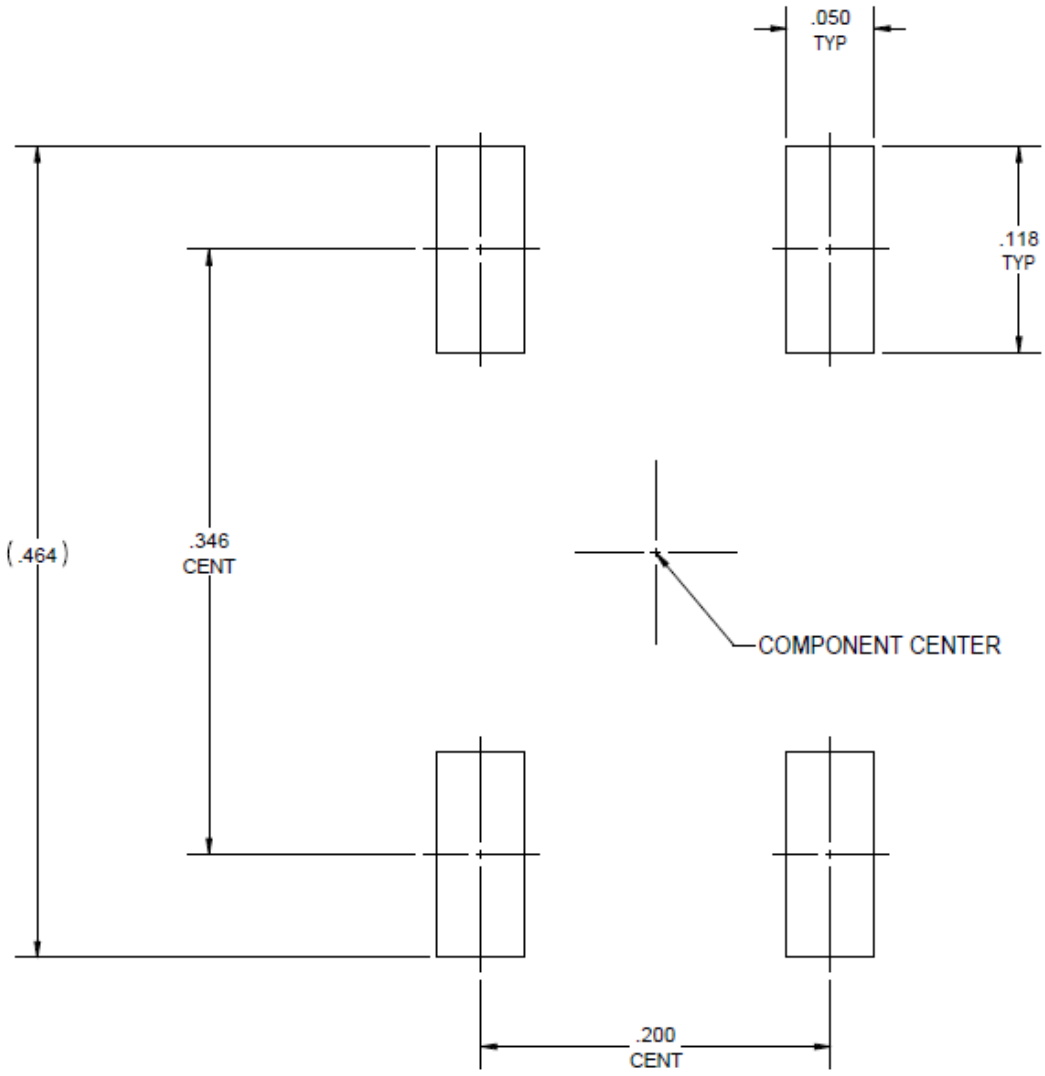


Pin	Function
1	Enable/Disable
2	GND
3	Out
4	Vcc

FIGURE 18
Model 1199 Package Outline

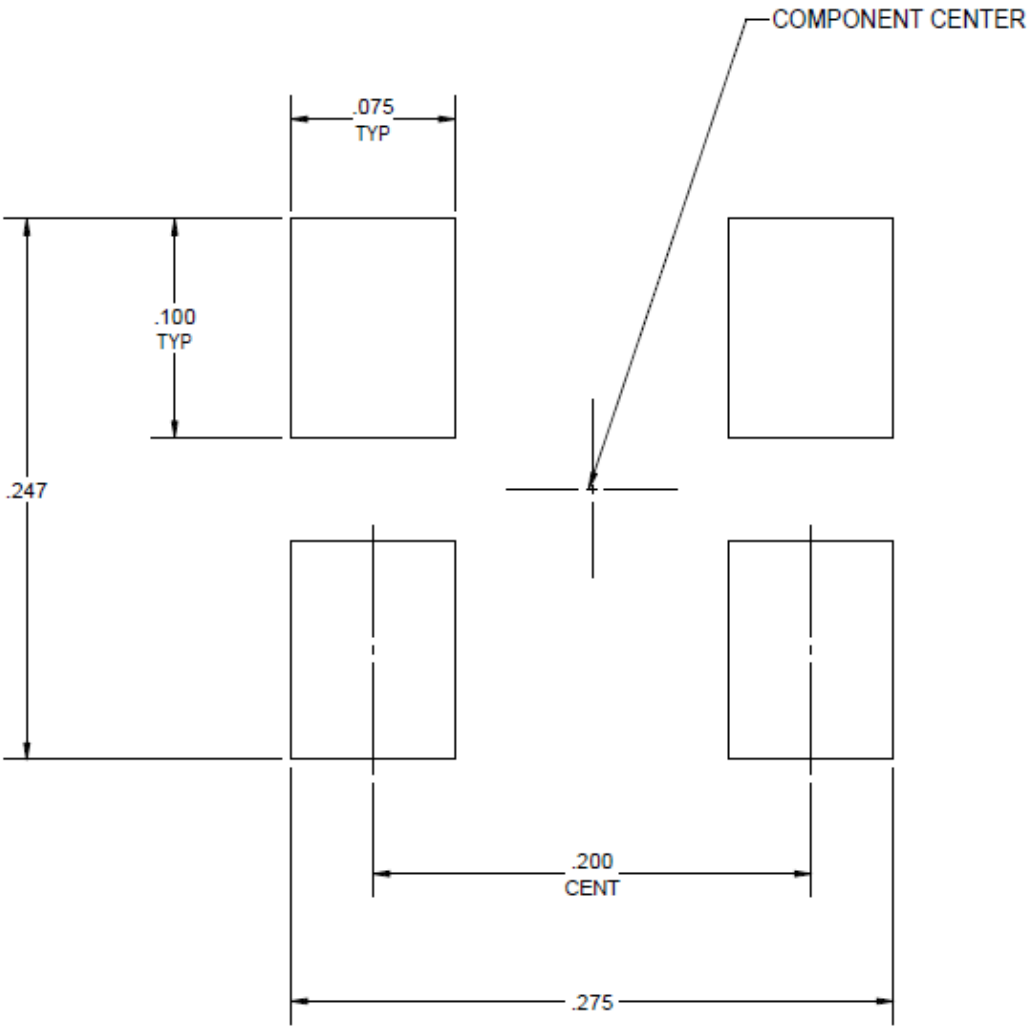
APPENDIX A

Recommended Land Patterns

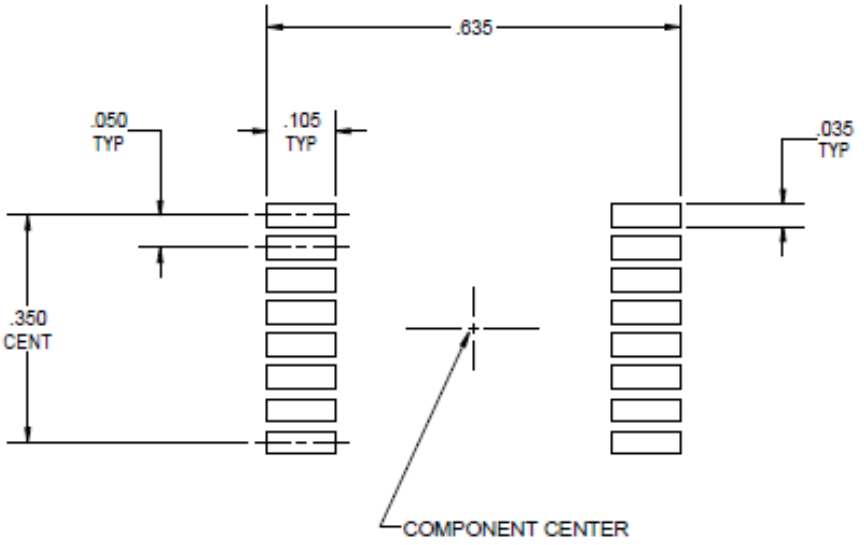


Model 1116 & 1117

SIZE	CODE IDENT NO.	THIRD ANGLE PROJECTION	UNSPECIFIED TOLERANCES	DWG NO.	REV.	SHEET
A	**00136**		**N/A**	**OS-68338**	Q	**32**

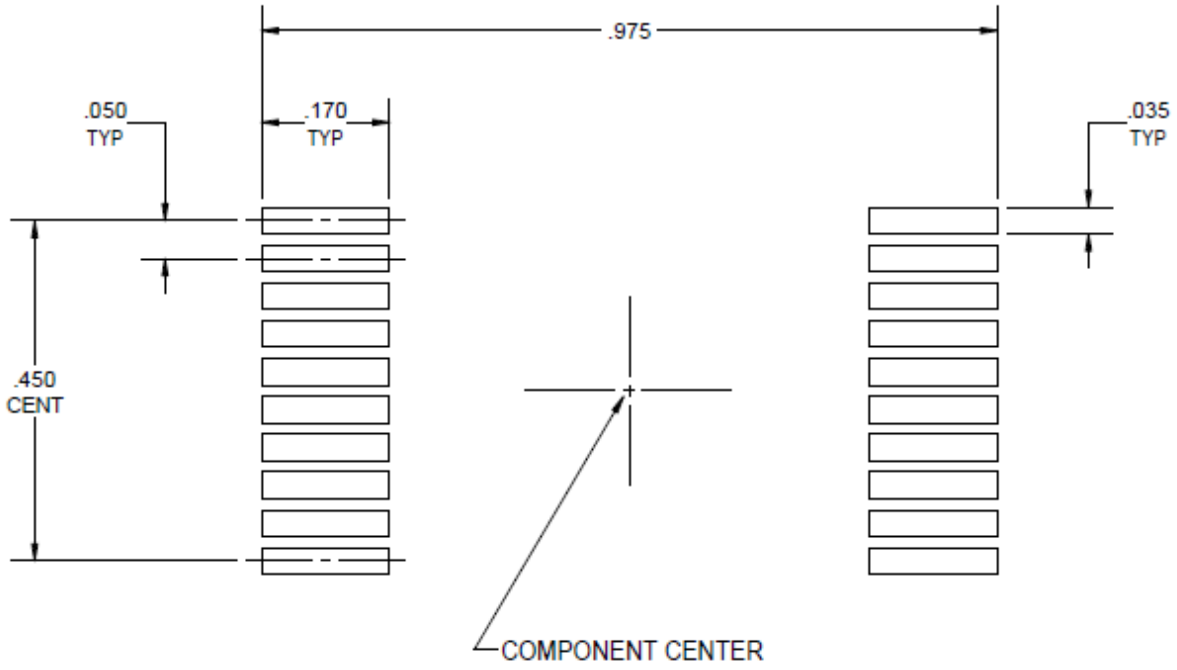


Model 1157

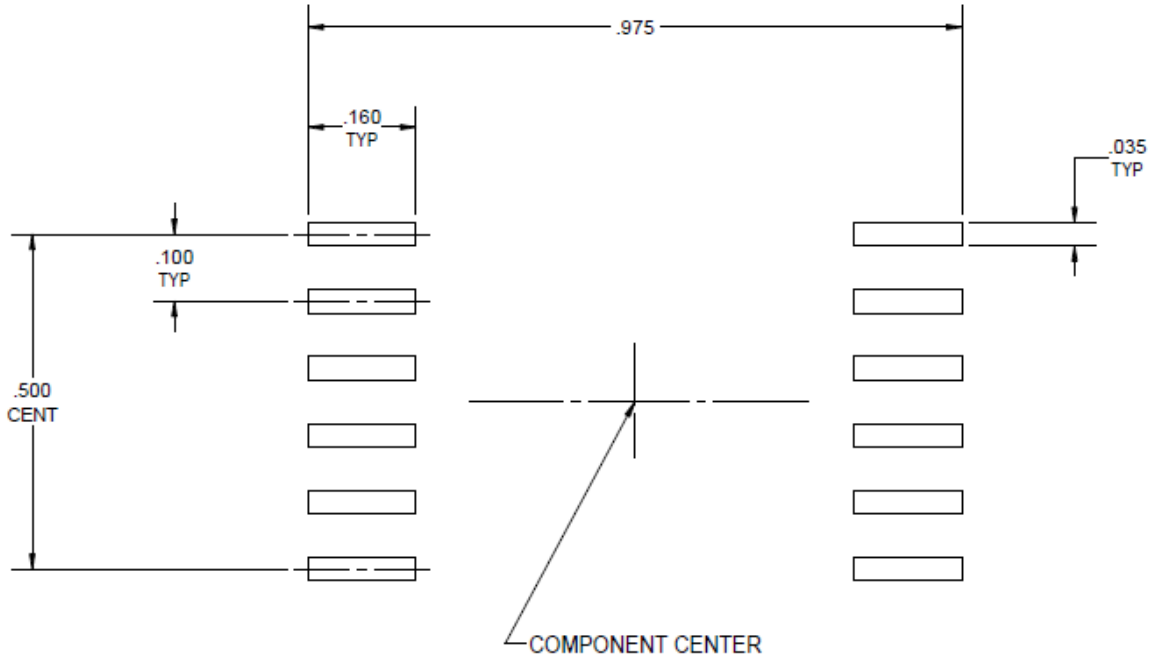


Model 1119

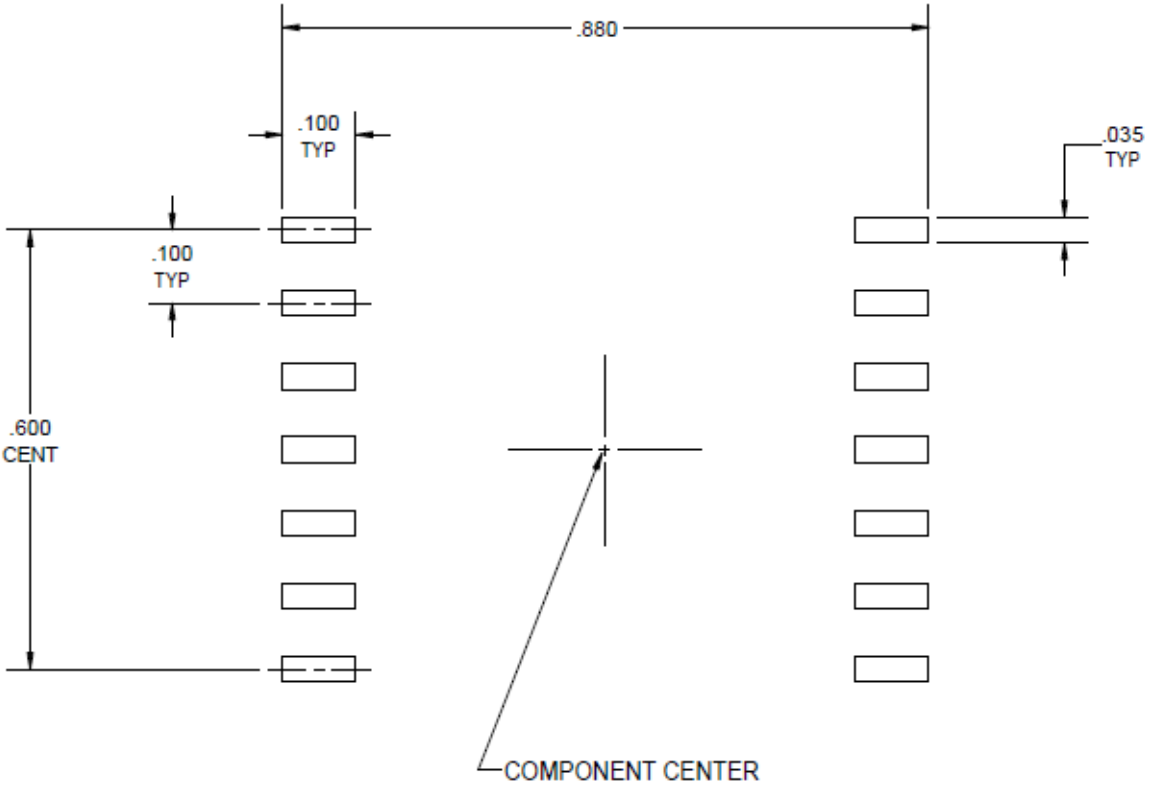
SIZE	CODE IDENT NO.	THIRD ANGLE PROJECTION	UNSPECIFIED TOLERANCES	DWG NO.	REV.	SHEET
A	**00136**		**N/A**	**OS-68338**	Q	**33**



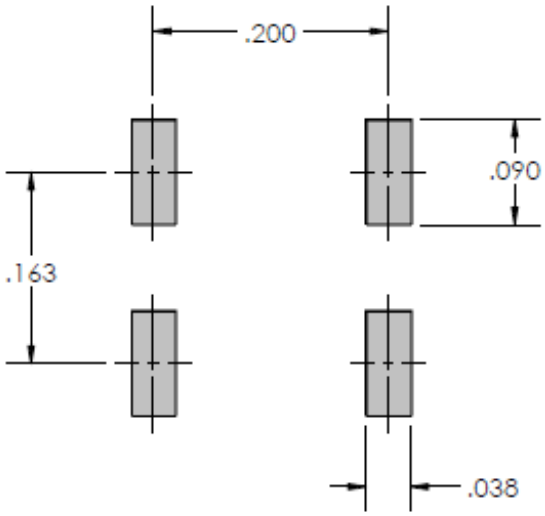
Model 1120



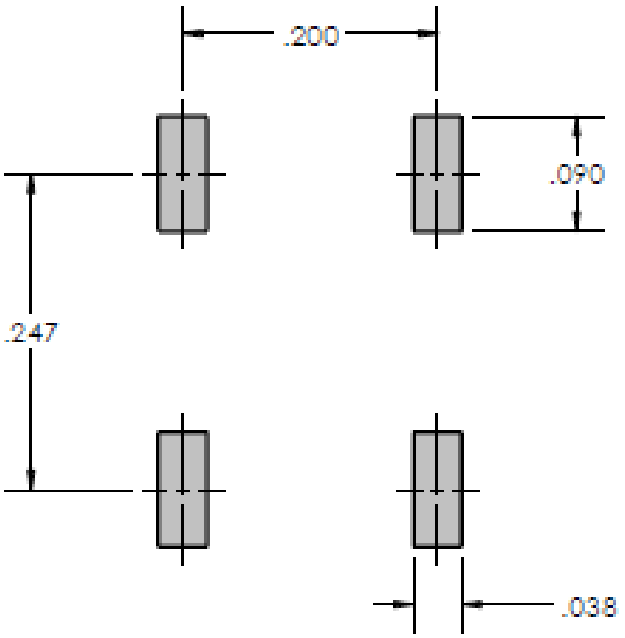
Model 1121



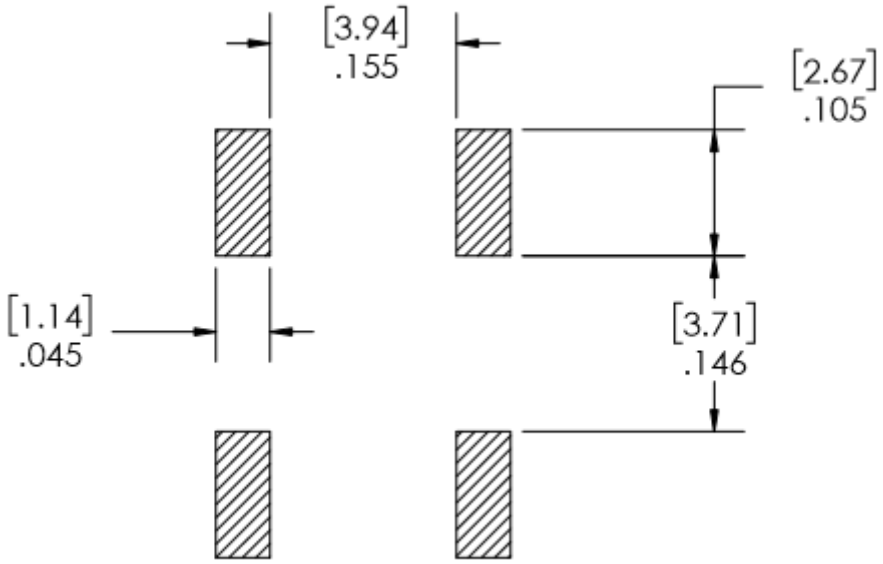
Model 1122



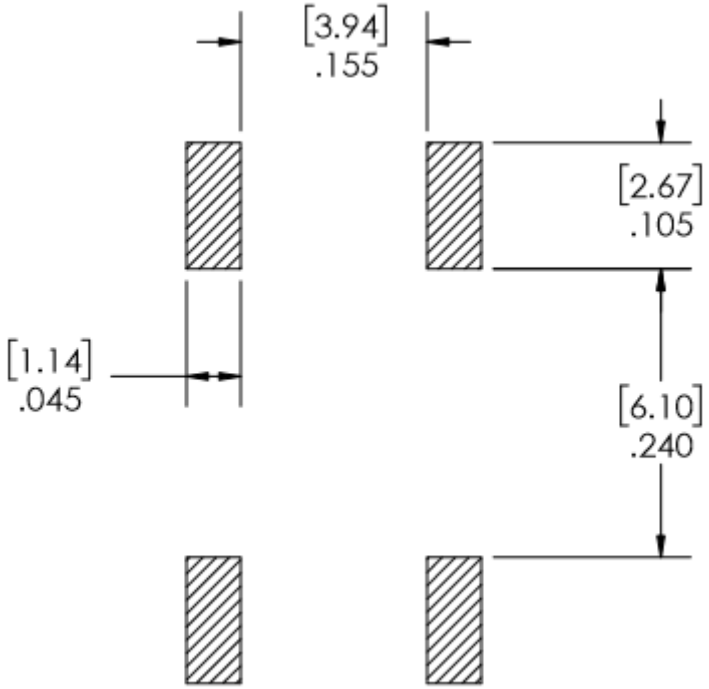
Model 1177



Model 1187



Model 1189



Model 1199

SIZE	CODE IDENT NO.	THIRD ANGLE PROJECTION	UNSPECIFIED TOLERANCES	DWG NO.	REV.	SHEET
A	**00136**		**N/A**	**OS-68338**	Q	**37**