

# MOSFET – N-Channel

## QFET®

### 600 V, 0.3 A, 11.5 Ω

## FQN1N60C

### Description

This N-Channel enhancement mode power MOSFET is produced using ON Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

### Features

- 0.3 A, 600 V,  $R_{DS(on)} = 11.5 \Omega$  (Max.) @  $V_{GS} = 10$  V,  $I_D = 0.15$  A
- Low Gate Charge (Typ. 4.8 nC)
- Low Crss (Typ. 3.5 pF)
- 100% Avalanche Tested

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit	
$V_{DSS}$	Drain to Source Voltage	600	V	
$V_{GSS}$	Gate to Source Voltage	$\pm 30$	V	
$I_D$	Drain Current Continuous ( $T_C = 25^\circ\text{C}$ ) Continuous ( $T_C = 100^\circ\text{C}$ )	0.3 0.18	A	
$I_{DM}$	Drain Current – Pulsed	(Note 1)	1.2	A
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	33	mJ
$I_{AR}$	Avalanche Current	(Note 1)	0.3	A
$E_{AR}$	Repetitive Avalanche Energy	(Note 1)	0.3	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$	(Note 3)	4.5	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ ) ( $T_L = 25^\circ\text{C}$ ) Derate above $25^\circ\text{C}$	1 3 0.02	W W W/ $^\circ\text{C}$	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$	
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$	

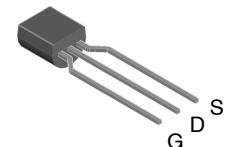
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2.  $L = 59$  mH,  $I_{AS} = 1.1$  A,  $V_{DD} = 50$  V,  $R_G = 25 \Omega$ , Starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 0.3$  A,  $di/dt \leq 200$  A/ $\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$ .

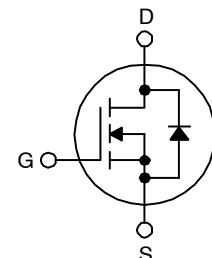


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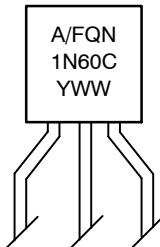
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TO-92 4.75x4.80  
CASE 135AV



### MARKING DIAGRAM



A = Assembly Site  
 FQN1N60C = Specific Device Code  
 Y = Year of Production  
 WW = Work Week Number

### ORDERING INFORMATION

Device	Package	Shipping
FQN1N60CTA	TO-92 3LD	2000 / Fan-Fold

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JL}$	Thermal Resistance, Junction-to-Lead, Max. (Note 5)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max. (Note 6)	140	

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTIC

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	600	–	–	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}, \text{Referenced to } 25^\circ\text{C}$	–	0.6	–	V/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 600 \text{ V}, V_{GS} = 0 \text{ V}$	–	–	50	$\mu\text{A}$
		$V_{DS} = 480 \text{ V}, T_C = 125^\circ\text{C}$	–	–	250	
$I_{GSSF}$	Gate to Body Leakage Current, Forward	$V_{GS} = 30 \text{ V}, V_{DS} = 0 \text{ V}$	–	–	100	nA
$I_{GSSR}$	Gate to Body Leakage Current, Reverse	$V_{GS} = -30 \text{ V}, V_{DS} = 0 \text{ V}$	–	–	-100	nA

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	2.0	–	4.0	V
$R_{DS(on)}$	Static Drain to Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 0.15 \text{ A}$	–	9.3	11.5	Ω
$g_{FS}$	Forward Transconductance	$V_{DS} = 40 \text{ V}, I_D = 0.3 \text{ A}$	–	0.75	–	S

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz}$	–	130	170	pF
$C_{oss}$	Output Capacitance		–	19	25	pF
$C_{rss}$	Reverse Transfer Capacitance		–	3.5	6	pF

### SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300 \text{ V}, I_D = 1.1 \text{ A}, R_G = 25 \Omega$ (Note 4)	–	7	24	ns
$t_r$	Turn-On Rise Time		–	21	52	ns
$t_{d(off)}$	Turn-Off Delay Time		–	13	36	ns
$t_f$	Turn-Off Fall Time		–	27	64	ns
$Q_g$	Total Gate Charge	$V_{DS} = 480 \text{ V}, I_D = 1.1 \text{ A}, V_{GS} = 10 \text{ V}$ (Note 4)	–	4.8	6.2	nC
$Q_{gs}$	Gate to Source Charge		–	0.7	–	nC
$Q_{gd}$	Gate to Drain Charge		–	2.7	–	nC

### DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

$I_S$	Maximum Continuous Drain to Source Diode Forward Current	–	–	0.3	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	–	–	1.2	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 0.3 \text{ A}$	–	–	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_S = 1.1 \text{ A}, dI_F/dt = 100 \text{ A}/\mu\text{s}$	–	190	–	ns
$Q_{rr}$	Reverse Recovery Charge		–	0.53	–	$\mu\text{C}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature.
5. Reference point of the  $R_{\theta JL}$  is the drain lead.
6. When mounted on 3"x4.5" FR-4 PCB without any pad copper in a still air environment  
( $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance.  $R_{\theta CA}$  is determined by the user's board design)

## TYPICAL CHARACTERISTICS

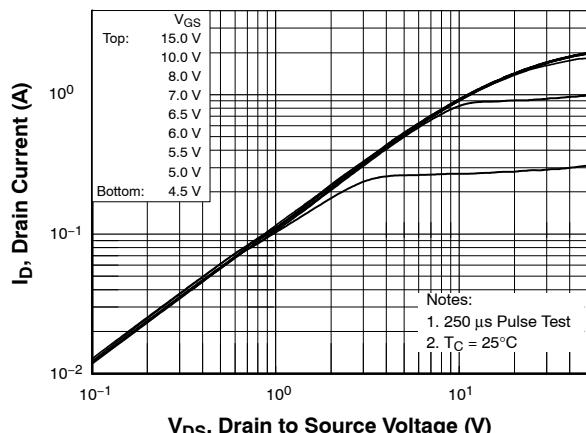


Figure 1. On-Region Characteristics

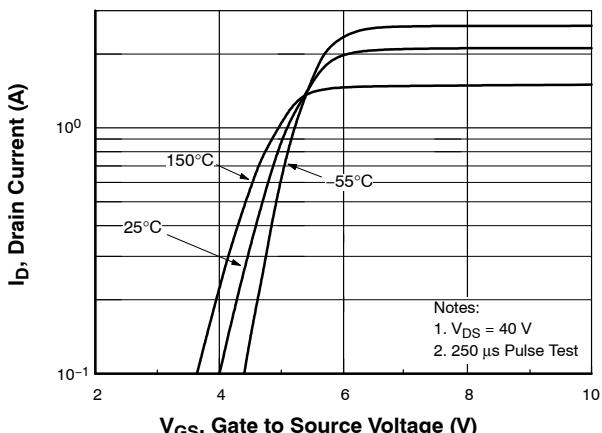


Figure 2. Transfer Characteristics

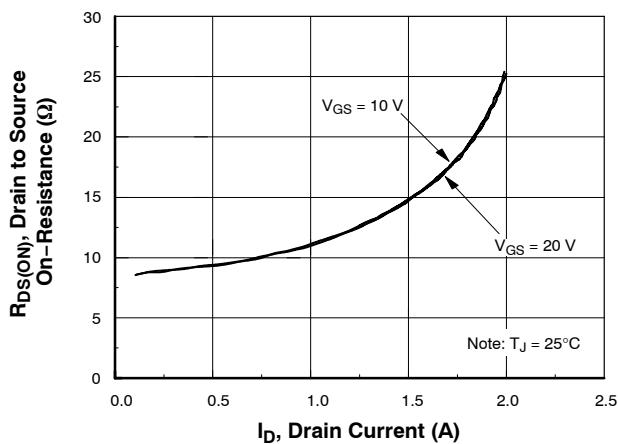


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

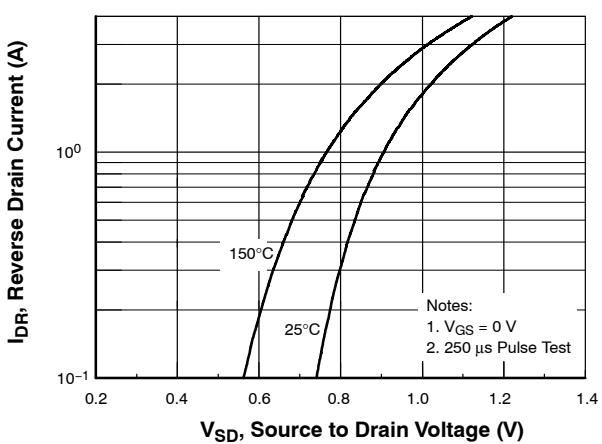


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

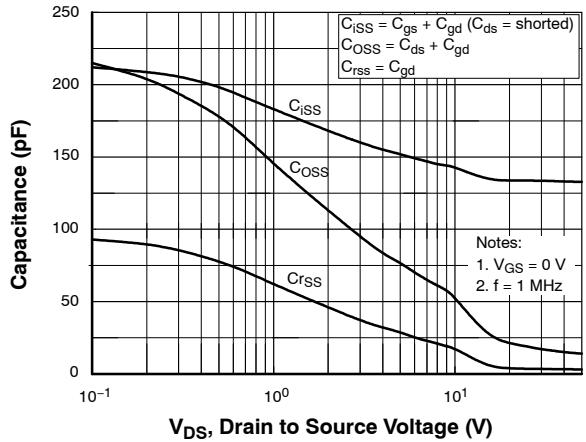


Figure 5. Capacitance Characteristics

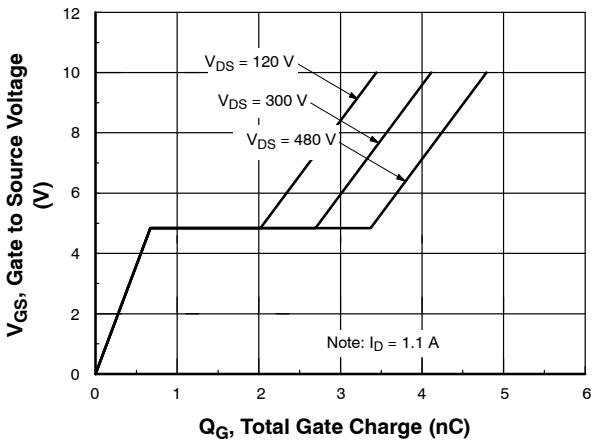
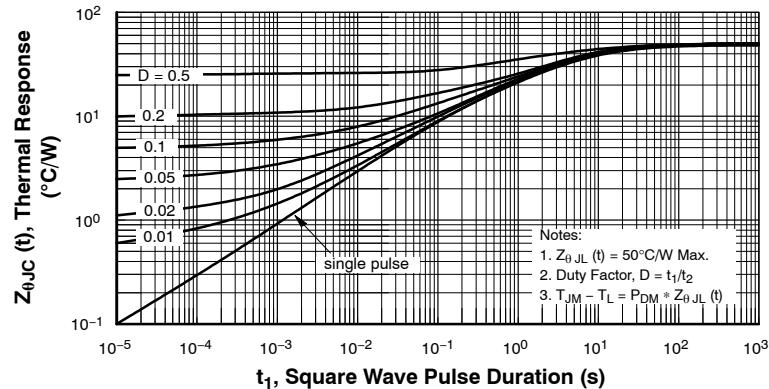
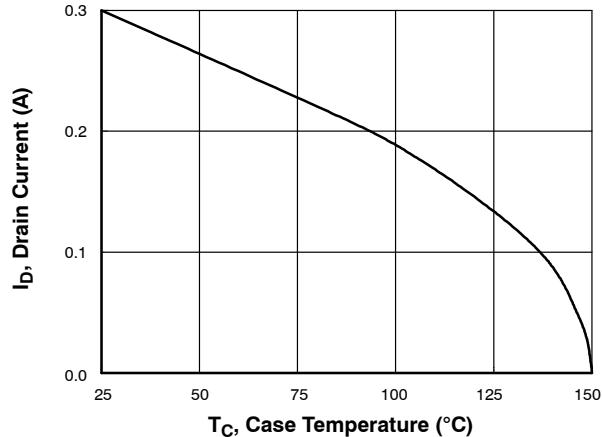
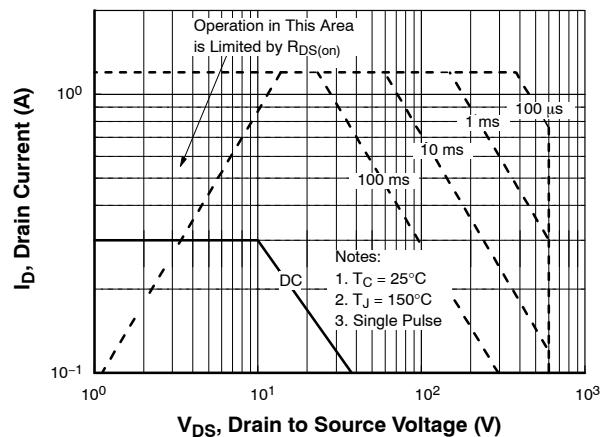
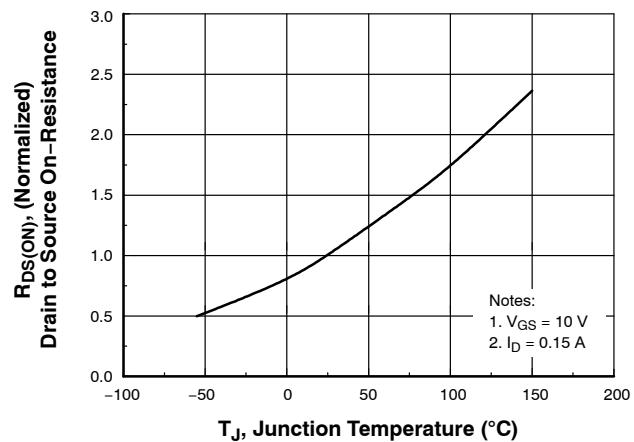
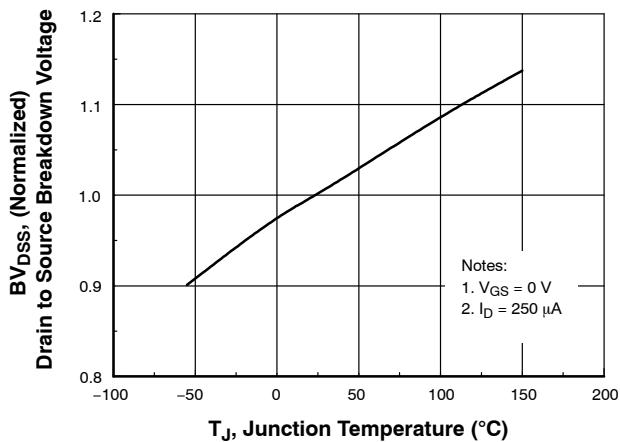


Figure 6. Gate Charge Characteristics

**TYPICAL CHARACTERISTICS (Continued)**



## FQN1N60C

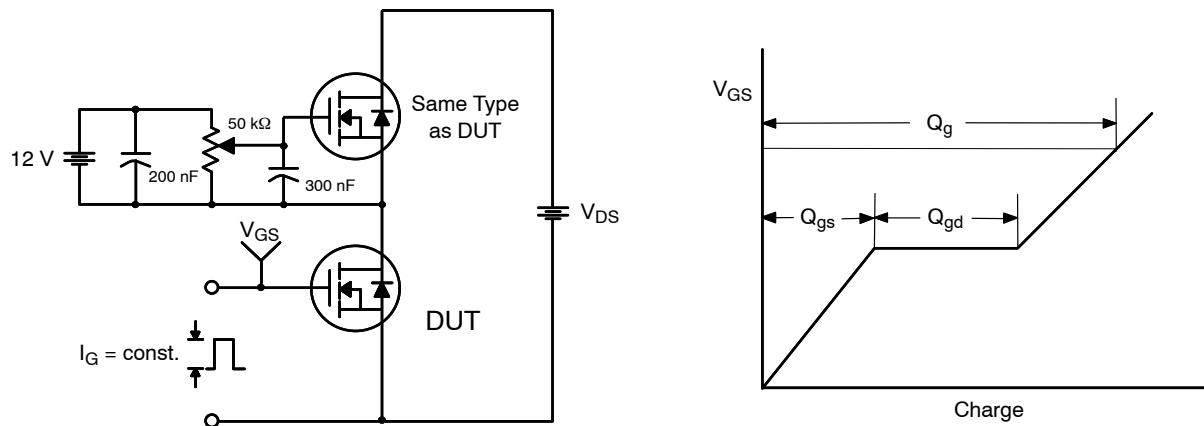


Figure 12. Gate Charge Test Circuit & Waveform

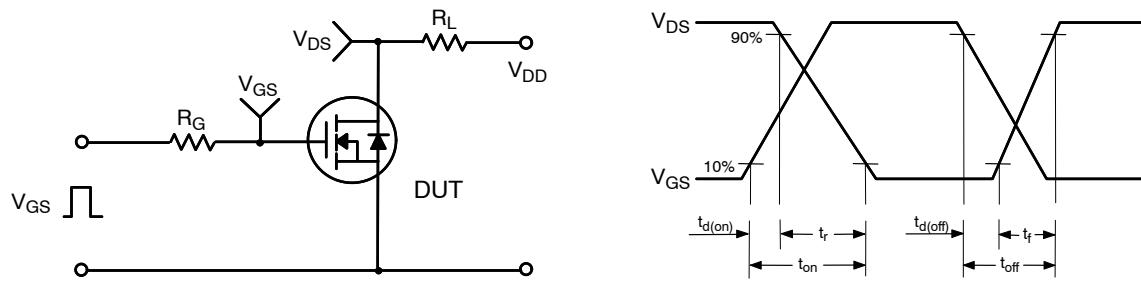


Figure 13. Resistive Switching Test Circuit & Waveforms

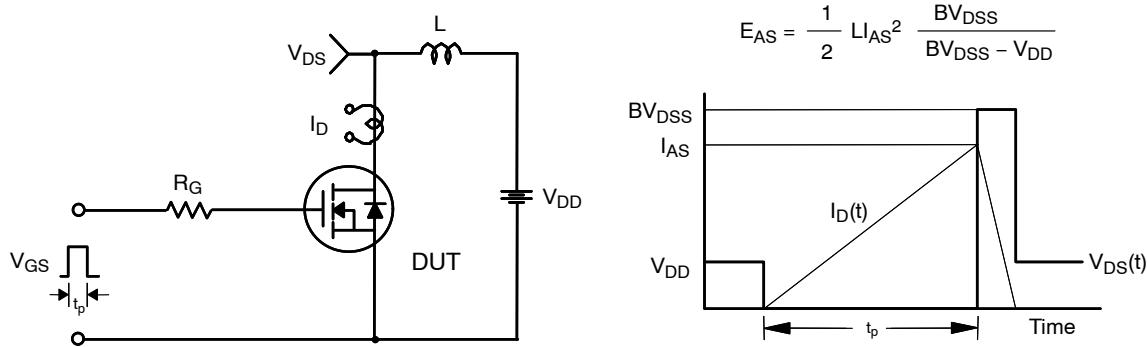


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

## FQN1N60C

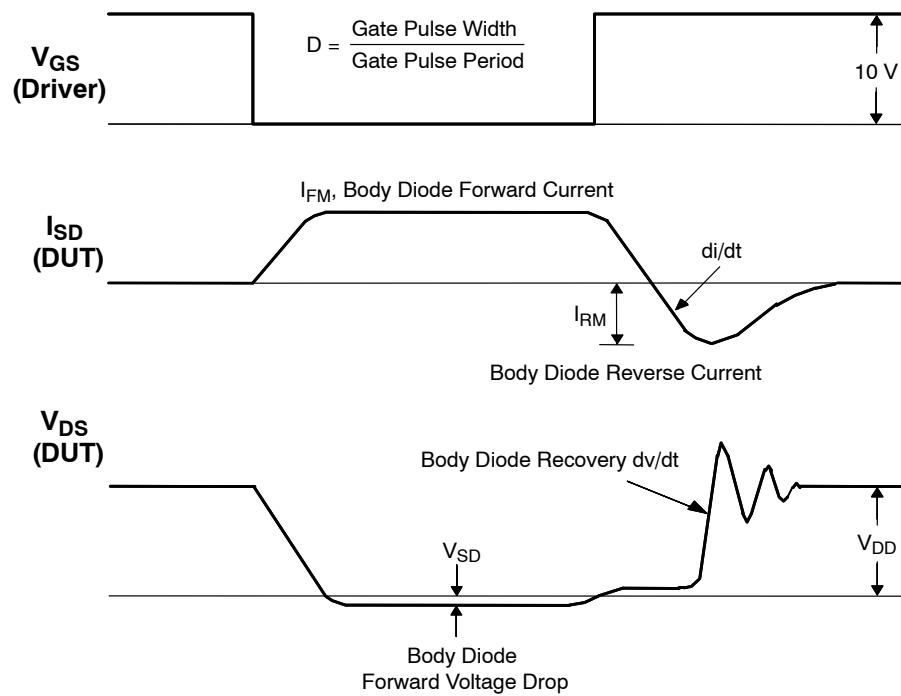
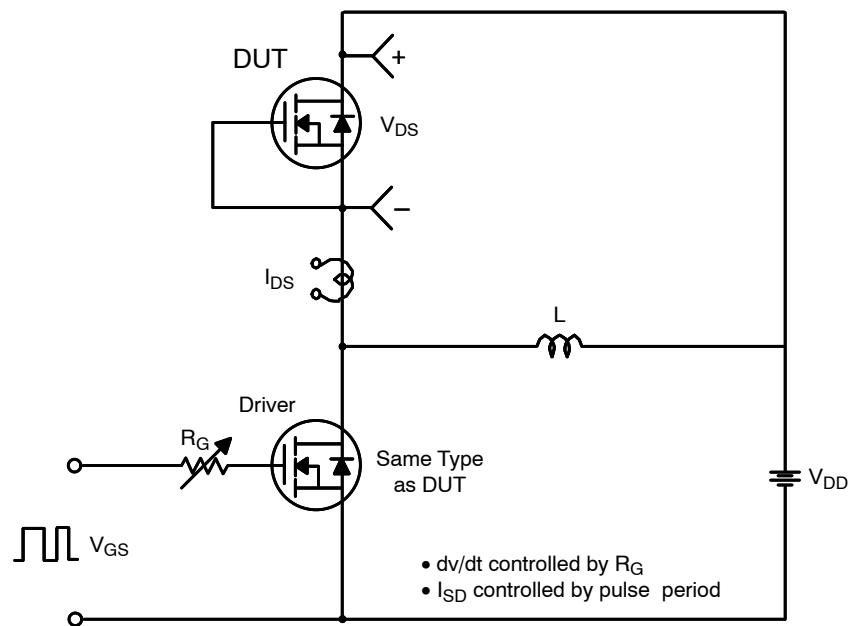
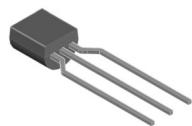
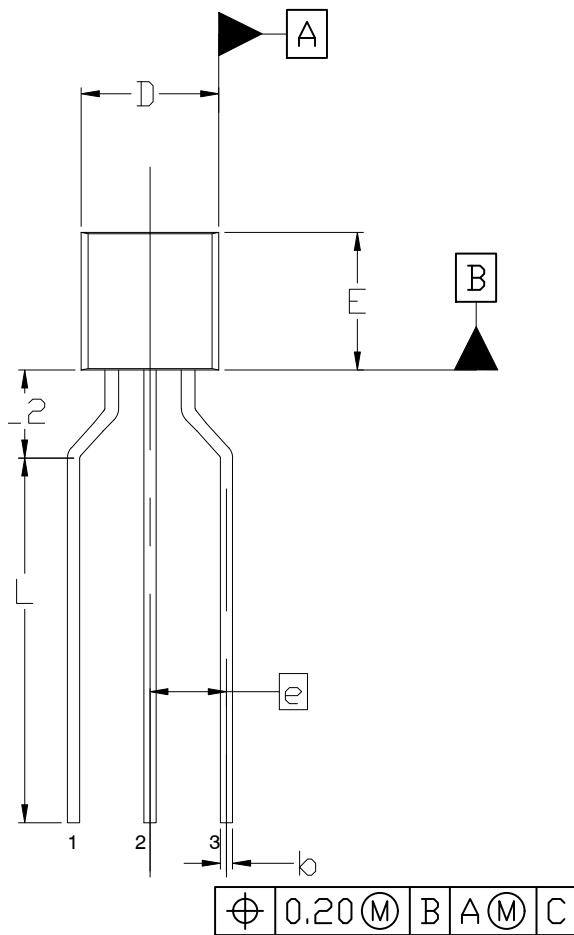


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



TO-92 3LD 4.75x4.80  
CASE 135AV  
ISSUE O

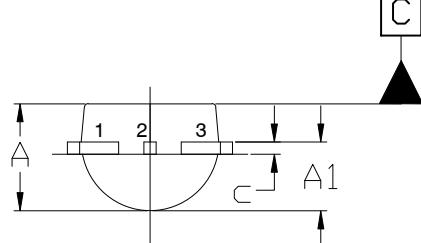
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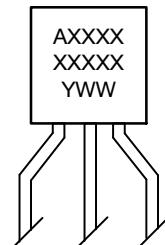
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, GATE REMAINS AND TIE BAR PROTRUSIONS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	3.05	3.60	4.19
A1	2.13	2.50	2.88
b	0.36	0.46	0.56
c	0.30	0.40	0.52
D	4.32	4.75	5.20
E	4.32	4.80	5.33
e	2.54 BSC		
L	10.50	11.75	13.00
L2	2.54	---	3.44



GENERIC  
MARKING DIAGRAM\*



XXXXX = Specific Device Code

A = Assembly Location

Y = Year

WW = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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