



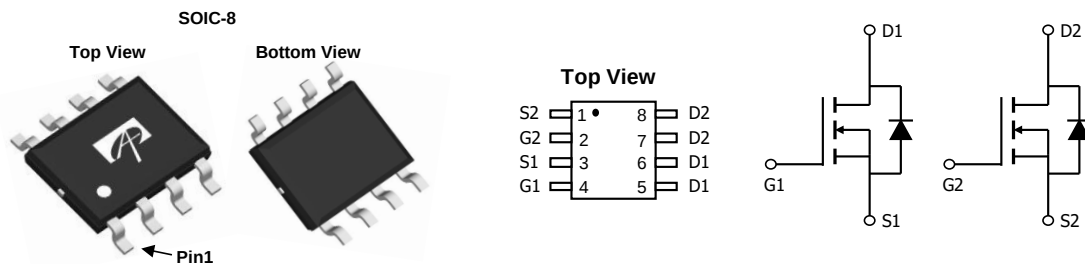
General Description

The AO4884 uses advanced trench technology to provide excellent $R_{DS(ON)}$ with low gate charge. This is an all purpose device that is suitable for use in a wide range of power conversion applications.

Product Summary

V_{DS}	40V
I_D (at $V_{GS}=10V$)	10A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 13m Ω
$R_{DS(ON)}$ (at $V_{GS} = 4.5V$)	< 16m Ω

100% UIS Tested
100% R_g Tested



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	10	A
		8	
Pulsed Drain Current ^C	I_{DM}	50	
Avalanche Current ^C	I_{AS}, I_{AR}	35	A
Avalanche energy $L=0.1\text{mH}$ ^C	E_{AS}, E_{AR}	61	mJ
Power Dissipation ^B	P_D	2	W
		1.3	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	48	62.5	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A D}		74	90	$^\circ\text{C/W}$
Maximum Junction-to-Lead	$R_{\theta JL}$	32	40	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	40			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =40V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.55	2.2	2.7	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	50			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =10A T _J =125°C		11 16.5	13 20	mΩ
		V _{GS} =4.5V, I _D =10A		12.7	16	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =10A		50		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current				2.5	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =20V, f=1MHz	1200	1500	1950	pF
C _{oss}	Output Capacitance		150	215	280	pF
C _{rss}	Reverse Transfer Capacitance		80	135	190	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	1.7	3.5	5.3	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =20V, I _D =10A	22	27.2	33	nC
Q _{g(4.5V)}	Total Gate Charge		10	13.6	16	nC
Q _{gs}	Gate Source Charge		3.6	4.5	5.4	nC
Q _{gd}	Gate Drain Charge		3.8	6.4	9	nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =20V, R _L =2Ω, R _{GEN} =3Ω		6.4		ns
t _r	Turn-On Rise Time			17.2		ns
t _{D(off)}	Turn-Off DelayTime			29.6		ns
t _f	Turn-Off Fall Time			16.8		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =10A, dI/dt=500A/μs	9	13	17	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =10A, dI/dt=500A/μs	25	35	45	nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150°C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

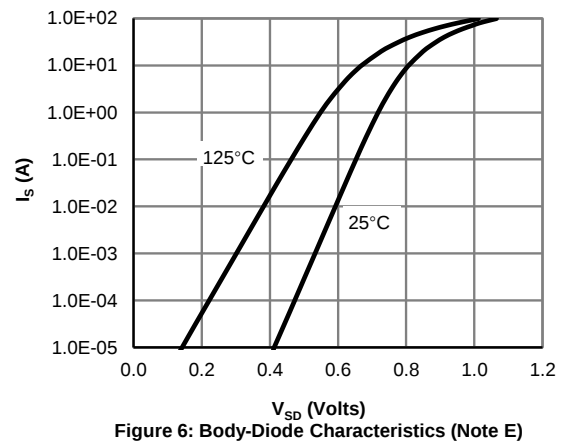
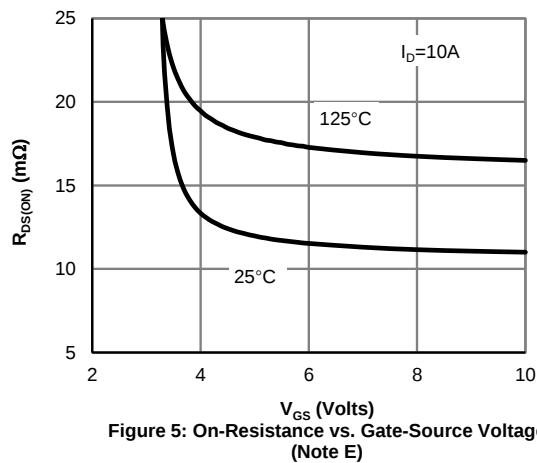
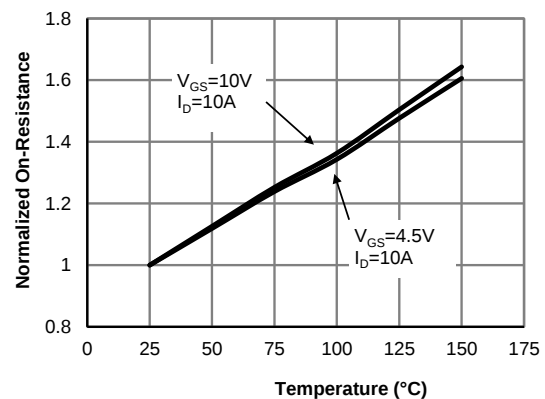
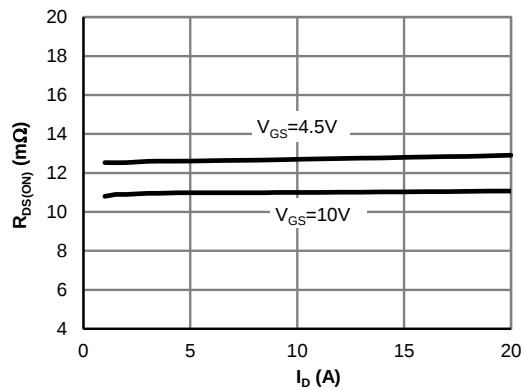
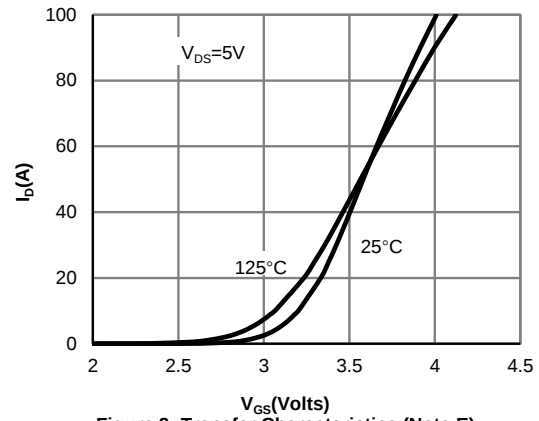
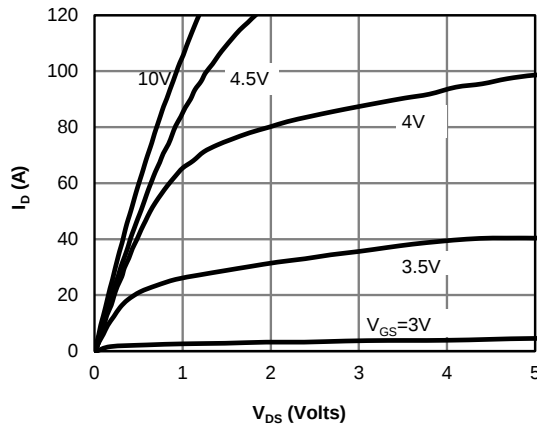
F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150°C. The SOA curve provides a single pulse rating.

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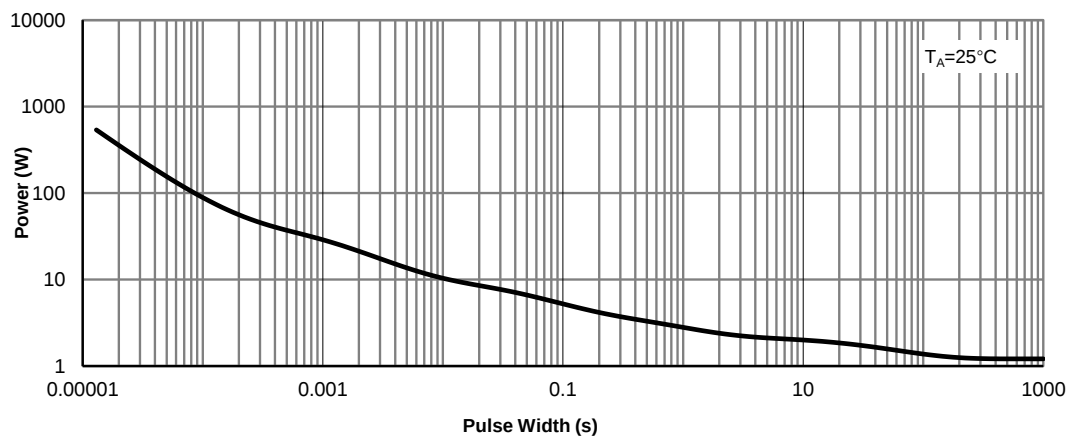
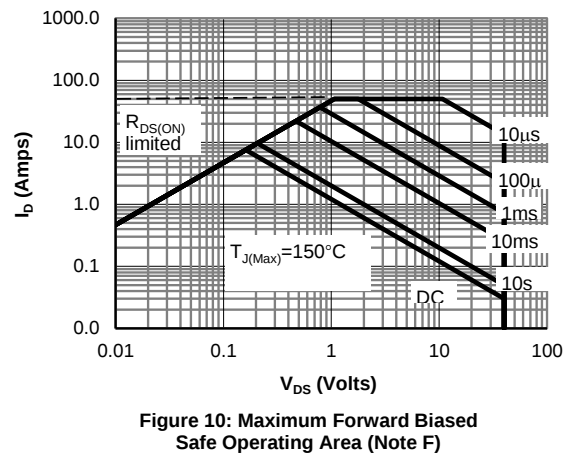
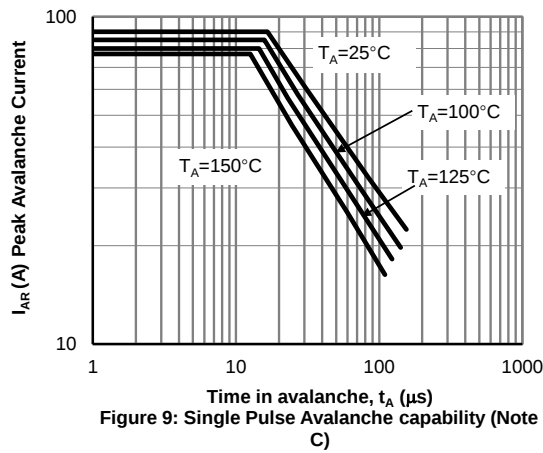
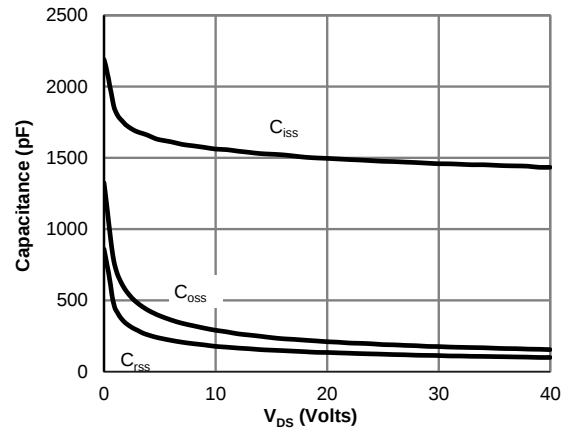
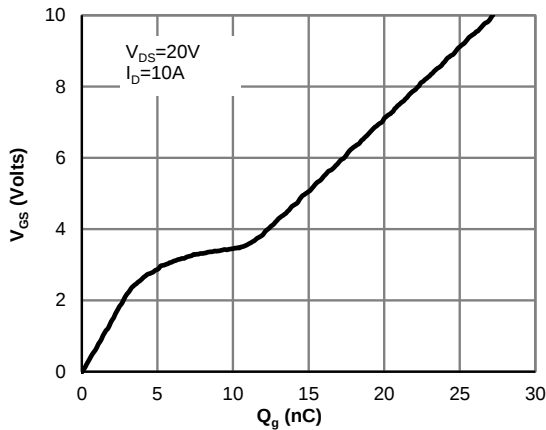
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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



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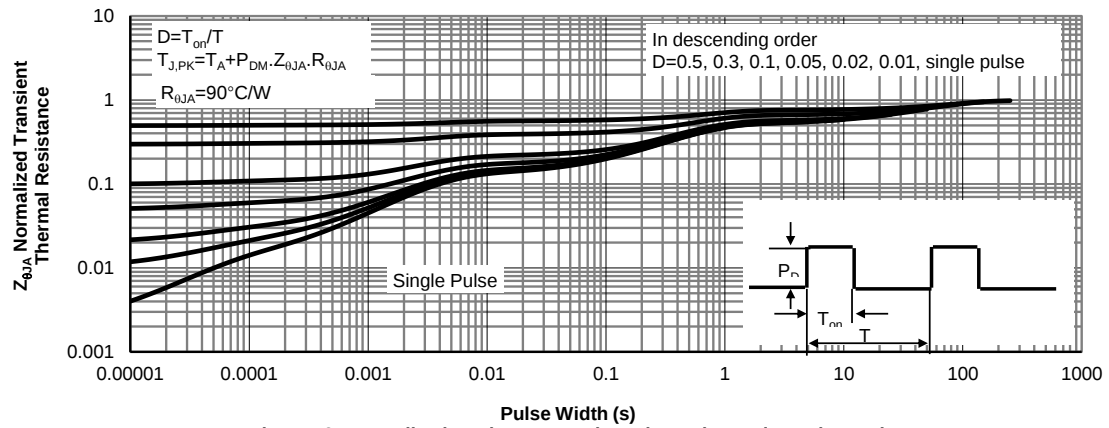
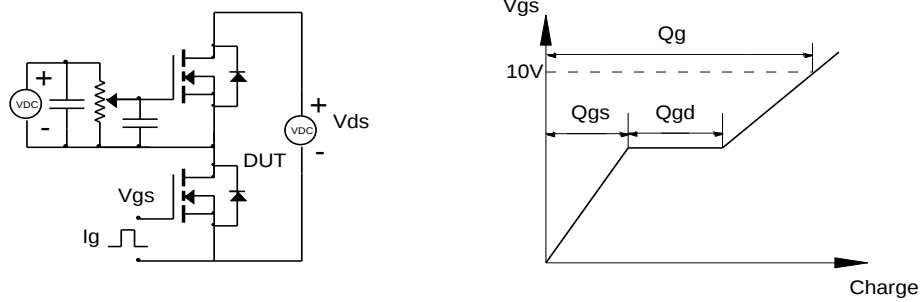
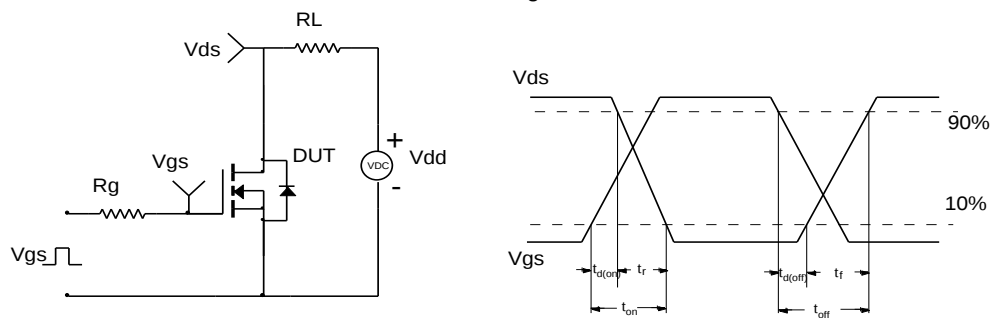


Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)

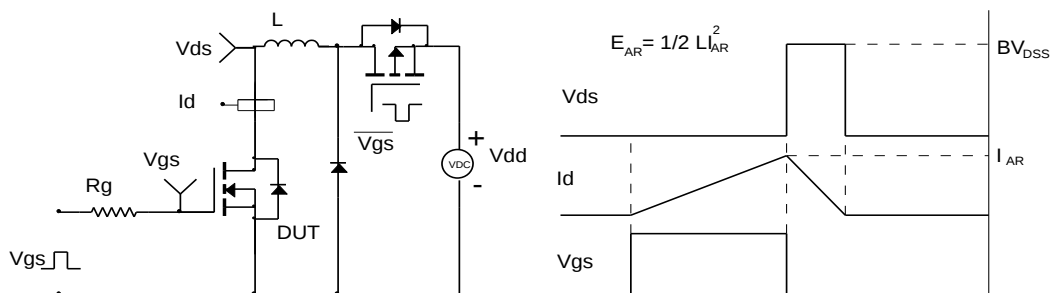
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

