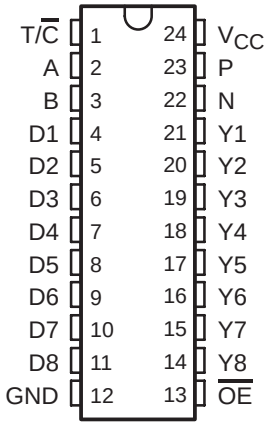
- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 15 ns at 5 V
- Schmitt-Trigger Inputs Allow for Slow Input Rise/Fall Time
- Polarity Control for Y Outputs Selects True or Complementary Logic
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} Supports Partial-Power-Down Mode Operation
- Supports Mixed-Mode Voltage Operation on All Ports
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

NT OR PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74LV8151 is a 10-bit universal Schmitt-trigger buffer with 3-state outputs, designed for 2-V to 5.5-V V_{CC} operation. The logic control (T/$\overline{C}$) pin allows the user to configure Y1 to Y8 as noninverting or inverting outputs. When T/$\overline{C}$ is high, the Y outputs are noninverted (true logic), and when T/$\overline{C}$ is low, the Y outputs are inverted (complementary logic).

When output-enable ($\overline{OE}$) input is low, the device passes data from Dn to Yn. When $\overline{OE}$ is high, the Y outputs are in the high-impedance state. The path A to P is a simple Schmitt-trigger buffer, and the path B to N is a simple Schmitt-trigger inverter.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP − NT	Tube	SN74LV8151NT	SN74LV8151NT
	TSSOP − PW	Tube	SN74LV8151PW	LV8151
		Tape and reel	SN74LV8151PWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

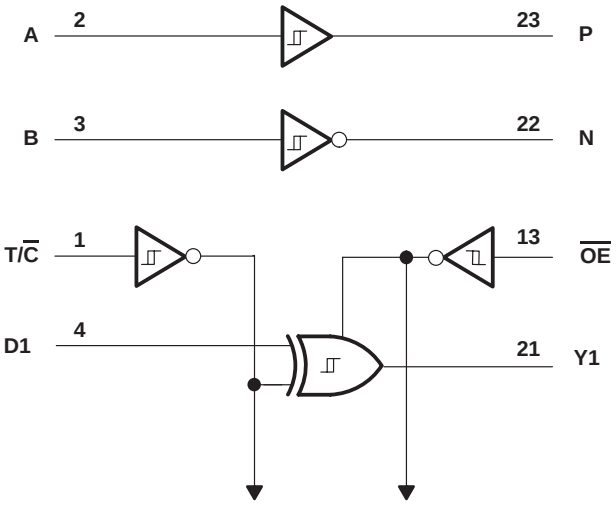
FUNCTION TABLES

INPUT A	OUTPUT P
L	L
H	H

INPUT B	OUTPUT N
L	H
H	L

INPUTS			OUTPUT Y
$\overline{OE}$	T/$\overline{C}$	D	
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	H
H	X	X	Z

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	−0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0)	−20 mA
Output clamp current, I_{OK} (V_O < 0)	−50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 3): NT package	67°C/W
(see Note 4): PW package	88°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-3.
4. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 5)

			V_{CC}	MIN	MAX	UNIT
V_{CC}	Supply voltage			2	5.5	V
V_{IH}	High-level input voltage		2 V	1.5		V
			2.3 V to 2.7 V	$V_{CC} \times 0.7$		
			3 V to 3.6 V	$V_{CC} \times 0.7$		
			4.5 V to 5.5 V	$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage		2 V		0.5	V
			2.3 V to 2.7 V		$V_{CC} \times 0.3$	
			3 V to 3.6 V		$V_{CC} \times 0.3$	
			4.5 V to 5.5 V		$V_{CC} \times 0.3$	
V_I	Input voltage			0	5.5	V
V_O	Output voltage	High or low state		0	V_{CC}	V
		3-state		0	5.5	
I_{OH}	High-level output current		2 V		−50	μA
			2.3 V to 2.7 V		−2	mA
			3 V to 3.6 V		−6	
			4.5 V to 5.5 V		−12	
I_{OL}	Low-level output current		2 V		50	μA
			2.3 V to 2.7 V		2	mA
			3 V to 3.6 V		6	
			4.5 V to 5.5 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	T/$\overline{C}$, $\overline{OE}$ inputs	2.3 V to 2.7 V		200	ns/V
			3 V to 3.6 V		100	
			4.5 V to 5.5 V		20	
		A, B, D inputs	2.3 V to 2.7 V		4	ms/V
			3 V to 3.6 V		3	
			4.5 V to 5.5 V		2	
T_A	Operating free-air temperature			−40	85	°C

NOTES: 5. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{T+} Positive-going input threshold voltage	A, B, and D inputs	2.5 V			1.75	V
		3.3 V			2.31	
		5 V			3.5	
V_{T-} Negative-going input threshold voltage	A, B, and D inputs	2.5 V	0.75			V
		3.3 V	0.99			
		5 V	1.5			
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)	A, B, and D inputs	2.5 V	0.25		1	V
		3.3 V	0.33		1.32	
		5 V	0.5		2	
V_{OH}	I_{OH} = −50 µA	2 V to 5.5 V	V_{CC} − 0.1			V
	I_{OH} = −2 mA	2.3 V	2			
	I_{OH} = −6 mA	3 V	2.48			
	I_{OH} = −12 mA	4.5 V	3.8			
V_{OL}	I_{OL} = 50 µA	2 V to 5.5 V			0.1	V
	I_{OL} = 2 mA	2.3 V			0.4	
	I_{OL} = 6 mA	3 V			0.44	
	I_{OL} = 12 mA	4.5 V			0.55	
I_I	V_I = 5.5 V or GND	0 to 5.5 V			±1	µA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±5	µA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			20	µA
I_{off}	V_I or V_O = 0 to 5.5 V	0			5	µA
C_i	$V_I = V_{CC}$ or GND	3.3 V		3		pF
		5 V		3		
C_o	$V_O = V_{CC}$ or GND	3.3 V		5		pF
		5 V		5		

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C TYP	MIN	MAX	UNIT
t_{pd}	A or B	P or N	C_L = 15 pF	22	1	45	ns
	D	Y		23	1	49	
	T/$\overline{C}$			24	1	50	
t_{en}	$\overline{OE}$	Y		12	1	25	ns
t_{dis}	$\overline{OE}$	Y		11	1	20	ns
t_{pd}	A or B	P or N	C_L = 50 pF	26	1	52	ns
	D	Y		28	1	57	
	T/$\overline{C}$			29	1	58	
t_{en}	$\overline{OE}$	Y		15	1	30	ns
t_{dis}	$\overline{OE}$	Y		15	1	26	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C TYP	MIN	MAX	UNIT
t_{pd}	A or B	P or N	C_L = 15 pF	14	1	26	ns
	D	Y		15	1	29	
	$\overline{T/C}$			16	1	30	
t_{en}	$\overline{OE}$	Y		9	1	16	ns
t_{dis}	$\overline{OE}$	Y		8	1	14	ns
t_{pd}	A or B	P or N	C_L = 50 pF	17	1	32	ns
	D	Y		18	1	34	
	$\overline{T/C}$			20	1	36	
t_{en}	$\overline{OE}$	Y		11	1	20	ns
t_{dis}	$\overline{OE}$	Y		11	1	18	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C TYP	MIN	MAX	UNIT
t_{pd}	A or B	P or N	C_L = 15 pF	9	1	15	ns
	D	Y		10	1	16	
	$\overline{T/C}$			11	1	17	
t_{en}	$\overline{OE}$	Y		6	1	10.5	ns
t_{dis}	$\overline{OE}$	Y		6	1	10	ns
t_{pd}	A or B	P or N	C_L = 50 pF	11	1	18	ns
	D	Y		12	1	20	
	$\overline{T/C}$			13	1	21	
t_{en}	$\overline{OE}$	Y		8	1	12.5	ns
t_{dis}	$\overline{OE}$	Y		8	1	11.5	ns

noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF (see Note 6)

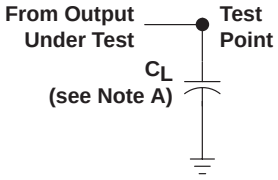
PARAMETER		T_A = 25°C MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.6		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.6		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 6: Characteristics are for surface-mount packages only.

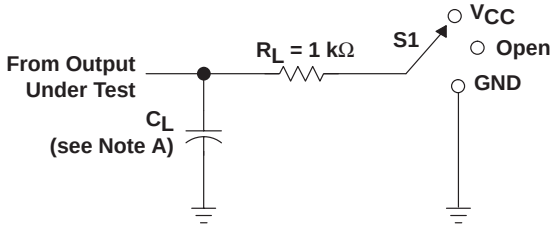
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = No load, f = 1 MHz	3.3 V	15	pF
			5 V	16	

PARAMETER MEASUREMENT INFORMATION

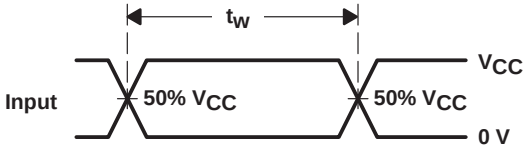


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

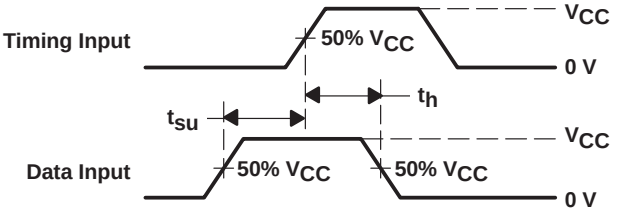


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

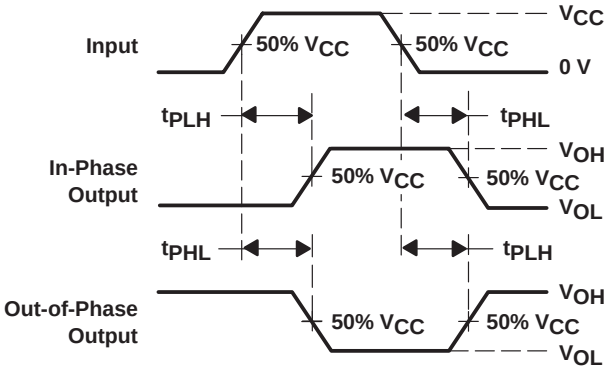
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



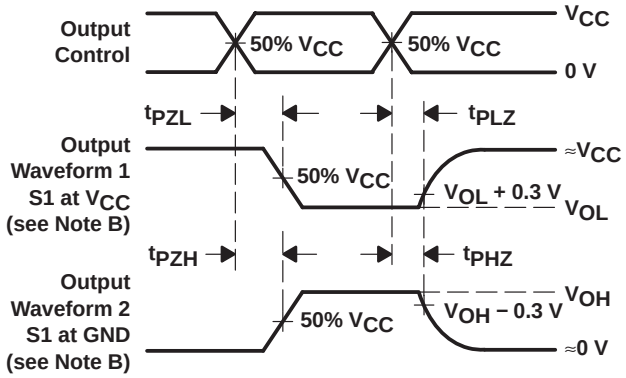
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV8151DGVR	ACTIVE	TVSOP	DGV	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV8151	Samples
SN74LV8151DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	-40 to 85	LV8151	
SN74LV8151DWR	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV8151	Samples
SN74LV8151PW	OBSOLETE	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85	LV8151	
SN74LV8151PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV8151	Samples
SN74LV8151PWRE4	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV8151	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

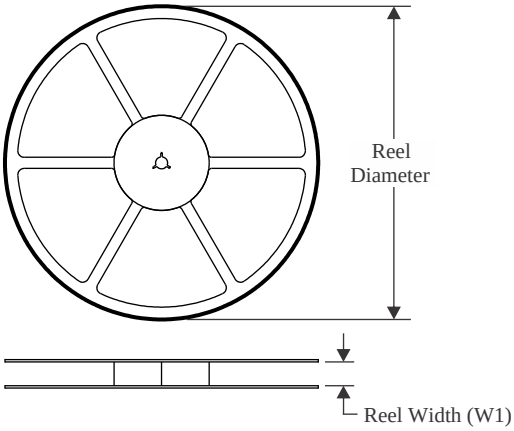
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

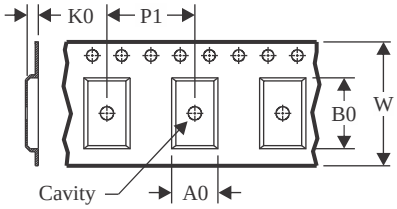
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

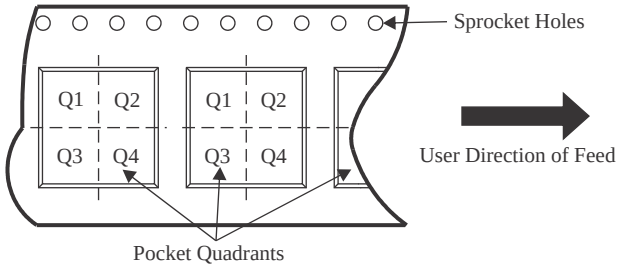


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

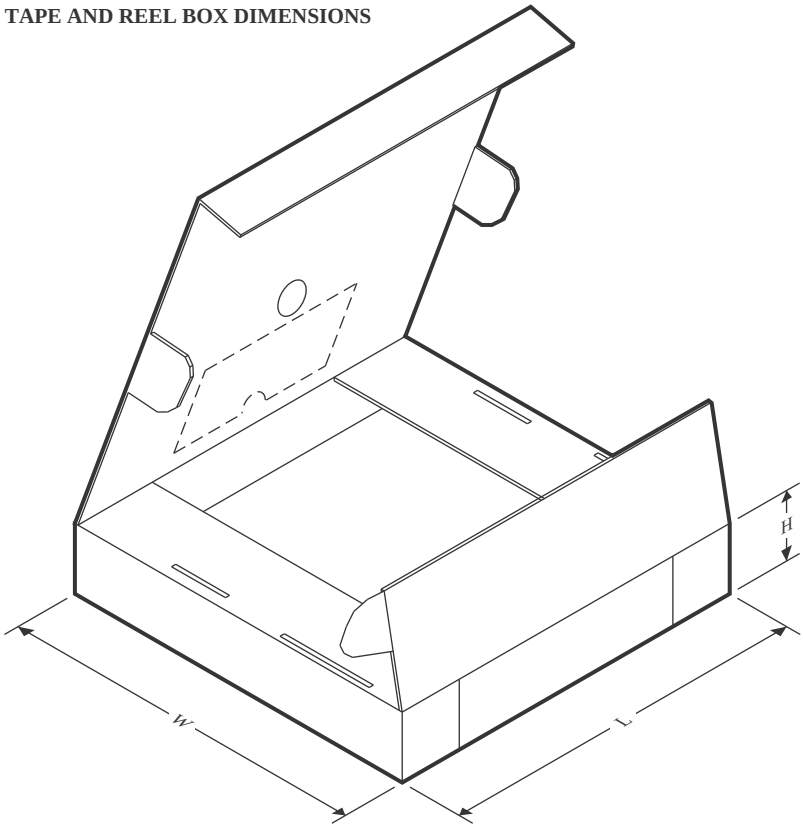
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV8151DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV8151DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LV8151PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



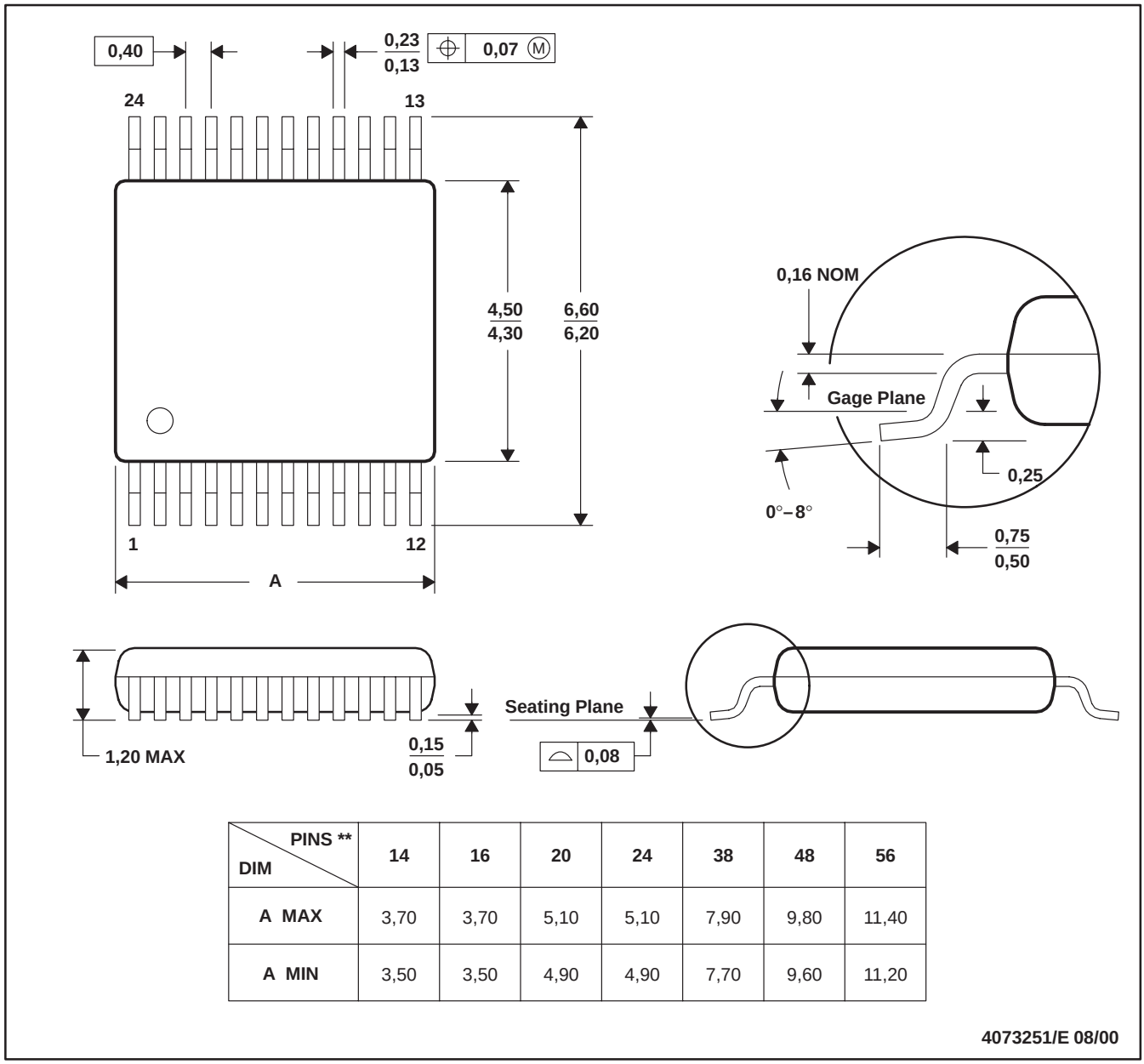
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV8151DGVR	TVSOP	DGV	24	2000	356.0	356.0	35.0
SN74LV8151DWR	SOIC	DW	24	2000	350.0	350.0	43.0
SN74LV8151PWR	TSSOP	PW	24	2000	356.0	356.0	35.0

MPDS006C – FEBRUARY 1996 – REVISED AUGUST 2000

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

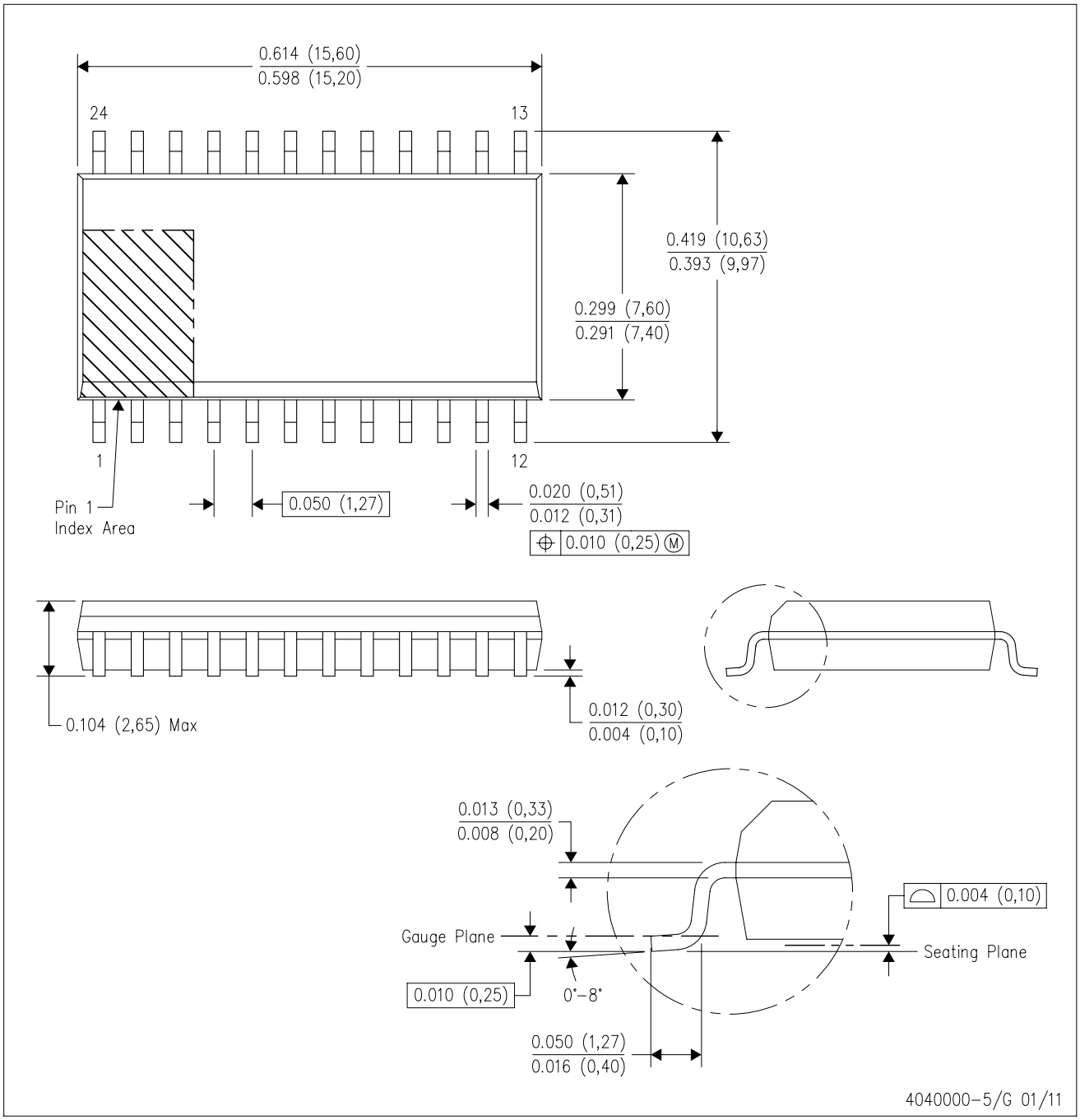


DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



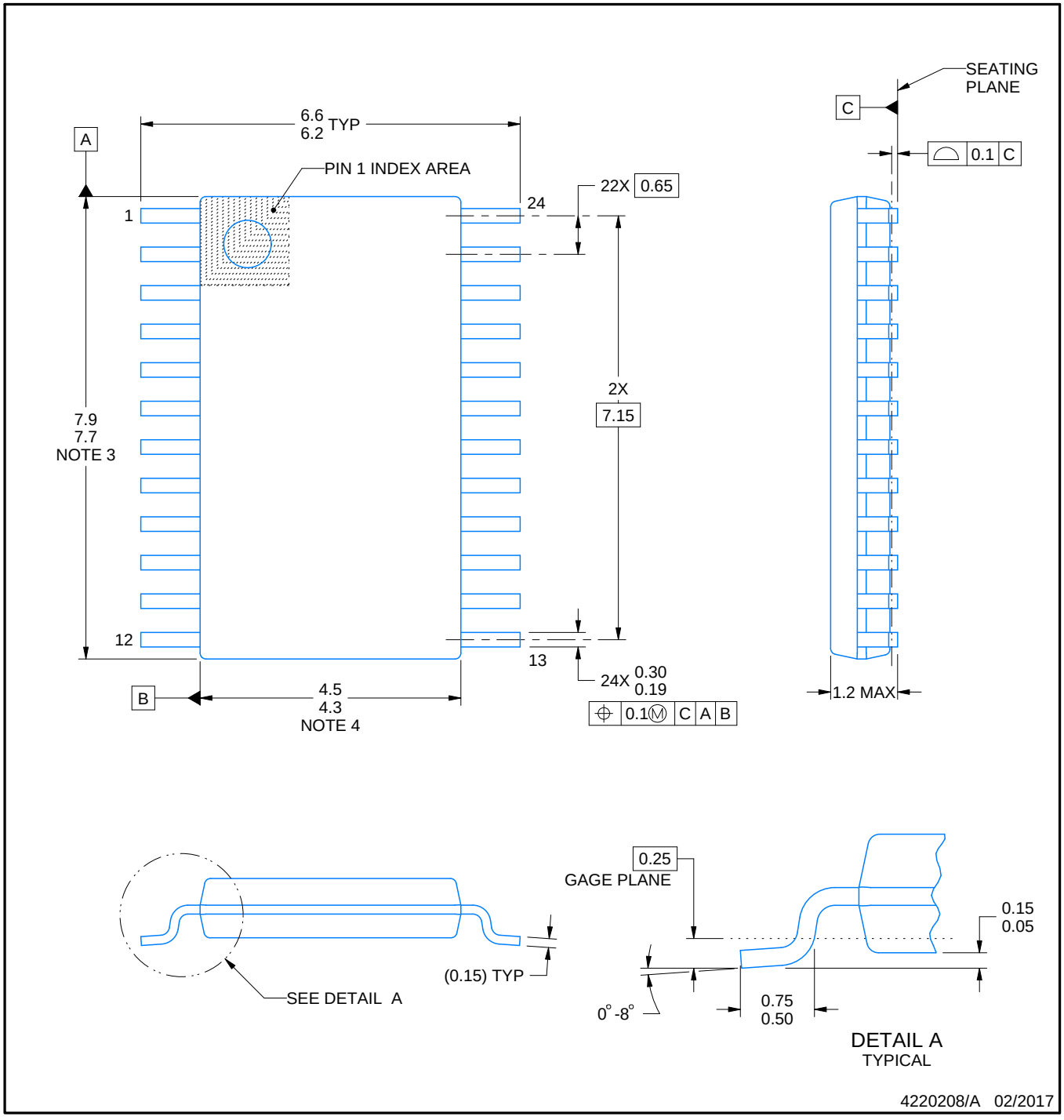
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

PACKAGE OUTLINE

PW0024A

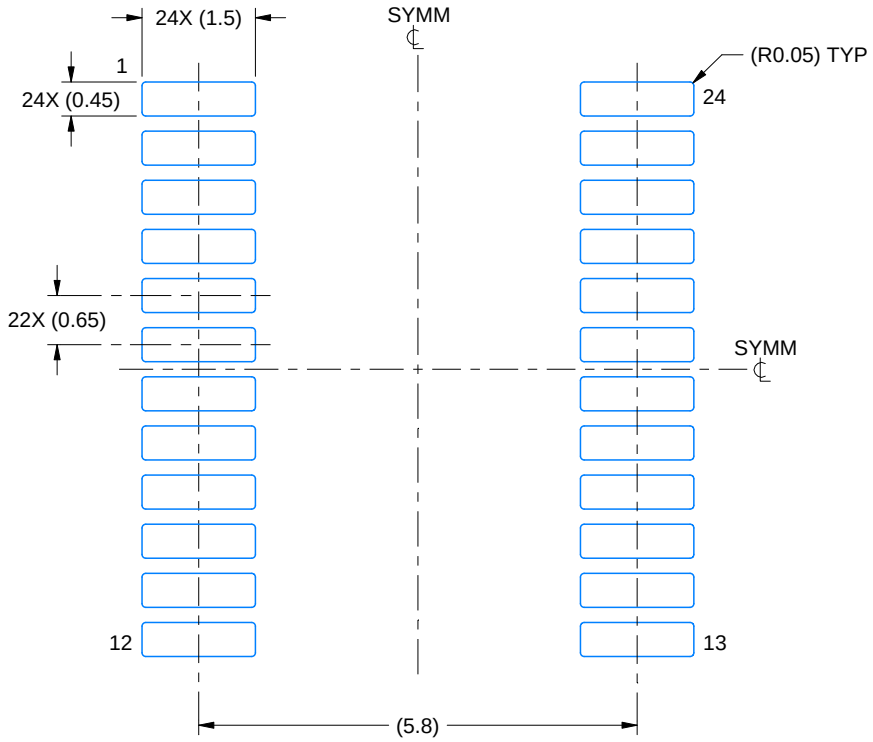
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

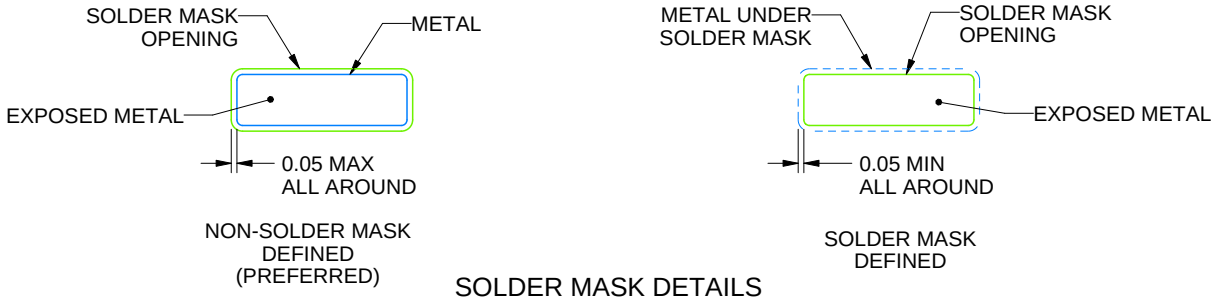


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

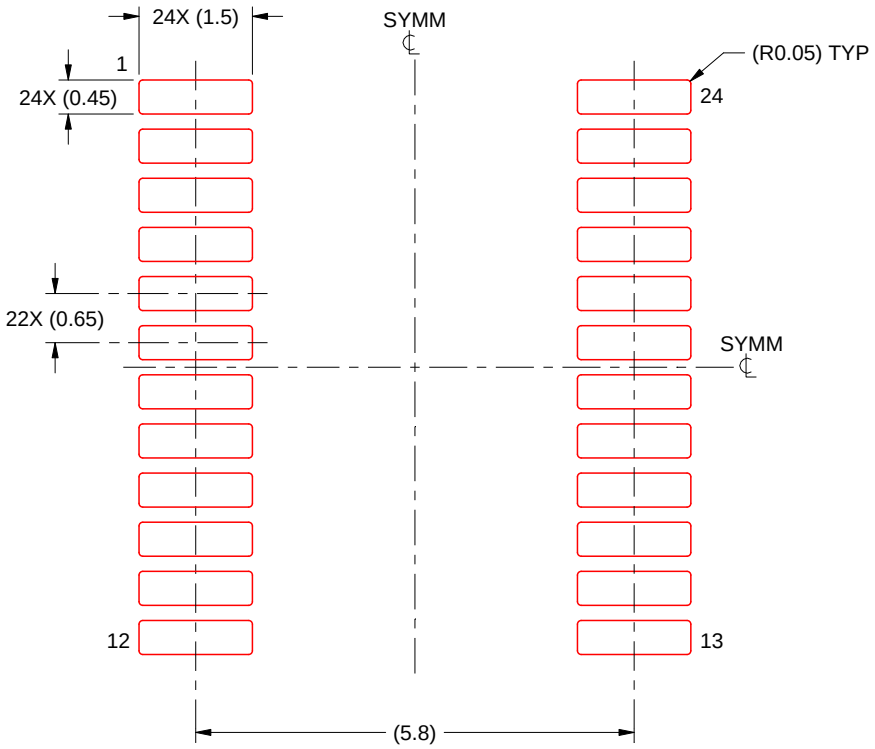


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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