QP SEMICONDUCTOR
an e2v company

QP7025 High-Speed 8K x 16 Dual-Port Static RAM

General Description

The QP7025 is a CMOS Fast 8K x 16 Dual-Port Static RAM (SRAM). QP Semiconductor designed the QP7025 to be a direct replacement for the IDT7025. It is designed to be used as a stand-alone 128K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 32-bit or larger (wider) word systems. Applications requiring a 32-bit or wider memory system can use the MASTER/SLAVE Dual-Port RAM approach to achieve full-speed, error free operation without additional discrete logic.

The QP7025 supports asynchronous access for reads or writes to any location in memory via two independent ports with separate control, address, and I/O pins that function identically to the IDT7025 that it replaces. The QP7025 has an automatic power down feature controlled by the appropriate Chip Enable (CE) pin that puts each port in a very low standby power mode.

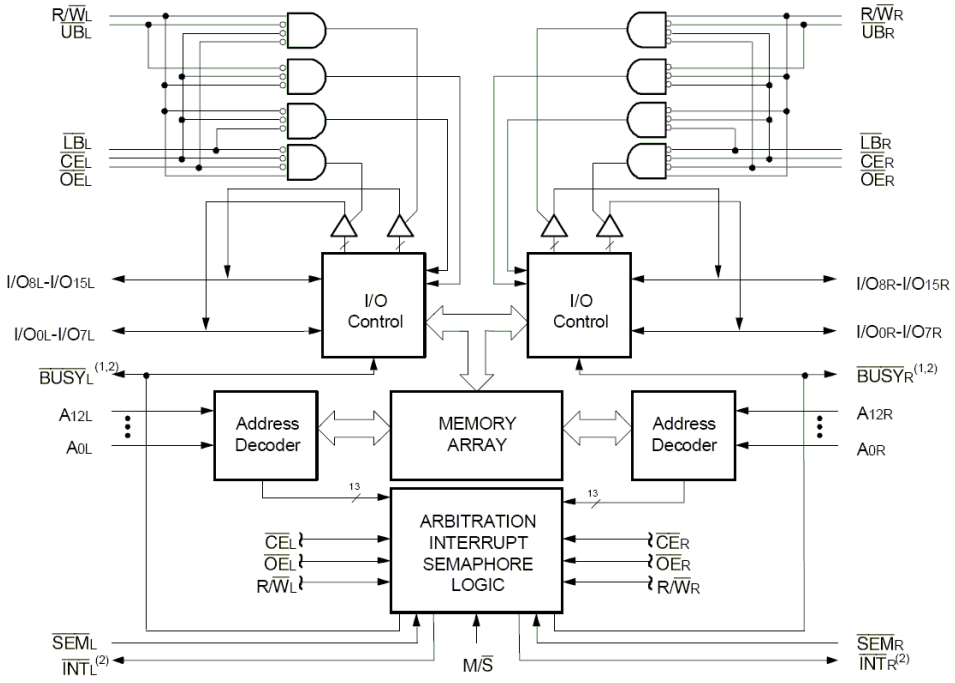
The QP7025 utilizes CMOS high-performance technology which allows the devices to typically operate on only 750mW of power. Low-power (L) versions offer battery backup data retention capability with typical power consumption of 10µW from a 2V source.

The QP7025 is available in a hermetic ceramic 84-pin PGA and a ceramic 84-pin Flatpack. Military grade product is manufactured in compliance with the latest revision of MIL-PRF-38535 QML, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

Features

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - Military: 35/45/55/70ns
  - Industrial: 20/25ns
- Low-power operation
  - QP7025S
    - Active: 750mW (typ.)
    - Standby: 0.2mW (typ.)
  - QP7025L
    - Active: 750mW (typ.)
    - Standby: 0.2mW (typ.)
- Separate upper-byte and lower-byte control for multiplexed bus compatibility
- Expands data bus width to 32 bits or more using the Master/Slave select when cascading more than one device
  - M/S = H for BUSY output flag on Master
  - M/S = L for BUSY input on Slave
  - Interrupt Flag
  - On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible, single 5V (±10%) power supply
- Packages: 84-pin PGA & 84-pin Flatpack
- Industrial temperature range (–40°C to +85°C) is available

Block Diagram



Notes:

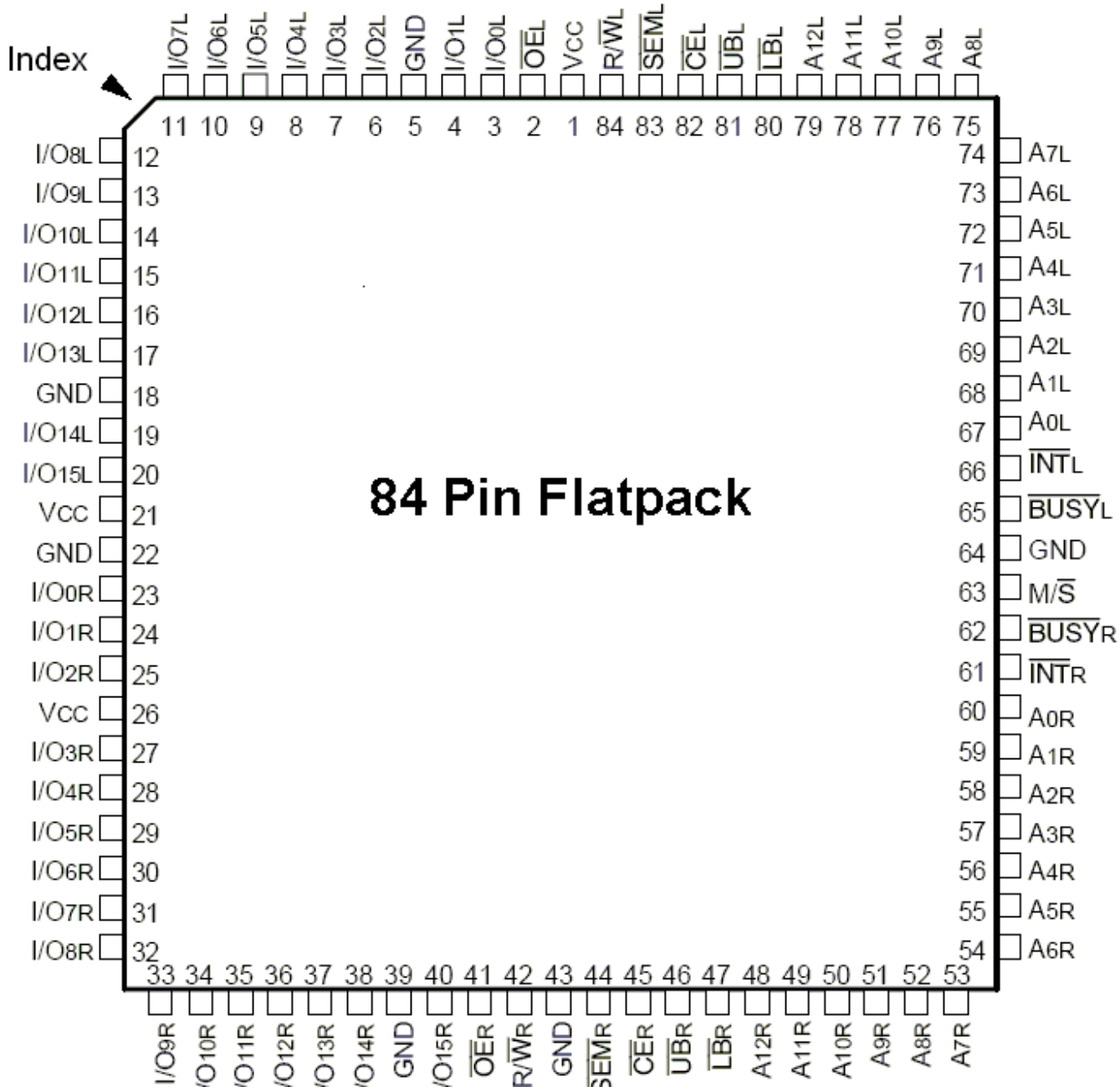
(Master): $\overline{BUSY}$ is output; (Slave): $\overline{BUSY}$ is input.

Outputs and $\overline{INT}$ outputs are non-tri-stated push-pull.

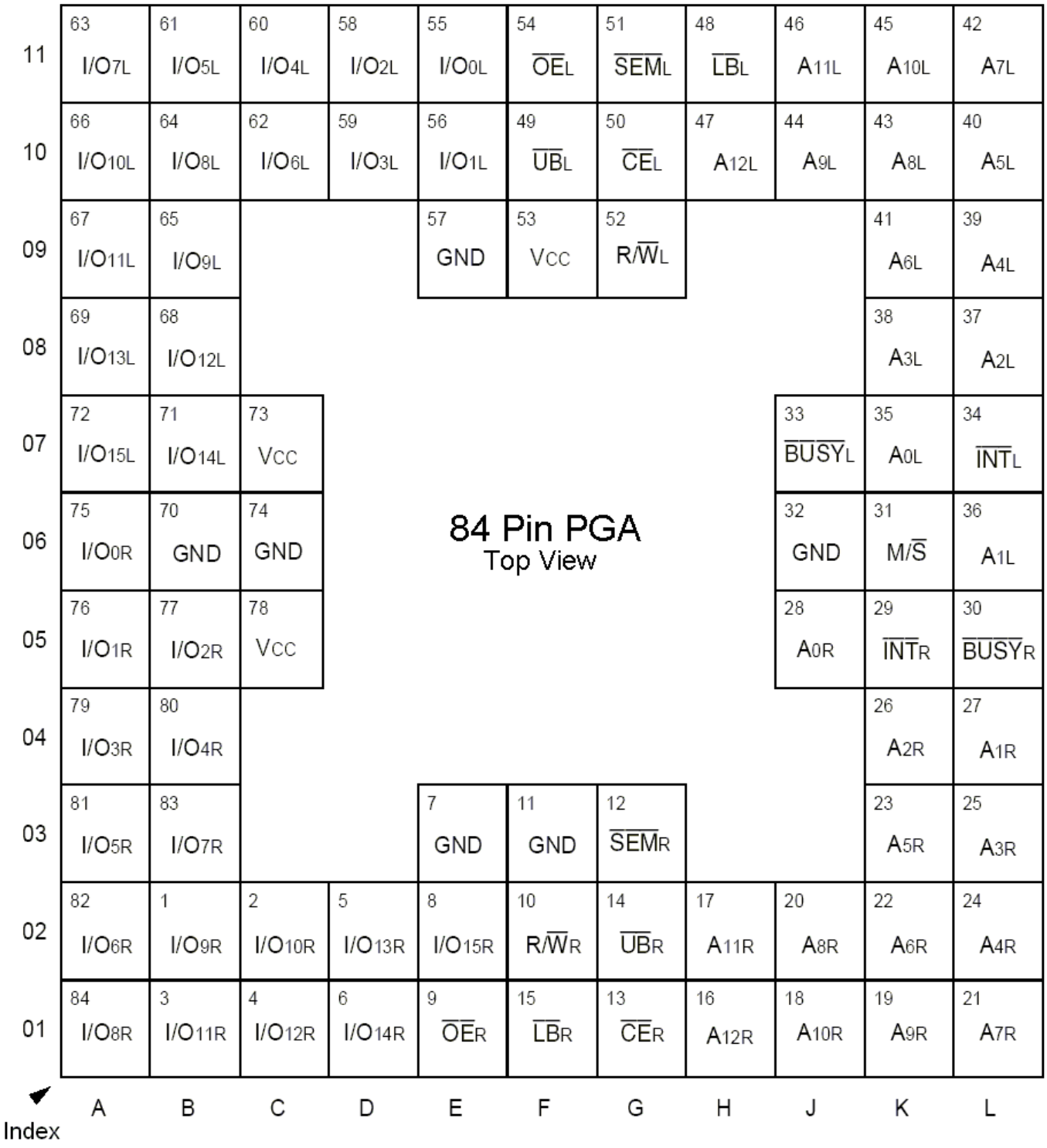
Functional Description

Left Port	Right Port	Functional Description
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} – A_{12L}$	$A_{0R} – A_{12R}$	Address
$I/O_{0L} – I/O_{15L}$	$I/O_{0R} – I/O_{15R}$	Data Input/Output
SEM_L	SEM_R	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master Slave Select
V_{CC}		Power- All V_{CC} pins must be connected to a power supply
GND		Ground- All GND pins must be connected to a good ground

Connection Diagrams



Connection Diagrams



Absolute Maximum Ratings /1

Condition	Rating	Units
Power Supply and Input Voltage	-0.5 to +7.0	Volts DC
Storage Temperature Range	-65 to +150	°C
Output Current	50	mA
Maximum Power Dissipation (P_D)	2.2	W
Lead Temperature (soldering, 10 seconds)	+260	ºC
Junction Temperature (T_J)	+150	ºC
DC Input and Output Voltage Range	-0.5 to V_{CC} +0.5	Volts DC
Output Voltage Applied in High Z State	-0.5 to V_{CC} +0.5	Volts DC

/1Stresses above the AMR may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.All voltages referenced to GND, unless otherwise specified.

Recommended Operating Conditions /1

Condition	Rating	Units	Notes
Supply Voltage Range (V_{CC})	4.5 to 5.5	Volts DC	
High-Level Input Voltage (V_{IH})	2.2 to 6.0	Volts DC	
Low-Level Input Voltage (V_{IL})	-0.5 to +0.8	Volts DC	
Case Operating Range (T_c)	-55C to +125	ºC	

/1Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

ELECTRICAL PERFORMANCE CHARACTERISTICS-DC

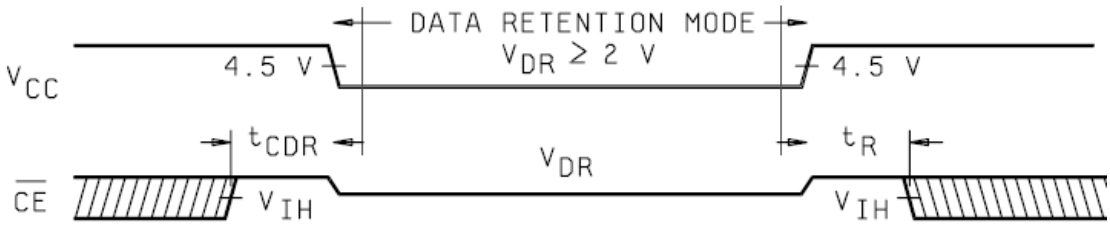
Test	Symbol	Conditions $-55^{o}C \le T_A \le +125^{o}C$ $4.5\ V \le V_{CC} \le 5.5\ V$ Unless Otherwise Specified	Min	Typ	Max	Unit
Output Low Voltage	V_{OL}	V_{CC} = 4.5V, I_{OL}= 4mA, V_{IH} = 2.2V, V_{IL}= 0.8V			0.4	V
Output High Voltage	V_{OH}	V_{CC}= 4.5V, I_{OH}= -4mA, V_{IH}= 2.2V, V_{IL}=0.8V	2.4			V
Input Leakage Current	I_{LI}	V_{CC}= 5.5V V_{IN}= GND to V_{CC}			5	µA
Output Leakage Current	I_{LO}	V_{CC}= 5.5V, $\overline{CE}$ =V_{IH}, V_{IN} = GND to V_{CC}			5	µA
Dynamic Operating Current (both ports active)	I_{CC1}	Outputs Open, V_{CC} = 5.5V, f= f_{max} /1, $\overline{SEM} \ge$VIH, $\overline{CE} \le V_{IL}$		150	250	mA
Standby Supply Current (both ports) TTL Inputs	I_{CC2}	$\overline{SEM}_R = \overline{SEM}_L \ge V_{IH}$, $\overline{CE}_R = \overline{CE}_L \ge V_{IH}$, V_{CC} = 5.5V, f= f_{max} /1		8	25	mA
Standby Supply Current (one port) TTL Inputs	I_{CC3}	Active ports outputs open $\overline{SEM}_R = \overline{SEM}_L \ge V_{IH}$, $\overline{CE}_R = \overline{CE}_L \ge V_{IH}$, Opposite Port = V_{IL}, V_{CC} = 5.5V, f= f_{max} \1		85	160	mA
Full Standby Supply Current (both ports) CMOS Inputs	I_{CC4}	$\overline{SEM}_R = \overline{SEM}_L \ge V_{cc} - 0.2V$, both ports $\overline{CE}_R = \overline{CE}_L \ge V_{cc} - 0.2V$, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{cc} - 0.2V$, V_{cc} = 5.5V, f= 0 \2		0.04	5	mA
Full Standby Supply Current (one port) CMOS Inputs	I_{CC5}	Active ports outputs open $\overline{SEM}_R = \overline{SEM}_L \ge V_{cc} - 0.2\ V$, one port $\overline{CE}_R = \overline{CE}_L \ge V_{cc} - 0.2V$, opposite port < 0.2 V $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{cc} - 0.2\ V$, V_{CC} = 5.5V, f= f_{max} \1		80	150	mA
Input Capacitance	C_{IN}	V_{IN} = 0 V, V_{CC} = 5.0V, f = 1MHz, T_A = 25°C /3			11	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V, V_{CC} = 5.0 V, f = 1MHz, T_A = 25°C /3			11	pF

1/ At f_{MAX}, address and data inputs (excluding OE) are cycling at the maximum frequency of read cycle of $1/t_{AVAV}$, and using AC test conditions of input levels of GND to 3.0 V.
2/ f = 0 Hz means no address or control lines change
3/ Measured at initial qualification only

ELECTRICAL PERFORMANCE CHARACTERISTICS-Data Retention						
Test	**Symbol**	**Conditions** **Conditions** **-55ºC ≤T_A≤+125ºC** **4.5 V ≤ Vcc ≤ 5.5 V** **Unless Otherwise Specified**	**Min**	**Typ**	**Max**	**Unit**
Data Retention Voltage ("L" Series Devices Only)	V_{DR}	$\overline{CE}$ ≥ V_{CC}– 0.2V, V_{CC} = 2.0 V V_{IN} ≥ V_{CC}– 0.2V or ≤ 0.2 V	2.0			V
Data Retention Current ("L" Series Devices Only)	I_{CCDR}	$\overline{CE}$ ≥ V_{CC}– 0.2V, V_{CC} = 2.0 V V_{IN} ≥ V_{CC}– 0.2V or ≤ 0.2 V		5	1000	µA
Chip Deselect to Data Retention Time /4 ("L" Series Devices Only)	t_{CDR}	$\overline{CE}$ ≥ V_{CC} – 0.2V, Vcc = 2.0V V_{IN} ≥ Vcc – 0.2V or ≤ 0.2V /5 See output test load figures	0			ns
Operation Recovery Time /4 ("L" Series Devices Only)	t_R	$\overline{CE}$ ≥ V_{CC} – 0.2V, Vcc = 2.0V V_{IN} ≥ Vcc – 0.2V or ≤ 0.2V /5 See output test load figures	t_{AVAV}			ns

/4 Parameter tested at initial characterization and after design change. Parameter guaranteed per limits in table.
/5 Measurement assumption: transition times ≤ 5 ns, input levels from GND to 3.0 V, timing ref levels of 1.5 V and output load per AC Output Test Load Type I shown herein.

Data Retention Mode Timing



ELECTRICAL PERFORMANCE CHARACTERISTICS- Read Cycle

Description	Symbol	Conditions $-55^{o}C \leq T_A \leq +125^{o}C$ $4.5\ V \leq Vcc \leq 5.5\ V$ Unless Otherwise Specified	Min	Max	Unit
Read Cycle Time /6	t_{AVAV}	S or L 70		70	ns
		S or L 55		55	
		S or L 45		45	
		S or L 35		35	
Address Access Time /6	t_{AVQV}	S or L 70		70	ns
		S or L 55		55	
		S or L 45		45	
		S or L 35		35	
Semaphore Flag Update Pulse $\overline{SEM}$ or $\overline{OE}$	t_{SOP}	ALL		15	ns
Chip Enable Access time /7	t_{ELQV}	S or L 70		70	ns
		S or L 55		55	
		S or L 45		45	
		S or L 35		35	
Byte Enable Access time /7	t_{ABE}	S or L 70		70	ns
		S or L 55		55	
		S or L 45		45	
		S or L 35		35	
Chip Enable to Pwr Up /6, /8	t_{ELPU}	ALL	0		ns
Chip Disable to Pwr Down /6, /8	t_{EHPD}	ALL		50	ns
Output Enable Access Time /7	t_{OLQV}	ALL		20	ns
Output Hold from Addr Change	t_{AVQX}	ALL	3		ns
Output- Low Z	t_{OLQX}	ALL	3		ns
Output- High Z	t_{OLQZ}	S or L 70		30	ns
		S or L 55		25	
		S or L 45		20	
		S or L 35		15	

/6 Measurement assumption: transition times ≤ 5 ns, input levels from GND to 3.0 V, timing ref levels of 1.5 V and output load per AC Output Test Load Type I shown herein.

/7 To access RAM: $\overline{CE}$ = L, $\overline{SEM}$ = H, $\overline{UB}$ or $\overline{LB}$ = L

/8 Parameter tested at initial characterization and after design change. Parameter guaranteed per limits in table.

ELECTRICAL PERFORMANCE CHARACTERISTICS- Write Cycle

Description	Symbol	Conditions $-55^oC \le T_A \le +125^oC$ $4.5\ V \le Vcc \le 5.5\ V$ Unless Otherwise Specified	Min	Max	Unit
Write Cycle	t_{AVAV}	S or L 70	70		ns
		S or L 55	55		
		S or L 45	45		
		S or L 35	35		
Chip Enable to End-of-Write /9 /12	t_{ELWH}	S or L 70	50		ns
		S or L 55	45		
		S or L 45	40		
		S or L 35	30		
Address valid to End of Write /12	t_{AVWH}	S or L 70	50		ns
		S or L 55	45		
		S or L 45	40		
		S or L 35	30		
Address Set-up /9, /12	t_{AVWL}	ALL	0		ns
Write Pulse /12	t_{WLWH}	S or L 70	50		ns
		S or L 55	40		
		S or L 45	35		
		S or L 35	30		
Write Recovery /12	t_{WHAX}	ALL	0		ns
Data Valid to End of Write /12	t_{DVWH}	S or L 70	40		ns
		S or L 55	30		
		S or L 45	25		
		S or L 35	25		
Output High Z	t_{WLQZ}	S or L 70		30	ns
		S or L 55		25	
		S or L 45		20	
		S or L 35		15	
Data Hold Time /10, /12	t_{WHDX}	ALL	0		ns
Write Enable to Output (in High Z) /11	t_{WLQZ}	S or L 70		30	ns
		S or L 55		25	
		S or L 45		20	
		S or L 35		15	
Output Active from End of Write /10	t_{WHQX}	ALL	0		ns
$\overline{SEM}$ Flag- Write to Read Time /12	t_{SWRD}	ALL	10		ns
$\overline{SEM}$ Flag Contention Window /12	t_{SPS}	ALL	10		ns

/9 To access RAM: $\overline{CE}$ = H, $\overline{SEM}$ = H, $\overline{UB}$ or $\overline{LB}$ = L To access Semaphore: $\overline{CE}$ = h, $\overline{SEM}$ = H, $\overline{UB}$ or $\overline{LB}$ = L. Either condition must be valid for the entire $t_{EL:WH}$ time.

/10 $t_{WHDX} < t_{WHQX}$

/11 Transition measured at steady-state high level -500mV or steady-state low level +500mV on the output from the 1.5 V level on the input; CL = 5 pF (ref AC Output Test Load Type II shown herein).

/12 Measurement assumption: transition times ≤ 5 ns, input levels from GND to 3.0 V, timing ref levels of 1.5 V and output load per AC Output Test Load Type I shown herein.

ELECTRICAL PERFORMANCE CHARACTERISTICS- $\overline{\text{BUSY}}$ Timing

Description	Symbol	Conditions $-55^{o}C \leq T_A \leq +125^{o}C$ $4.5\ V \leq Vcc \leq 5.5\ V$ Unless Otherwise Specified M/$\overline{S}$ = V_{IH} /12	Min	Max	Unit
$\overline{\text{BUSY}}$ Access Time from Address Match	t_{BAA}	S or L 70		45	ns
		S or L 55		45	ns
		S or L 45		35	ns
		S or L 35		35	ns
$\overline{\text{BUSY}}$ Disable Time from Address Not Matched	t_{BDA}	S or L 70		40	ns
		S or L 55		40	ns
		S or L 45		30	ns
		S or L 35		30	ns
$\overline{\text{BUSY}}$ Access Time from Chip Enable Low	T_{BAC}	S or L 70		40	ns
		S or L 55		40	ns
		S or L 45		30	ns
		S or L 35		30	ns
$\overline{\text{BUSY}}$ Disable Time from Chip Enable High	T_{BDC}	S or L 70		35	ns
		S or L 55		35	ns
		S or L 45		25	ns
		S or L 35		25	ns
Arbitration priority Set-up Time	T_{APS}	ALL	5		ns
$\overline{\text{BUSY}}$ Disable to Chip Enable High	T_{BDD}	ALL		35	ns
Write Hold after $\overline{\text{BUSY}}$	t_{WH}	ALL	25		ns

/12 Measurement assumption: transition times ≤ 5 ns, input levels from GND to 3.0 V, timing ref levels of 1.5 V and output load per AC Output Test Load Type I shown herein.

ELECTRICAL PERFORMANCE CHARACTERISTICS- $\overline{\text{BUSY}}$ Timing

Description	Symbol	Conditions $-55^{o}C \leq T_A \leq +125^{o}C$ $4.5\ V \leq Vcc \leq 5.5\ V$ Unless Otherwise Specified M/$\overline{S}$ = V_{IL} /12	Min	Max	Unit
$\overline{\text{BUSY}}$ Input to Write	t_{WB}	ALL	0		ns
Write Hold After $\overline{\text{BUSY}}$	t_{WH}	ALL	25		ns

/12 Measurement assumption: transition times ≤ 5 ns, input levels from GND to 3.0 V, timing ref levels of 1.5 V and output load per AC Output Test Load Type I shown herein.

ELECTRICAL PERFORMANCE CHARACTERISTICS- Port-to-Port Delay Timing

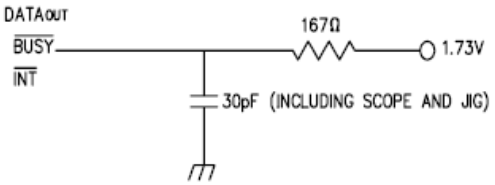
Description	Symbol	Conditions $-55^{o}C \leq T_A \leq +125^{o}C$ $4.5\ V \leq Vcc \leq 5.5\ V$ Unless Otherwise Specified	Min	Max	Unit
Write Pulse to Data Delay	t_{WDD}	S or L 70		95	ns
		S or L 55		80	
		S or L 45		70	
		S or L 35		60	
Write Data Valid to Read Data Delay	t_{DDD}	S or L 70		80	ns
		S or L 55		65	
		S or L 45		55	
		S or L 35		45	

ELECTRICAL PERFORMANCE CHARACTERISTICS- Interrupt Timing

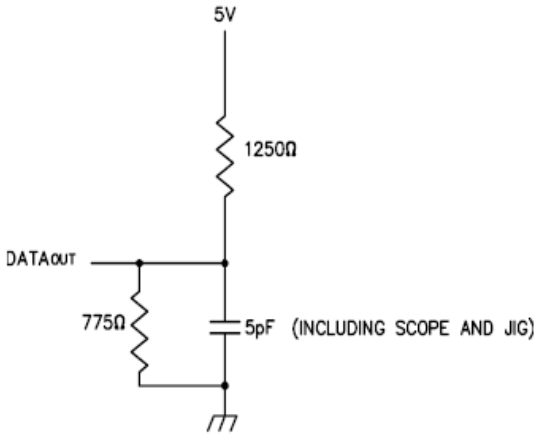
Description	Symbol	Conditions $-55^{o}C \leq T_A \leq +125^{o}C$ $4.5\ V \leq Vcc \leq 5.5\ V$ Unless Otherwise Specified	Min	Max	Unit
Address Set-up Time	t_{AS}	ALL	0		ns
Write Recovery Time	t_{WR}	ALL	0		ns
Interrupt Set Time	t_{NS}	S or L 70		50	ns
		S or L 55		40	
		S or L 45		35	
		S or L 35		30	
Interrupt Reset Time	t_{inr}	S or L 70		50	ns
		S or L 55		40	
		S or L 45		35	
		S or L 35		30	

AC Output Test Load

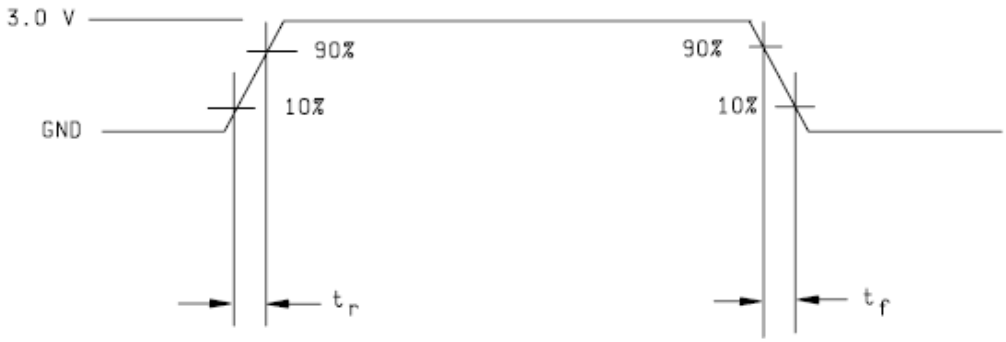
Type I



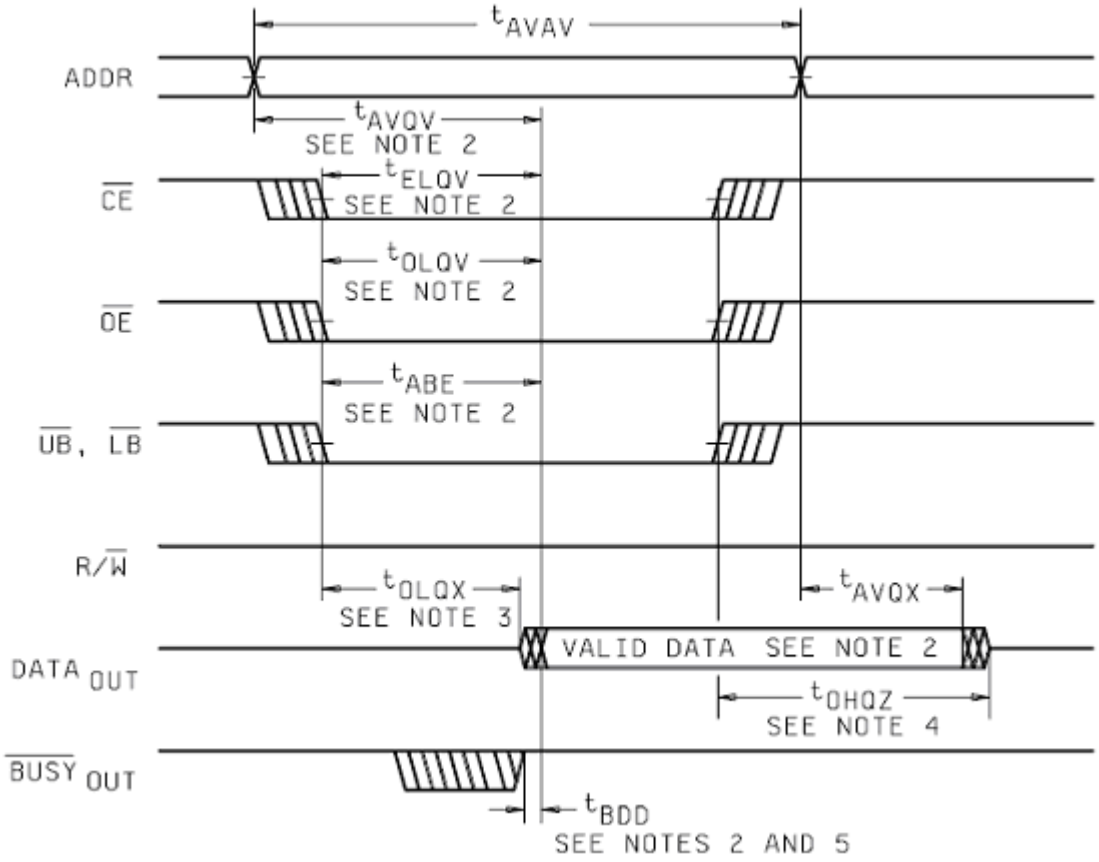
Type II
(t_{OLQX} t_{WLQZ} t_{WHQX})



AC TEST CONDITIONS	
Input Pulse levels	GND to 3.0 V
Input rise & fall times (t_r & t_f)	≤ 5ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V



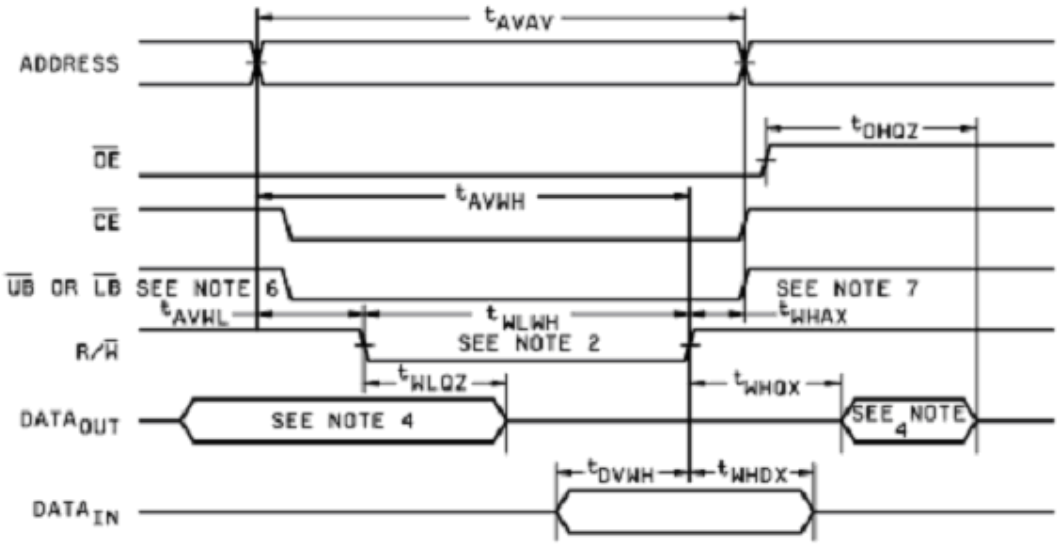
Read Cycle Timing



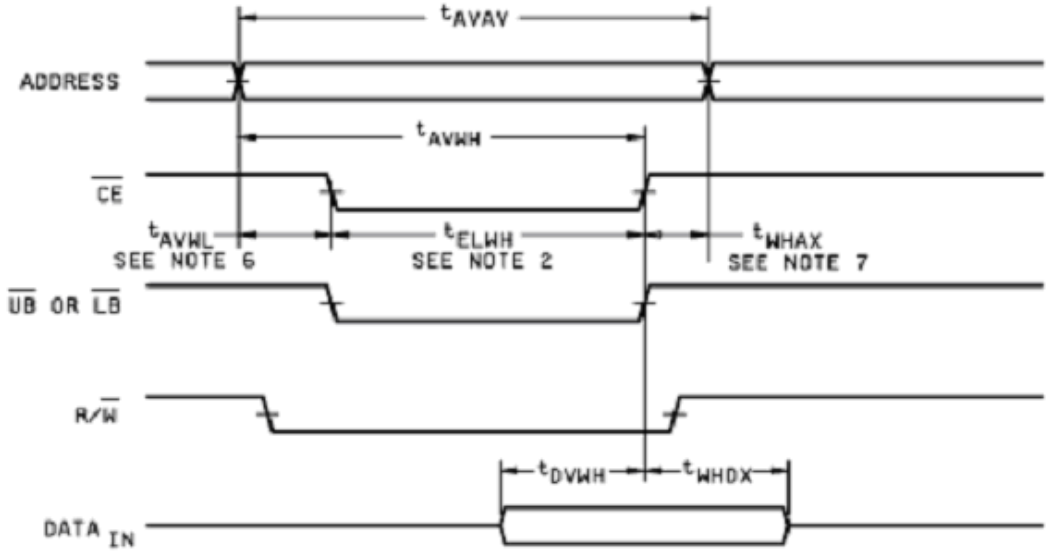
Notes on read operation:

1. $\overline{SEM}$ = V_{IH}
2. Start of valid data dependant upon which timing becomes effective last (t_{ABE}, t_{OLQV}, t_{ELQV}, t_{AVQV}, t_{BDD})
3. Timing dependant upon which signal asserted last ($\overline{OE}$, $\overline{CE}$, $\overline{LB}$ OR $\overline{UB}$).
4. Timing dependant upon which signal de-asserted first ($\overline{OE}$, $\overline{CE}$, $\overline{LB}$ OR $\overline{UB}$).
5. t_{BDD} delay is required only in the case where opposite port is completing a write operation to the same address location. For simultaneous read operations, BUSY has no relation to valid output data.

Write Cycle Nº 1 Timing- R/$\overline{W}$ Controlled (see notes 1, 3, 5, 8)



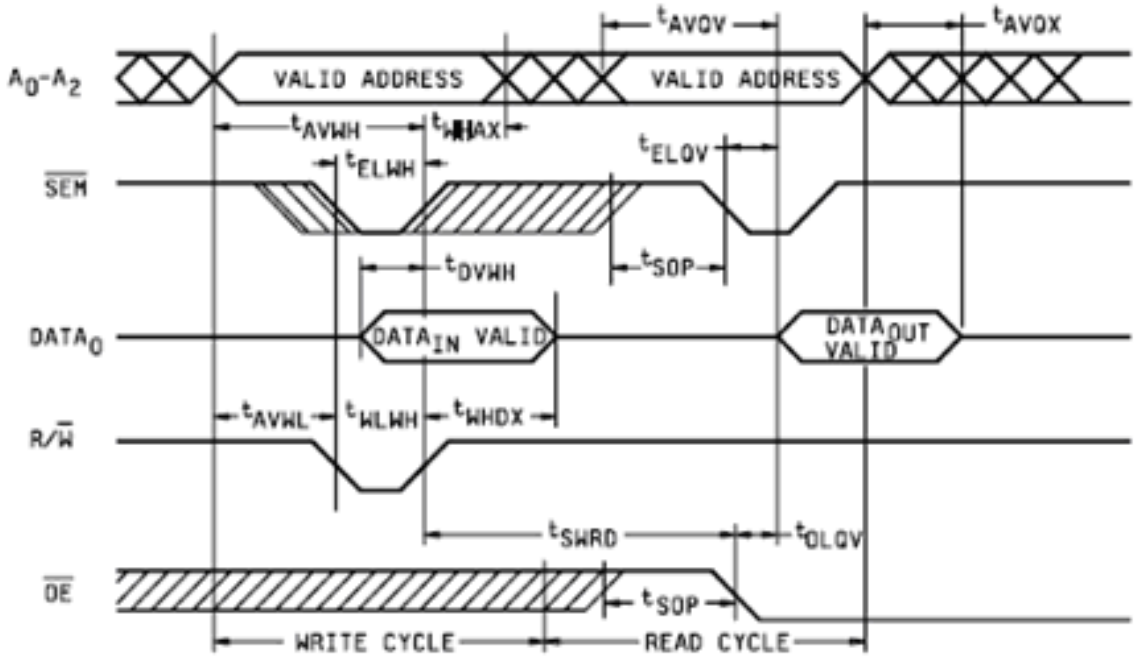
Write Cycle Nº 2 Timing- $\overline{CE}$, $\overline{UB}$, $\overline{LB}$ Controlled (see notes 1, 3, 5, 8)



Notes on Write Cycle

1. R/$\overline{W}$ or $\overline{CE}$ or $\overline{UB}$ and $\overline{LB}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{ELWH} or t_{WLWH}) of a low $\overline{UB}$ or $\overline{LB}$ and a low $\overline{CE}$ and a low R/$\overline{W}$ for memory array write cycle.
3. t_{WHAX} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing dependant upon which enable signal is asserted last.
7. Timing dependant upon which enable signal is de-asserted first.
8. For Write Cycle No.1, if $\overline{OE}$ is low during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WLWH} or (t_{WLQZ} + t_{DVWH}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DVWH}. If $\overline{OE}$ is high during the R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WLWH}.

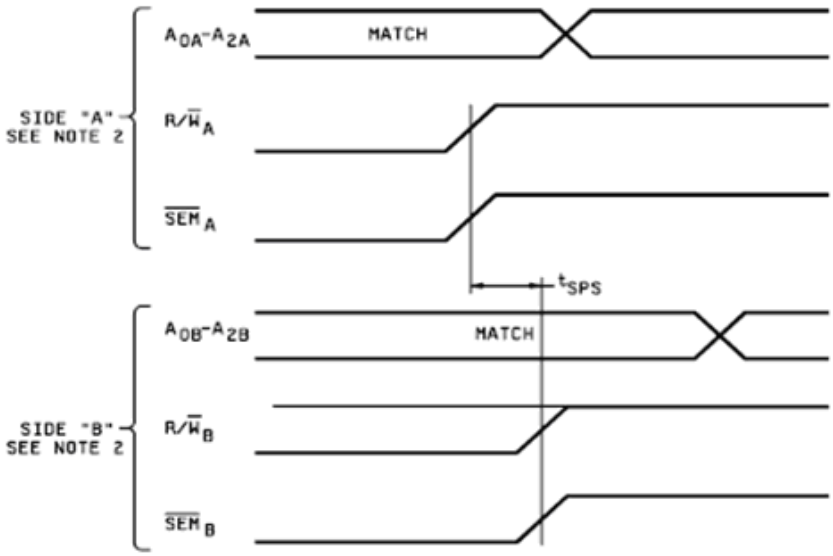
Semaphore Read After Write Timing



Notes

1. $\overline{CE}$ = V_{IH} or $\overline{UB}$; $\overline{LB}$ = V_{IH} for period of above timing for both the read and write operation.
2. All inputs and outputs equal to the same semaphore value for $DATA_{OUT}$ VALID condition.

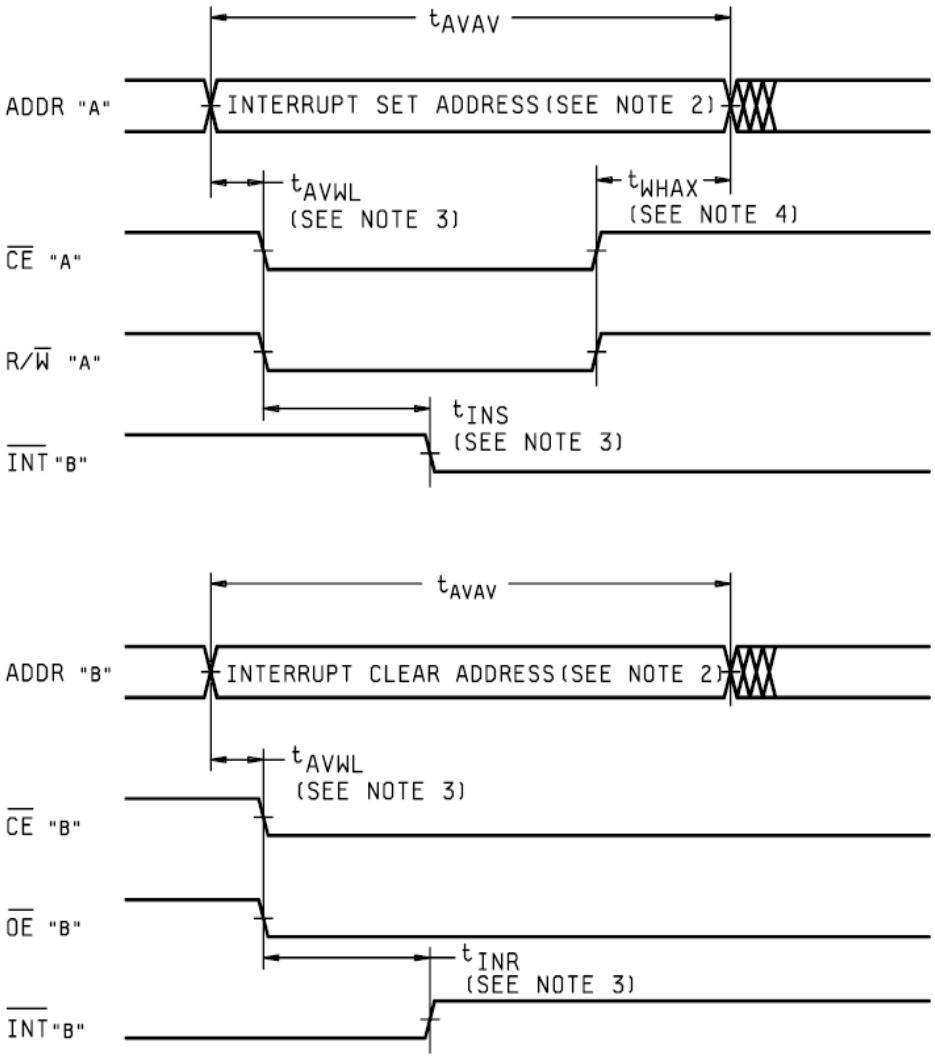
Semaphore Write Contention Timing



Notes:

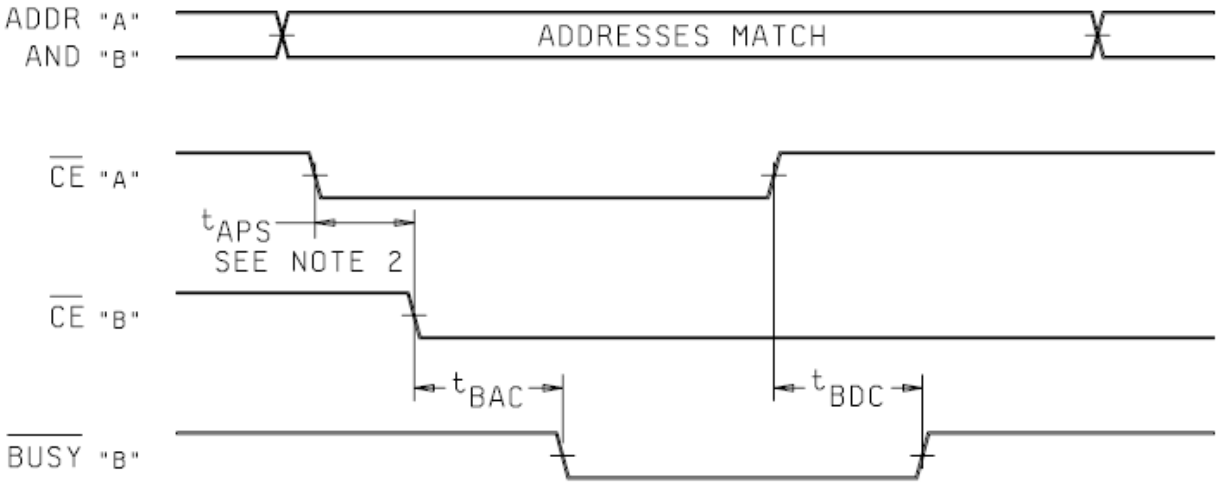
1. D_{OR} = D_{OL}, $\overline{CE}$ R = $\overline{CE}$ L = H, semaphore flag is released from both sides (reads as one from both sides) at cycle start.
2. 'A' may either be the left or right port. 'B' is the opposite port from 'A'
3. This parameter is measured from R/$\overline{W_A}$ or $\overline{SEM_A}$ going high to R/$\overline{W_B}$ or $\overline{SEM_B}$ going high.
4. If t_{SPS} is violated, semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.
5. CE = H for the duration of the Semaphore Read After Write Timing (both read and write cycle)

Interrupt Timing

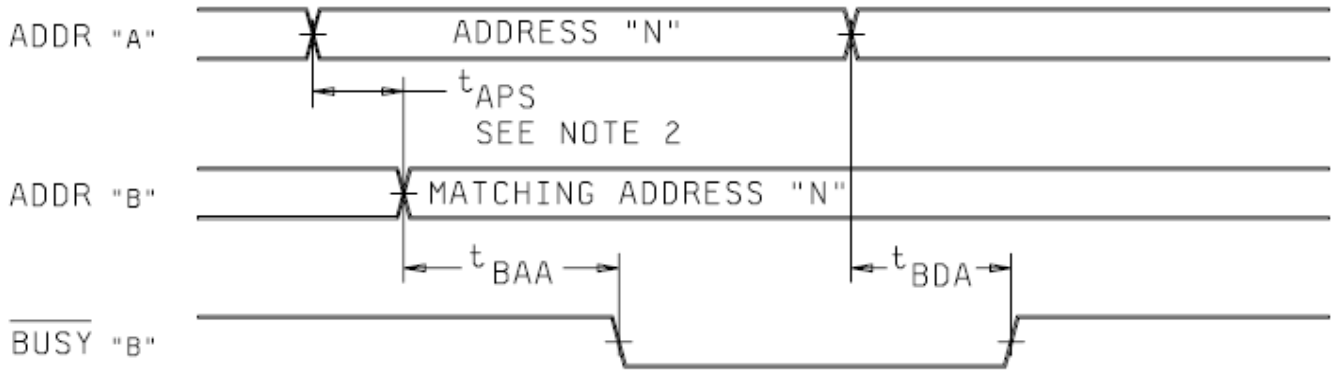


Notes
1. All timing is the same for left and right ports.
2. Port 'A' may be either the left or right port.
3. See Interrupt Truth Table
4. Timing is dependant upon which enable signal is asserted last ($\overline{CE}$ or R/$\overline{W}$)
5. Timing is dependant upon which enable signal is de-asserted first ($\overline{CE}$ or R/$\overline{W}$)

Busy Arbitration ($\overline{CE}$ Controlled) (M/$\overline{S}$ = H)



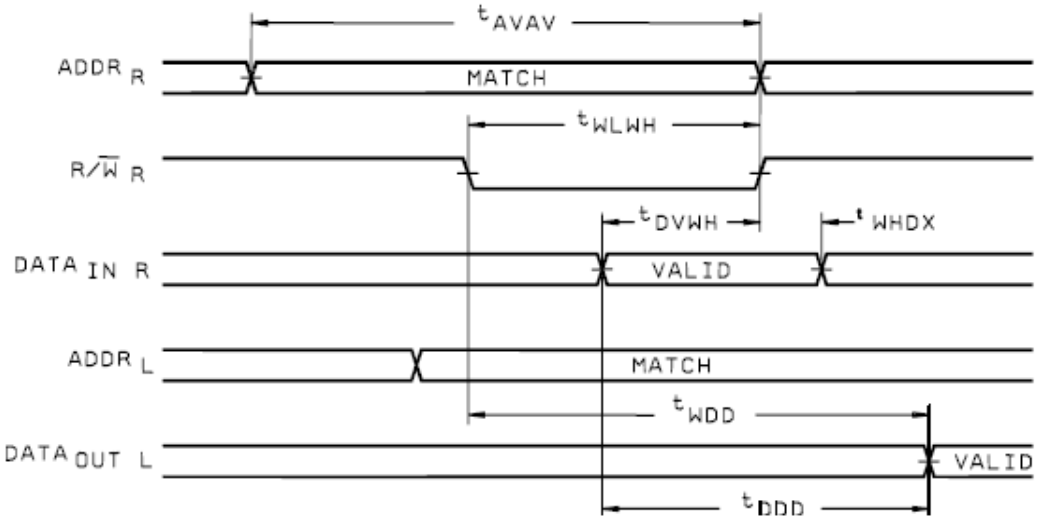
Busy Arbitration Cycle (Address Match Controlled) (M/$\overline{S}$ = H)



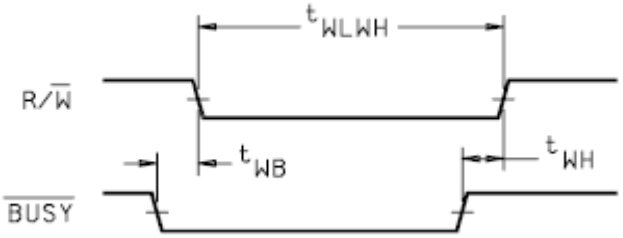
Notes:

1. All timing is the same for left and right ports. Port ‘A’ may be either the left or right port. Port ‘B’ is the port opposite from ‘A’.
2. If t_{APS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee on which side the busy signal will be asserted.

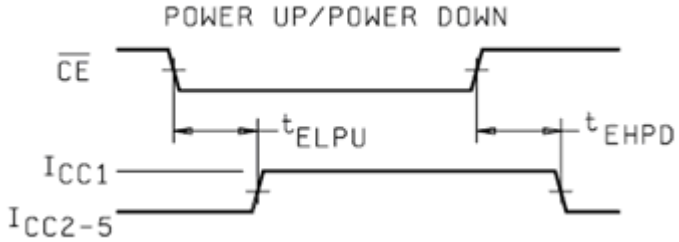
Write with Port - to - Port Delay (M/S = L)



Slave Write (M/$\overline{S}$ = L)



Power-Up / Power-Down Timing



Truth Table: Non-contention read write control

Inputs						Outputs		
$\overline{CE}$	R $\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O_{8-15}	I/O_{0-7}	Mode
H	X	X	X	X	H	High-Z	High-Z	Deselected: Power-down
X	X	X	H	H	H	High-Z	High-Z	Both Bytes Deselected
L	L	X	L	H	H	DATAIN	High-Z	Write to Upper Byte Only
L	L	X	H	L	H	High-Z	$DATA_{IN}$	Write to Lower Byte Only
L	L	X	L	L	H	$DATA_{IN}$	$DATA_{IN}$	Write to Both Bytes
L	H	L	L	H	H	$DATA_{OUT}$	High-Z	Read Upper Byte Only
L	H	L	H	L	H	High-Z	$DATA_{OUT}$	Read Lower Byte Only
L	H	L	L	L	H	$DATA_{OUT}$	$DATA_{OUT}$	Read Both Bytes
X	X	H	X	X	X	High-Z	High-Z	Outputs Disabled

Notes:

1. Read/Write controls are separate for independent left and right address ports ($A_{0L} – A_{12L}$ and $A_{0R} – A_{12R}$)

Truth Table: Semaphore Read/Write Control

Inputs						Outputs		
$\overline{CE}$	R $\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O_{8-15}	I/O_{0-7}	Mode
H	H	L	X	X	L	$DATA_{OUT}$	$DATA_{OUT}$	Read semaphore flag data out
X	H	L	H	H	L	$DATA_{OUT}$	$DATA_{OUT}$	Read semaphore flag data out
H	↑	X	X	X	L	$DATA_{IN}$	$DATA_{IN}$	Write I/O_0 into semaphore flag
X	↑	X	H	H	L	$DATA_{IN}$	$DATA_{IN}$	Write I/O_0 into semaphore flag
L	X	X	L	X	L	-	-	-
L	X	X	X	L	L	-	-	-

Notes:

1. Semaphore flags are addressed by $A_0 – A_2$
2. Semaphore Flags are written via I/O_0 and read from $I/O_0 – I/O_{15}$.

Truth Table: Address $\overline{BUSY}$ Arbitration

Outputs			Inputs		
$\overline{CE}_L$	$\overline{CE}_R$	$A_{0L} - A_{12L}$ $A_{0R} - A_{12R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	Function
X	X	No Match	H	High-Z	Normal
H	X	Match	H	High-Z	Normal
X	H	Match	H	High-Z	Normal
L	L	Match	High-Z	$DATA_{IN}$	Write Inhibit [2]

Truth Table: Interrupt Flag

Left Port					Right Port					
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{0L} - A_{12L}$	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{0R} - A_{12R}$	$\overline{INT}_R$	Function
L	L	X	1FFF	X	X	X	X	X	L	Set right $\overline{INT}_R$ flag
X	X	X	X	X	X	L	L	1FFF	H	Reset right $\overline{INT}_R$ flag
X	X	X	X	L	L	L	X	1FFE	X	Set left $\overline{INT}_L$ flag
X	L	L	1FFE	H	X	X	X	X	X	Set left $\overline{INT}_L$ flag

Notes:

1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R = V_{IH}$
2. If $\overline{BUSY}_L = V_{IL}$, no change
3. If $\overline{BUSY}_R = V_{IL}$, no change
1. $\overline{INT}_L$ and $\overline{INT}_R$ must be initialized at power-up

Ordering Information

Part Number	Package (Mil-Std-1835)	Generic
5962-9161701MXA	CMGA15-PN	QP7025S70GB
5962-9161701MYA	CQFP84 –See Note 2	QP7025S70FB
5962-9161702MXA	CMGA15-PN	QP7025L70GB
5962-9161702MYA	CQFP84 –See Note 2	QP7025L70FB
5962-9161703MXA	CMGA15-PN	QP7025S55GB
5962-9161703MYA	CQFP84 –See Note 2	QP7025S55FB
5962-9161704MXA	CMGA15-PN	QP7025L55GB
5962-9161704MYA	CQFP84 –See Note 2	QP7025L55FB
5962-9161705MXA	CMGA15-PN	QP7025S45GB
5962-9161705MYA	CQFP84 –See Note 2	QP7025S45FB
5962-9161706MXA	CMGA15-PN	QP7025L45GB
5962-9161706MYA	CQFP84 –See Note 2	QP7025L45FB
5962-9161707MXA	CMGA15-PN	QP7025S35GB
5962-9161707MYA	CQFP84 –See Note 2	QP7025S35FB
5962-9161708MXA	CMGA15-PN	QP7025L35GB
5962-9161708MYA	CQFP84 –See Note 2	QP7025L35FB

Notes:

1. Package outline information and specifications are defined by Mil-Std-1835 package dimension requirements.
2. See SMD 5962-91617 Fig.1 Case Outline 'Y' Fig. 1
3. QP Semiconductor supports Source Control Drawing (SCD), and custom package development for this product family.
4. The listed drawings, Mil-PRF-38535, Mil-Std-883 and Mil-Std-1835 are available online at http://www.dscc.dla.mil/
5. Additional information is available at our website http://www.qpsemi.com

Document Revision History

Date	Revision Level	Description
20 June 2010	0	initial release