DC/DC Driver

Power Factor Correction Controller IC

BD7691FJ

General Description

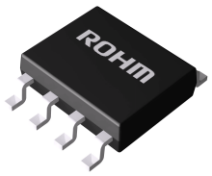
BD7691FJ is Power Factor Correction for AC/DC supplies the system which is suitable for all the products needing power factor improvement. The PFC adopts boundary conduction mode (BCM), and switching loss reduction and noise reduction are possible by Zero Current Detection(ZCD). ZCD detects by resistance, the auxiliary winding is unnecessary.

Key Specifications

- Input Voltage Range: 10V to 26V
- Operating Current: 360uA(Typ)
- Max Frequency: 220kHz(RT:220kΩ)
- Operating Temperature Range: -40°C to +105°C

Package(s)

	W(Typ) x D(Typ) x H(Max)
SOP-J8	4.90mm x 6.00mm x 1.65mm



SOP-J8

Features

- Boundary Conduction Mode
- Low Power consumption
- VCCUVLO
- Resister detection for ZCD
- Switching loss reduction, noise reduction by ZCD
- Improving the efficiency by the max frequency control
- Dynamic and Static OVP by the VS pin
- High accuracy over current detection(±4%)
- Error amplifier input short protection
- Stable MOSFET gate drive by the Clamper
- Protection function by the OVP pin

Applications

- AC adopter, TV, Lighting equipment, Refrigerator, etc.

Typical Application Circuit(s)

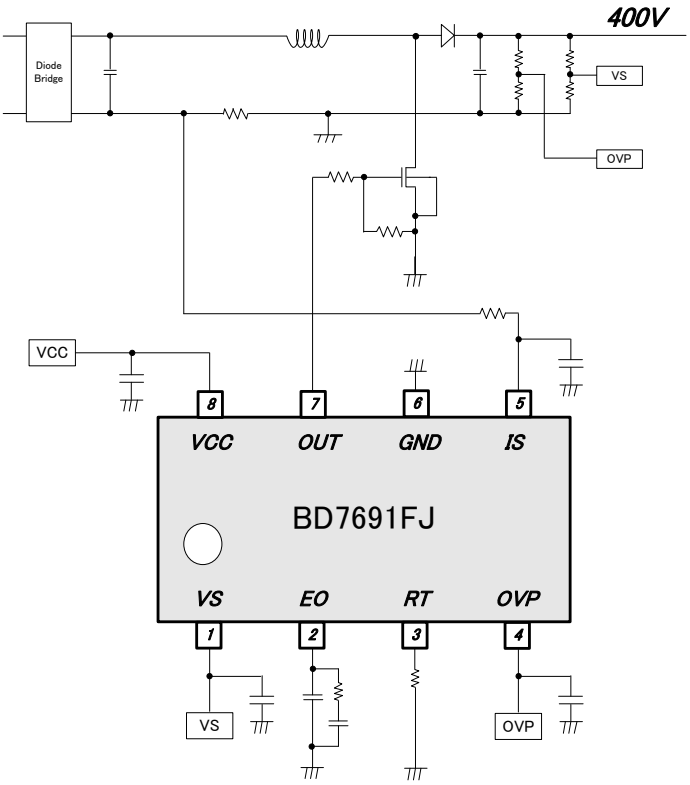


Figure 1. Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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Pin Configuration(s)

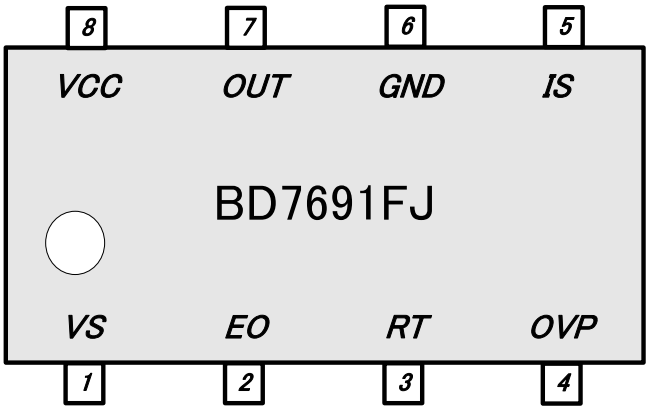


Figure 2. Pin Configuration（Top View）

Pin Description(s)

Table 1. Pin Description

Pin Name	I/O	Pin No.	Function	ESD Diode	
				VCC	GND
VS	I	1	Feedback input	-	○
EO	I/O	2	Error amp output	-	○
RT	I/O	3	Max frequency setting	-	○
OVP	I	4	Over voltage protection	-	○
IS	I	5	Zero current and over current detection	-	○
GND	-	6	GND	○	-
OUT	O	7	MOSFET gate control	-	○
VCC	I	8	VCC	-	○

Block Diagram(s)

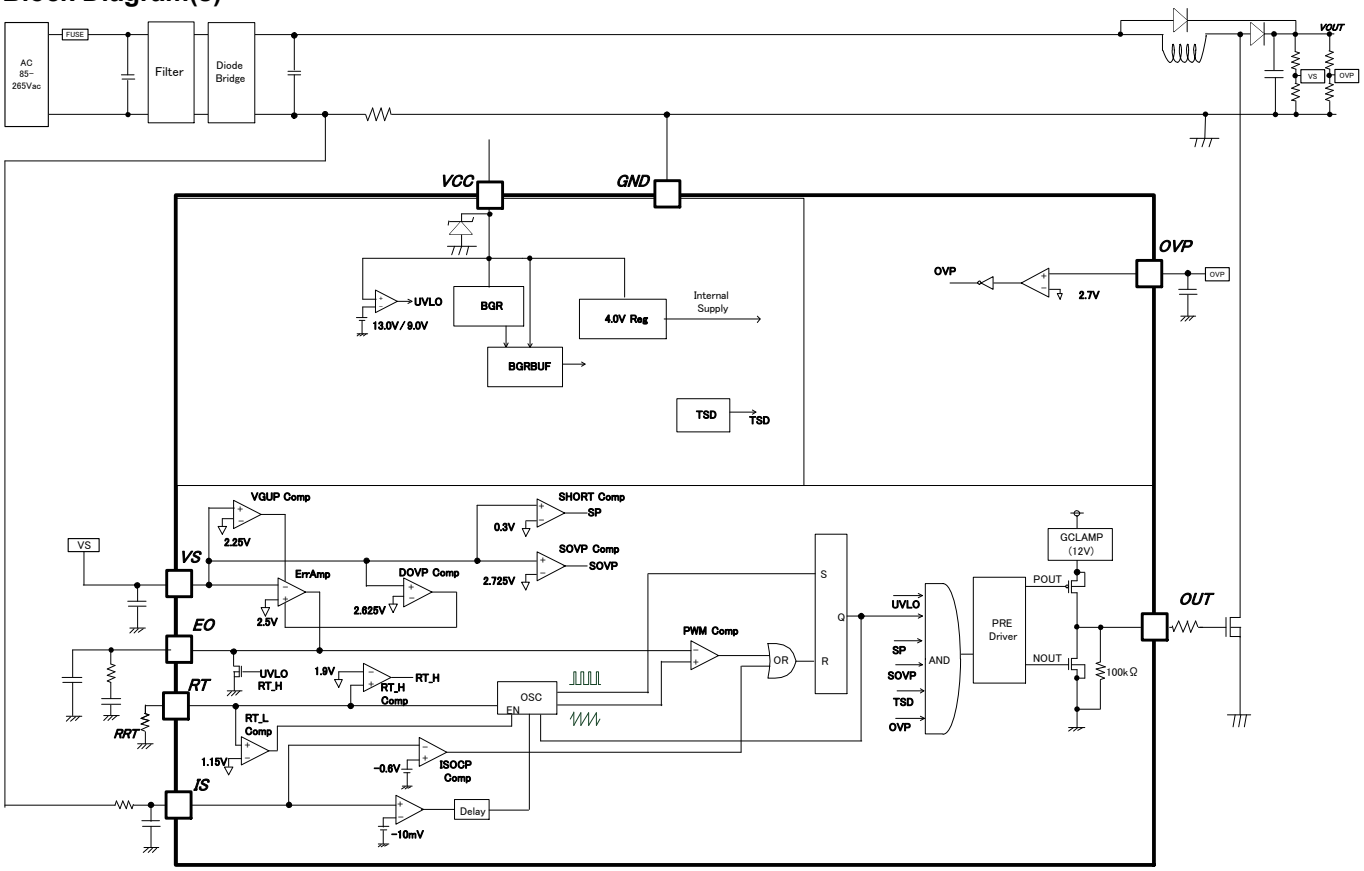


Figure 3 Block Diagram

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Description of Block(s)

(1) VCC protection

This IC incorporates VCC UVLO (Under Voltage Lock Out) of the VCC pin. Switching stops at the time of VCC voltage drop.

(2) Power Factor Correction

The power factor improvement circuit is a voltage control method of Boundary Conduction Mode.
The outline operation circuit diagram is shown in Figure 4. The switching operation is shown in Figure 5.

Switching Operation

1. MOSFET is turned on, and I_L increases
2. The IC compares V_{EO} with Vramp, and MOSFET is off when the Vramp voltage higher than V_{EO}
3. MOSFET is off, and I_L decreases
4. The IC detects a zero point of the I_L in IS pin and turns on MOSFET

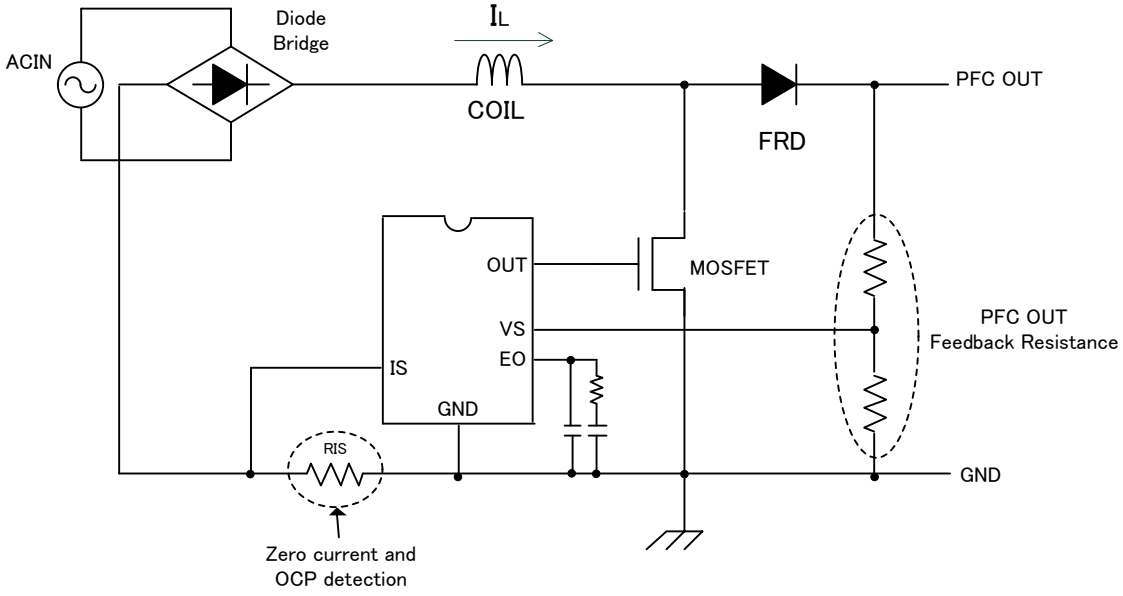


Figure 4. Operation circuit outline

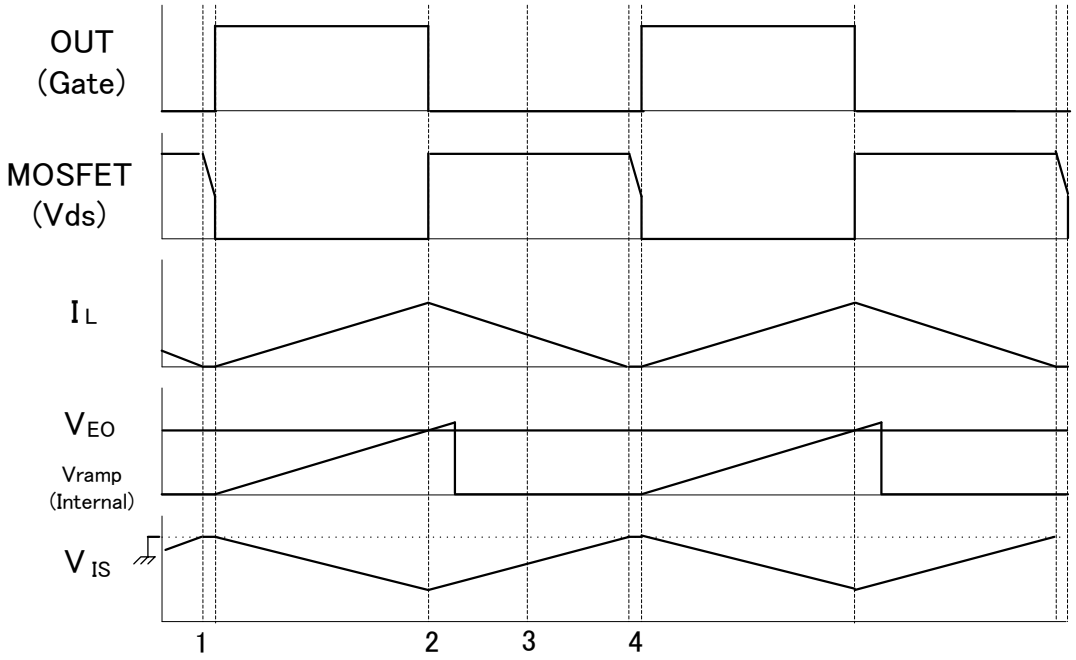


Figure 5. Switching operation timing chart

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(3) About ErrAMP

(3-1) gmAMP

The VS pin monitors a divided voltage of the output voltage. The ripple voltage of AC frequency (50Hz/60Hz) overlaps with VS pin. gmAMP removes this ripple voltage. gmAMP compares VAMP (2.5V typ.) with the divided voltage of the output voltage, gmAMP controls the EO voltage by this gap. When EO pin voltage rises, ON width of the OUT pin becomes wide. When the EO voltage less than about 0.7V, the IC stops switching. Therefore it can stop switching operation when EO pin connects to the GND.

External parts value of EO pin should be set that the ripple voltage of AC frequency does not conduct to EO pin. And, please confirm it by real board.

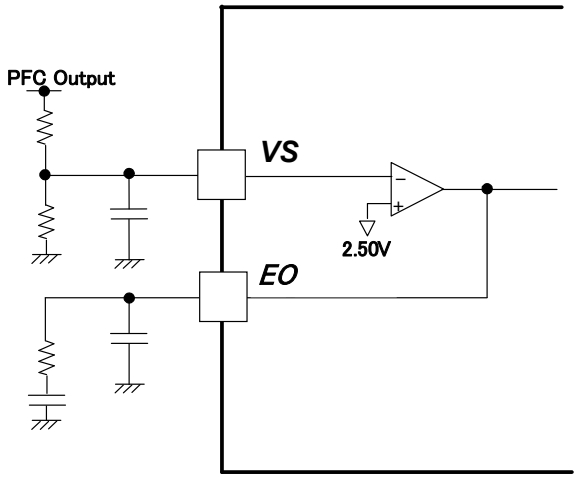


Figure 6. gmAMP block diagram

(3-2) VS short protection

VS pin has a short protection function.

A state of PFC output voltage < V_{SHORT} (0.3V typ.) continues more than T_{VS_SH} (150us typ.), it stops switching.

It shows operation in Figure 7.

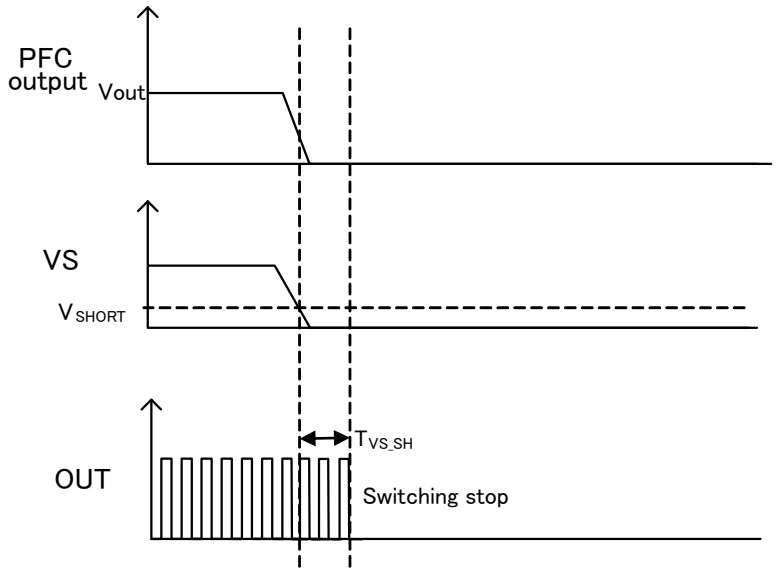


Figure 7. Operation of VS short protection

(3-3) VS low voltage gain increase function

When output voltage decreases by output load sudden changes, an output voltage drop period becomes long because a voltage control loop is slow. VS pin voltage becomes lower than VGUP (2.25V typ.) (equivalent to -10% of output voltage), the error amplifier increases a gain. By this operation, ON width of OUT increases and prevents a long-term drop of the output voltage. When VS pin voltage rises from V_{GUP}(2.25V typ.), this operation stops.

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(3-4) VS overvoltage gain increase function (Dynamic OVP)

When output voltage rises by startup or a rapid change of the output load, output voltage rises for a long term because a voltage control loop is slow. VS pin voltage becomes higher than VOVP (2.625V typ.) (equivalent to +5% of output voltage), the error amplifier increases a gain. By this operation, it reduces ON width of OUT and prevents a long-term rise of the output voltage. When VS pin voltage decreases under V_{OVP}(2.625V typ.), this operation stops.

(3-5) VS overvoltage protection function (Static OVP)

VS pin rises across V_{OVP}, static OVP acts, and VS pin voltage rises from V_{OVP1}(2.7V typ.), it stops switching immediately. VS pin voltage under than V_{OVP2}(2.6V typ.), it starts switching. It shows operation in Figure 8.

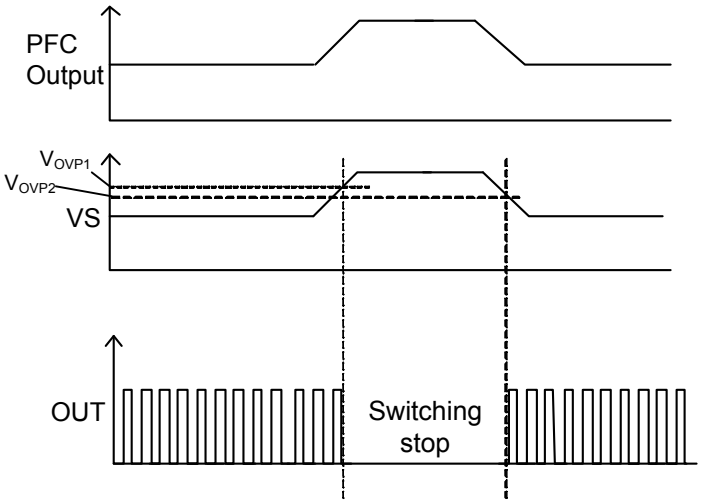


Figure 8. VS overvoltage protection operation

(4) OVP pin over voltage protection

The OVP pin is an overvoltage protection function in case of VS feedback circuit rises over static OVP (cf. Figure 9). When OVP pin voltage rises over V_{OVP3} (2.7V typ.), it stops switching operation after T_{OVP3}(60us typ.) (cf. Figure 9). If OVP pin becomes less than V_{OVP4} (2.6V typ.), it becomes restart operation.

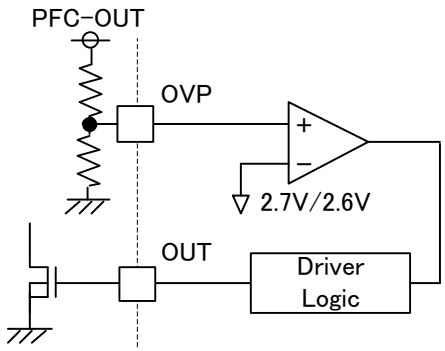


Figure 9. OVP pin over voltage protection

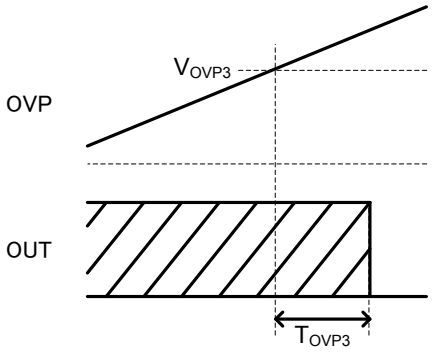


Figure 10. Timing chart

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(5) IS pin Zero current detection and overcurrent detection function

The zero current detection circuit is a function to detect a zero cross of the inductor current (I_L) (cf. Figure 11). When the voltage of the IS pin becomes higher than the zero current detection voltage, the OUT output becomes High after progress at zero current detection delay time(T_{ZCDD}.). Please set the RIS value (cf. Figure.4) so that IS pin voltage becomes less than V_{IS_OCP} (-0.6V typ.). In addition, it recommends that it adds CR filter for switching noise reduction. It shows operation in Figure 12.

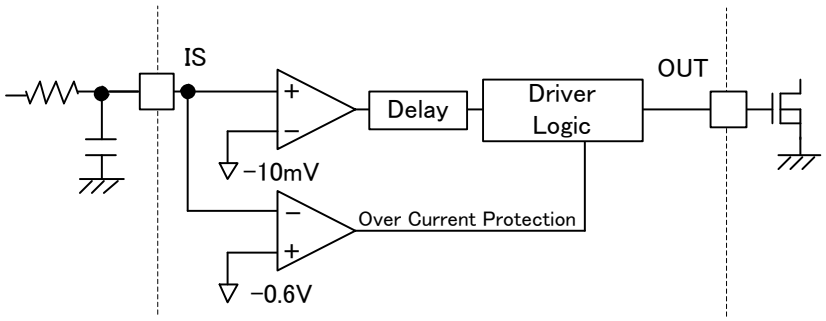


Figure 11. IS pin current detection circuit

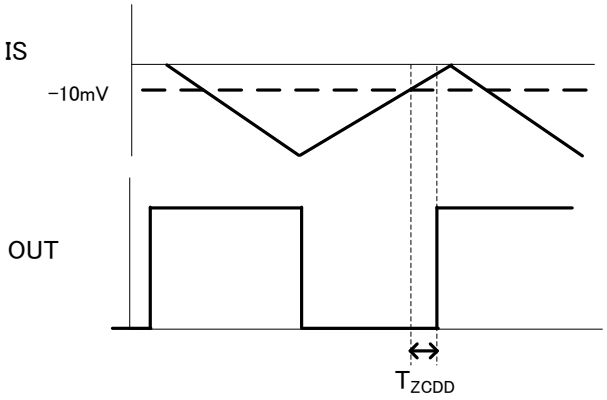


Figure 12. IS zero current detection delay time

(6) RT pin

This pin sets a slope wave pattern formed in the IC inside by external resistance. It shows RT resistor value and relations of the maximum frequency in Figure 13. The maximum ON width on the application is calculated in the following formula. It shows relations of RT resistor value and maximum ON width in Figure 14.

$$T_{ON_MAX}[s] = \frac{2 \times L \times P_O}{V_{ACMin}{}^2 \times \eta}$$

V_{AC}: Input voltage, L: Inductance, Po: Max output power, η :Efficiency

Necessary TON_MAX on application can be check as upper formula. Please set ON width in RT pin more than TONMAX.
In addition, it shows relations of RT resistor value and PFC zero current detection Delay in Figure 15.
The high-speed frequency in the light load is limited in RT pin. The external resistance range of the RT pin is 51kΩ - 390kΩ.

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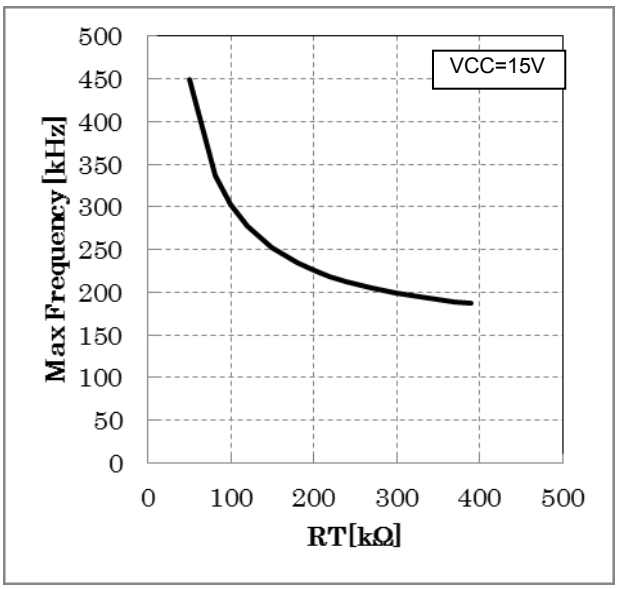


Figure 13. Relations of RT resistor value and the Max frequency (reference value)

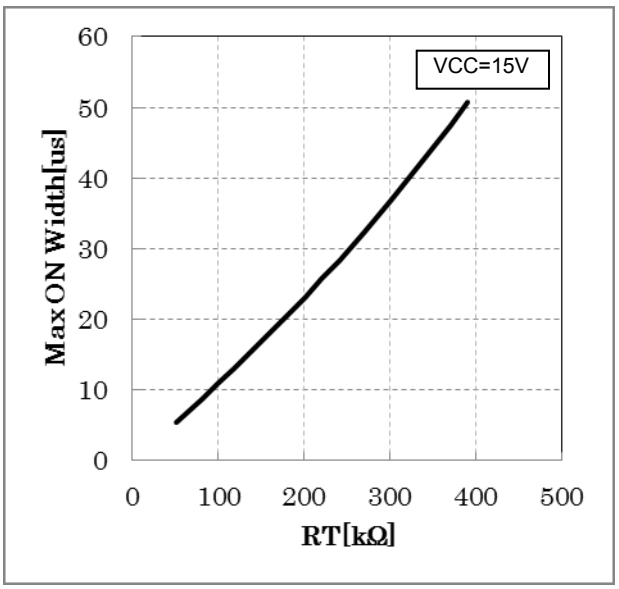


Figure 14. Relations of RT resistor value and the max ON width (reference value)

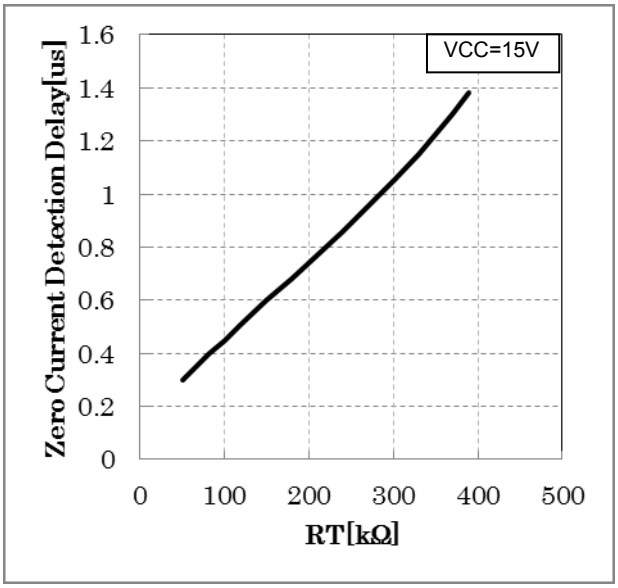


Figure 15. Relations of RT resistor value and PFC zero current detection delay (reference value)

*The graph mentioned above is reference value. After the confirmation of the actual board, please set the fixed number.

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Operation mode of the protective circuit

It shows the operation mode of each protection function in Table 2.

Table 2. Operation mode of each protective circuit

Parameter	Contents	Protection mode			
		Detection method	Detect operation	Cancellation method	Cancellation operation
VCCUVLO	VCC pin low voltage protection	VCC<9.0V(typ.) (VCC drop)	OUT stop EO discharge	VCC>13.0V(typ.) (VCC rise)	Startup operation
IS OCP	IS pin short protection	IS<−0.60V(typ.) (IS drop)	OUT stop	IS>−0.60V(typ.) (IS rise)	Normal operation
VS short protection	VS pin short protection	VS<0.30V(typ.) (VS drop)	OUT stop	VS>0.30V(typ.) (VS rise)	Normal operation
VS gain increase	VS pin low voltage gain increase	VS<2.25V(typ.) (VS drop)	GM amplifier GAIN increase	VS>2.25V(typ.) (VS rise)	Normal operation
VS Dynamic OVP	VS pin overvoltage protection 1	VS>2.625V(typ.) (VS rise)	GM amplifier GAIN increase	VS<2.625V(typ.) (VS drop)	Normal operation
VS Static OVP	VS pin overvoltage protection 2	VS>2.700V(typ.) (VS rise)	OUT stop	VS<2.600V(typ.) (VS drop)	Normal operation
OVP	OVP pin overvoltage protection 3	OVP>2.700V(typ.) (OVP rise)	OUT stop	OVP<2.700V(typ.) (OVP drop)	Normal operation

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Absolute Maximum Ratings (Tj = 25°C)

Parameter	Symbol	Rating	Unit	Condition
Max Voltage 1	V_{max1}	-0.3 to +28.0	V	VCC
Max Voltage 2	V_{max2}	-0.3 to +15.0	V	OUT
Max Voltage 3	V_{max3}	-0.3 to +6.5	V	OVP, RT, VS, EO
Max Voltage 4 (Excluded after input voltage injection between 20ms)	V_{max4}	-6.5 to +0.3	V	IS
IS Pin Max Current (Less than 20ms after input voltage injection)	I_{IS}	-20	mA	IS
OUT Pin Output Peak Current 1	I_{OUT1}	-0.5	A	Source current
OUT Pin Output Peak Current 2	I_{OUT2}	+1.0	A	Sink current
Operation Temperature Range	T_{opr}	-40 to +105	°C	
Storage Temperature Range	T_{str}	-55 to +150	°C	

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Thermal Resistance(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 3)	2s2p(Note 4)	
SOP-J8				
Junction to Ambient	θ_{JA}	149.3	76.9	°C/W
Junction to Top Characterization Parameter(Note 2)	Ψ_{JT}	18	11	°C/W

*(Note 1)*Based on JESD51-2A(Still-Air)
*(Note 2)*The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
*(Note 3)*Using a PCB board based on JESD51-3.
*(Note 4)*Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

Recommended Operating Conditions（Ta=25°C）

Parameter	Symbol	Rating	Unit	Condition
Supply Voltage	V_{CC}	10.0～26.0	V	VCC voltage

Recommended range of the external component（Ta=25°C）

Parameter	Symbol	Range	Unit
VCC pin connection capacity	C_{VCC}	More than 10.0	uF
RT pin connection resistance	R_{RT}	51 to 390	kΩ

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Electrical Characteristics (Unless otherwise specified VCC=15V Ta=25°C)

Parameter	Symbol	Specifications			Unit	Condition
		Min	Typ	Max		
[Circuit Current]						
Circuit Current(ON)1	I_{ON1}	-	360	600	uA	EO=0.0V, RT=220kΩ
Circuit Current (ON)2	I_{ON2}	-	540	900	uA	EO=3.0V, RT=220kΩ (Switching operation)
Start Up Current	I_{ON3}	-	65	130	uA	VCC=12V
[VCC pin protection]						
VCC UVLO Voltage1	V_{UVLO1}	12.0	13.0	14.0	V	VCC rise
VCC UVLO Voltage2	V_{UVLO2}	8.0	9.0	10.0	V	VCC drop
VCC UVLO Hysteresis	V_{UVLO3}	-	4.0	-	V	$V_{UVLO3} = V_{UVLO1} - V_{UVLO2}$
[Gm Amplifier Block]						
VS pin Pull Up Current	I_{VS}	-	0.5	-	uA	
Gm Amplifier Reference Voltage 1	V_{AMP}	2.465	2.500	2.535	V	
Gm Amplifier Line Regulation	$V_{AMP\ line}$	-20	-1	-	mV	VCC10V to 26V
Gm Amplifier Trans Conductance	T_{VS}	50	75	100	uA/V	EO=2.5V V_{GUP} <VS＜V_{OVP}
Gm Amplifier Source Current	$I_{EO\ source}$	30	50	70	uA	VS=1.0V
Gm Amplifier Sink Current	$I_{EO\ sink}$	30	50	70	uA	VS=3.5V
[EO Block]						
OFF Threshold Voltage	EO_{OFF_TH}	0.57	0.67	0.77	V	
EO Discharge Resistance	R_{EO}	2.3	4.3	6.3	kΩ	VCC=12V, EO=3V
[OSC Block]						
MAX ON Width	$T_{MAXDUTY}$	23.4	26.0	28.6	us	RT=220kΩ EO=4V
MAX Frequency	$F_{MAXDUTY}$	160	220	280	kHz	RT=220kΩ EO=0.7V
RT Output Voltage	V_{RT}	0.90	1.15	1.40	V	
[IS Block]						
Zero Current Detection Voltage	V_{ZCD}	-15m	-10m	-5m	V	
Zero Current Detection Voltage Delay	T_{ZCDD}	-	0.85	1.70	us	RT=220kΩ
IS Overcurrent Detection Voltage	V_{IS_OCP}	-0.62	-0.60	-0.58	V	
[VS Protection Block]						
VS Short Protection Detection Voltage	V_{SHORT}	0.200	0.300	0.400	V	
VS Shortstop Protection Detection Time	T_{VS_SH}	50	150	300	us	
VS Overvoltage Gain Increase Voltage	V_{OVP}	1.025×V_{AMP}	1.050×V_{AMP}	1.075×V_{AMP}	V	
VS Overvoltage Protection Detection Voltage 1	V_{OVP1}	1.065×V_{AMP}	1.080×V_{AMP}	1.095×V_{AMP}	V	VS rise
VS Overvoltage Protection Detection Voltage 2	V_{OVP2}	1.020×V_{AMP}	1.040×V_{AMP}	1.060×V_{AMP}	V	VS drop
VS Overvoltage Protection Detection Voltage Hys	V_{HYS}	0.030×V_{AMP}	0.040×V_{AMP}	0.050×V_{AMP}	V	
VS Low Voltage Gain Increase Voltage	V_{GUP}	0.840×V_{AMP}	0.900×V_{AMP}	0.960×V_{AMP}	V	
[OVP Block]						
OVP Detection Voltage 1	V_{OVP3}	2.6	2.7	2.8	V	OVP rise
OVP Detection Voltage 2	V_{OVP4}	2.5	2.6	2.7	V	OVP drop
OVP Detect Time	T_{OVP3}	20	60	150	us	
[OUT Block]						
OUT H Voltage	V_{POUTH}	10.8	12.0	13.2	V	IO=-20mA
OUT L Voltage	V_{POUTL}	-	-	1.00	V	IO=+20mA
OUT Pull-down Resistance	R_{PDOUT}	75	100	125	kΩ	

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Typical Performance Curves
(Reference data)

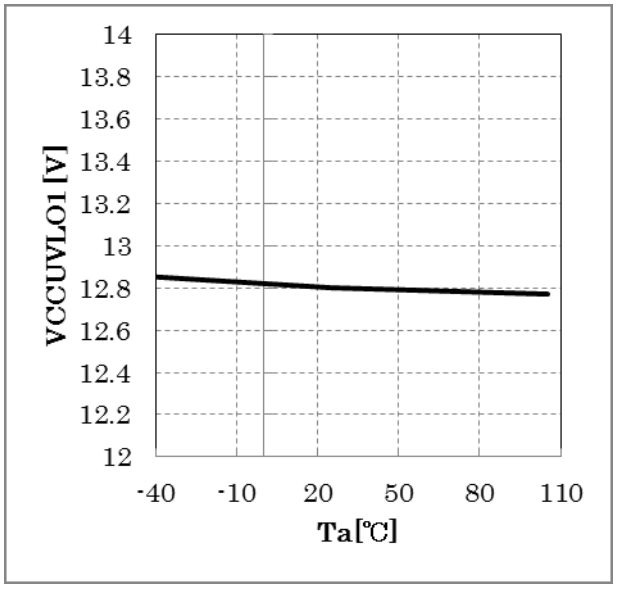


Figure 16. VCC UVLO voltage1 (VCCUVLO1) vs Ambient temperature (Ta)

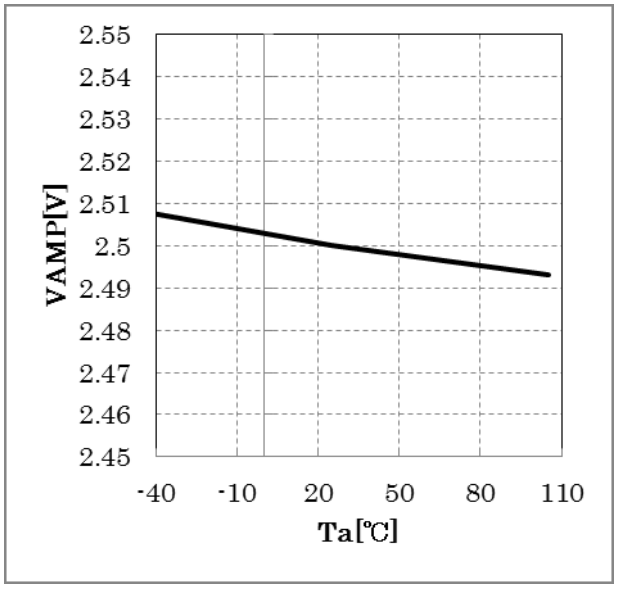


Figure 17. Gm amplifier reference voltage1 (VAMP) vs Ambient temperature (Ta)

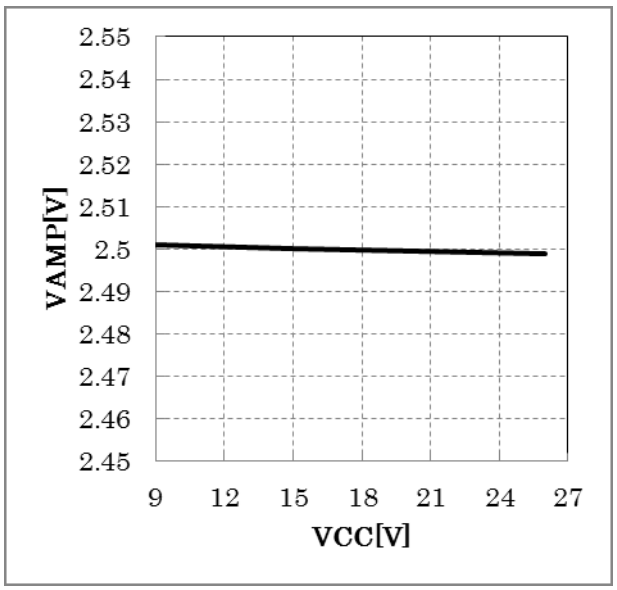


Figure 18. Gm amplifier reference voltage1 (VAMP) vs VCC

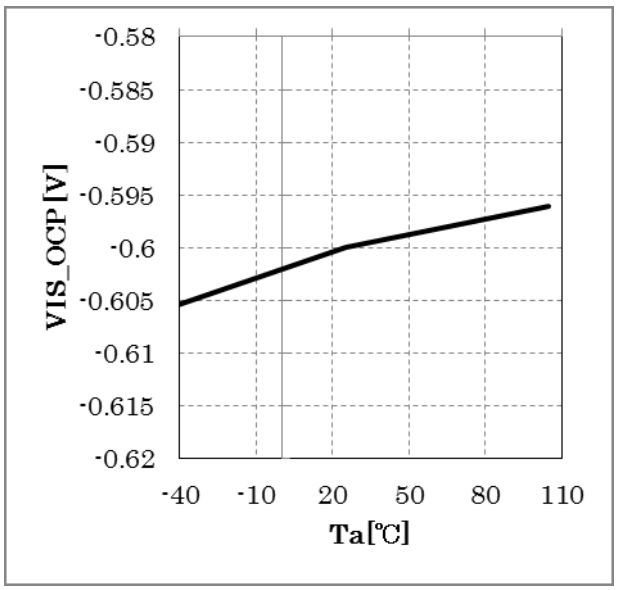


Figure 19. IS overcurrent detection voltage (VIS_OCP) vs Ambient temperature (Ta)

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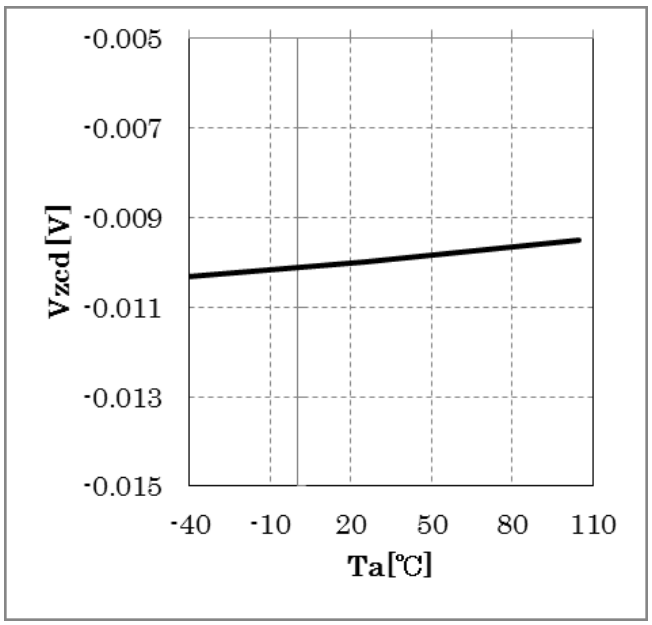


Figure 20. Zero current detection voltage (Vzcd) vs vs Ambient temperature (Ta)

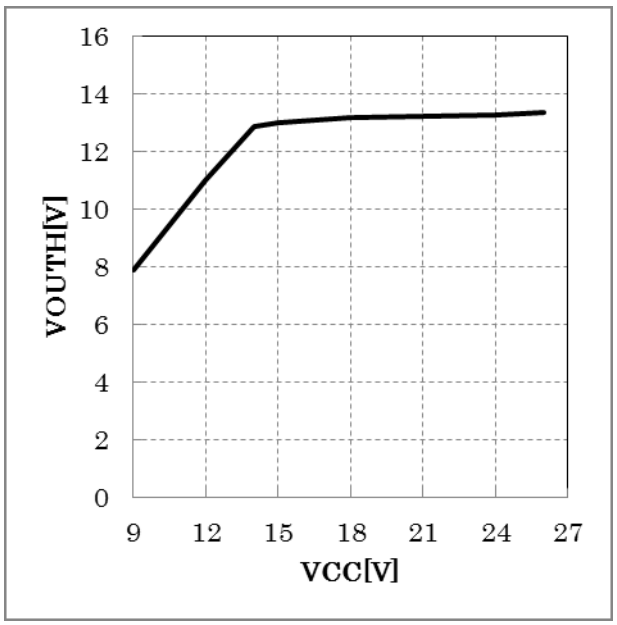


Figure 21. OUT pin H voltage (VOUTH) vs VCC

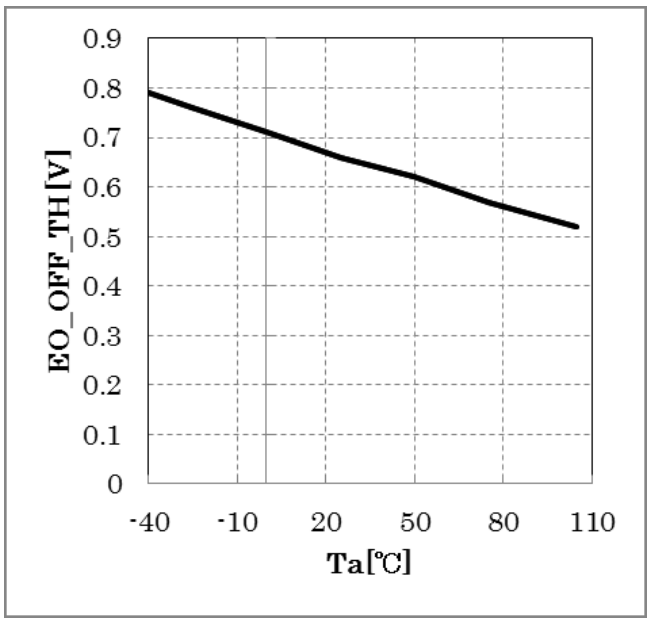


Figure 22. EO pin off threshold (EO_OFF_TH) vs Ambient temperature (Ta)

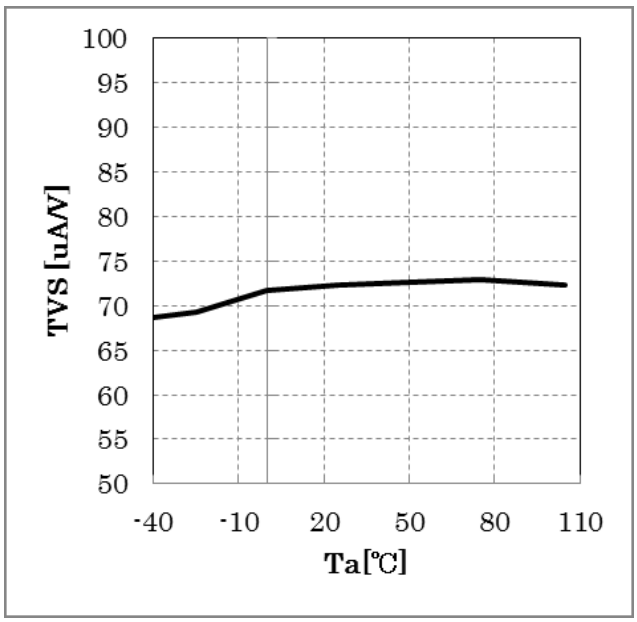


Figure 23. Gm amplifier trans conductance (TVS) vs Ambient temperature (Ta)

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I/O Equivalence Circuits

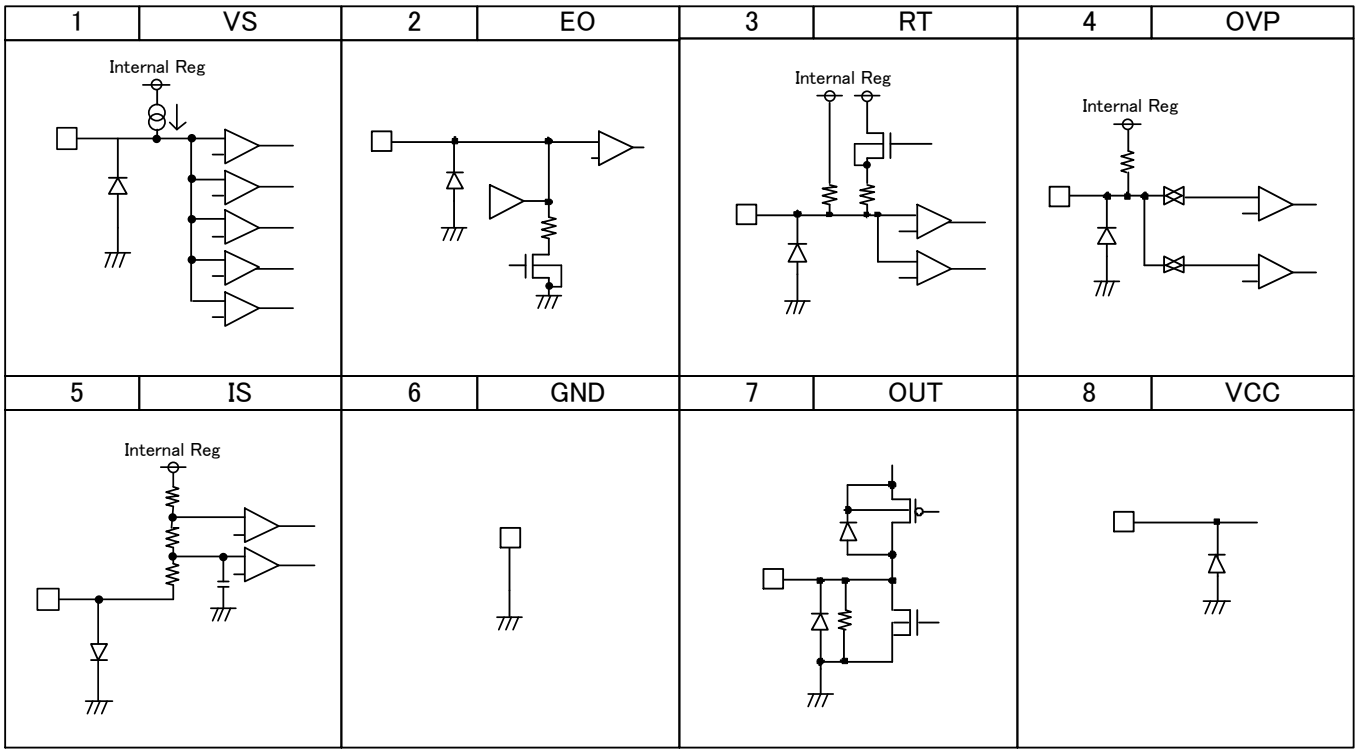


Figure 24. I/O Equivalence Circuits

Application Example

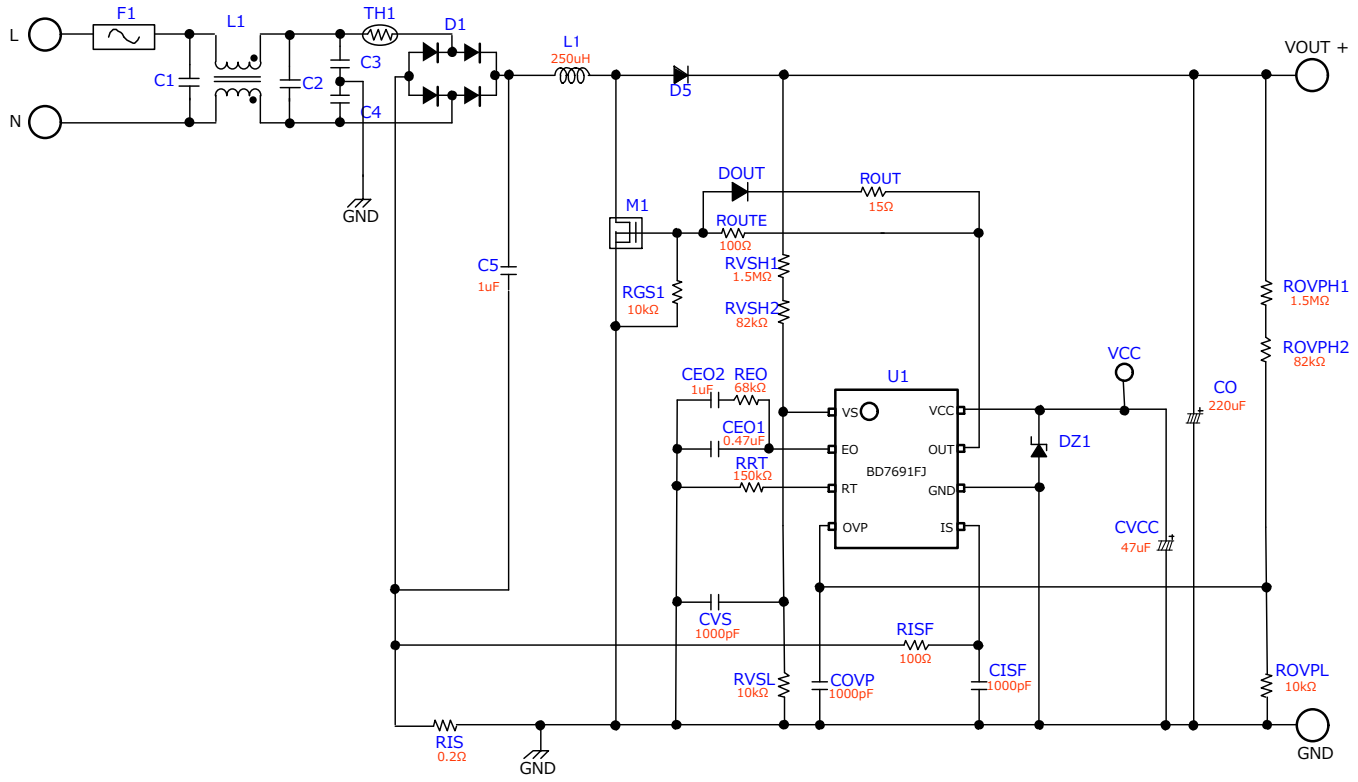


Figure 25. Application Example

1. Output voltage setting

The output voltage is decided in resistor value of RVSH and RVSL.

$$Vo_PFC = \left(1 + \frac{RVSH}{RVSL}\right) \times VAMP = \left(1 + \frac{1582k\Omega}{10k\Omega}\right) \times 2.5V = 398V$$

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2. Decision of minimum frequency fsw
The switching frequency of PFC

$$fsw = \frac{\eta_PFC \times Vin^2}{2 \times Po_PFC \times L} \times \frac{Vo_PFC - \sqrt{2} \times Vin}{Vo_PFC}$$

The frequency is minimized in the minimum input voltage. Slow frequency is effective about loss and noise. However, inductance is large value at low frequency. In addition, it enters the audible band when frequency lowers to 20kHz or less, and sound banging occurs. It designs the minimum frequency as 50kHz this time.

3. Calculation of the inductance

$$L = \frac{\eta_PFC \times Vin^2}{2 \times Po_PFC \times fsw} \times \frac{Vo_PFC - \sqrt{2} \times Vin}{Vo_PFC}$$

Ex) Vin=AC90V, Vo_PFC=400V, Po_PFC=200W, η_PFC=0.9, fsw=50kHz

$$L = 248.5uH \approx 250uH$$

4. Calculation of the inductor current

$$Ipk = \frac{\sqrt{2} \times Vin}{L} \times ton = \frac{2\sqrt{2} \times Po_PFC}{\eta_PFC \times Vin} = 6.98A$$

5. Calculation of the ON width

$$T_{ON_MAX}[s] = \frac{2 \times L \times P_O_PFC}{V_{ACMin}{}^2 \times \eta_PFC}$$

ON width is short at the high AC voltage. Therefore, the ON width is decided with the minimum AC voltage.
It recommends RT setting such as the maximum ON width is just covered at the minimum AC voltage. ON width is small when the high AC voltage. And the EO voltage range is small. EO voltage band width is the large then the ON width setting by the RT resistance is short.

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Attention in the board design

About parts placement
Please locate the parts in the Fig.26 inside dot line near the IC. In addition, please do parts placement to avoid the interference with switching lines and high current lines such as inductor, DRAIN.

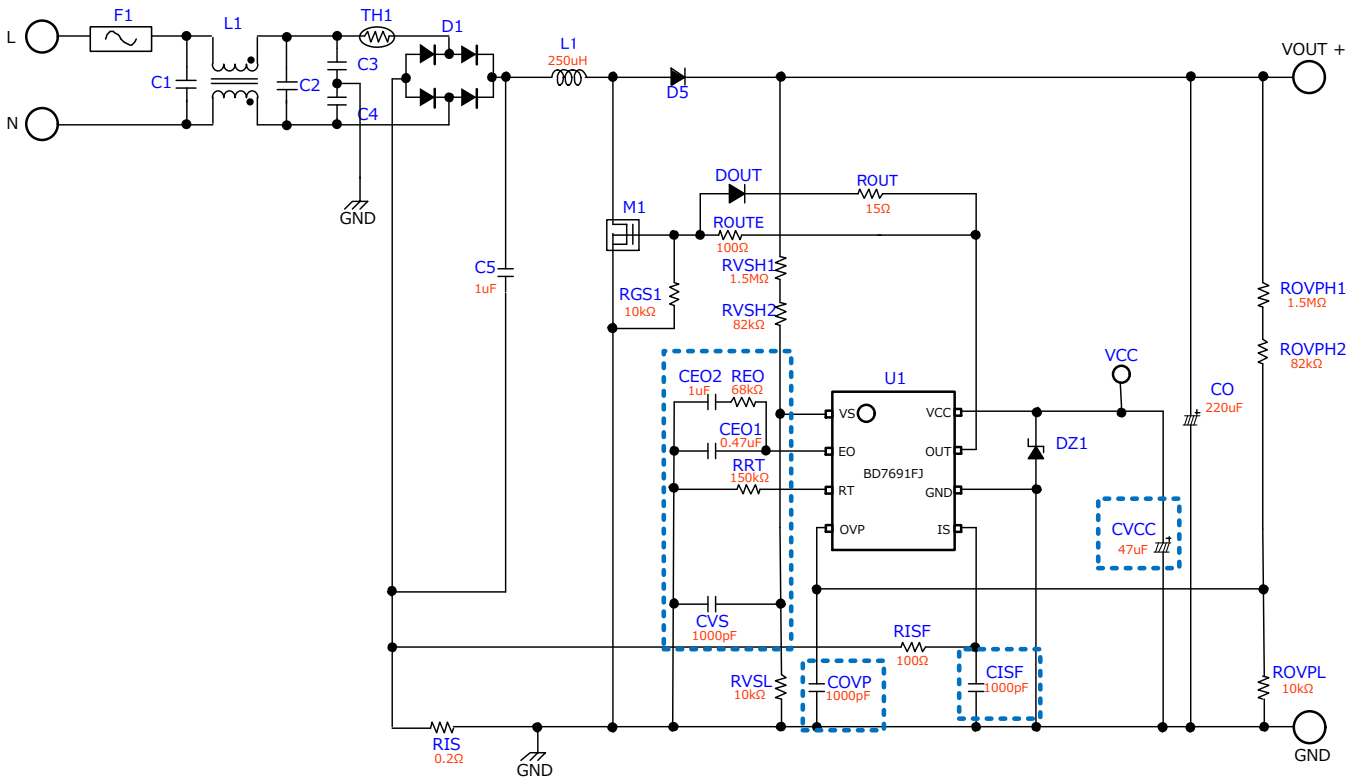


Figure 26. Parts placement

About GND wiring guidance
The red line of Fig.27 becomes the GND lines which large current flows. Each line independence wires it, and please wire it briefly and thickly. A blue line is ICGND. Please make a common use ICGND and GND of IC outskirts parts.

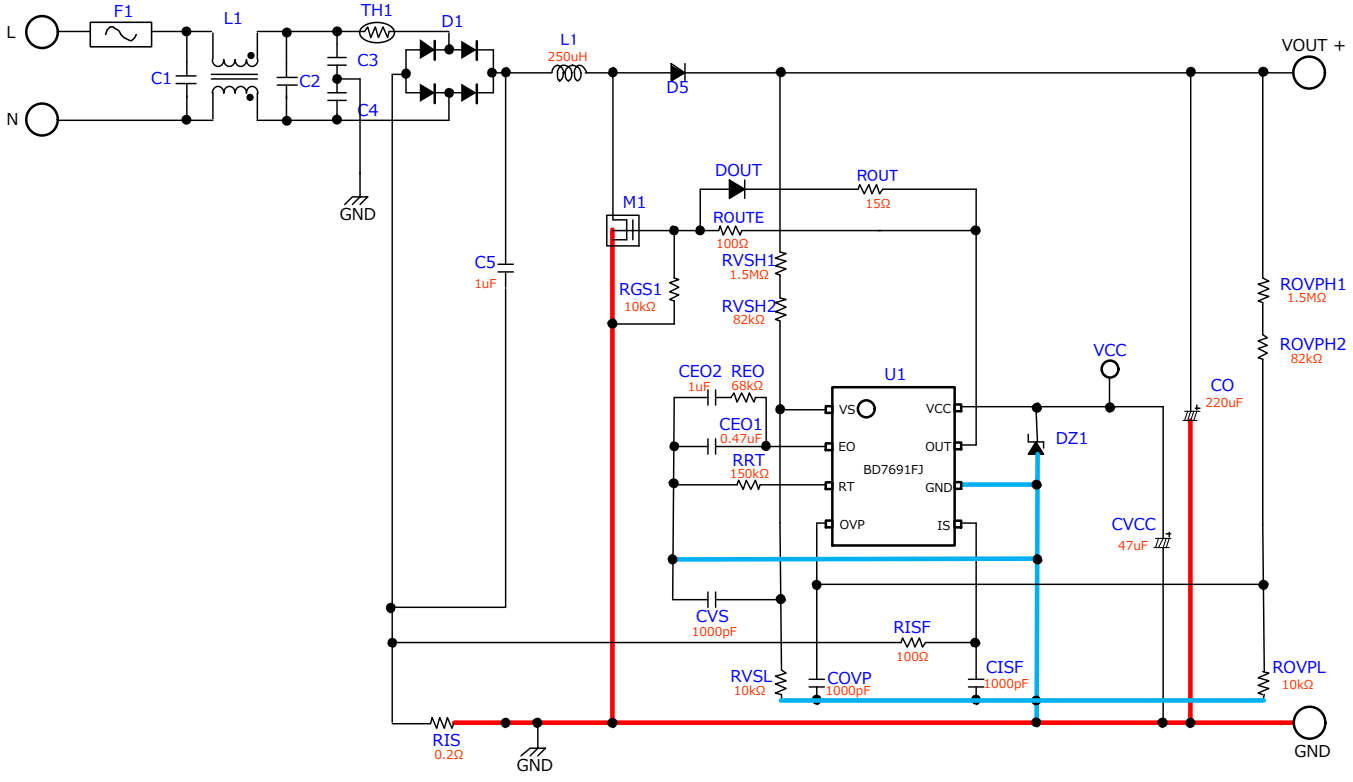


Figure 27. GND line layout

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About large current line

Large circuit current flows through the part of the red line of Fig.25. Please wire it briefly and thickly. Please do not place IC and high impedance line near red line. Because red line is very noisy.

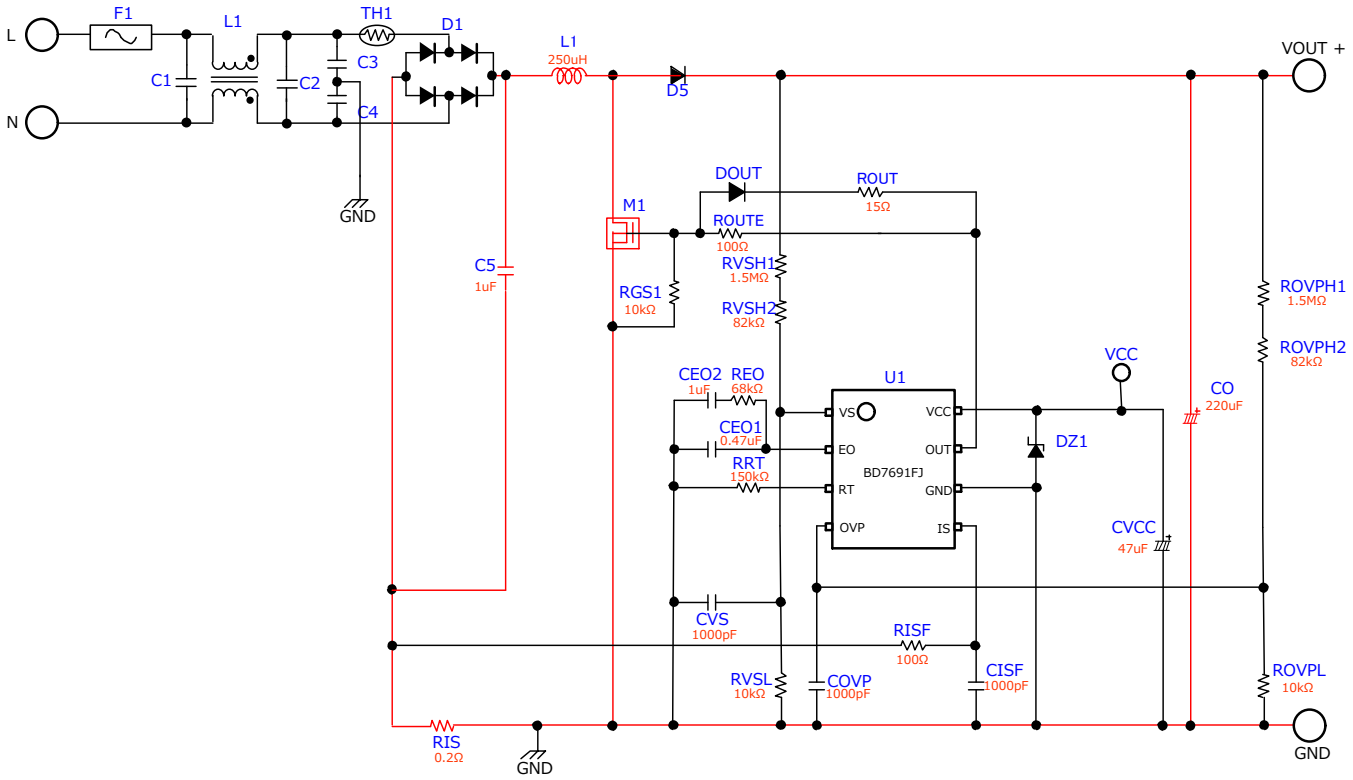


Figure 28. High current line layout

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Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

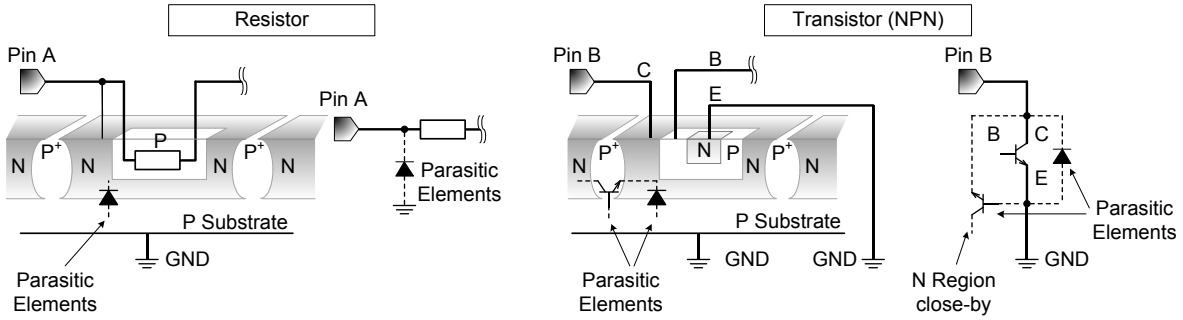


Figure xx. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

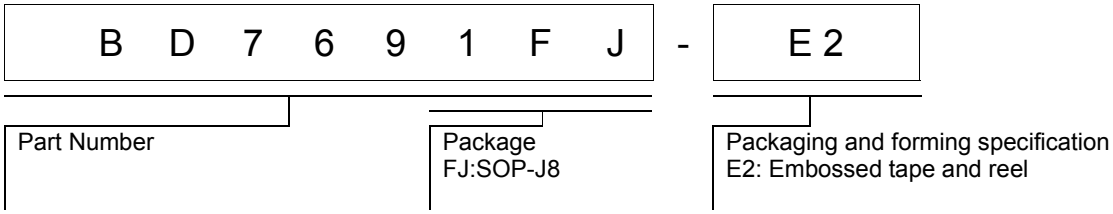
17. Disturbance light

In a device where a portion of silicon is exposed to light such as in a WL-CSP, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

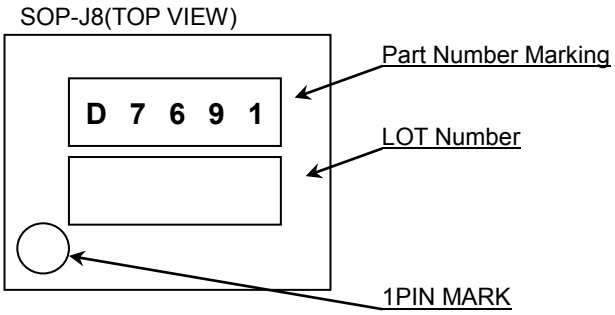
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Ordering Information



Marking Diagrams



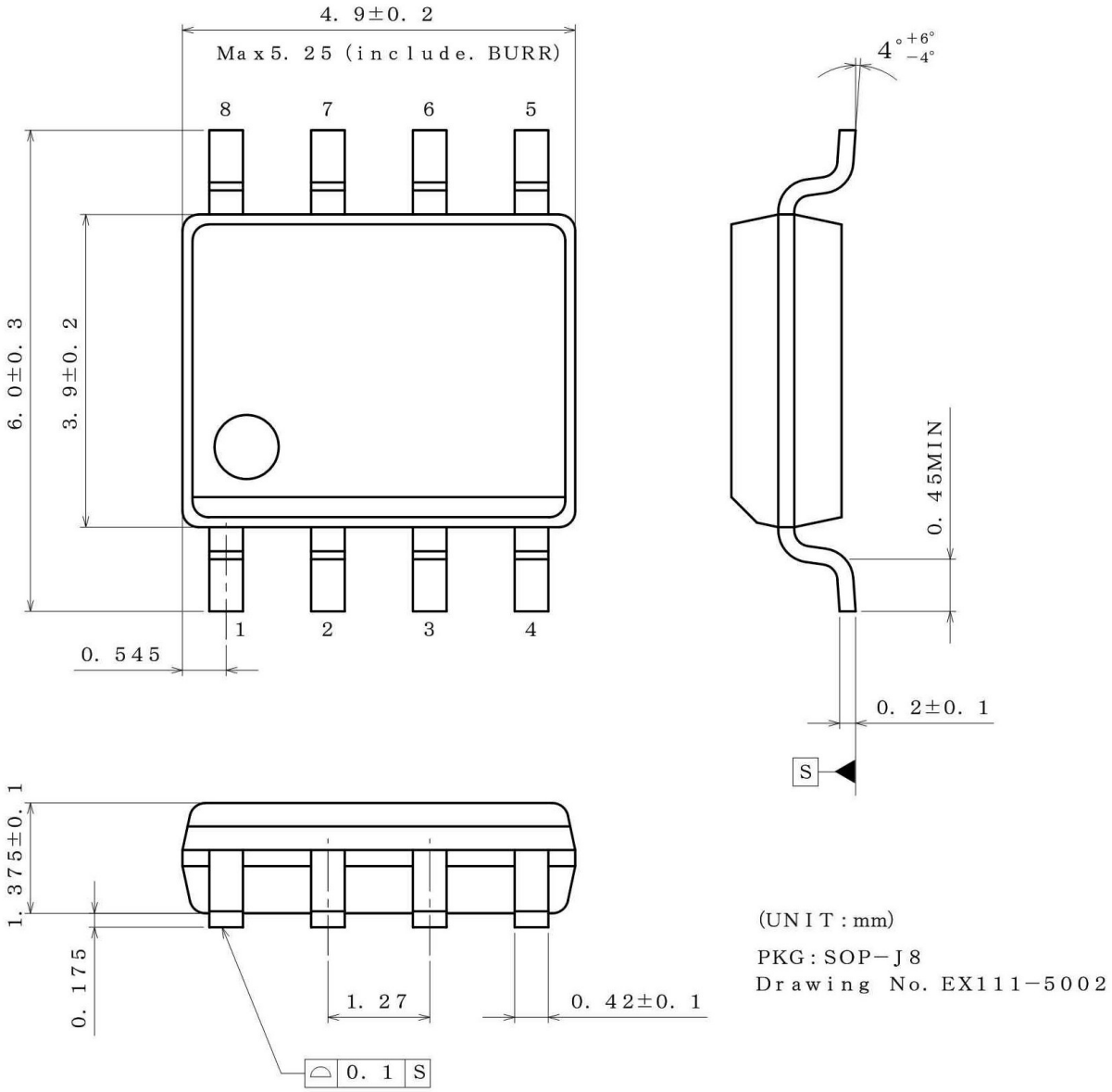
Part Number Marking	Package	Orderable Part Number
D7691	SOP-J8	BD7691FJ-E2

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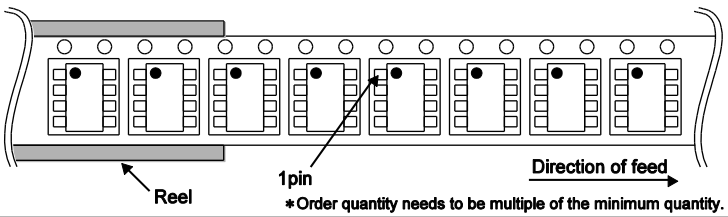
Physical Dimension, Tape and Reel Information

Package Name	SOP-J8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

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Revision History

Date	Revision	Changes
23. Jan. 2017	001	Release
9. May. 2017	002	p.10 Add IS pin maximum ratings p.11 Add electrical characteristics

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes

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