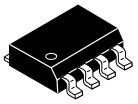
# Half-Bridge Gate Driver

# FL73282



SOIC8
CASE 751EB

## Description

The FL73282, a monolithic half bridge gate−drive IC, can drive MOSFETs and IGBTs that operate up to +900 V. **onsemi**'s high−voltage process and common mode noise canceling technique provides stable operation of the high−side driver under high−$dV_S/dt$ noise circumstances. An advanced level−shift circuit allows high−side gate driver operation up to $V_S$ = −9.8 V (typical) for $V_{BS}$ = 15 V. The UVLO circuits for both channels prevent malfunction when $V_{CC}$ or $V_{BS}$ is lower than the specified threshold voltage. Output drivers typically source/sink 350 mA / 650 mA, respectively, which is suitable for all kinds of half− and full−bridge inverters.

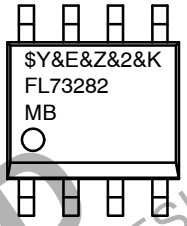
## Features

- Floating Channel for Bootstrap Operation to +900 V
- Typically 350 mA / 650 mA Sourcing/Sinking Current Driving Capability for Both Channels
- Common−Mode dv/dt Noise Canceling Circuit
- Extended Allowable Negative $V_S$ Swing to −9.8 V for Signal Propagation at $V_{CC}$ = $V_{BS}$ = 15 V
- $V_{CC}$ & $V_{BS}$ Supply Range from 10 V to 20 V
- UVLO Functions for Both Channels
- Matched Propagation Delay Below 50 ns
- Built−in 170 ns Dead−Time
- Output in Phase with Input Signal

## Applications

- Fluorescent Lamp Ballast
- HID Ballast
- SMPS
- Motor Driver
- General Purpose Half Bridge Topology

## MARKING DIAGRAM




FL73282MB = Device Code
$Y = **onsemi** Logo
&E = Designates Space
&Z = Assembly Plant Code
&2 = 2−Digit Date Code Format
&K = 2−Digits Lot Run Traceability Code

## ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

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## APPLICATION DIAGRAM

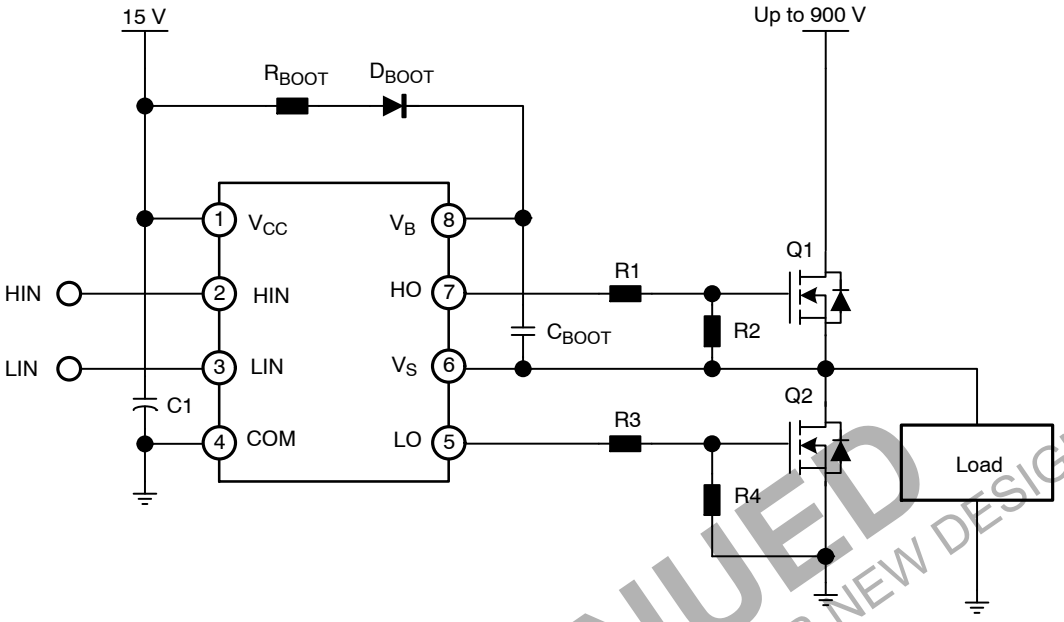



**Figure 1. Application Circuit for Half Bridge Topology**

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## BLOCK DIAGRAM

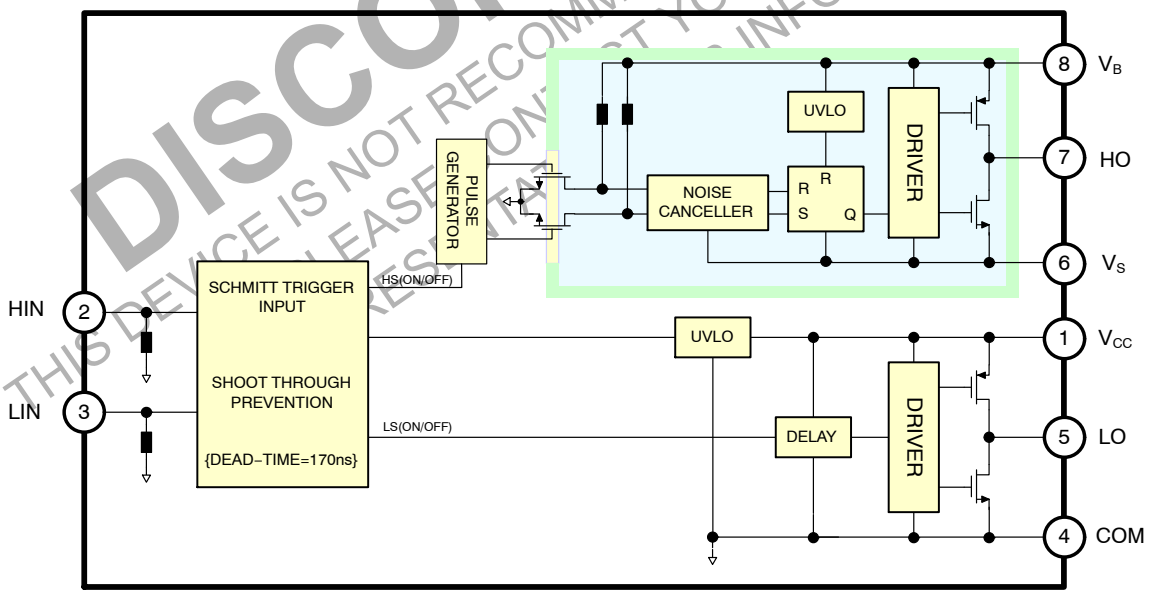



**Figure 2. Functional Block Diagram**



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## PIN CONFIGURATION

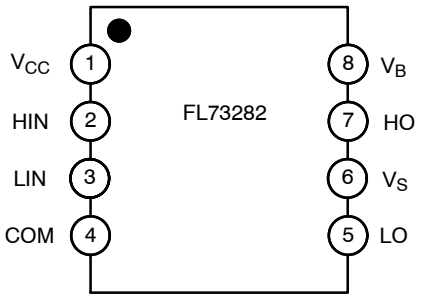



**Figure 3. Pin Assignments (Top View)**

### PIN DEFINITIONS

| Pin No. | Name | I/O | Description |
|---|---|---|---|
| 1 | $V_{CC}$ | I | Low−Side Supply Voltage |
| 2 | HIN | I | Logic Input for High−Side Gate Driver Output |
| 3 | LIN | I | Logic Input for Low−Side Gate Driver Output |
| 4 | COM | | Logic Ground and Low−Side Driver Return |
| 5 | LO | O | Low−Side Driver Output |
| 6 | $V_S$ | I | High−Voltage Floating Supply Return |
| 7 | HO | O | High−Side Driver Output |
| 8 | $V_B$ | I | High−Side Floating Supply |

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## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_S$ | High−Side Floating Offset Voltage | $V_B$−24 | $V_B$+0.3 | V |
| $V_B$ | High−Side Floating Supply Voltage | −0.3 | 924.0 | V |
| $V_{CC}$ | Low−Side and Logic−Fixed Supply Voltage | −0.3 | 24 | V |
| $V_{HO}$ | High−Side Floating Output Voltage $V_{HO}$ | $V_S$−0.3 | $V_B$+0.3 | V |
| $V_{LO}$ | Low−Side Floating Output Voltage $V_{LO}$ | −0.3 | $V_{CC}$+0.3 | V |
| $V_{IN}$ | Logic Input Voltage (HIN, LIN) | −0.3 | $V_{CC}$+0.3 | V |
| COM | Logic Ground | $V_{CC}$−24 | $V_{CC}$+0.3 | V |
| $dV_S/dt$ | Allowable Offset Voltage Slew Rate | − | ±50 | V/ns |
| $P_D$ | Power Dissipation (Notes 2, 3, 4) | − | 0.625 | W |
| $\theta_{JA}$ | Thermal Resistance | − | 200 | °C/W |
| $T_J$ | Junction Temperature | − | 150 | °C |
| $T_{STG}$ | Storage Temperature | −55 | 150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted on 76.2 x 114.3 x 1.6 mm PCB (FR−4 glass epoxy material).
2. Refer to the following standards:
   *JESD51−2: Integral circuit's thermal test method environmental conditions, natural convection;*
   *JESD51−3: Low effective thermal conductivity test board for leaded surface−mount packages.*
3. Do not exceed maximum power dissipation ($P_D$) under any circumstances.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_B$ | High−Side Floating Supply Voltage | $V_S$+10 | $V_S$+20 | V |
| $V_S$ | High−Side Floating Supply Offset Voltage | 6−$V_{CC}$ | 900 | V |
| $V_{HO}$ | High−Side (HO) Output Voltage | $V_S$ | $V_B$ | V |
| $V_{LO}$ | Low−Side (LO) Output Voltage | COM | $V_{CC}$ | V |
| $V_{IN}$ | Logic Input Voltage (HIN, LIN) | COM | $V_{CC}$ | V |
| $V_{CC}$ | Low−Side Supply Voltage | 10 | 20 | V |
| $T_A$ | Ambient Temperature | −40 | +125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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## STATIC ELECTRICAL CHARACTERISTICS

$V_{BIAS}(V_{CC}, V_{BS})$ = 15.0 V, $T_A$ = 25°C, unless otherwise specified. The $V_{IN}$ and $I_{IN}$ parameters are referenced to COM. The $V_O$ and $I_O$ parameters are referenced to $V_S$ and COM and are applicable to the respective outputs HO and LO.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **POWER SUPPLY SECTION** | | | | | | |
| $I_{QCC}$ | Quiescent $V_{CC}$ Supply Current | $V_{IN}$ = 0 V or 5 V | – | 80 | 180 | μA |
| $I_{QBS}$ | Quiescent $V_{BS}$ Supply Current | $V_{IN}$ = 0 V or 5 V | – | 50 | 120 | μA |
| $I_{PCC}$ | Operating $V_{CC}$ Supply Current | $f_{IN}$ = 20 kHz, rms value | – | – | 550 | μA |
| $I_{PBS}$ | Operating $V_{BS}$ Supply Current | $f_{IN}$ = 20 kHz, rms value | – | – | 600 | μA |
| $I_{LK}$ | Offset Supply Leakage Current | $V_B$ = $V_S$ = 900 V | – | – | 10 | μA |
| **BOOTSTRAPPED SUPPLY SECTION** | | | | | | |
| $V_{CCUV+}$ $V_{BSUV+}$ | $V_{CC}$ & $V_{BS}$ Supply Under−Voltage Positive going Threshold | | 8.2 | 9.2 | 10.0 | V |
| $V_{CCUV-}$ $V_{BSUV-}$ | $V_{CC}$ & $V_{BS}$ Supply Under−Voltage Negative going Threshold | | 7.6 | 8.7 | 9.6 | V |
| $V_{CCUVH}$ $V_{BSUVH}$ | $V_{CC}$ Supply Under−Voltage Lockout Hysteresis | | – | 0.5 | – | V |
| **INPUT SECTION** | | | | | | |
| $V_{IH}$ | Logic “1” Input Voltage | | 2.5 | – | – | V |
| $V_{IL}$ | Logic “0” Input Voltage | | – | – | 0.8 | V |
| $I_{IN+}$ | Logic “1” Input Bias Current | $V_{IN}$ = 5 V | – | 20 | 50 | μA |
| $I_{IN-}$ | Logic “0” Input Bias Current | $V_{IN}$ = 0 V | – | 1.0 | 2.0 | μA |
| $R_{IN}$ | Logic Input Pull−Down Resistance | | 100 | 250 | – | kΩ |
| **GATE DRIVER OUTPUT SECTION** | | | | | | |
| $V_{OH}$ | High−Level Output Voltage, $V_{BIAS-VO}$ | $I_O$ = 0 A | – | – | 85 | mV |
| $V_{OL}$ | Low−Level Output Voltage, $V_O$ | $I_O$ = 0 A | – | – | 85 | mV |
| $I_{O+}$ | Output HIGH Short−Circuit Pulsed Current | $V_O$ = 0 V, $V_{IN}$ = 5 V with PW ≤ 10 μs | 250 | 350 | – | mA |
| $I_{O-}$ | Output LOW Short−Circuit Pulsed Current | $V_O$ = 15 V, $V_{IN}$ = 0 V with PW ≤ 10 μs | 500 | 650 | – | mA |
| $V_S$ | Allowable Negative VS Pin Voltage for HIN Signal Propagation to HO | | – | −9.8 | −7.0 | V |

## DYNAMIC ELECTRICAL CHARACTERISTICS

$V_{BIAS}(V_{CC}, V_{BS})$ = 15.0 V, $V_S$ = COM, $C_L$ = 1000 pF and $T_A$ = 25°C, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{ON}$ | Turn−On Propagation Delay | $V_S$ = 0 V | 80 | 150 | 220 | ns |
| $t_{OFF}$ | Turn−Off Propagation Delay | $V_S$ = 0 V or 900 V (Note 4) | 80 | 150 | 220 | ns |
| $t_R$ | Turn−On Rise Time | $V_{LIN}$ = $V_{HIN}$ = 5 V | – | 60 | 140 | ns |
| $t_F$ | Turn−Off Fall Time | $V_{LIN}$ = $V_{HIN}$ = 0 V | – | 30 | 80 | ns |
| DT | Dead Time | | 70 | 170 | 270 | ns |
| MT | Delay Matching, HS & LS Turn−on/off | | – | – | 50 | ns |
| $t_{PW}$ | Minimum Input Pulse Width that Changes the Output (Notes 4, 5) | | – | – | 220 | ns |

4. These parameters are guaranteed by design.
5. The minimum input pulse width time included dead time.

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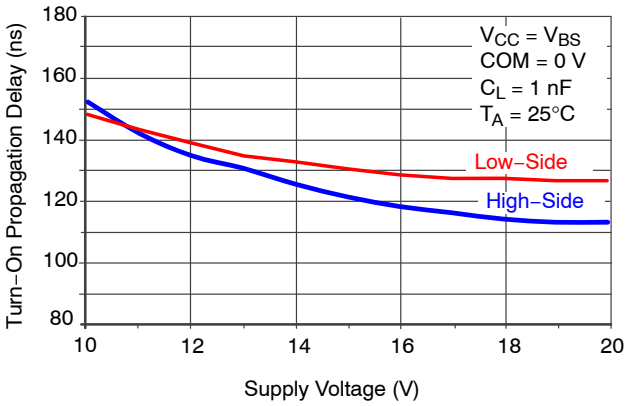



**Figure 4. Turn−On Propagation Delay vs. Supply Voltage**

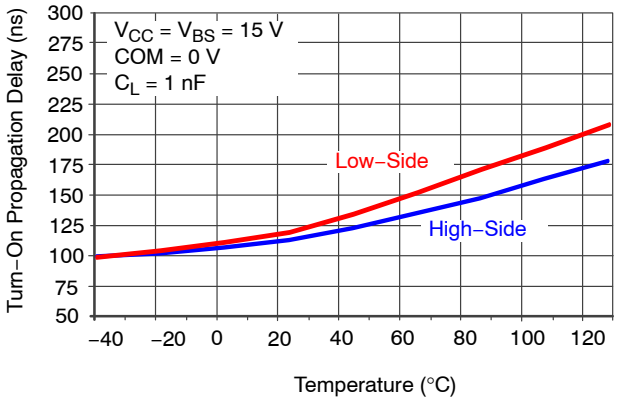



**Figure 5. Turn−On Propagation Delay vs. Temperature**

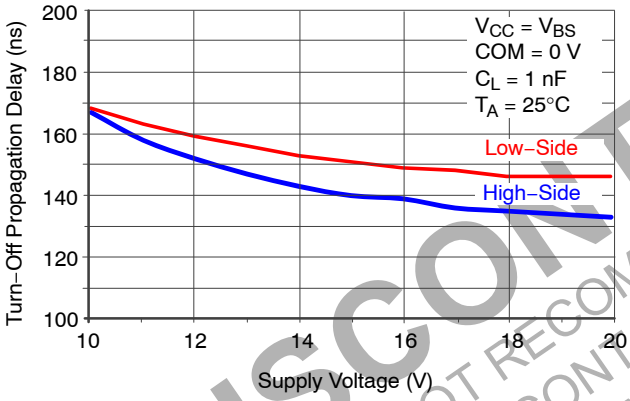



**Figure 6. Turn−Off Propagation Delay vs. Supply Voltage**

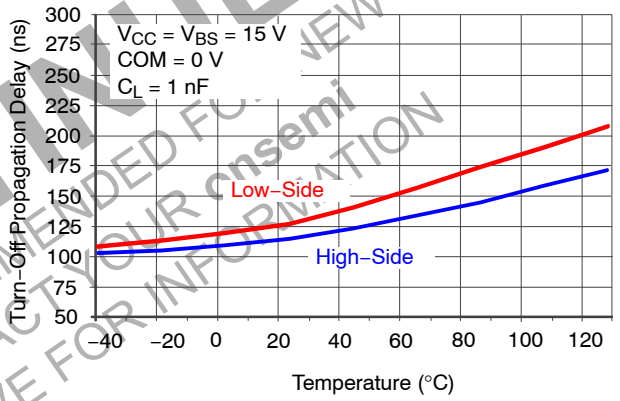



**Figure 7. Turn−Off Propagation Delay vs. Temperature**

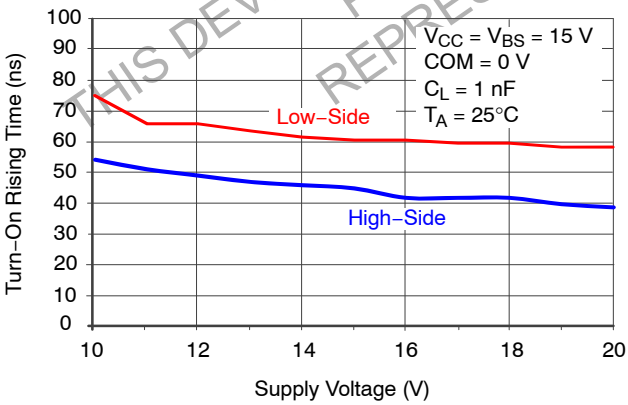



**Figure 8. Turn−On Rising Time vs. Supply Voltage**

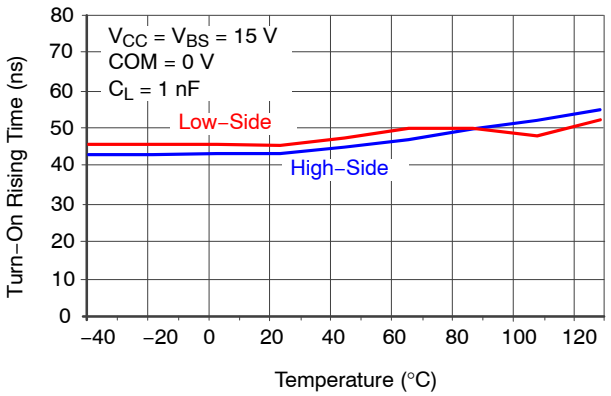



**Figure 9. Turn−On Rising Time vs. Temperature**

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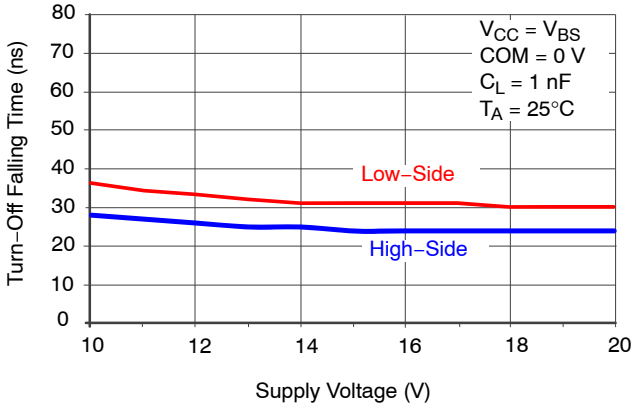



**Figure 10. Turn−Off Falling Time vs. Supply Voltage**

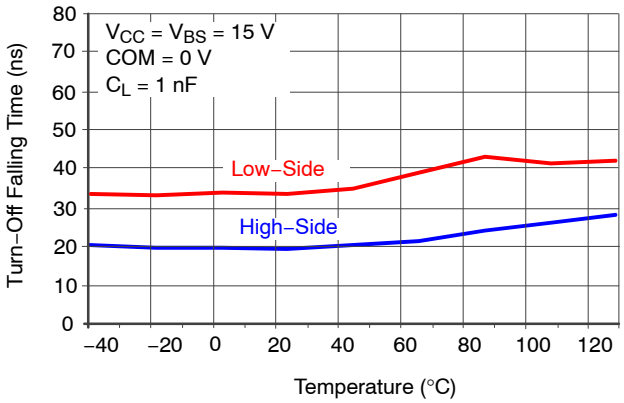



**Figure 11. Turn−Off Falling Time vs. Temperature**

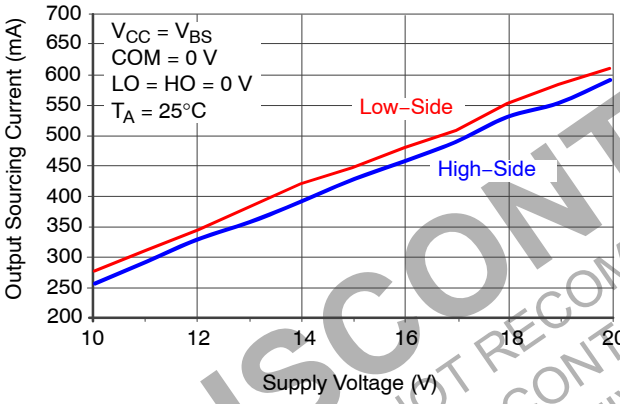



**Figure 12. Output Sourcing Current vs. Supply Voltage**

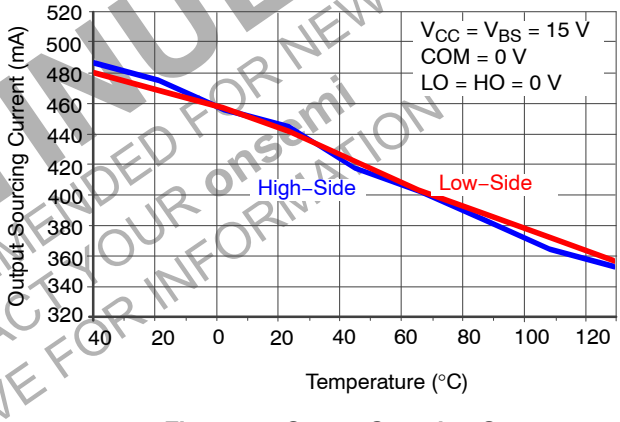



**Figure 13. Output Sourcing Current vs. Temperature**

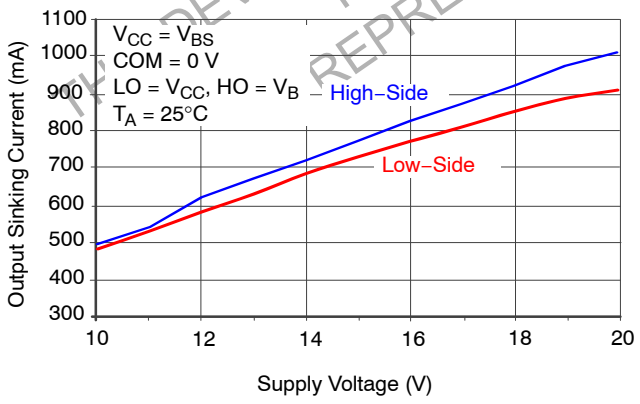



**Figure 14. Output Sinking Current vs. Supply Voltage**

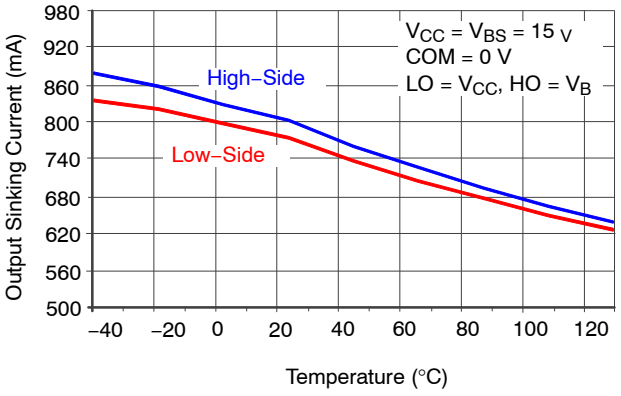



**Figure 15. Output Sinking Current vs. Temperature**

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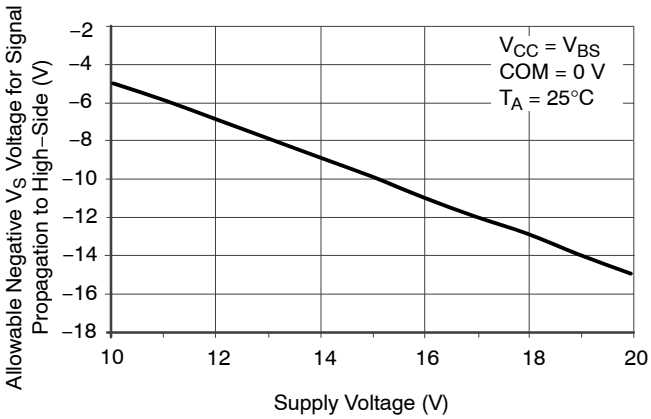



**Figure 16. Allowable Negative $V_S$ Voltage for Signal Propagation to High Side vs. Supply Voltage**

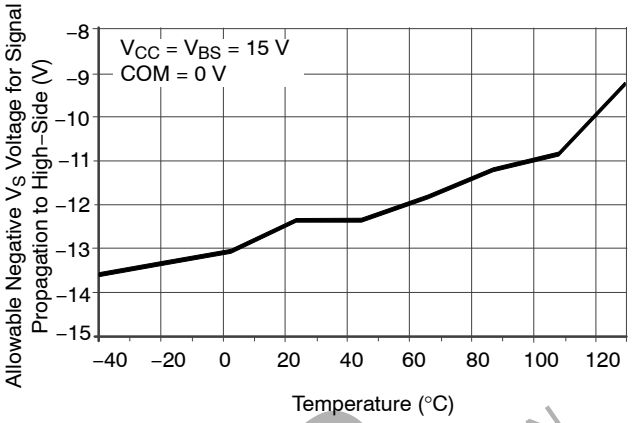



**Figure 17. Allowable Negative $V_S$ Voltage for Signal Propagation to High Side vs. Temperature**

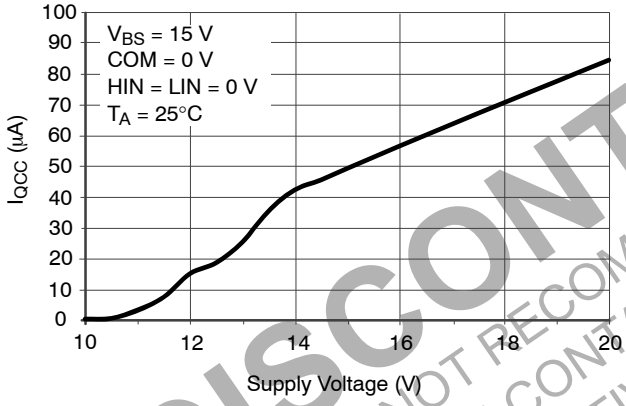



**Figure 18. $I_{QCC}$ vs. Supply Voltage**

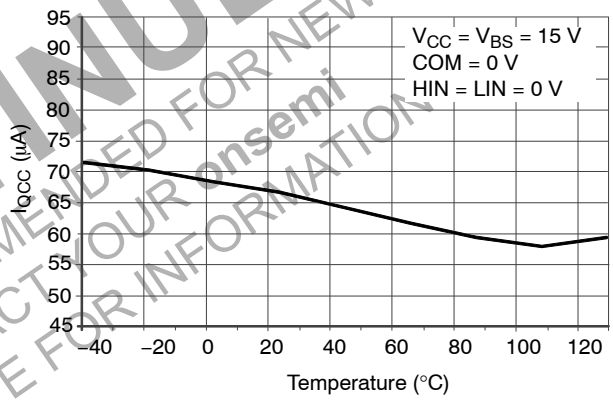



**Figure 19. $I_{QCC}$ vs. Temperature**

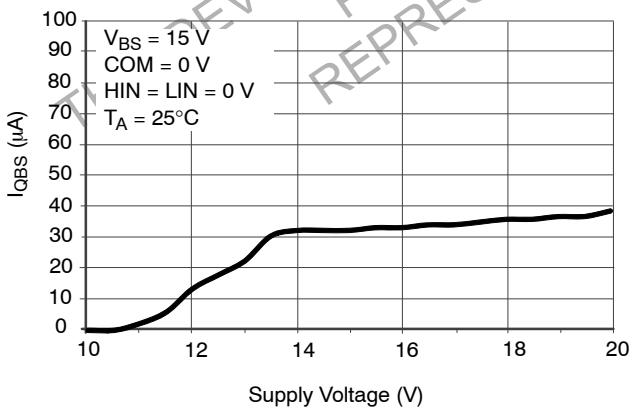



**Figure 20. $I_{QBS}$ vs. Supply Voltage**

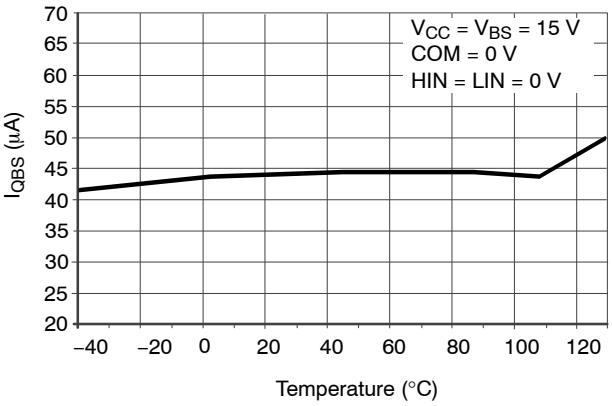



**Figure 21. $I_{QBS}$ vs. Temperature**

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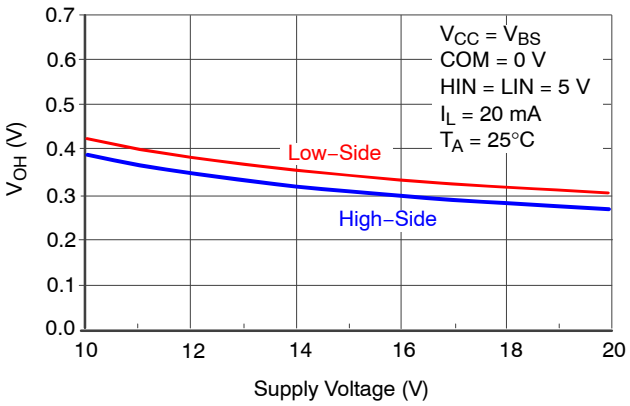



**Figure 22. High−Level Output Voltage vs. Supply Voltage**

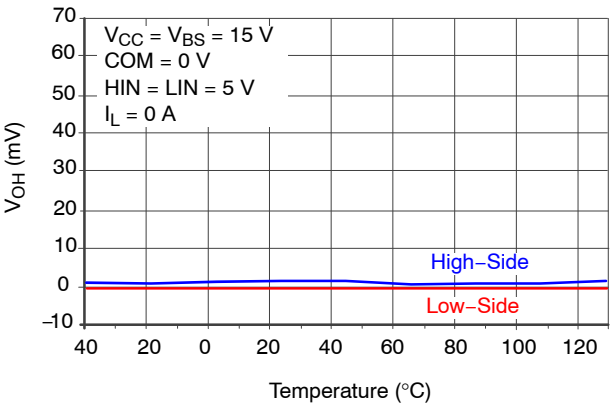



**Figure 23. High−Level Output Voltage vs. Temperature**

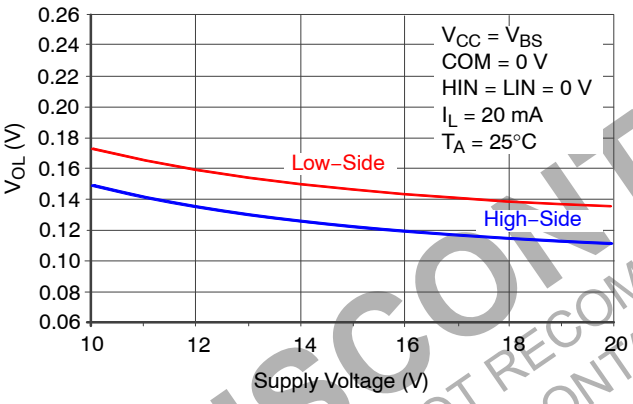



**Figure 24. Low−Level Output Voltage vs. Supply Voltage**

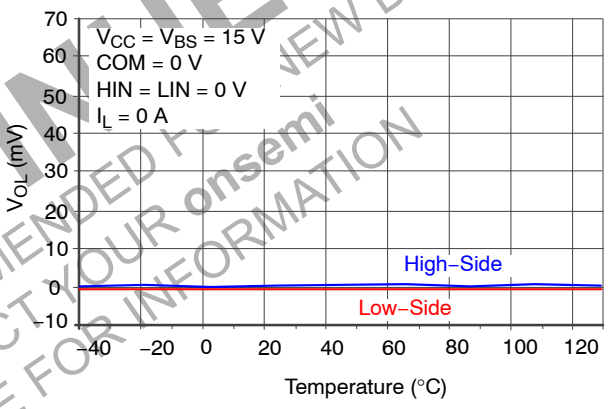



**Figure 25. Low−Level Output Voltage vs. Temperature**

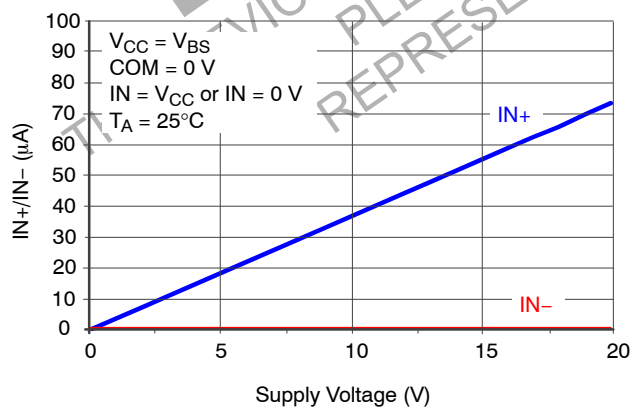



**Figure 26. Input Bias Current vs. Supply Voltage**

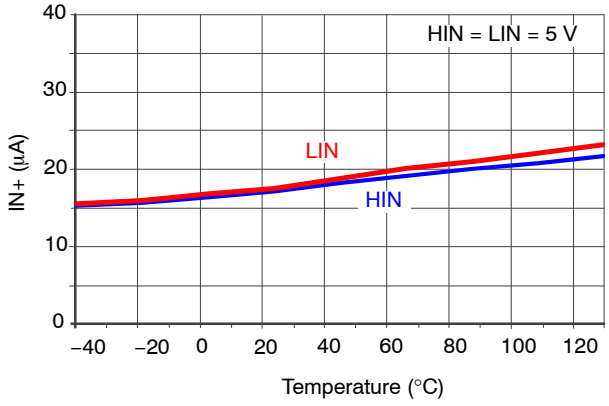



**Figure 27. Input Bias Current vs. Temperature**

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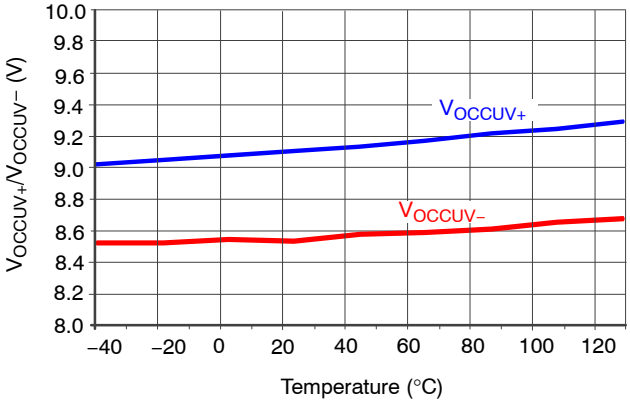



**Figure 28. $V_{CC}$ UVLO Threshold Voltage vs. Temperature**

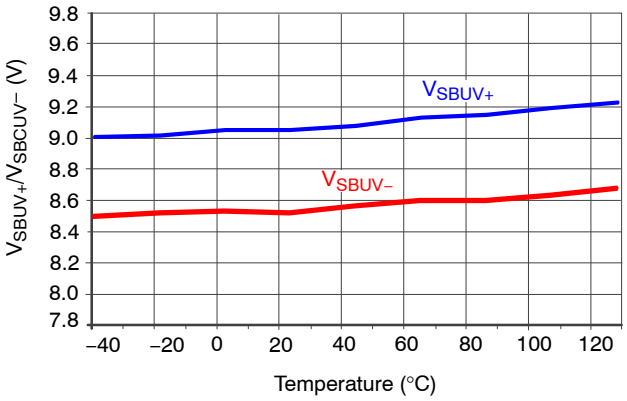



**Figure 29. $V_{BS}$ UVLO Threshold Voltage vs. Temperature**

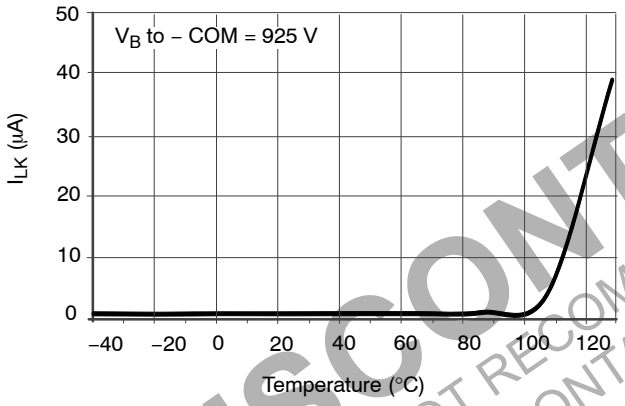



**Figure 30. $V_B$ to COM Leakage Current vs. Temperature**

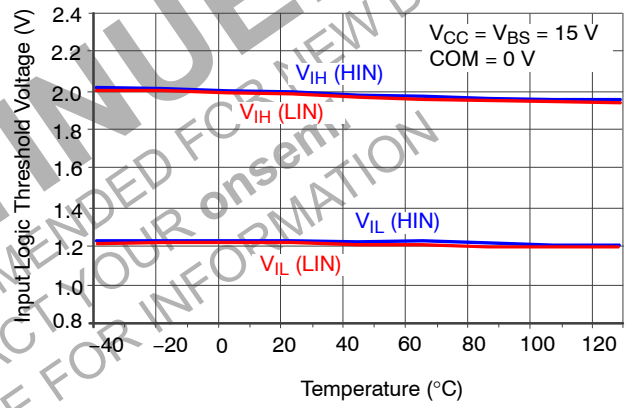



**Figure 31. Input Logic Threshold Voltage vs. Temperature**

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## SWITCHING TIME DEFINITIONS

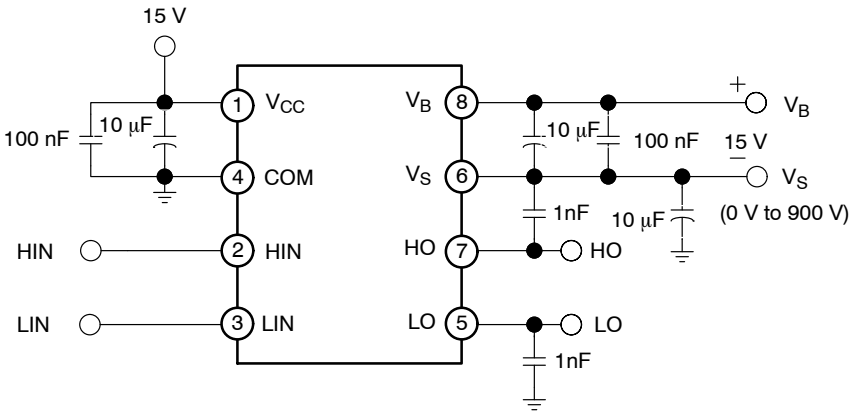



**Figure 32. Switching Time Test Circuit**

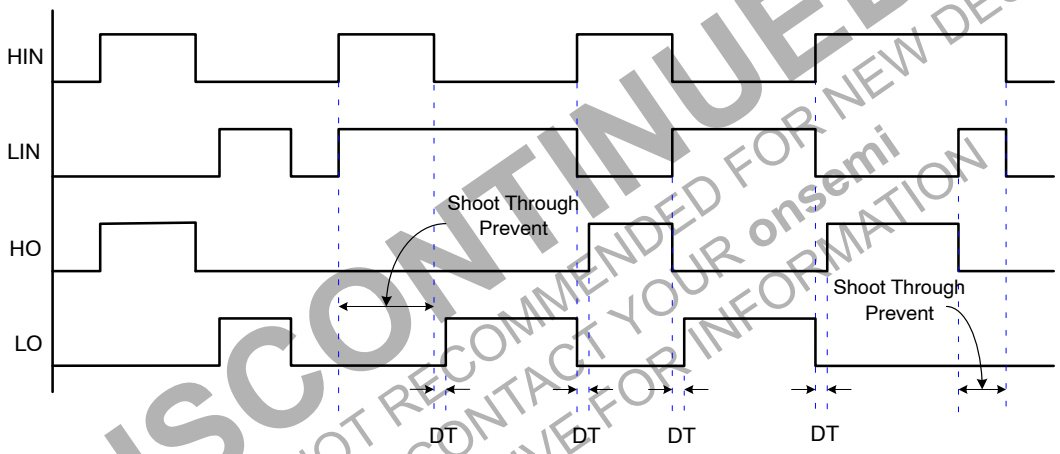



**Figure 33. Input / Output Timing Diagram**

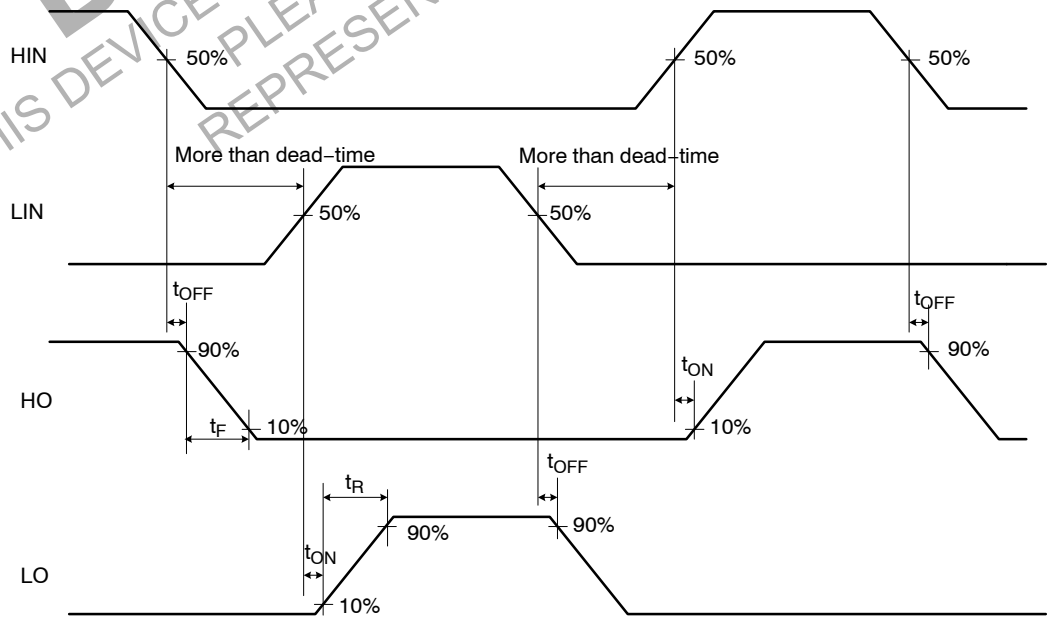


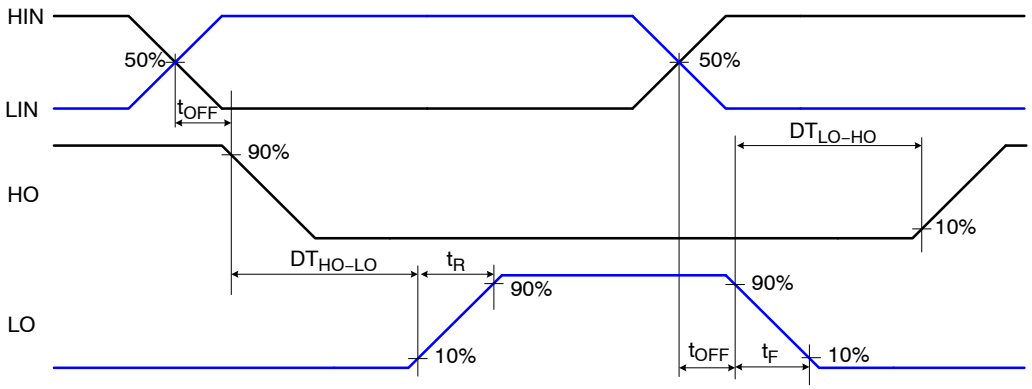

**Figure 34. Switching Time Definition**

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## SWITCHING TIME DEFINITIONS (continued)




$$MDT = |DT_{HO-LO} - DT_{LO-HO}|$$

**Figure 35. Internal Dead Time Definition**

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## ORDERING INFORMATION

| Part Number | Operating Temperature Range | Package | Shipping† |
|---|---|---|---|
| FL73282MX (Note 6) | −40°C to +125°C | 8−Lead, Small Outline Integrated Circuit, (SOIC), (Pb−Free) | 2500 / Tape & Reel |

6. These devices passed wave−soldering test by JESD22A−111.

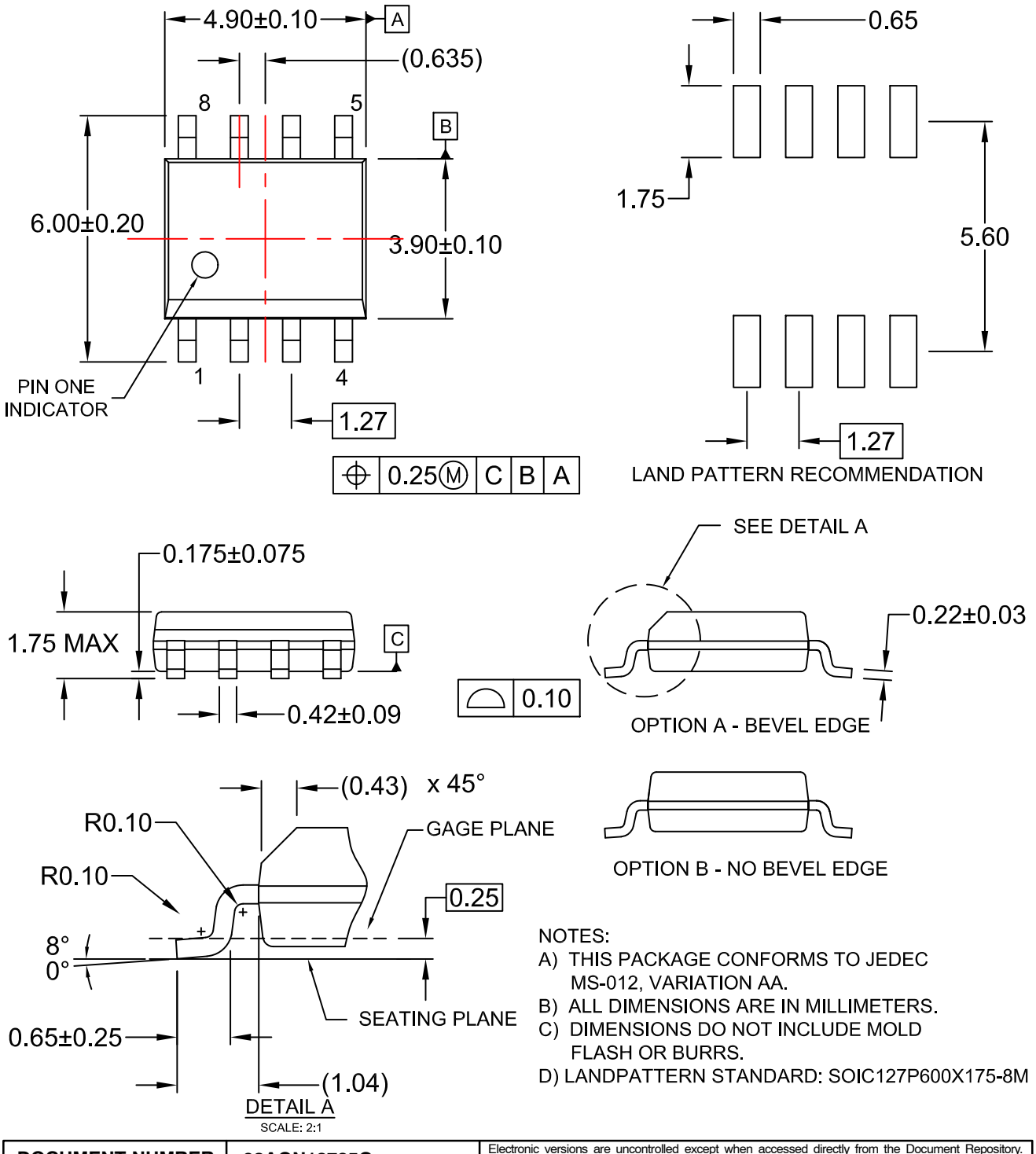
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**SOIC8**
CASE 751EB
ISSUE A

DATE 24 AUG 2017




NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

| | | | |
|---|---|---|---|
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