

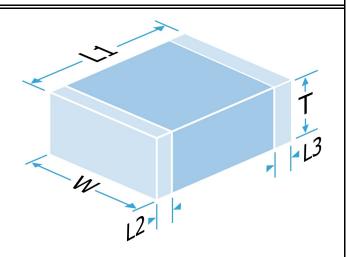
Multilayer Ceramic Chip Capacitor

Part Number: 222523K69P10BQTAF9LM

Description:

2225 3600Vdc / 2500Vac 30MHz 9.1pF ±0.10pF C0G - Hi Q/Low ESR Non-Mag (PME)

Ultra stable HighQ Low ESR multi-layer ceramic capacitors offering very stable 0±30ppm/°C, 0±15ppm/°C or +90±20ppm/°C High Q material systems that provide excellent low loss performance and guaranteed non-magnetic / relative permeability of 1.000 for critical applications such as NMR / MRI. Optimised for the lowest possible ESR and with maximised voltage ratings, this range provides the best possible conduction of high power RF signals.



Mechanical Specification

Size Code

Length (L1) in mm (")

Width (W) in mm (")

Thickness (T) in mm (")

Minimum Termination Band (L2,L3) in mm (")

Maximum Termination Band (L2,L3) in mm (")

Termination Material

Solderability

Packaging

2225

 $5.7 \pm 0.40 (0.225 \pm 0.016)$

 $6.30 \pm 0.40 (0.252 \pm 0.016)$

4.0 Max (0.157 Max)

0.25 (0.010)

1.00 (0.040)

Copper Barrier, Sn Plated Solder (Non-Mag., RoHS compliant)

IEC-60068-2-58

7" Reel Horizontal Orientation, 500 per reel

General Electrical Specification

Rated Voltage

Nominal Capacitance Value

Capacitance Tolerance

Tangent of Loss Angle (Tan δ)

Capacitance and Tan δ Test Conditions

Voltage Proof

(Voltage applied for 5 secs max. @ 50mA max. charge current)

Min Insulation Resistance (IR)

Dielectric Classification

Rated Temperature Range

Maximum Capacitance Change over Temperature Range

Climatic Category (IEC)
Ageing Characteristic

3600Vdc / 2500Vac 30MHz

9.1pF

±0.10pF

≤0.0014

1.0Vrms @ 1MHz

4320Vdc

100.00GOhm @ 100Vdc

C0G - Hi Q/Low ESR Non-Mag (PME)

-55°C / +125°C

No DC Voltage 0±30ppm/°C

Rated DC Voltage -

55/125/56

Zero

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This datasheet is for a standard item and is confirmed valid on the date generated, the latest published data for this part may differ and is available at http://www.knowlescapacitors.com or by contacting us.

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Date: Wednesday, March 31, 2021

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2225 3600Vdc / 2500Vac 30MHz 9.1pF ±0.10pF C0G - Hi Q/Low ESR Non-Mag

(PME)

Environmental

RoHS Compliant to 2011/65/EC as amended by 2015/863/EU

Compliant

REACH Compliant

209 compliant

California Proposition 65

No exposure risk

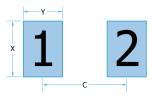
Board Layout

Knowles' conventional 2-terminal chip capacitors can generally be mounted using pad designs in accordance with international specification IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should be considered.

Some high voltage parts may require modifications to the board layout and/or the addition of a conformal coating to prevent flashover. Refer to application note AN0043 for further information.

IPC-7351 pad design

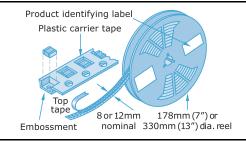
	2225	
С	5.20mm	0.205"
Υ	1.65mm	0.065"
X	6.70mm	0.264"



Packaging

Tape packaging information for tape-and-reel parts:

Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.



Soldering

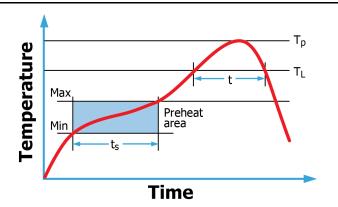
Reflow solder in accordance with IPC-A-610. Recommended reflow profile as laid down in IPC/JEDEC J-STD-020.

Wave soldering is also possible, but care must be taken for case sizes 1210 and larger and component thickness >1.0mm. Trials are encouraged.

Hand soldering is not recommended and can lead to component damage through thermal shock.

PdAg terminations are primarily intended for conductive epoxy attachment - they may be suitable for soldering but trials are recommended.

DLI



Application notes with mounting and handling guidance are available on request.

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