# MPQ4560-AEC1

**Industrial-Grade, 2A, 2MHz, 55V Step-Down Converter Available in AEC-Q100**

## DESCRIPTION

The MPQ4560 is a high-frequency, step-down, switching regulator with an integrated, high-side, high-voltage, power MOSFET. It provides a 2A output with current mode control for fast loop response and easy compensation.

The wide 3.8V-to-55V input range accommodates a variety of step-down applications, including those in automotive input environment. A 12µA shutdown mode supply current allows use in battery-powered applications.

High-power conversion efficiency over a wide load range is achieved by scaling down the switching frequency in light load conditions to reduce the switching and gate driving losses.

Frequency foldback prevents inductor current runaway during startup and thermal shutdown provides reliable, fault tolerant operation.

By switching at 2MHz, the MPQ4560 can prevent electromagnetic interference problems, such as those found in AM radio and ADSL applications.

The MPQ4560 is available in small 3mm x 3mm QFN10 and SOIC8E packages.

## FEATURES

- Guaranteed Industrial Automotive Temperature Range Limits
- Wide 3.8V-to-55V Operating Input Range
- 250mΩ Internal Power MOSFET
- Up to 2MHz Programmable Switching Frequency
- 140µA Quiescent Current
- Ceramic Capacitor Stable
- Internal Soft-Start
- Up to 95% Efficiency
- Output Adjustable from 0.8V to 52V
- Available in QFN10 (3mmx3mm) and SOIC8E Packages
- AEC-Q100 Qualified

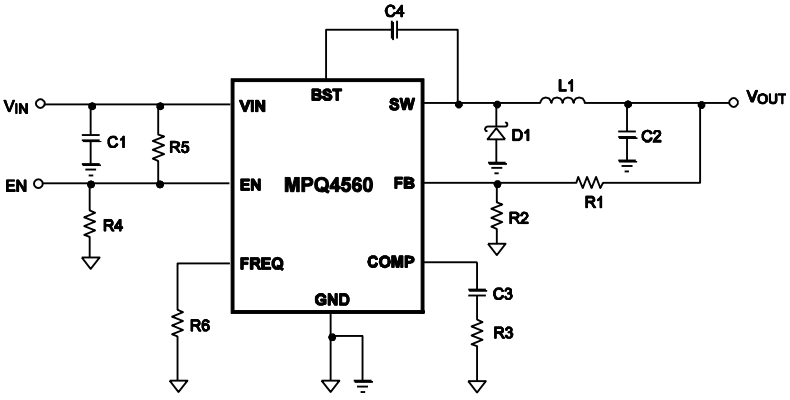
## APPLICATIONS

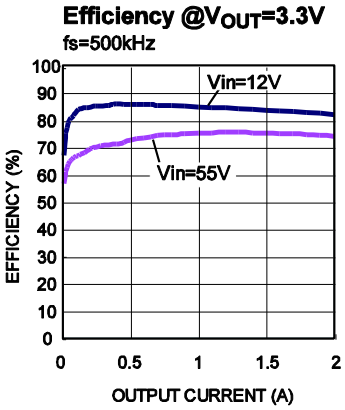
- High-Voltage Power Conversion
- Automotive Systems
- Industrial Power Systems
- Distributed Power Systems
- Battery Powered Systems

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## TYPICAL APPLICATION





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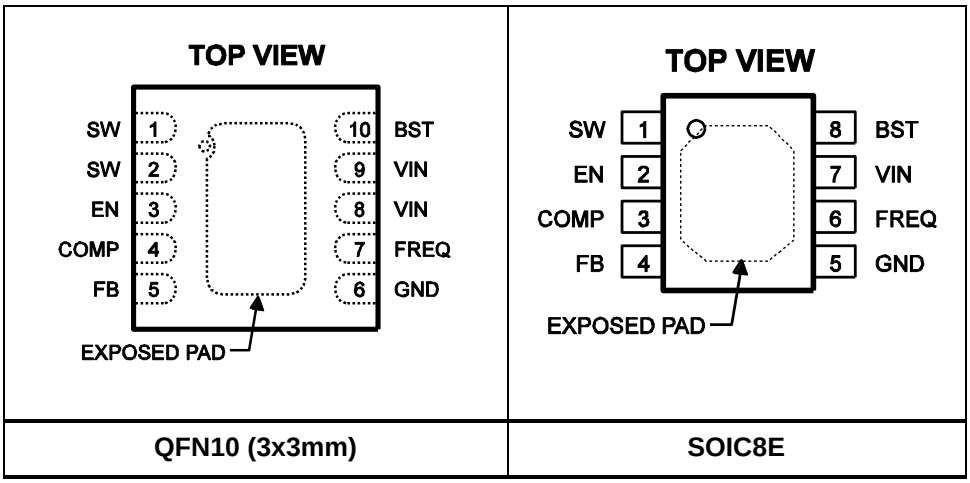
## ORDERING INFORMATION

| Part Number | Package | Top Marking | Junction Temperature ($T_J$) |
|---|---|---|---|
| MPQ4560DN* | SOIC8E | MP4560DN | –40°C to +125°C |
| MPQ4560DQ** | QFN10 (3×3mm) | T8 | |
| MPQ4560DN-AEC1 | SOIC8E | MP4560DN | |
| MPQ4560DQ-AEC1 | QFN10 (3×3mm) | T8 | |

* For Tape & Reel, add suffix –Z (e.g. MPQ4560DN-Z)
For RoHS Compliant Packaging, add suffix –LF, (e.g. MPQ4560DN-LF–Z)

** For Tape & Reel, add suffix –Z (e.g. MPQ4560DQ-Z)
For RoHS Compliant Packaging, add suffix –LF, (e.g. MPQ4560DQ-LF–Z)

## PACKAGE REFERENCE




QFN10 (3x3mm) | SOIC8E

## ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage ($V_{IN}$) ..... –0.3V to +60V
Switch Voltage ($V_{SW}$) ..... –0.5V to ($V_{IN}$ + 0.5V)
BST to SW ..... –0.3V to +5V
All Other Pins ..... –0.3V to +5V
Continuous Power Dissipation .....($T_J$ = 25°C)(2)
QFN10 (3×3mm) ..... 2.5W
SOIC8E ..... 2.5W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... –65°C to +150°C

## *Recommended Operating Conditions* (3)

Supply Voltage $V_{IN}$ ..... 3.8V to 55V
Output Voltage $V_{OUT}$ ..... 0.8V to 52V
Maximum Junction Temp. ($T_J$) ..... +125°C

## *Thermal Resistance* (4) $\theta_{JA}$ $\theta_{JC}$

QFN10 (3x3mm) ..... 50 ..... 12 ...°C/W
SOIC8E ..... 50 ..... 10 ...°C/W

**Notes:**

1) Exceeding these ratings may damage the device
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$(MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature TA. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$(MAX)=($T_J$(MAX)-$T_A$)/ $\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7 4-layer board.


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## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 12V, $V_{EN}$ = 2.5V, $V_{COMP}$ = 1.4V, $T_J$= –40°C to +125°C, unless otherwise noted. Typical Values are at $T_J$=25°C.**

| Parameter | Symbol | Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Feedback Voltage | $V_{FB}$ | 4.5V < $V_{IN}$ < 55V | $T_J$=25°C | 0.780 | 0.797 | 0.820 | V |
| | | | −40°C ≤ $T_J$ ≤85°C | 0.772 | | 0.829 | |
| | | | −40°C ≤ $T_J$ ≤125°C | 0.766 | | 0.829 | |
| Feedback Leakage Current | $I_{FB}$ | | | | 0.1 | 1.0 | µA |
| Upper Switch On Resistance (5) | $R_{DS(ON)}$ | $V_{BST}$ – $V_{SW}$ = 5V | $T_J$=25°C | 175 | 250 | 330 | mΩ |
| | | | | 160 | | 400 | |
| Upper Switch Leakage | $I_{SW}$ | $V_{EN}$ = 0V, $V_{SW}$ = 0V | | | 1 | | µA |
| Current Limit | $I_{LIM}$ | $T_J$=25°C | Duty Cycle ≤ 60% | 2.6 | 3.2 | 4.5 | A |
| | | | | 2.2 | | 4.7 | |
| COMP to Current Sense Transconductance (5) | $G_{CS}$ | | | | 5.7 | | A/V |
| Error Amp Voltage Gain (6) | | | | | 400 | | V/V |
| Error Amp Transconductance | | $I_{COMP}$ = ±3µA | | | 120 | | µA/V |
| Error Amp Min Source current | | $V_{FB}$ = 0.7V | | | 10 | | µA |
| Error Amp Min Sink current | | $V_{FB}$ = 0.9V | | | −10 | | µA |
| VIN UVLO Threshold | | $T_J$=25°C | | 2.7 | 3.0 | 3.3 | V |
| | | | | 2.4 | | 3.6 | |
| VIN UVLO Hysteresis | | | | | 0.35 | | V |
| Soft-Start Time (5) | | 0V < $V_{FB}$ < 0.8V | | 0.19 | 0.5 | | ms |
| Oscillator Frequency | $f_{SW}$ | $R_{FREQ}$ = 95kΩ | $T_J$=25°C | 0.8 | 1 | 1.2 | MHz |
| | | | | 0.7 | | 1.3 | |
| Shutdown Supply Current | $I_S$ | $V_{EN}$ < 0.3V | | | 12 | 20 | µA |
| Quiescent Supply Current | $I_Q$ | No load, $V_{FB}$ = 0.9V (no switching) | | | 140 | 200 | µA |
| Thermal Shutdown (5) | | Hysteresis = 20°C | | | 150 | | °C |
| Minimum Off Time (5) | $t_{OFF}$ | | | | 100 | | ns |
| Minimum On Time (5) | $t_{ON}$ | | | | 100 | | ns |
| EN Rising Threshold | | $T_J$=25°C | | 1.4 | 1.55 | 1.7 | V |
| | | | | 1.3 | | 1.8 | |
| EN Threshold Hysteresis | | | | | 320 | | mV |

**Note:**

5) Derived from bench characterization. Not tested in production.
6) Guaranteed by design. Not tested in production.


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## PIN FUNCTIONS

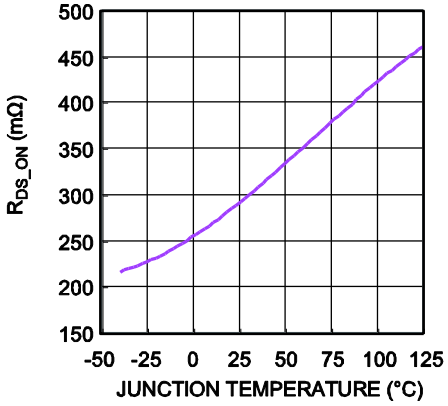
| QFN Pin # | SOIC8 Pin # | Name | Description |
|---|---|---|---|
| 1, 2 | 1 | SW | Switch Node. Output from the high-side switch. A low $V_F$ Schottky rectifier to ground is required. The rectifier must be close to the SW pins to reduce switching spikes. |
| 3 | 2 | EN | Enable Input. Pull this pin below the specified threshold to shutdown the chip. Pull it up above the specified threshold or leaving it floating to enable the chip. |
| 4 | 3 | COMP | Compensation. Output of the GM error amplifier. Control loop frequency compensation is applied to this pin. |
| 5 | 4 | FB | Feedback. Input to the error amplifier. Sets the regulator voltage by comparing the tap of an external resistive divider connected between the output and GND to the internal +0.8V reference. |
| 6 | 5 | GND, Exposed pad | Ground. Connect as close as possible to the output capacitor and avoid the high-current switch paths. Connect exposed pad to GND plane for optimal thermal performance. |
| 7 | 6 | FREQ | Switching Frequency Program Input. Connect a resistor from this pin to ground to set the switching frequency. |
| 8, 9 | 7 | VIN | Input Supply. This supplies power to all the internal control circuitry, both BS regulators, and the high-side switch. Place a decoupling capacitor to ground close to this pin to minimize switching spikes. |
| 10 | 8 | BST | Bootstrap. Positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor between this pin and SW pin. |


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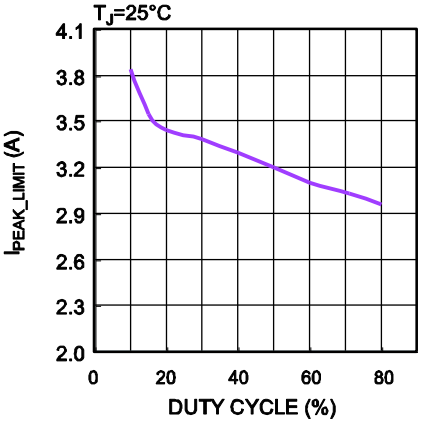
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## TYPICAL CHARACTERISTICS

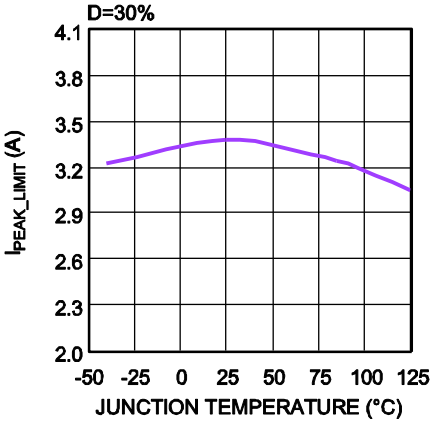
**On Resistance vs. Junction Temperature**



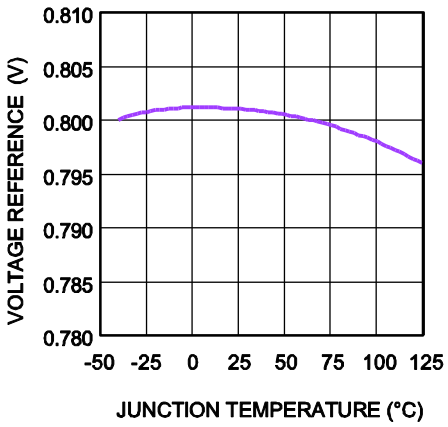

**Current Limit vs. Duty Cycle**



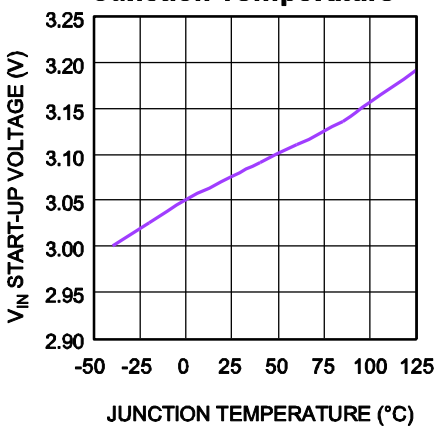

**Current Limit vs. Junction Temperature**



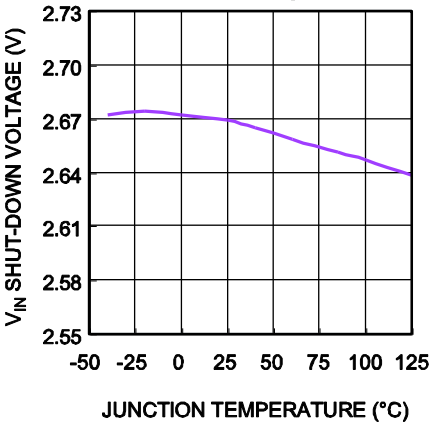

**Voltage Reference vs. Junction Temperature**



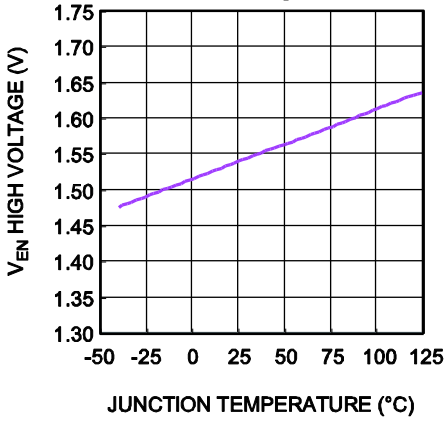

**$V_{IN}$ Start-up vs. Junction Temperature**



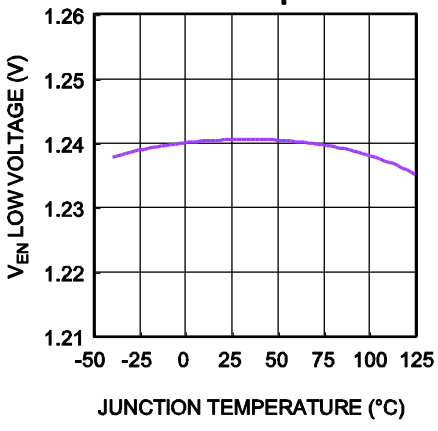

**$V_{IN}$ Shut-down vs. Junction Temperature**



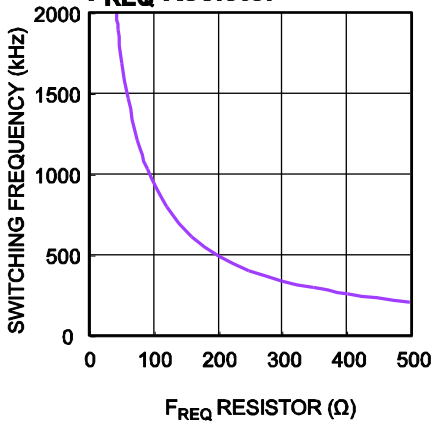

**Venable-high vs. Junction Temperature**




**Venable-low vs. Junction Temperature**




**Frequency vs. $F_{REQ}$ Resistor**





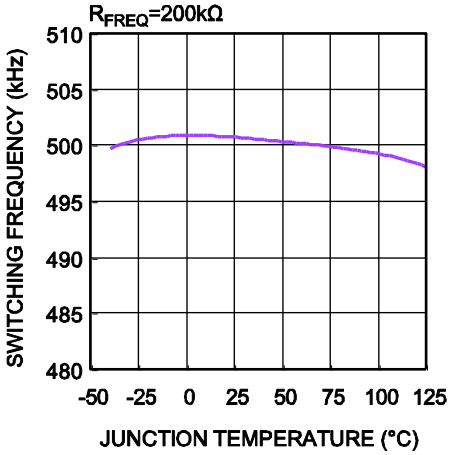
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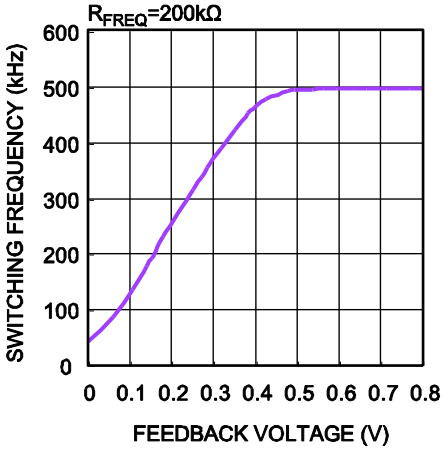
**Frequency vs. Junction Temperature**

$R_{FREQ}$=200kΩ



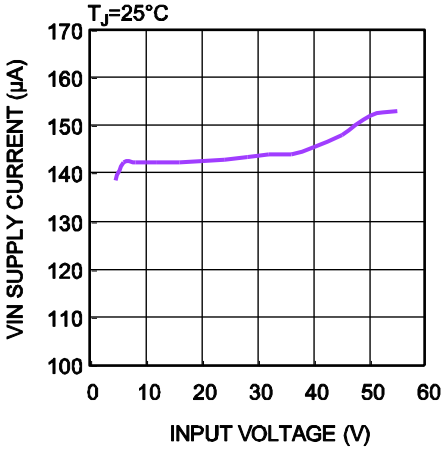

**Frequency vs. Feedback Voltage**

$R_{FREQ}$=200kΩ



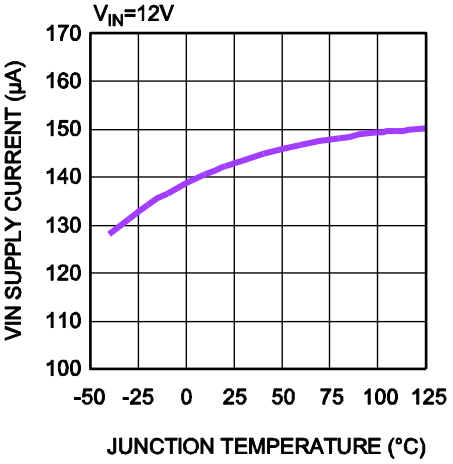

**$V_{IN}$ Quiescent Current vs. Input Voltage**

$T_J$=25°C



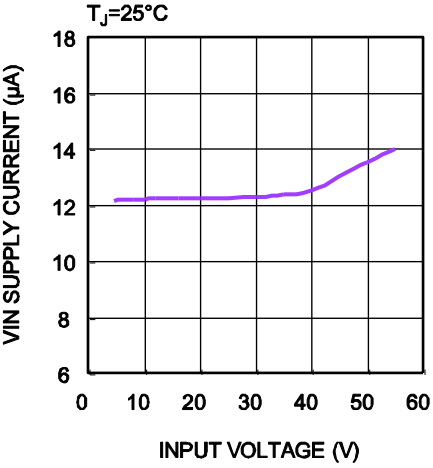

**$V_{IN}$ Quiescent Current vs. Junction Temperature**

$V_{IN}$=12V



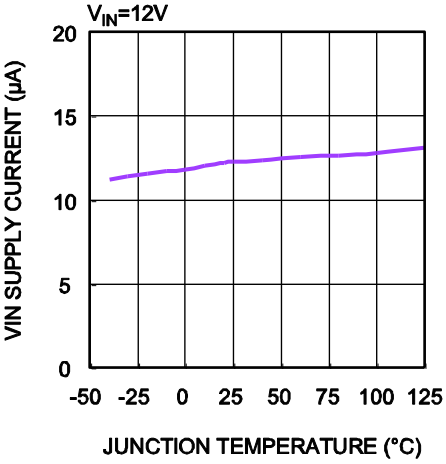

**Shutdown Current vs. Input Voltage**

$T_J$=25°C




**Shutdown Current vs. Junction Temperature**

$V_{IN}$=12V





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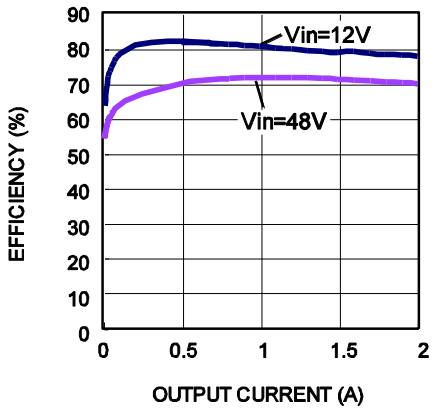
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## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{IN}$ = 12V, $V_{OUT}$ =3.3V, C1 = 4.7µF, C2 = 22µF, L1 = 10µH and $T_A$ = 25°C, unless otherwise noted.**

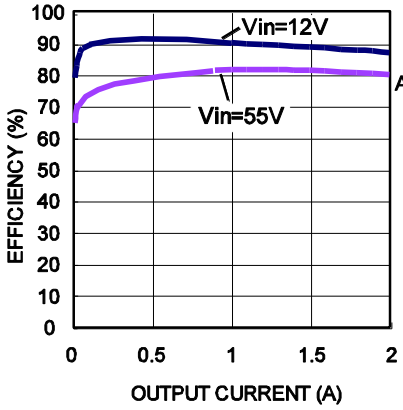
**Efficiency @$V_{OUT}$=2.5V**

L1=10uH, fs=500kHz



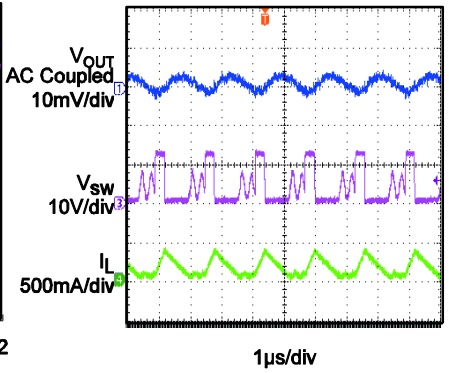

**Efficiency @$V_{OUT}$=5V**

L1=15uH, fs=500kHz



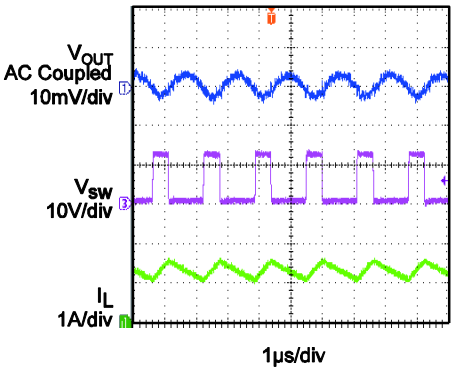

**Output Voltage Ripple**

$I_{OUT}$=0.1A



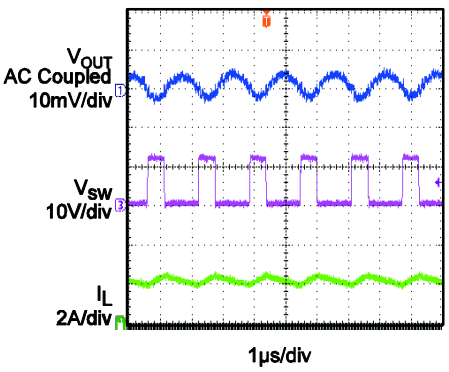

**Output Voltage Ripple**

$I_{OUT}$=1A




**Output Voltage Ripple**

$I_{OUT}$=2A





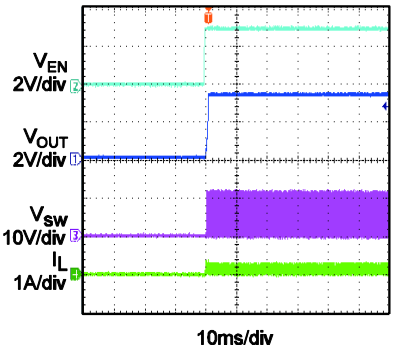
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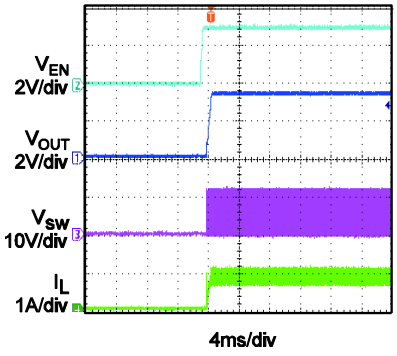
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $V_{OUT}$ =3.3V, C1 = 4.7µF, C2 = 22µF, L1 = 10µH and $T_A$ = 25°C, unless otherwise noted.**

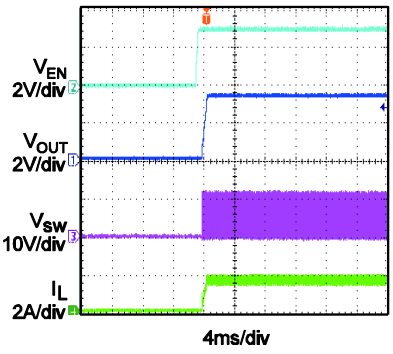
**Start up**
$I_{OUT}$=0.1A



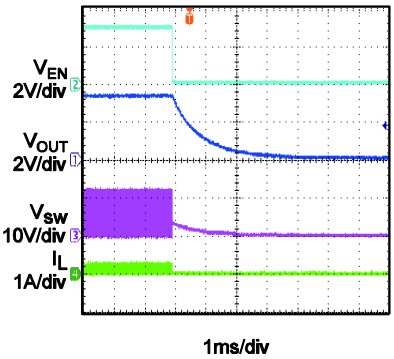

**Start up**
$I_{OUT}$=1A



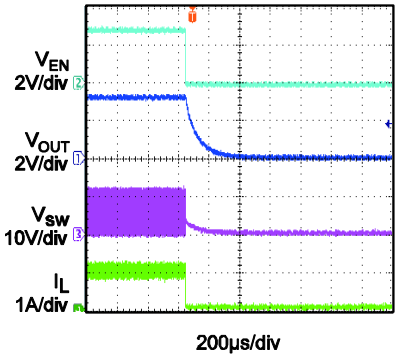

**Start up**
$I_{OUT}$=2A



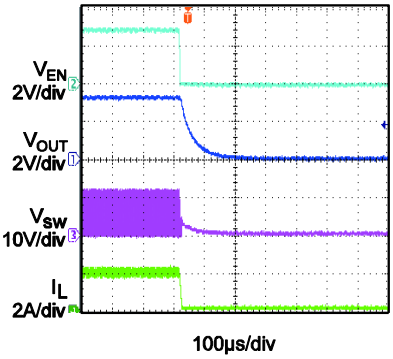

**Shut down**
$I_{OUT}$=0.1A



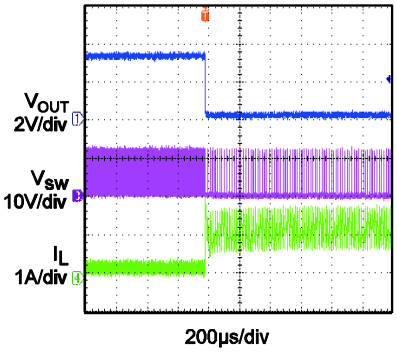

**Shut down**
$I_{OUT}$=1A



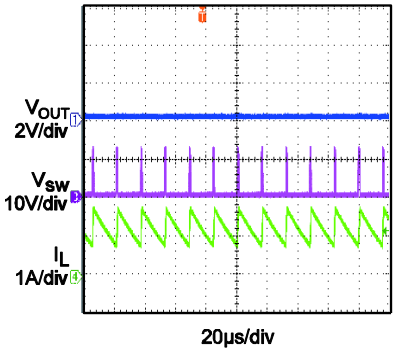

**Shut down**
$I_{OUT}$=2A



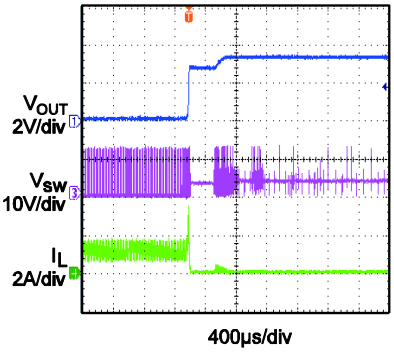

**Short Circuit Entry**
$I_{OUT}$=0.1A to Short




**Short Circuit Steady State**




**Short Circuit Recovery**
$I_{OUT}$=Short to 0A





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## BLOCK DIAGRAM

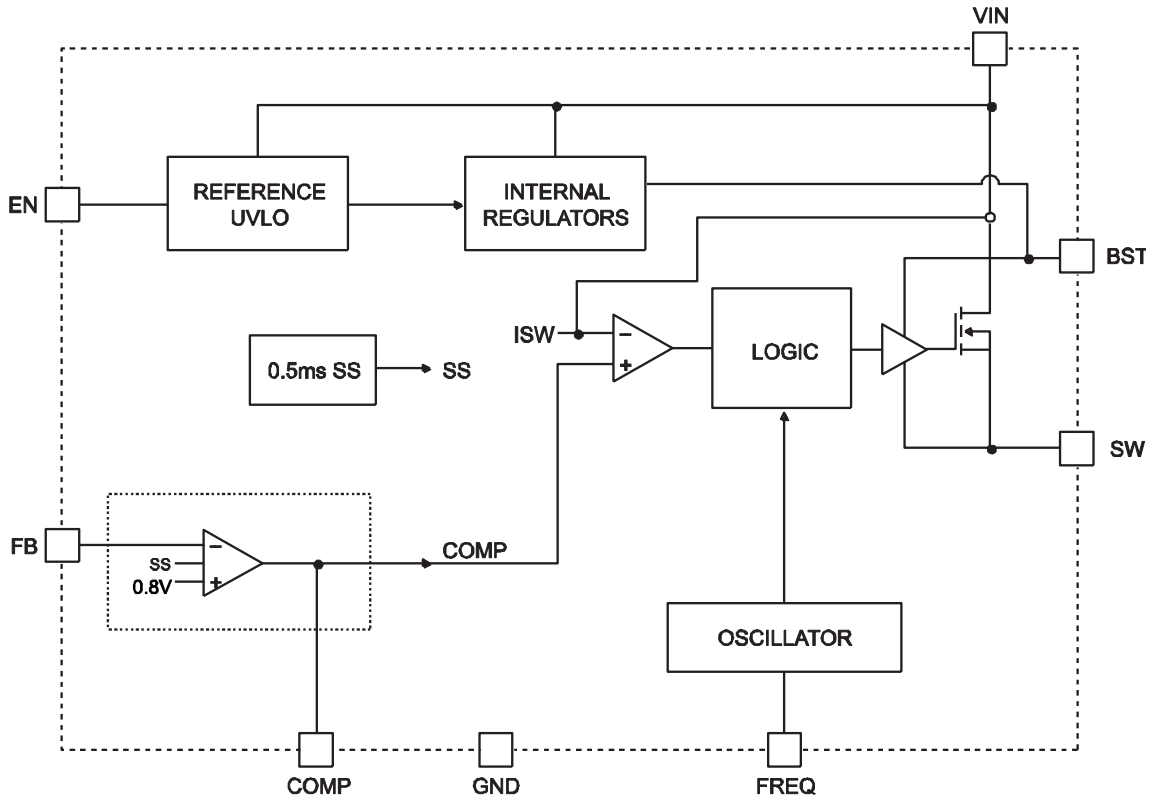



**Figure 1: Functional Block Diagram**


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## OPERATION

The MPQ4560 is an asynchronous, step-down, switching regulator with an integrated high-side, high-voltage, power MOSFET and a programmable frequency. It provides a single highly-efficient solution with current-mode control for fast loop response and easy compensation. It features a wide input voltage range, internal soft-start control, and precise current limiting. Its very low operational quiescent current makes it suitable for battery-powered applications.

### PWM Control

The MPQ4560 operates in a fixed-frequency, peak-current-control mode to regulate the output voltage at moderate-to-high output current. The internal clock initiates a PWM cycle. The power MOSFET turns ON and remains ON until its current reaches the value set by the COMP voltage. When the power switch is OFF, it remains OFF for at least 100ns before the next cycle starts. If the current in the power MOSFET does not reach the COMP-set current value within one PWM period, the power MOSFET remains ON, saving a turn-off operation.

### Pulse-Skipping Mode

Under light-load condition the switching frequency stretches the zero-voltage period to reduce the switching loss and driving loss.

### Error Amplifier

The error amplifier compares the FB pin voltage ($V_{FB}$) to the internal reference ($V_{REF}$) and outputs a current proportional to the difference. This output current charges the external compensation network to form $V_{COMP}$, which controls the power MOSFET current.

During operation, the minimum $V_{COMP}$ is clamped to 0.9V and its maximum is clamped to 2.0V. COMP is internally pulled down to GND in shutdown mode. Do not pull $V_{COMP}$ above 2.6V.

### Internal Regulator

An internal 2.6V regulator powers most of the internal circuits. This regulator takes the VIN input and operates in the full $V_{IN}$ range. When $V_{IN}$ exceeds 3.0V, the output of the regulator is in full regulation. When $V_{IN}$ is less than 3.0V, the output decreases.

### Enable Control

The MPQ4560 has a dedicated enable control pin (EN) that can enable or disable the chip when the input voltage exceeds an upper threshold. Its falling threshold (turn-off) is 1.2V, and its rising threshold (turn-on) is 1.5V (300mV higher).

When floating, an internal 1μA current source pulls EN up to ~3.0V to enable the chip. Pull-down requires a 1μA current.

When EN is pulled below 1.2V, the chip enters its lowest shutdown current mode. When EN exceeds 0V but remains lower than its rising threshold, the chip remains in shutdown mode but the shutdown current increases slightly.

### Under-Voltage Lockout

Under-voltage lockout (UVLO) protects the chip from operating at insufficient supply voltage. The UVLO rising threshold is about 3.0V while its falling threshold is a consistent 2.6V.

### Internal Soft-Start

Soft-start prevents the converter output voltage from overshooting during startup and short-circuit recovery. When the chip starts, the internal circuit generates a soft-start voltage (SS) ramping up from 0V to 2.6V. When it is less than the $V_{REF}$, SS overrides $V_{REF}$ so the error amplifier uses SS as the reference. When SS exceeds $V_{REF}$, $V_{REF}$ regains control.

### Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds its upper threshold, the whole chip shuts down. When the temperature is less than its lower threshold, the chip is enabled again.

### Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The driver's UVLO is soft-start related: When the bootstrap voltage hits its UVLO threshold, the soft-start circuit resets. To prevent noise, there is 20μs delay before the reset action. When bootstrap UVLO is gone, the reset is off and then the soft-start process resumes.

The dedicated internal bootstrap regulator regulates and charges the bootstrap capacitor to


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~5V. When the voltage between the BST and SW nodes is less than its regulation, a PMOS pass transistor from VIN to BST turns ON. The charging current path is from VIN, BST and then to SW. An external circuit must provide enough voltage headroom to facilitate charging.

As long as $V_{IN}$ is sufficiently higher than $V_{SW}$, the bootstrap capacitor can charge. When the power MOSFET is ON, $V_{IN} \approx V_{SW}$ so the bootstrap capacitor cannot charge. When the external diode is ON, the difference between $V_{IN}$ and $V_{SW}$ is at its largest, thus making it the best period to charge. When there is no current in the inductor, $V_{SW}=V_{OUT}$ so the difference between $V_{IN}$ and $V_{OUT}$ can charge the bootstrap capacitor.

At higher duty cycles, the time period available for bootstrap charging is shorter so the bootstrap capacitor may not sufficiently charge. If the internal circuit does not have sufficient voltage and the bootstrap capacitor is not charged, extra external circuitry can ensure the bootstrap voltage is within the normal operational region.

The DC quiescent current of the floating driver is about 20μA. Make sure the bleeding current at the SW node exceeds this value, such that:

$$I_O + \frac{V_O}{(R1+R2)} > 20\mu A$$

**Current Comparator and Current Limit**

A current-sense MOSFET accurately senses the power MOSFET's current. The result goes to the high-speed current comparator for current-mode control.: When the power MOSFET turns ON, the comparator is first blanked till the end of the turn-on transition to avoid noise issues. The comparator then compares the power switch current to $V_{COMP}$. When the sensed current exceeds $V_{COMP}$, the comparator output is LOW, turning OFF the power MOSFET. The cycle-by-cycle maximum current of the internal power MOSFET is internally limited.

**Short Circuit Protection**

When the output is shorted to the ground, the switching frequency folds back and the current limit falls to lower the short-circuit current. When $V_{FB}$ is zero, the current limit drops to about 50% of its full current limit. When $V_{FB}$ exceeds 0.4V, current limit reaches 100%.

During a short circuit, the $V_{FB}$ voltage is low and pulls down $V_{SS}$ to ~100mV above $V_{FB}$. Removing the short circuit causes the output voltage to recover with $V_{SS}$. When $V_{FB}$ is high enough, the frequency and current limit return to normal values.

**Startup and Shutdown**

If both $V_{IN}$ and $V_{EN}$ exceed their respective thresholds, the chip starts. The reference block initiates to generate a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET OFF for about 50μs to blank the startup noise. When the internal soft-start block is enabled, it first holds its SS output low to ensure the remaining circuitries are ready and then slowly ramps up.

Three events can shut down the chip: $V_{EN}$ LOW, $V_{IN}$ LOW and thermal shutdown. During shutdown, the power MOSFET turns OFF first to avoid any fault triggering. Then $V_{COMP}$ and the internal supply rail drop.

**Programmable Oscillator**

An external resistor ($R_{FREQ}$) from the FREQ pin to ground sets the MPQ4560 oscillating frequency. The value of $R_{FREQ}$ can be calculated from:

$$R_{FREQ}(k\Omega) = \frac{100000}{f_S(kHz)} - 5$$

For example, for $f_{SW}$=500kHz, $R_{FREQ}$=195kΩ.


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# APPLICATION INFORMATION

## COMPONENT SELECTION

### Setting the Output Voltage

A resistive voltage divider from the output voltage to FB pin sets the output voltage. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB}=V_{OUT}\times\frac{R2}{R1+R2}$$

Thus the output voltage is:

$$V_{OUT}=V_{FB}\times\frac{R1+R2}{R2}$$

For example, the value for R2 can be 10kΩ. With this value, R1 is:

$$R1=12.5\times(V_{OUT}-0.8)(K\Omega)$$

So for a 3.3V output voltage, R2 is 10kΩ, and R1 is 31.6kΩ.

### Inductor

The inductor provides constant current to the output load while being driven by the switched input voltage. A larger-value inductor will result in lower ripple current that will lower the output ripple voltage. However, a larger inductor value will be physically larger, have higher series resistance, or lower saturation current.

To determine the inductance, allow the inductor's peak-to-peak ripple current to approximately equal 30% of the maximum switch current limit. Make sure that the peak inductor current is less than the maximum switch current limit. The inductance value can be calculated by:

$$L1=\frac{V_{OUT}}{f_s\times\Delta I_L}\times(1-\frac{V_{OUT}}{V_{IN}})$$

Where $V_{OUT}$ is the output voltage, $V_{IN}$ is the input voltage, $f_S$ is the switching frequency, and $\Delta I_L$ is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$$I_{LP}=I_{LOAD}+\frac{V_{OUT}}{2\times f_S\times L1}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Where $I_{LOAD}$ is the load current.

Table 1 lists several suitable inductors from various manufacturers. The different inductor choices include price vs. size requirements and any EMI requirements.


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**Table 1: Inductor Selection Guide**

| Part Number | Inductance (µH) | Max DCR (Ω) | Current Rating (A) | Dimensions L × W × H (mm3) |
|---|---|---|---|---|
| **Wurth Electronics** | | | | |
| 7447789004 | 4.7 | 0.033 | 2.9 | 7.3×7.3×3.2 |
| 744066100 | 10 | 0.035 | 3.6 | 10×10×3.8 |
| 744771115 | 15 | 0.025 | 3.75 | 12×12×6 |
| 744771122 | 22 | 0.031 | 3.37 | 12×12×6 |
| **TDK** | | | | |
| RLF7030T-4R7 | 4.7 | 0.031 | 3.4 | 7.3×6.8×3.2 |
| SLF10145T-100 | 10 | 0.0364 | 3 | 10.1×10.1×4.5 |
| SLF12565T-150M4R2 | 15 | 0.0237 | 4.2 | 12.5×12.5×6.5 |
| SLF12565T-220M3R5 | 22 | 0.0316 | 3.5 | 12.5×12.5×6.5 |
| **Toko** | | | | |
| FDV0630-4R7M | 4.7 | 0.049 | 3.3 | 7.7×7×3 |
| 919AS-100M | 10 | 0.0265 | 4.3 | 10.3×10.3×4.5 |
| 919AS-160M | 16 | 0.0492 | 3.3 | 10.3×10.3×4.5 |
| 919AS-220M | 22 | 0.0776 | 3 | 10.3×10.3×4.5 |

**Output Rectifier Diode**

The output rectifier diode supplies the current to the inductor when the high-side switch is OFF. Use a Schottky diode to reduce losses from the diode forward voltage and recovery times.

Choose a diode whose maximum reverse voltage rating exceeds the maximum input voltage, and whose current rating exceeds the maximum load current. Table 2 lists example Schottky diodes and manufacturers.

**Table 2: Diode Selection Guide**

| Diodes | Voltage/ Current Rating | Manufacturer |
|---|---|---|
| B290-13-F | 90V, 2A | Diodes Inc. |
| B380-13-F | 80V, 3A | Diodes Inc. |
| CMSH2-100M | 100V, 2A | Central Semi |
| CMSH3-100MA | 100V, 3A | Central Semi |


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**Input Capacitor**

The input current to the step-down converter is discontinuous and requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Use capacitors with low equivalent series resistances (ESR) for the best performance. Ceramic capacitors are best, but tantalum or low-ESR electrolytic capacitors may also suffice.

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitor (C1) can be electrolytic, tantalum, or ceramic.

When using electrolytic or tantalum capacitors, place a small, high-quality, ceramic capacitor (0.1μF) as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by capacitance is approximately:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

**Output Capacitor**

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. Low-ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L is the inductor value and $R_{ESR}$ is the ESR value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and contributes the most to the output voltage ripple. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple is approximately:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ4560 can be optimized for a wide range of capacitances and ESR values.

**Compensation Components**

MPQ4560 employs current-mode control for easy compensation and fast transient response. The COMP pin controls the system stability and transient response. The COMP pin is the output of the internal error amplifier. A series capacitor-resistor combination sets a pole-zero combination to control the control system's characteristics. The DC gain of the voltage feedback loop is:

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_{VEA} \times \frac{V_{FB}}{V_{OUT}}$$

Where

- $A_{VEA}$ is the error-amplifier voltage gain, 400V/V;
- $G_{CS}$ is the current-sense transconductance, 5.6A/V; and
- $R_{LOAD}$ is the load resistor value.

The system has two important poles: One from the compensation capacitor (C3) and the output resistor of error amplifier, and the other due to the output capacitor and the load resistor. These poles are located at:

$$f_{P1} = \frac{G_{EA}}{2\pi \times C3 \times A_{VEA}}$$

$$f_{P2} = \frac{1}{2\pi \times C2 \times R_{LOAD}}$$

Where, $G_{EA}$ is the error-amplifier transconductance, 120μA/V.

The system has one important zero due to the compensation capacitor and the compensation resistor (R3). This zero is located at:

$$f_{Z1} = \frac{1}{2\pi \times C3 \times R3}$$


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The system may have another significant zero if the output capacitor has a large capacitance or a high ESR value. This zero is located at:

$$f_{ESR} = \frac{1}{2\pi \times C2 \times R_{ESR}}$$

In this case, a third pole set by the compensation capacitor (C5) and the compensation resistor can compensate for the effect of the ESR zero. This pole is located at:

$$f_{P3} = \frac{1}{2\pi \times C5 \times R3}$$

The goal of compensation design is to shape the converter transfer function for a desired loop gain. The system crossover frequency where the feedback loop has unity gain is important: Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies lead to system instability. Generally, set the crossover frequency to ~0.1×$f_{SW}$.

**Table 3: Compensation Values for Typical Output Voltage/Capacitor Combinations**

| $V_{OUT}$ (V) | L (μH) | C2 (μF) | R3 (kΩ) | C3 (pF) | C6 (pF) |
|---|---|---|---|---|---|
| 1.8 | 4.7 | 33 | 32.4 | 680 | None |
| 2.5 | 4.7 - 6.8 | 22 | 26.1 | 680 | None |
| 3.3 | 6.8 -10 | 22 | 68.1 | 220 | None |
| 5 | 15 - 22 | 33 | 47.5 | 330 | None |
| 12 | 10 | 22 | 16 | 470 | 2 |

To optimize the compensation components for conditions not listed in Table 3, follow these steps:

1. Choose R3 to set the desired crossover frequency:

$$R3 = \frac{2\pi \times C2 \times f_C}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}}$$

Where $f_C$ is the desired crossover frequency.

2. Choose C3 to achieve the desired phase margin. For applications with typical inductor values, set the compensation zero ($f_{Z1}$) <0.25 ×$f_C$ to provide sufficient phase margin. C3 is then:

$$C3 > \frac{4}{2\pi \times R3 \times f_C}$$

3. C5 is required if the ESR zero of the output capacitor is located at <0.5 ×$f_{SW}$ , or the following relationship is valid:

$$\frac{1}{2\pi \times C2 \times R_{ESR}} < \frac{f_S}{2}$$

If this is the case, use C5 to set the pole ($f_{P3}$) at the location of the ESR zero. Determine the C5:

$$C5 = \frac{C2 \times R_{ESR}}{R3}$$

**High-Frequency Operation**

The switching frequency of MPQ4560 can be programmed up to 2MHz by an external resistor.

The minimum on time of MPQ4560 is about 100ns (typ). Pulse-skipping occurs more readily at higher switching frequencies due to the minimum ON time.

Since the internal bootstrap circuitry has higher impedance, which may not sufficiently charge the bootstrap capacitor during each (1−D)×$\tau_S$ charging period, add an external bootstrap charging diode if the switching frequency is about 2MHz (see External Bootstrap Diode section for detailed implementation information).

With higher switching frequencies, the capacitors' inductive reactances (XL) dominate so that the ESL of input/output capacitors determine the input/output ripple voltages at higher switching frequencies. As a result, use high-frequency ceramic capacitors as input decoupling capacitors and output filtering capacitors for high-frequency operation.

**External Bootstrap Diode**

An external bootstrap diode from the 5V rail to the BST pin may enhance the efficiency under the following conditions:

- There is a 5V rail available in the system;
- $V_{IN}$ ≤5V;
- 3.3V<$V_{OUT}$<5V; and


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- for high duty-cycle operation (when $V_{OUT}/V_{IN}$ > 65%).

The bootstrap diode can be a low cost one such as IN4148 or BAT54.

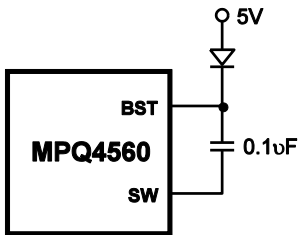



**Figure 2: External Bootstrap Diode**

At no-load or light-load, the converter may operate in pulse-skipping mode in order to maintain output-voltage regulation. Thus there is less time to refresh the BS voltage. For sufficient gate voltage during pulse-skipping, $V_{IN}$–$V_{OUT}$>3V. For example, if the $V_{OUT}$=3.3V, $V_{IN}$ must be exceed 3.3V+3V=6.3V to maintain sufficient BST voltage at no-load or light-load. To meet this requirement, the EN pin can program the input UVLO voltage to $V_{OUT}$+3V.


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## TYPICAL APPLICATION CIRCUITS

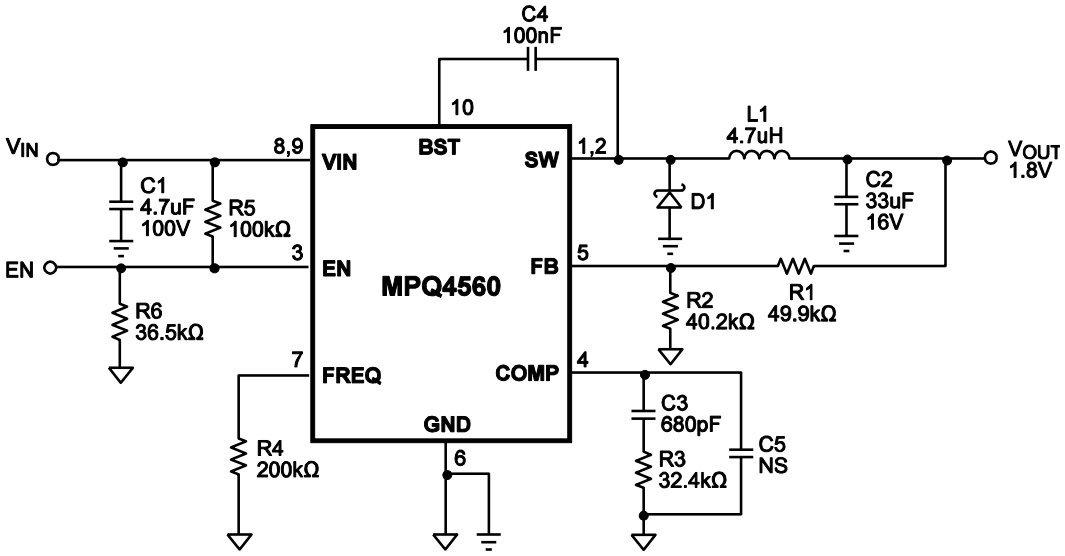



**Figure 3: Typical Application, 1.8V Output**

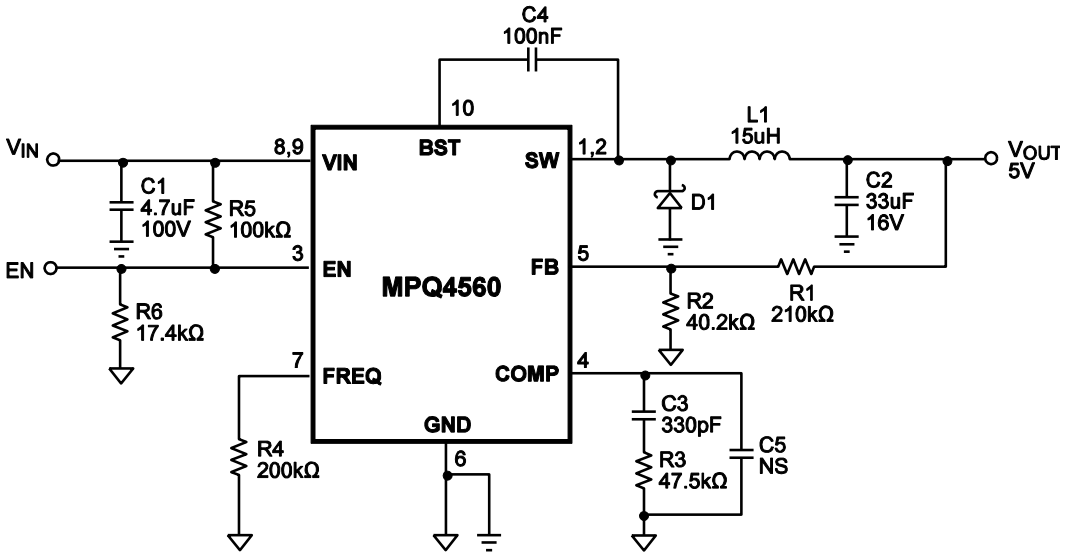



**Figure 4: Typical Application, 5V Output**


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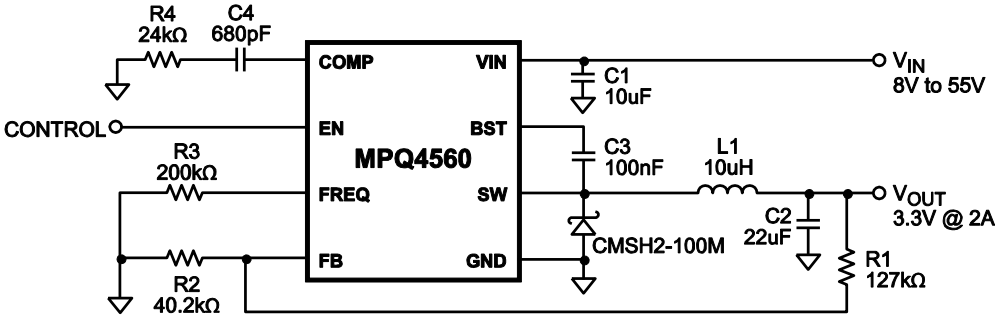
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## PCB LAYOUT GUIDE

PCB layout is very important for stable operation. Try to duplicate the EVB layout for optimum performance.

For changes, please follow these guidelines and use Figure 5 as reference.

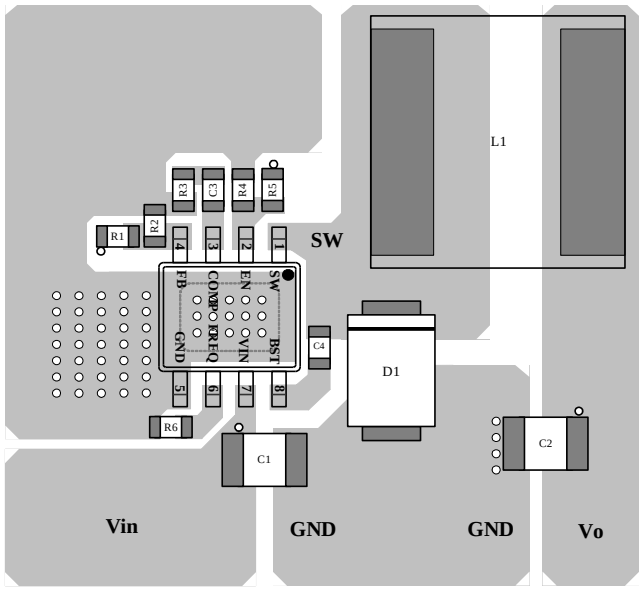
1) Place the input decoupling capacitor and the catch diode as close to the MPQ4560 (VIN pin, SW pin and PGND) as possible, with traces that are very short and fairly wide. This can help to greatly reduce the voltage spike on SW node, and the EMI noise.
2) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible. Try to run the feedback trace as far from the inductor and noisy power traces as possible. Run the feedback trace on the side of the PCB opposite of the inductor with a ground plane separating the two.
3) Route SW away from sensitive analog areas such as FB.
4) Connect IN, SW, and especially GND to large copper surfaces to cool the chip to improve thermal performance and long-term reliability.
5) Place the compensation components close to the MPQ4560. Avoid placing the compensation components close to or under high dv/dt SW node, or inside the high di/dt power loop. If necessary, add a ground plane to isolate the loops.
6) Switching loss increases at higher frequencies. To improve thermal conduction, add a grid of thermal vias under the exposed pad. Use small vias (15mil barrel diameter) so that the hole fills during the plating process: larger vias can cause solder-wicking during the reflow process. The pitch (distance between the centers) between these thermal vias is typically 40mil.

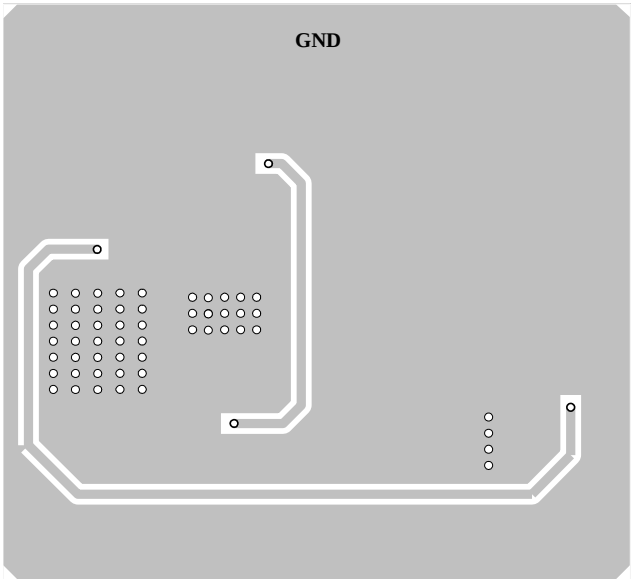



**MPQ4560 Typical Application Circuit**


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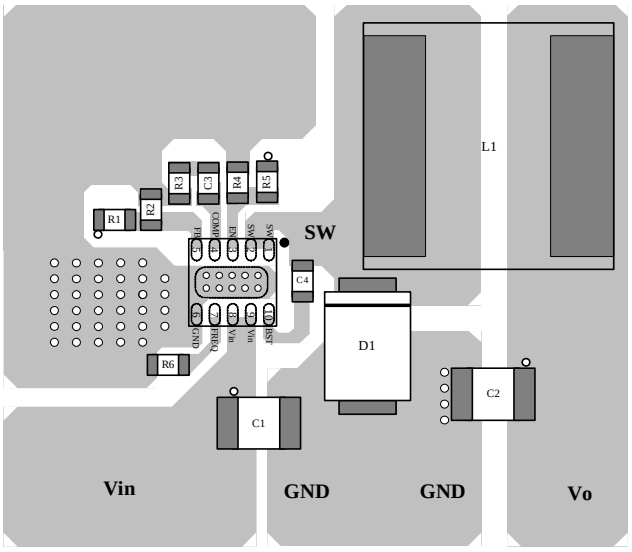
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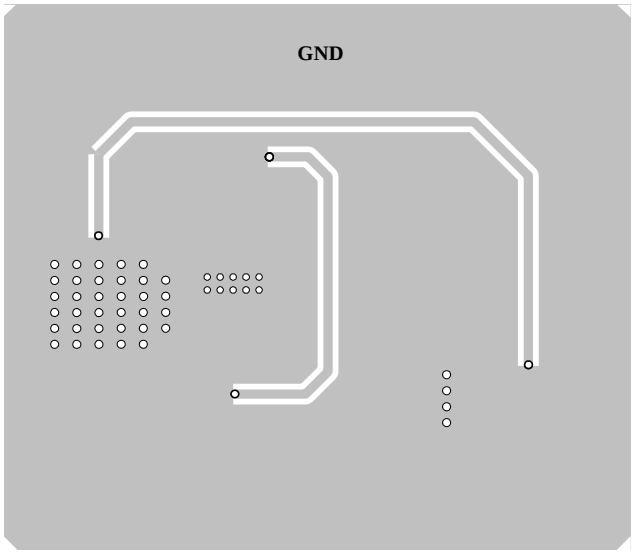



**TOP Layer** **Bottom Layer**

**MPQ4560DN Layout Guide**




**TOP Layer** **Bottom Layer**

**MPQ4560DQ Layout Guide**

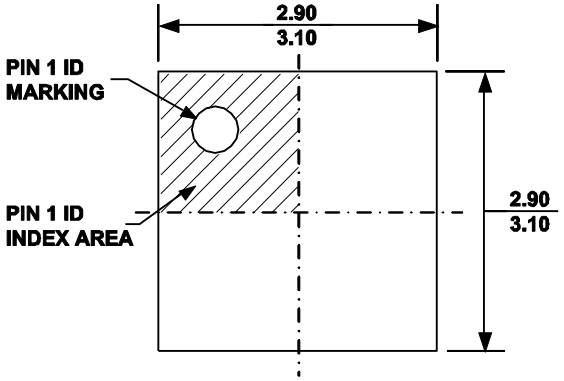
**Figure 5: MPQ4560 Typical Application Circuit and PCB Layout Guide**


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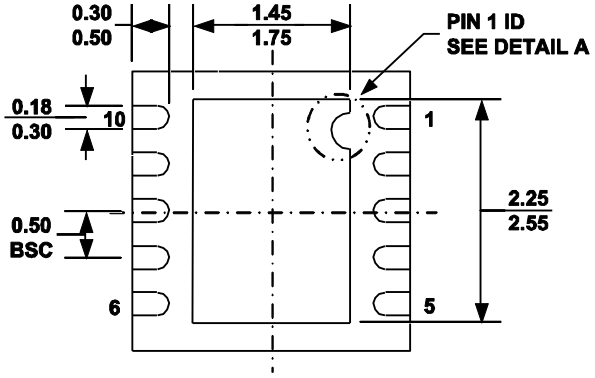
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## PACKAGE INFORMATION

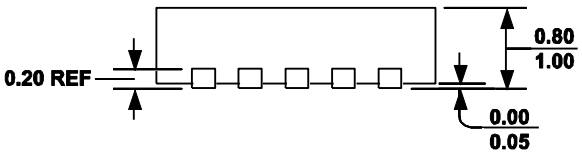
### 3mm × 3mm QFN10 (EXPOSED PAD)



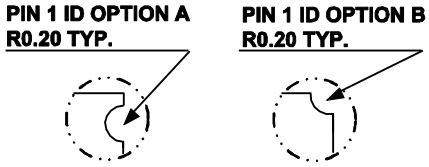

TOP VIEW



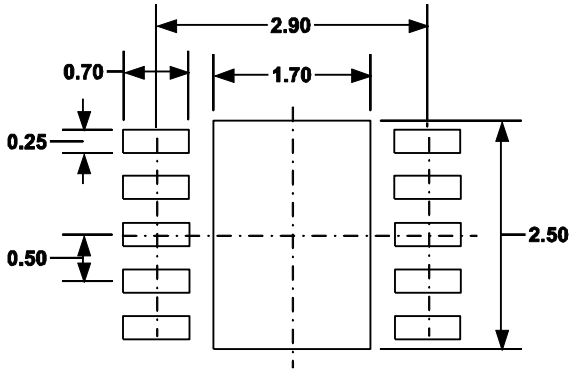

BOTTOM VIEW




SIDE VIEW




DETAIL A




RECOMMENDED LAND PATTERN

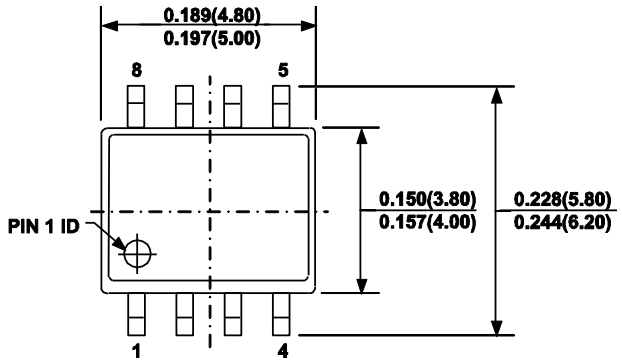
**NOTE:**

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.

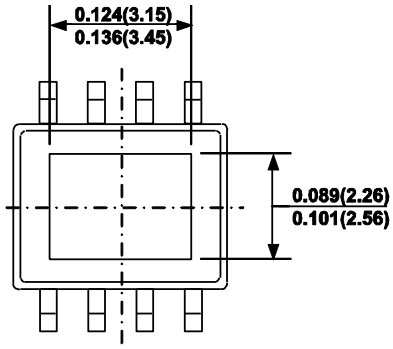

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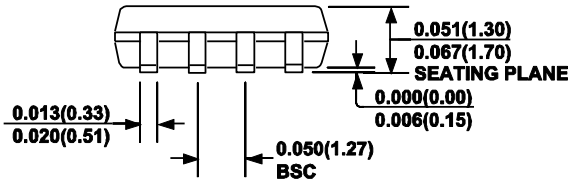
## SOIC8E



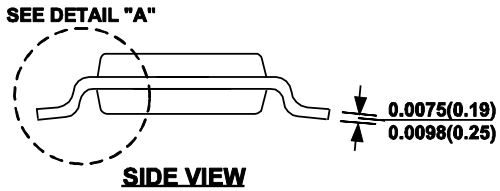

TOP VIEW



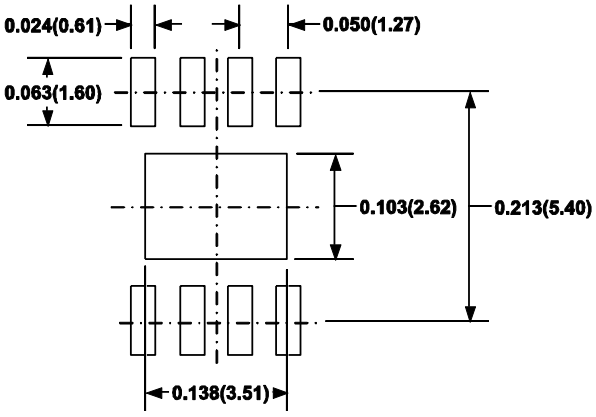

BOTTOM VIEW



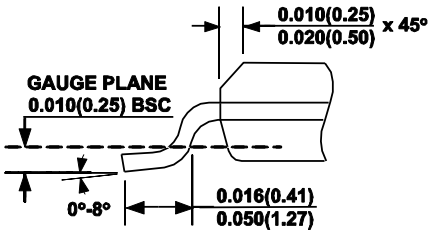

FRONT VIEW




SIDE VIEW




RECOMMENDED LAND PATTERN




DETAIL "A"

**NOTE:**

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.

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