Future Technology Devices International Ltd

FT4233HP / FT4232HP

(High Speed USB Bridge with Type-C/PD3.0 Controller)



The FT4233HP/FT4232HP is a Hi-Speed USB device with a Type-C/PD3.0 controller that fully supports the latest USB Type-C and Power Delivery (PD) standards enabling support for power negotiation with the ability to source current to or sink current from a Type C USB host controller. The USB bridge function delivers 4 independent channels compatible with the existing FT4232H – Quad Hi-speed USB to multipurpose UART/MPSSE solution.

The FT4233HP/FT4232HP has the following advanced features:

- Supports the USB-PD specification Rev 3.0
- Port 1 mode configuration for Sink or Dual Role Power. Initial sink on power up. Power role switchable to source after PD negotiation.
- Port 2 works as Sink, supporting charge through to Port 1 (FT4233HPQ only)
- Supports 5V3A, 9V3A, 12V3A, 15V3A and 20V3A PDOs sink or source
- Supports up to 20 V/5 A (100 W) as a sink when attached to a PD source with 5 A certified type C cable
- Supports Fast Role Swap to switch from source to sink so that VBUS power will be uninterruptible
- Supports dead battery mode for sink devices to be powered from dead battery state through external source
- Type-C/PD Physical Layer Protocol
- PD policy engine using 32-bit RISC controller with 8 kB data RAM and 48 kB code ROM
- PD mode configuration through external EEPROM
- Options to use external MCU controlling PD policy through I^2C interface
- USB to quad serial ports with a variety of configurations
- Entire USB protocol handled on the chip. No USB specific firmware programming required
- USB 2.0 High Speed (480 Mbits/s) and Full Speed (12 Mbits/s) compatible
- Two Multi-Protocol Synchronous Serial Engine (MPSSE) on channel A and channel B, to simplify synchronous serial protocol (USB to JTAG, I^2C, SPI or bit-bang) design
- Independent Baud rate generators
- RS232/RS422/RS485 UART Transfer Data Rate up to 12 Mbaud. (RS232 Data Rate limited by external level shifter)
- FTDI's royalty-free Virtual Com Port (VCP) and Direct (D2XX) drivers eliminate the requirement for USB driver development in most cases
- Optional traffic TX/RX indicators can be added with LEDs and an external 74HC595 shift register
- Adjustable receive buffer timeout
- Support for USB suspend and resume conditions via PWREN#, SUSPEND# and RI# pins
- FTDI FT232R/FT-X style, asynchronous serial UART interface option with full hardware handshaking and modem interface signals
- Fully assisted hardware or X-On / X-Off software handshaking
- UART Interface supports 7/8-bit data, 1/2 stop bits, and Odd/Even/Mark/Space/No Parity
- Enable control for RS485 serial applications using TXDEN pin through external EEPROM
- Operational configuration mode and USB Description strings configurable in external EEPROM over the USB interface
- Low operating and USB suspend current
- UHCI/OHCI/EHCI host controller compatible
- Configurable I/O drive strength (4, 8, 12, or 16 mA) and slew rate
- USB Bulk data transfer mode (512-byte packets in High-Speed mode)
- Dedicated Windows/Linux DLLs available for USB to SPI, and USB to I^2C applications
- +3.3 V single supply operating voltage range
- +1.2 V (chip core) and +3.3 V I/O interfacing (+5 V Tolerant)
- Highly integrated design includes +1.2 V LDO regulator for VCORE, integrated POR function and on chip clock multiplier PLL (12 MHz – 480 MHz)
- Extended -40°C to 85°C industrial operating temperature range
- Available in Pb-free QFN-76/QFN-68 package (RoHS compliant)

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1 Typical Applications

- USB Bridge with Type-C/PD3.0
- Up to 60 W power delivery via USB PD and/or Type-C port as source
- Up to 100W power delivery via USB PD and/or Type-C port as sink
- Get power from USB device functions, e.g., portable USB host needs charging when USB is connected
- Single chip USB to four channels UART (RS232, RS422 or RS485) or Bit-Bang interfaces
- Single chip USB to 2 JTAG channels plus 2 UARTS
- Single chip USB to 1 JTAG channel plus 3 UARTS
- Single chip USB to 1 SPI channel plus 3 UARTS
- Single chip USB to 2 SPI channels plus 2 UARTS
- Single chip USB to 2 Bit-Bang channels plus 2 UARTS
- Single chip USB to 1 SPI channel, plus 1 JTAG channel plus 2 UARTS
- Single chip USB to 2 I^2C channels plus 2 UARTS
- Numerous combinations of 4 channels
- Upgrading Legacy Peripheral Designs to USB
- Field Upgradable USB Products
- Cellular and cordless phone USB data transfer cables and interfaces
- Interfacing MCU / PLD / FPGA based designs to USB
- PDA to USB data transfer
- USB Smart Card Readers
- USB Instrumentation
- USB Industrial Control
- USB FLASH Card Reader / Writers
- Set Top Box PC – USB interface
- USB Digital Camera Interface
- USB Bar Code Readers

1.1 Driver Support

D2XX Direct Drivers are available for the following Operating Systems (OS):

- Windows
- Linux
- Mac
- Android (J2xx / D2xx only)

See the following website link for the full driver support list including OS versions and legacy OS.

https://ftdichip.com/drivers/

Virtual COM Port (VCP) drivers cause the USB device to appear as an additional COM port available to the PC. Application software can access the USB device in the same way as it would access a standard COM port.

D2XX Direct Drivers allow direct access to the USB device through a DLL. Application software can access the USB device through a series of DLL function calls. The functions available are listed in the D2XX Programmer's Guide document which is available from the Documents section of our website.

Please also refer to the Installation Guides webpage for details on how to install the drivers.

The following additional installation guides application notes and technical notes are also available:

- AN_108 Command Processor for MPSSE and MCU Host Bus Emulation Modes
- AN_110 Programmer's Guide for High-Speed FTCJTAG DLL
- AN_113 Interfacing FT2232H Hi-Speed Devices to I2C Bus
- AN_114 Interfacing FT2232H Hi-Speed Devices to SPI Bus
- AN_135 MPSSE Basics
- AN_177 User Guide for LibMPSSE-I2C
- AN_178 User Guide for LibMPSSE-SPI
- AN_411 FTX232H MPSSE I2C Master Example in C#
- AN_448 FT4233HP/FT2233HP/FT233HP Configuration Guide
- AN_551 FT4232HP/FT2232HP/FT232HP Configuration Guide
- TN_104 Guide to Debugging Customer's Failed Driver Installation

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1.2 Part Numbers

Part Number	Package	Packing
FT4232HPQ-TRAY	QFN 68	260 pieces per tray
FT4232HPQ-REEL	QFN 68	3,000 pieces per reel
FT4233HPQ-TRAY	QFN 76	260 pieces per tray
FT4233HPQ-REEL	QFN 76	3,000 pieces per reel

Please refer to Section 6 for all the package mechanical parameters.

Note: FT4233HP and FT4232HP ICs should only be selected if you are planning on using USB Power Delivery features for higher power sink and source. If you do not require USB Power Delivery features, see the following table for a list of standard USB 2.0 Hi-Speed Single Channel ICs which offer the same data bridging functionality without USB Power Delivery features. These standard ICs can also be used with a USB Type-C connector according to TN_181 Type-C USB Connectors with FTDI Products although power is limited to sink at 5V/500mA.

Part Number	Package
FT4232HQ	QFN 48
FT4232HL	LQFP 48

1.3 USB Compliant

The FT4233HP/FT4232HP is fully compliant with the USB 2.0 specification and the USB PD 3.0 specification.

It has been given the USB-IF Test-ID 4484* for FT4233HP and 6244 for FT4232HP*.

*For PD port1

The timing of the rise/fall time of the USB signals is not only dependent on the USB signal drivers, but also on system and is affected by factors such as PCB layout, external components, and any transient protection present on the USB signals. For USB compliance these may require a slight adjustment. Timing can be changed by adding appropriate passive components to the USB signals.



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2 FT4233HP Block Diagram

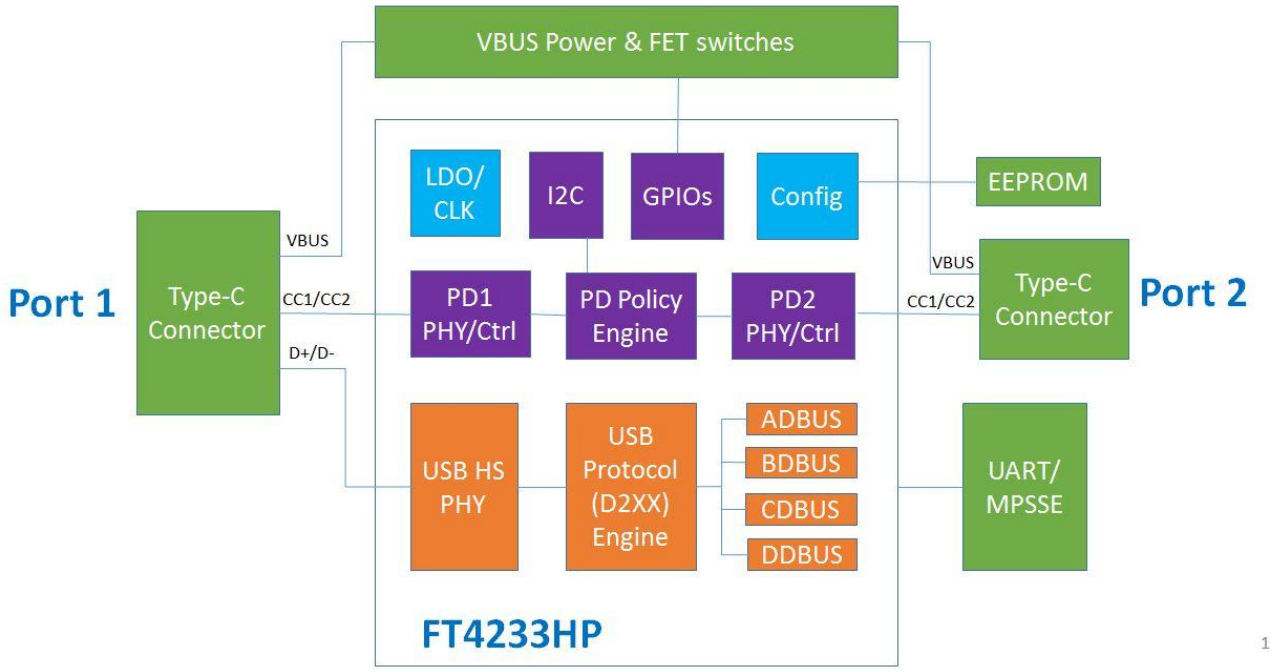


Figure 1 - FT4233HP Block Diagram

For a description of each function please refer to Section 4.

Note: GPIOs block are for PD control only
Note: FT4232HP does not include Port 2.

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3 Device Pin Out and Signal Description

3.1 QFN–76 Package Pin Out

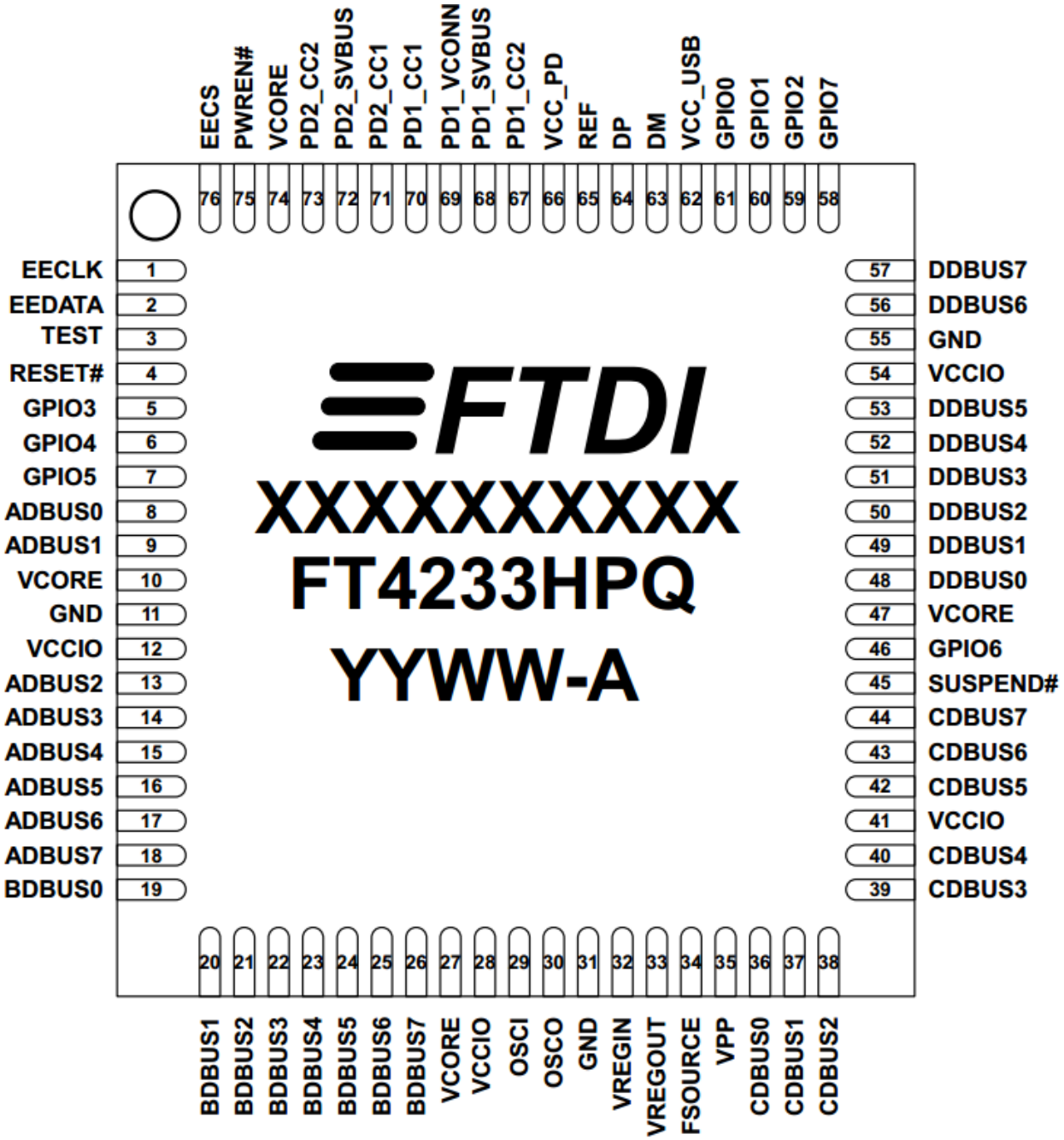


Figure 2 - QFN-76 Package Pin Out

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3.2 QFN–68 Package Pin Out

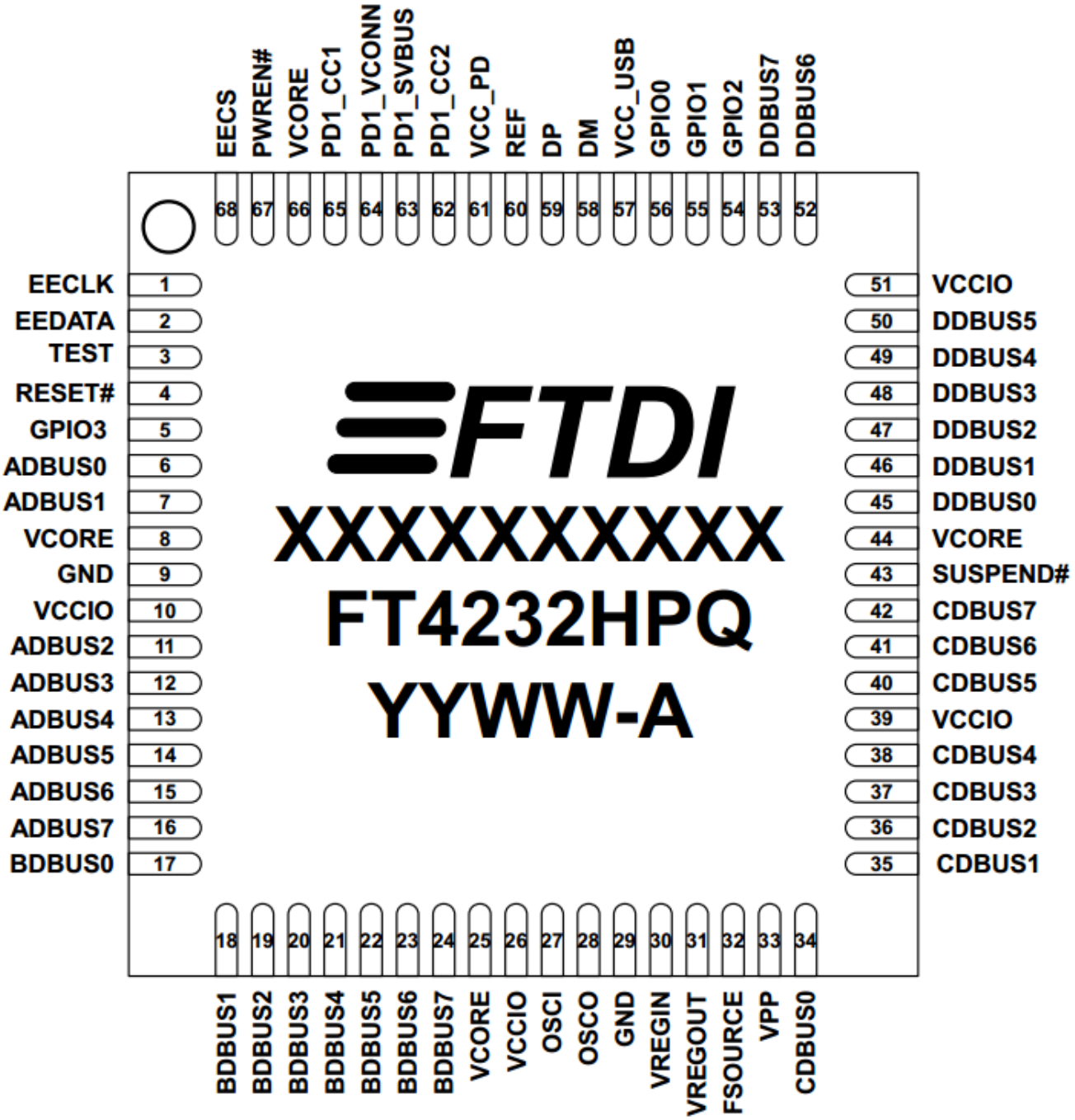


Figure 3 - QFN-68 Package Pin Out

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3.3 Pin Description

This section describes the operation of the FT4233HP/FT4232HP pins. The function of many pins is determined by the configuration of the FT4233HP/FT4232HP. The following table details the function of each pin dependent on the configuration of the interface. Each of the functions is described in **Table 1**.

Note: The convention used throughout this document for active low signals is the signal name followed by #

FT4233HP/FT4232HP						
Pin			Pin functions (depend on configuration)			
QFN-68	QFN-76	Pin Name	ASYNC Serial UART (RS232/422/485)	ASYNC Bit-bang	SYNC Bit-bang	MPSSE
Channel A						
6	8	ADBUS0	TXD	D0	D0	TCK/SK
7	9	ADBUS1	RXD	D1	D1	TDI/DO
11	13	ADBUS2	RTS#	D2	D2	TDO/DI
12	14	ADBUS3	CTS#	D3	D3	TMS/CS
13	15	ADBUS4	DTR#	D4	D4	GPIOL0
14	16	ADBUS5	DSR#	D5	D5	GPIOL1
15	17	ADBUS6	DCD#	D6	D6	GPIOL2
16	18	ADBUS7	RI#/ TXDEN*	D7	D7	GPIOL3
Pin			Pin functions (depend on configuration)			
QFN-68	QFN-76	Pin Name	ASYNC Serial UART (RS232/422/485)	ASYNC Bit-bang	SYNC Bit-bang	MPSSE
Channel B						
17	19	BDBUS0	TXD	D0	D0	TCK/SK
18	20	BDBUS1	RXD	D1	D1	TDI/DO
19	21	BDBUS2	RTS#	D2	D2	TDO/DI
20	22	BDBUS3	CTS#	D3	D3	TMS/CS
21	23	BDBUS4	DTR#	D4	D4	GPIOL0
22	24	BDBUS5	DSR#	D5	D5	GPIOL1
23	25	BDBUS6	DCD#	D6	D6	GPIOL2
24	26	BDBUS7	RI#/ TXDEN*	D7	D7	GPIOL3
Pin			Pin functions (depend on configuration)			
QFN-68	QFN-76	Pin Name	ASYNC Serial UART (RS232/422/485)	ASYNC Bit-bang	SYNC Bit-bang	MPSSE
Channel C						
34	36	CDBUS0	TXD	D0	D0	UART (RS232/422/485) or Bit-Bang interface
35	37	CDBUS1	RXD	D1	D1	UART (RS232/422/485) or Bit-Bang interface
36	38	CDBUS2	RTS#	D2	D2	UART (RS232/422/485) or Bit-Bang interface
37	39	CDBUS3	CTS#	D3	D3	UART (RS232/422/485) or Bit-Bang interface
38	40	CDBUS4	DTR#	D4	D4	UART (RS232/422/485) or Bit-Bang interface
40	42	CDBUS5	DSR#	D5	D5	UART (RS232/422/485) or Bit-Bang interface
41	43	CDBUS6	DCD#	D6	D6	UART (RS232/422/485) or Bit-Bang interface
42	44	CDBUS7	RI#/ TXDEN*	D7	D7	UART (RS232/422/485) or Bit-Bang interface
Pin			Pin functions (depend on configuration)			
QFN-68	QFN-76	Pin Name	ASYNC Serial UART (RS232/422/485)	ASYNC Bit-bang	SYNC Bit-bang	MPSSE
Channel D						
45	48	DDBUS0	TXD	D0	D0	UART (RS232/422/485) or Bit-Bang interface

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46	49	DDBUS1	RXD	D1	D1	UART (RS232/422/485) or Bit-Bang interface
47	50	DDBUS2	RTS#	D2	D2	UART (RS232/422/485) or Bit-Bang interface
48	51	DDBUS3	CTS#	D3	D3	UART (RS232/422/485) or Bit-Bang interface
49	52	DDBUS4	DTR#	D4	D4	UART (RS232/422/485) or Bit-Bang interface
50	53	DDBUS5	DSR#	D5	D5	UART (RS232/422/485) or Bit-Bang interface
52	56	DDBUS6	DCD#	D6	D6	UART (RS232/422/485) or Bit-Bang interface
53	57	DDBUS7	RI#/ TXDEN*	D7	D7	UART (RS232/422/485) or Bit-Bang interface

Table 1 - FT4233HP/FT4232HP Pin Description

***** RI#/ or TXDEN is selectable in the EEPROM. The default is RI#.

Note: Initial Pin States - The device will always start up as four UART ports. Therefore, pins which are output in UART mode will be driving out. If an application uses MPSSE or bit-bang, ensure that any external signals do not drive into these pins and cause contention until the application has configured the mode and direction of these lines.

3.4 Common Pins

The operation of the following FT4233HP/FT4232HP pins are the same regardless of the configured mode:

FT4233HP/FT4232HP				
QFN-68	**QFN-76**	**Name**	**Type**	**Description**
8,25, 44,66	10,27, 47, 74	VCORE	POWER Input	+1.2 V input. Core supply voltage input. Connect to VREGOUT when using internal regulator.
10, 26, 39, 51	12,28, 41, 54	VCCIO	POWER Input	+3.3 V input. I/O interface power supply input. Failure to connect all VCCIO pins will result in failure of the device.
57	62	VCC_USB	POWER Input	+3.3 V Input. Internal USB PHY power supply input. Note that this cannot be connected directly to the USB supply. A +3.3 V regulator must be used. It is recommended that this supply is filtered using an LC filter.
61	66	VCC_PD	POWER Input	+3.3 V Input. Internal PD PHY power supply input.
30	32	VREGIN	POWER Input	+3.3 V Input. Integrated 1.2 V voltage regulator input.
31	33	VREGOUT	POWER Output	+1.2 V Output. Integrated voltage regulator output. Connect to VCORE with 3.3µF filter capacitor. This output should not be used to power other circuits apart from VCORE.
32	34	FSOURCE	POWER Input	FSOURCE input pin for EFUSE. Leave floating for normal operation.
33	35	VPP	POWER Input	VPP input pin for EFUSE. Leave floating for normal operation.
9, 29	11, 31, 55	GND	POWER Input	Ground.

Table 2 - FT4233HP/FT4232HP Power and Ground Pins

QFN-68	QFN-76	Name	Type	Description
27	29	OSCI	INPUT	Oscillator input.
28	30	OSCO	OUTPUT	Oscillator output.

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QFN-68	QFN-76	Name	Type	Description
60	65	REF	INPUT	Current reference – connect via a 12 kΩ resistor @ 1% to GND.
58	63	DM	I/O	USB Data Signal Minus.
59	64	DP	I/O	USB Data Signal Plus.
3	3	TEST	INPUT	IC test pin – for normal operation should be connected to GND.
4	4	RESET#	INPUT	Reset input (active low).
67	75	PWREN#	OUTPUT	Active low power-enable output. PWREN# = 0: Normal operation. PWREN# = 1: USB SUSPEND mode or device has not been configured. This can be used by external circuitry to power down logic when device is in USB suspend or has not been configured.
43	45	SUSPEND#	OUTPUT	Active low when USB is in suspend mode.

Table 3 - Common Function Pins

QFN-68	QFN-76	Name	Type	Description
68	76	EECS*	I/O	EEPROM – Chip Select. Tri-State during device reset.
1	1	EECLK*	OUTPUT	Clock signal to EEPROM. Tri-State during device reset. When not in reset, this outputs the EEPROM clock.
2	2	EEDATA*	I/O	EEPROM – Data I/O Connect directly to Data-In of the EEPROM and to Data-Out of the EEPROM via a 2.2 K resistor. Also, pull Data-Out of the EEPROM to VCC via a 10K resistor for correct operation. Tri-State during device reset.

Table 4 - EEPROM Interface Pins

* If no EEPROM, pull each of these pins via separate 10 K resistor to VCCIO.

QFN-68	QFN-76	Name	Type	Description
63	68	PD1_SVBUS	AI	Analog input. Scaled down VBUS sensing input for PD1. VBUS is required to be scaled down between 7.5 and 7.7 before input to this pin.
64	69	PD1_VCONN	Power Input	Power input for PD1 VCONN power source. Connect to 3.3 V.
65	70	PD1_CC1	AI/O	Analog IO pin. PD1 CC1 pin.
62	67	PD1_CC2	AI/O	Analog IO pin. PD1 CC2 pin.
-	72	PD2_SVBUS	AI	Analog input. Scaled down VBUS sensing input for PD2. VBUS is required to be scaled down between 7.5 and 7.7 before input to this pin.
-	71	PD2_CC1	AI/O	Analog IO pin. PD2 CC1 pin.
-	73	PD2_CC2	AI/O	Analog IO pin. PD2 CC2 pin.

Table 5 - Type-C/PD Port Pins

QFN-68	QFN-76	Name	Type	Description
56	61	GPIO0	I/O	GPIO0 or I2C_SDA pin. Default function is GPIO0 input with weak pull-down.

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QFN-68	QFN-76	Name	Type	Description
55	60	GPIO1	I/O	GPIO1 or I2C_SCL pin. Default function is GPIO1 input with weak pull-down.
54	59	GPIO2	I/O	GPIO2 or I2C_INT# pin. Default function is GPIO2 input with weak pull-down.
5	5	GPIO3	I/O	GPIO3 pin. Default function is GPIO3 input with weak pull-down.
-	6	GPIO4	I/O	GPIO4 pin. Default function is GPIO4 input with weak pull-down.
-	7	GPIO5	I/O	GPIO5 pin. Default function is GPIO5 input with weak pull-down.
-	46	GPIO6	I/O	GPIO6 pin. Default function is GPIO6 input with weak pull-down.
-	58	GPIO7	I/O	GPIO7 pin. Default function is GPIO7 input with weak pull-down.

Table 6 - GPIO Pins

Note that these GPIOs are used only for PD profile indicator and controller. Not to be used as GPIO to be controlled by a USB application.

3.5 Configured Pins

The following sections describe the function of the configurable pins referred in **Table 1**. This is determined by how the FT4233HP/FT4232HP is configured.

3.5.1 Pins used as an Asynchronous Serial Interface

Any of the 4 channels of the FT4233HP/FT4232HP can be configured as an asynchronous serial UART interface (RS232/422/485). When configured in this mode, the pins used, and the descriptions of the signals are shown in **Table 7**.

FT4233HP/FT4232HP										
Channel A Pin No.		Channel B Pin No.		Channel C Pin No.		Channel D Pin No.		Name	Type	ASYNC Serial UART (RS232/422/485) Configuration Description
QFN-68	QFN-76	QFN-68	QFN-76	QFN-68	QFN-76	QFN-68	QFN-76			
6	8	17	19	34	36	45	48	TXD	OUTPUT	TXD = transmitter output
7	9	18	20	35	37	46	49	RXD	INPUT	RXD = receiver input
11	13	19	21	36	38	47	50	RTS#	OUTPUT	RTS# = Ready To send handshake output
12	14	20	22	37	39	48	51	CTS#	INPUT	CTS# = Clear To Send handshake input
13	15	21	23	38	40	49	52	DTR#	OUTPUT	DTR# = Data Transmit Ready modem signaling line
14	16	22	24	40	42	50	53	DSR#	INPUT	DSR# = Data Set Ready modem signaling line
15	17	23	25	41	43	51	56	DCD#	INPUT	DCD# = Data Carrier Detect modem signaling line
16	18	24	26	42	44	52	57	RI#/TXDEN	INPUT/ OUTPUT	RI# = Ring Indicator Control Input. When the Remote Wake-Up option is enabled in the EEPROM, taking RI# low can be used to resume the PC USB Host controller from suspend. (See note 1, 2, and 3) TXDEN = TRANSMIT ENABLE (TTL level). For use with RS485 level converters.

Table 7 - Channel A, B, C and D Asynchronous Serial Interface Configured Pin Descriptions

Notes

1. When using remote wake-up, ensure the resistors are pulled-up in suspend. Also ensure peripheral designs do not allow any current sink paths that may partially power the peripheral.

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2. A peripheral is allowed to draw up to 2.5 mA in suspend.
3. If a Pull-down is enabled, the FT4233HP/FT4232HP will not wake up from suspend.

3.5.2 Pins used in a Synchronous or Asynchronous Bit-Bang Interface

The FT4233HP/FT4232HP channel A, B, C, or channel D can be configured as a bit-bang interface. There are two types of bit-bang modes: **synchronous** and **asynchronous**.

When configured in any bit-bang mode (synchronous or asynchronous), the pins used and the descriptions of the signals are shown in **Table 8**.

FT4233HP/FT4232HP				
QFN-68	**QFN-76**	**Name**	**Type**	**Synchronous or Asynchronous Bit-Bang Configuration Description**
6,7,11-16	8,9,13-18	ADBUS[7:0]	I/O	Channel A, D7 to D0 bidirectional bit-bang data.
17-24	19-26	BDBUS[7:0]	I/O	Channel B, D7 to D0 bidirectional bit-bang data.
34-38,40-42	36-44	CDBUS[7:0]	I/O	Channel C, D7 to D0 bidirectional bit-bang data.
45-50, 52,53	48-53,56, 57	DDBUS[7:0]	I/O	Channel D, D7 to D0 bidirectional bit-bang data.

Table 8 - Channel A, B, C and D Synchronous/Asynchronous Bit-Bang Configured Pin Descriptions

For a functional description of this mode, please refer to Section 4.5.

3.5.3 FT4233HP/FT4232HP pins used in an MPSSE

FT4233HP/FT4232HP channel A and channel B, each have a Multi-Protocol Synchronous Serial Engine (MPSSE). Each MPSSE can be independently configured to several industry standard serial interface protocols such as JTAG, I^2C or SPI, or it can be used to implement a proprietary bus protocol. For example, it is possible to use one of the FT4233HP/FT4232HP's channels (e.g., channel A) to connect to an SRAM configurable FPGA such as supplied by Altera or Xilinx. The FPGA device would normally be un-configured (i.e., have no defined function) at power-up. Application software on the PC could use the MPSSE to download configuration data to the FPGA over USB. This data would define the hardware function on power up. The other MPSSE channel (e.g., channel B) would be available for another serial interface function while channel C and channel D can be configured as UART or bit-bang mode. Alternatively, each MPSSE can be used to control several GPIO pins. When configured in this mode, the pins used, and the descriptions of the signals are shown in Table 9.

FT4233HP/FT4232HP						
Channel A Pin No.		**Channel B Pin No.**		**Name**	**Type**	**MPSSE Configuration Description**
QFN-68	**QFN-76**	**QFN-68**	**QFN-76**			
6	8	17	19	TCK/SK	OUTPUT	Clock Signal Output. For example: JTAG – TCK, Test interface clock SPI – SK, Serial Clock
7	9	18	20	TDI/DO	OUTPUT	Serial Data Output. For example: JTAG – TDI, Test Data Input SPI – DO, serial data output
11	13	19	21	TDO/DI	INPUT	Serial Data Input. For example:

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FT4233HP/FT4232HP						
Channel A Pin No.		**Channel B Pin No.**		**Name**	**Type**	**MPSSE Configuration Description**
QFN-68	**QFN-76**	**QFN-68**	**QFN-76**			
						JTAG – TDO, Test Data output SPI – DI, Serial Data Input
12	14	20	22	TMS/CS	OUTPUT	Output Signal Select. For example: JTAG – TMS, Test Mode Select SPI – CS, Serial Chip Select
13	15	21	23	GPIOL0	I/O	General Purpose input/output
14	16	22	24	GPIOL1	I/O	General Purpose input/output
15	17	23	25	GPIOL2	I/O	General Purpose input/output
16	18	24	26	GPIOL3	I/O	General Purpose input/output

Table 9 - Channel A and B MPSSE Configured Pin Descriptions

For a functional description of this mode, please refer to Section 4.4.

When either Channel A or Channel B or both channels are used in MPSSE mode, Channel C and Channel D can be configured as asynchronous serial UART interface (RS232/422/485) or Bit-Bang mode or a combination of both.

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4 Function Description

The FT4233HP/FT4232HP is a USB 2.0 High Speed (480 Mb/s) to UART/MPSSE IC with USB Type-C/PD ports. It has the capability of being configured in a variety of industry standard serial interfaces. The FT4233HP/FT4232HP has four independent configurable interfaces. Two of these interfaces can be configured as UART, bit-bang mode or JTAG, SPI, I^2C mode, using the MPSSE, with independent baud rate generators. The remaining two interfaces can be configured as UART or bit-bang.

The FT4233HP has two Type-C/PD ports, with PD1 port supporting both power sink and source roles, and PD2 port (FT4233HPQ only) works as a power sink port. Both PD ports support 5V3A, 9V3A, 12V3A, 15V3A 20V3A and 20V5A PDO profiles, and these profiles are configurable through the external EEPROM at power-up or reset. PD1 port share the same Type-C connector with USB data, and PD2 port is power port only without USB data.

4.1 Key Features

USB Type-C/PD Controller. FT4233HP/FT4232HP supports USB Type-C specification version 1.3. The FT4233H/ FT4232HP integrated with USB PD 3.0 controller. USB PD port 1 is USB PD 3.0 with the USB 2.0 function. The first USB PD power is initial power sink when local power source is presented, it can become power source via PD negotiation. FT4233HP has a second USB PD sink only port to connect to PD power source. FT4233HP/FT4232HP USB PD 3.0 function is backward compatible to USB PD 2.0 standard.

USB High Speed to Quad Interface. The FT4233HP/FT4232HP is a USB 2.0 High Speed (480 Mbits/s) to four independent flexible/configurable serial interfaces. This function is backward compatible to FT4232H.

Functional Integration. The FT4233HP/FT4232HP integrates a USB protocol engine which controls the physical Universal Transceiver Macrocell Interface (UTMI) and handles all aspects of the USB 2.0 High Speed interface. The FT4233HP/FT4232HP include an integrated +1.2 V Low Drop-Out (LDO) regulator and 12 MHz to 480 MHz PLL. It also includes 2 Kbytes Tx and Rx data buffers per channel. The FT4233HP/FT4232HP effectively integrates the entire USB protocol on a chip.

MPSSE. Multi-Purpose Synchronous Serial Engines (MPSSE), capable of speeds up to 30 Mbits/s, provides flexible synchronous interface configurations.

Data Transfer Rate. The FT4233HP/FT4232HP support a data transfer rate up to 12 Mbit/s when configured as a UART (RS232/RS422/RS485) interface. Please note the FT4233HP/FT4232HP do not support the baud rates of 7 Mbaud, 9 Mbaud, 10 Mbaud, and 11 Mbaud. Only limited high speed baud rates are possible down to 6Mbaud, below this rate the divider and sub-integer dividers start to have effect offering a wider range of baud rates.

Latency Timer. This is used as a timeout to flush short packets of data back to the PC. The default is 16 ms, but it can be altered between 2 ms and 255 ms. Lower values may reduce latency but may also increase USB bandwidth usage and reduce efficiency.

4.2 Functional Block Descriptions

Type-C/PD PHY and Controller. The FT4233HP has two Type-C/PD ports. Each port has Type-C/PD required Physical Layer (PHY) and controllers. PD1 port has built-in Vconn switches supporting up to 115 mW VCONN power.

PD Policy Engine. The PD policy engine is a 32-bit RISC processor with 8 kB data RAM and 48 kB ROM. It manages both PD port 1 and port 2. Default PD configurations are stored in the ROM code. PD1 port can act as power sink or source role, supporting both normal power role swap. PD2 port (FT4233HPQ only) acts as power sink, which can be connected to a PD source. Additionally Fast Role Swap is supported to switch from source to sink so that VBUS will be uninterruptible. By using an external EEPROM, it is possible to change the PD configuration based on specific use cases, such as Port 1 sink, Port 1 sink/source or PD charge through from Port 2 to Port 1. PDO voltage/current profiles can also be customised using EEPROM.

I^2C Slave Interface. The application can also choose to control the PD policy by external MCU through I2C interface. In this case the built-in PD policy engine is halted. The external MCU has full control to the two PD controller registers (FT4233HPQ only) through I^2C access. An interrupt signal is also provided, so that an interrupt to an external MCU could be asserted when a PD event occurs.

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GPIO block. The GPIO block provides up to 8 GPIO pins which can be used as power switch controls based on the PD policy and profiles. Note that these cannot be used as GPIO to be controlled by an application.

Note: Unless an external MCU is used for PD control, GPIO0 and GPIO1 should not be pulled high when the EEPROM is blank or there is no EEPROM fitted.

Quad Multi-Purpose UART/MPSSE Controllers. The FT4233HP/FT4232HP have four independent UART/MPSSE Controllers. These blocks control the UART data or control the Bit-Bang mode if selected by the SETUP command. The blocks used on channel A and channel B also contain a MPSSE (Multi-Protocol Synchronous Serial Engine) in each of them which can be used independently of each other and the remaining UART channels. Using this, the device can be configured under software command to have 1 MPSSE + 3 UARTS (each UART can be set to Bit Bang mode to gain extra I/O if required) or 2 MPSSE + 2 UARTS.

USB Protocol Engine and FIFO control. The USB Protocol Engine controls and manages the interface between the UTMI PHY and the FIFOs of the chip. It also handles power management and the USB protocol specification.

Dual Port FIFO TX Buffer (2 Kbytes per channel). Data from the Host PC is stored in these buffers to be used by the Multi-purpose UART/FIFO controllers. This is controlled by the USB Protocol Engine and FIFO control block.

Dual Port FIFO RX Buffer (2Kbytes per channel). Data from the Multi-purpose UART/FIFO controllers is stored in these blocks to be sent back to the Host PC when requested. This is controlled by the USB Protocol Engine and FIFO control block.

RESET Generator. The integrated Reset Generator Cell provides a reliable power-on reset to the device internal circuitry at power up. The RESET# input pin allows an external device to reset the FT4233HP/FT4232HP. RESET# should be tied to VCCIO (+3.3 V) if not being used.

Independent Baud Rate Generators. The Baud Rate Generators provide an x16 or an x10 clock input to the UART's from a 120 MHz reference clock and consist of a 14-bit pre-scaler and 4 register bits which provide fine tuning of the baud rate (used to divide by a number plus a fraction). This determines the Baud Rate of the UART which is programmable from 183 baud to 12 Million baud. The FT4233HP/FT4232HP do not support the baud rates of 7 Mbaud, 9 Mbaud, 10 Mbaud, and 11 Mbaud.

Refer to application note AN_120 Aliasing VCP Baud Rates for more details.

LDO Regulator. The +1.2 V LDO regulator generates the +1.2 V for the core and the USB transceiver cell. Its input (VREGIN) must be connected to a +3.3 V external power source. It is also recommended to add an external filtering capacitor to the VREGIN. There is no direct connection from the +1.2 V output (VREGOUT) and the internal functions of the FT4233HP/FT4232HP. The PCB must be routed to connect VREGOUT to VCORE, the pins that require the +1.2 V. This output should not be used to power other circuits apart from VCORE.

USB HS PHY. The Universal Transceiver Macrocell Interface (UTMI) physical interface cell. This block handles the Full speed / High Speed SERDES (serialise – de-serialise) function for the USB TX/RX data. It also provides the clocks for the rest of the chip. A 12 MHz crystal should be connected to the OSCI and OSCO pins. A 12 kΩ resistor should be connected between REF and GND on the PCB.

EEPROM Interface. EEPROM is mandatory for configuration of PD Port and the power profiles. Adding an external EEPROM allows customization of USB VID, PID, Serial Number, Product Description Strings and Power Descriptor value of the FT4233HP/FT4232HP for OEM applications, as well as PD port configurations and power profiles. Other parameters controlled by the EEPROM include Remote Wake Up, Soft Pull Down on Power-Off and I/O pin drive strength.

The EEPROM must have a 16-bit wide configuration such as a Microchip 93LC66B or equivalent capable of a 1 Mbit/s clock rate at VCC = 3.0 V to 3.6 V. The minimum EEPROM size required is 4Kb. The EEPROM is programmable in-circuit over USB using a utility program called FT_PROG available from FTDI's website. This allows a blank part to be soldered onto the PCB and programmed as part of the manufacturing and test process.

If no EEPROM is connected (or the EEPROM is blank), the FT4233HP/FT4232HP will default to serial ports. The device uses its built-in default VID (0403), PID (6041), Product Description and Power Descriptor Value.

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In this case, the device will not have a serial number as part of the USB descriptor. As for the power delivery configuration, please refer to the following application notes: AN_448_FT4233HP/FT2233HP/FT233HP Configuration Guide for FT4233HP and AN_551_FT4232HP/FT2232HP/FT232HP_Configuration_Guide for FT4232HP.

4.3 FT232 UART Interface Mode Description

The FT4233HP/FT4232HP can be configured in similar UART modes as the FT232R/FT-X devices (an asynchronous serial interface). The following examples illustrate how to configure the FT4233HP with an RS232, RS422 or RS485 interfaces. The FT4233HP can be configured as a mixture of these interfaces.

4.3.1 RS232 Configuration

Figure 4 illustrates how the FT4233HP channel A can be configured with an RS232 interface. This can be repeated for channels B, C and D to provide a quad RS232, but has been omitted for clarity.

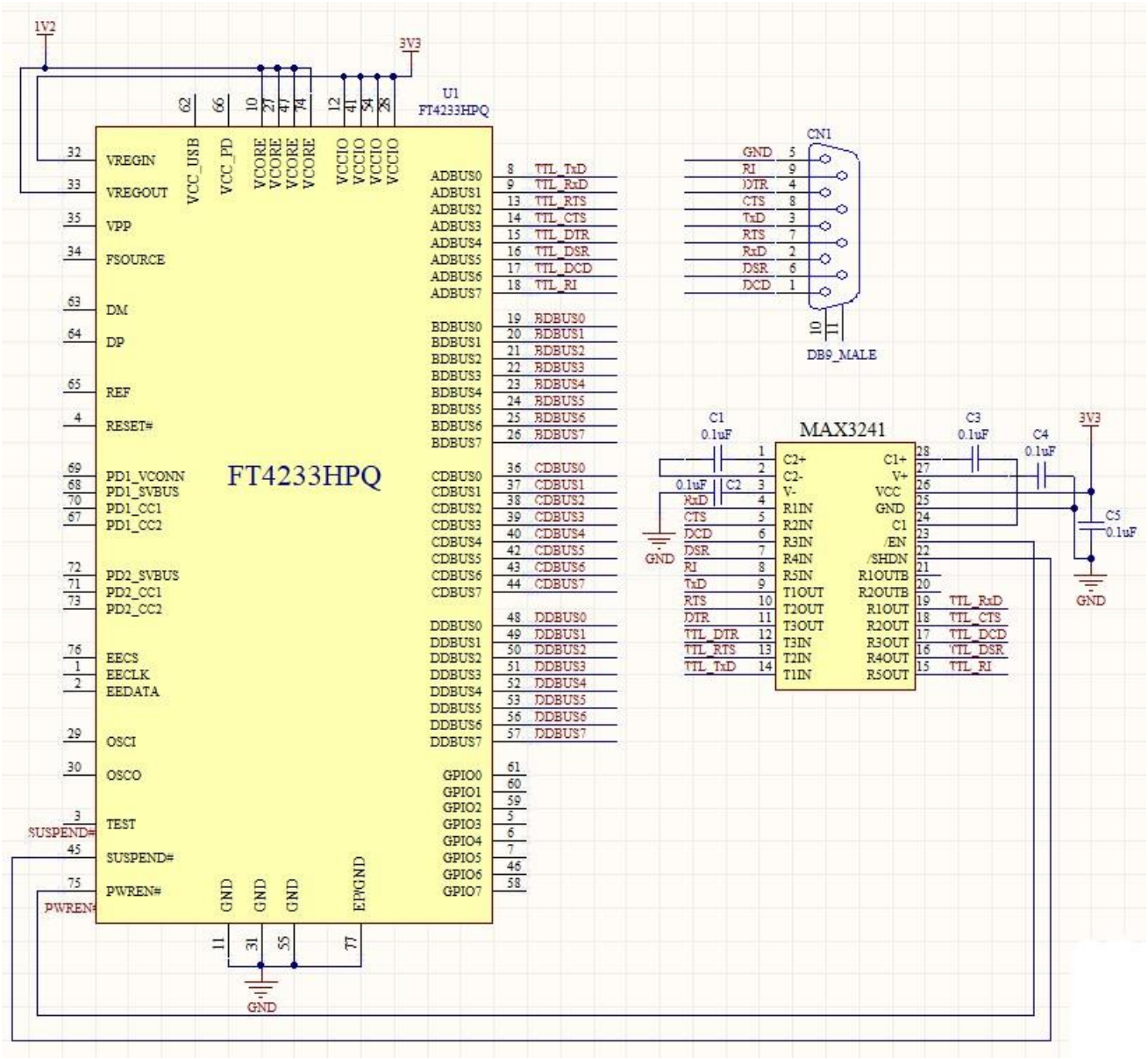


Figure 4 - Single RS232 Configurations

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4.3.2 RS422 Configuration

Figure 5 Illustrates how the FT4233HP can be configured as a dual RS422 interface. The FT4233HP can have all 4 channels connected as RS422, but only channel A and channel C are shown for clarity.

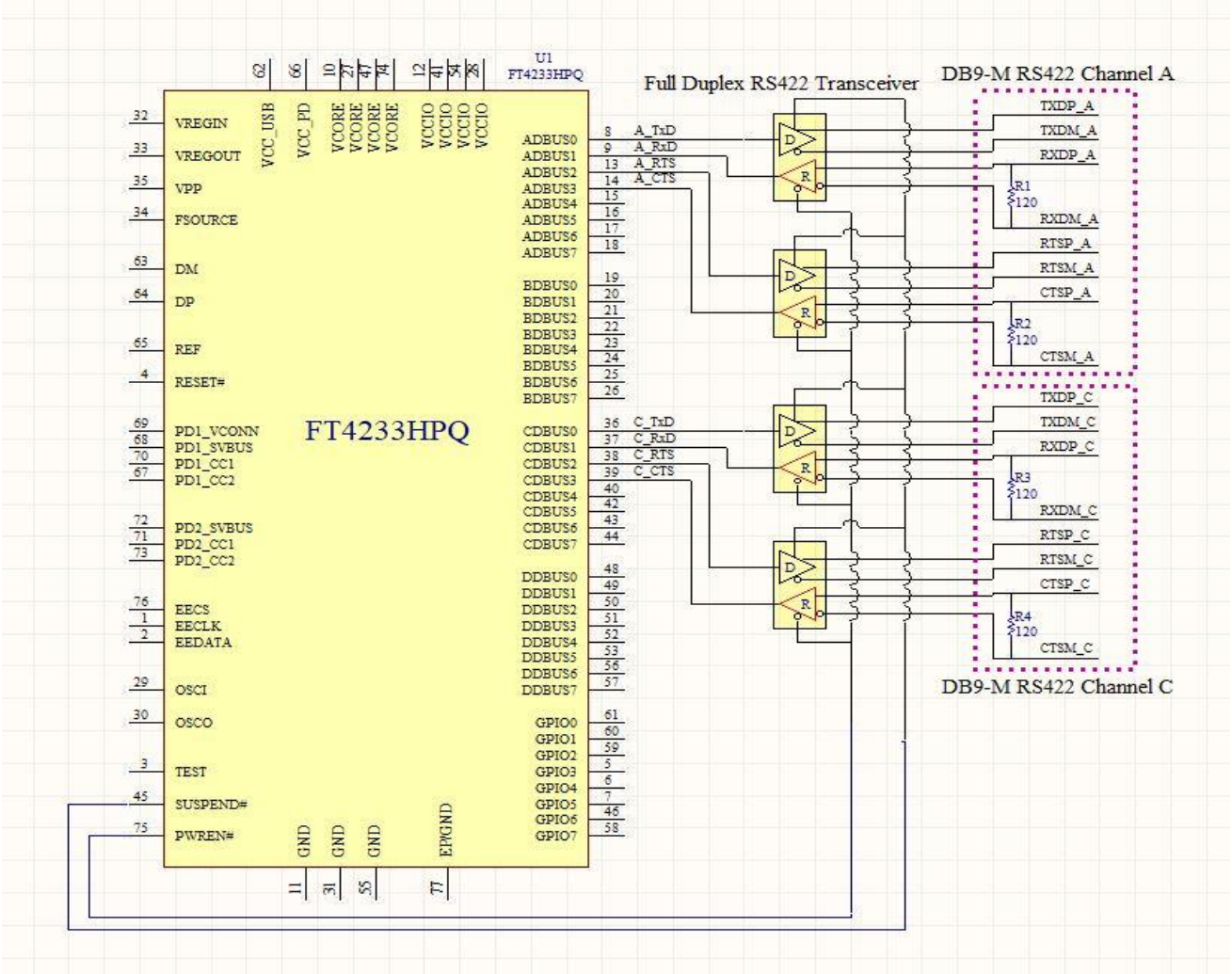


Figure 5 - Dual RS422 Configuration

In this case both channel A and channel C are configured as UART operating at TTL levels and a level converter device (full duplex RS422 transceiver) is used to convert the TTL level signals from the FT4233HP to RS422 levels. The PWREN# signal is used to power down the level shifters such that they operate in a low quiescent current when the USB interface is in suspend mode.

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4.3.3 RS485 Configuration

Figure 6 illustrates how the FT4233HP can be configured as a dual RS485 interface. The FT4233HP can have all 4 channels connected as RS485, but only channel A and channel C are shown for clarity.

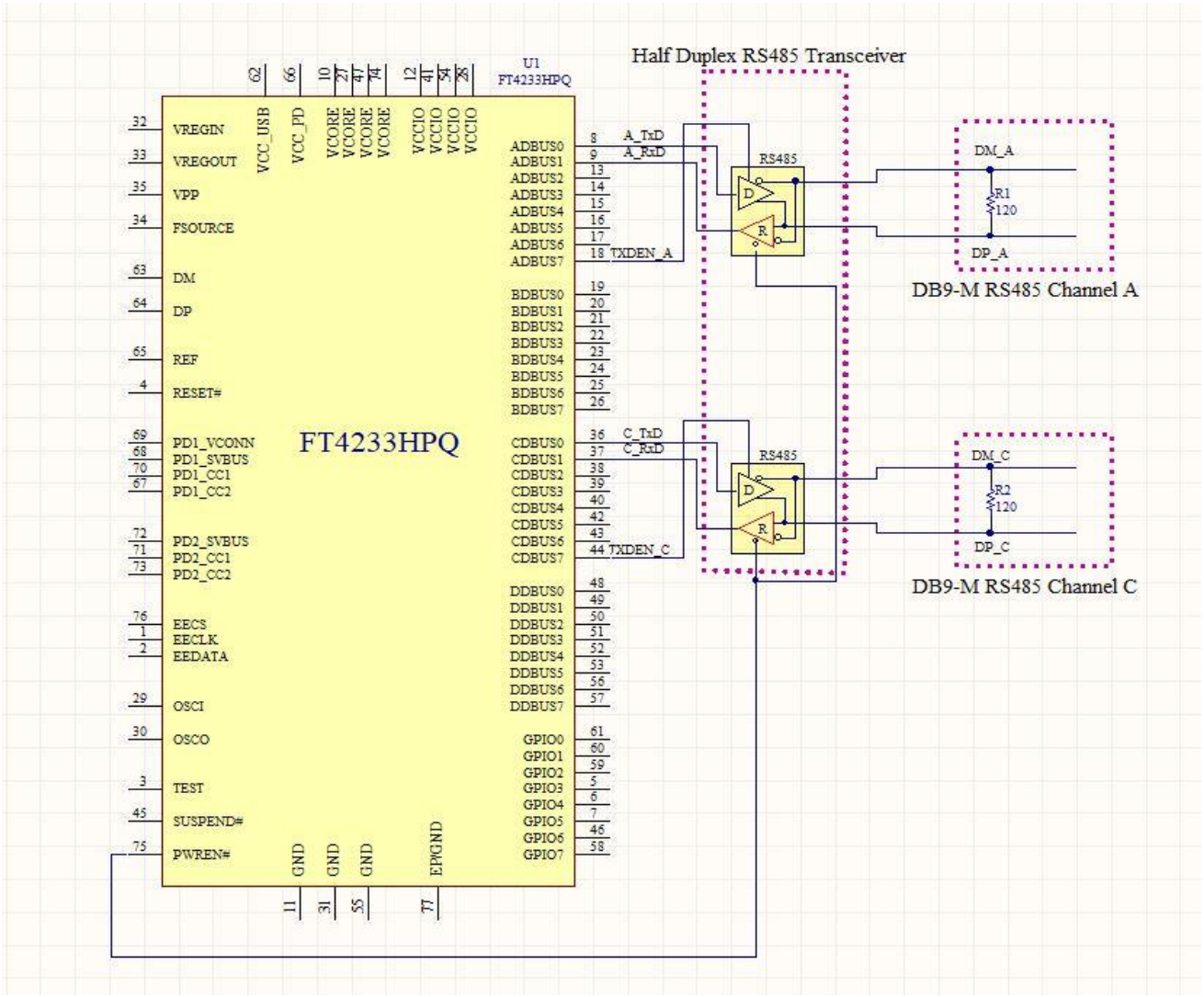


Figure 6 - Dual RS485 Configuration

In this case both channel A and channel C are configured as RS485 operating at TTL levels and a level converter device (half duplex RS485 transceiver) is used to convert the TTL level signals from the FT4233HP to RS485 levels. It has separate enables on both the transmitter and receiver. With RS485, the transmitter is only enabled when a character is being transmitted from the UART. The TXDEN pins on the FT4233HP are provided for exactly that purpose, and so the transmitter enables are wired to the TXDEN pins. The TXDEN function is enabled via the external EEPROM. The receiver enable is active low, so it is wired to the PWREN# pin to disable the receiver when in USB suspend mode.

RS485 is a multi-drop network – i.e., many devices can communicate with each other over a single two wire cable connection. The RS485 cable requires to be terminated at each end of the cable. Links are provided to allow the cable to be terminated if the device is physically positioned at either end of the cable.

In this example the data transmitted by the FT4233HP is also received by the device that is transmitting. This is a common feature of RS485 and requires the application software to remove the transmitted data from the received data stream. With the FT4233HP it is possible to do this entirely in hardware – simply

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modify the schematic so that RXD of the FT4233HP is the logical OR of the level converter device receiver output with TXDEN using an HC32 or similar logic gate.

4.4 MPSSE Interface Mode Description

MPSSE Mode is designed to allow the FT4233HP/FT4232HP to interface efficiently with synchronous serial protocols such as JTAG, I2C and SPI Bus. It can also be used to program SRAM based FPGAs over USB. The MPSSE interface is designed to be flexible so that it can be configured to allow any synchronous serial protocol (industry standard or proprietary) to be implemented using the FT4233HP/FT4232HP. MPSSE is only available on channel A and channel B.

MPSSE is fully configurable and is programmed by sending commands down the data stream. These can be sent individually or more efficiently in packets. MPSSE is capable of a maximum sustained data rate of 30 Mbits/s.

When a channel is configured in MPSSE mode, the IO timing and signals used are shown in **Figure 7** and **Table 10**. These show timings for TCK=30 MHz. TCK can be divided internally to be provide a slower clock.

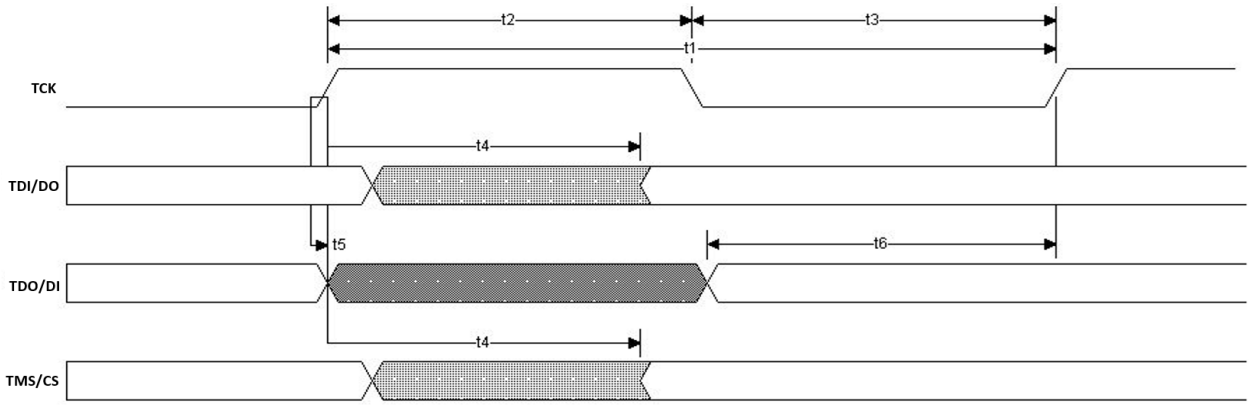


Figure 7 - MPSSE Signal Waveforms

Name	Minimum	Nominal	Maximum	Units	Description
t1		33.33		ns	TCK period
t2	15	16.67		ns	TCK high period
t3	15	16.67		ns	TCK low period
t4	1		7.15	ns	TCK to TDI/DO delay
t5	0			ns	TDO/DI hold time
t6			11	ns	TDO/DI setup time

Table 10 - MPSSE Signal Timings

MPSSE mode is enabled using Set Bit Bang Mode driver command. A hex value of 2 will enable it, and a hex value of 0 will reset the device. See application note AN2232-02 Bit Mode Functions for the FT2232 for more details and examples.

The MPSSE command set is fully described in application note AN_108 Command Processor for MPSSE and MCU Host Bus Emulation Modes.

The application notes in the Document References section is available for configuring the MPSSE.

4.4.1 MPSSE Adaptive Clocking

Adaptive clocking is a new MPSSE feature added to the FT4233HP/FT4232HP MPSSE engine.

The mode is effectively handshaking the CLK signal with a return clock RTCK. This is a technique used by ARM processors.

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The FT4233HP/FT4232HP will assert the CLK line and wait for the RTCK to be returned from the target device to GPIOL3 line before changing the TDO (data out line).

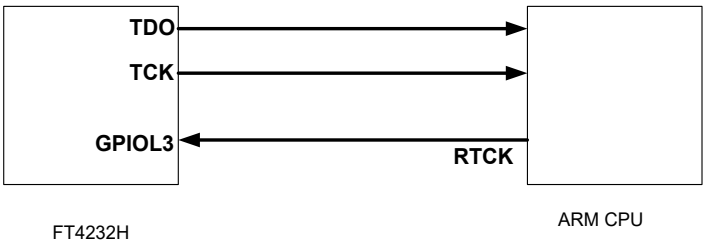


Figure 8 - Adaptive Clocking Interconnect

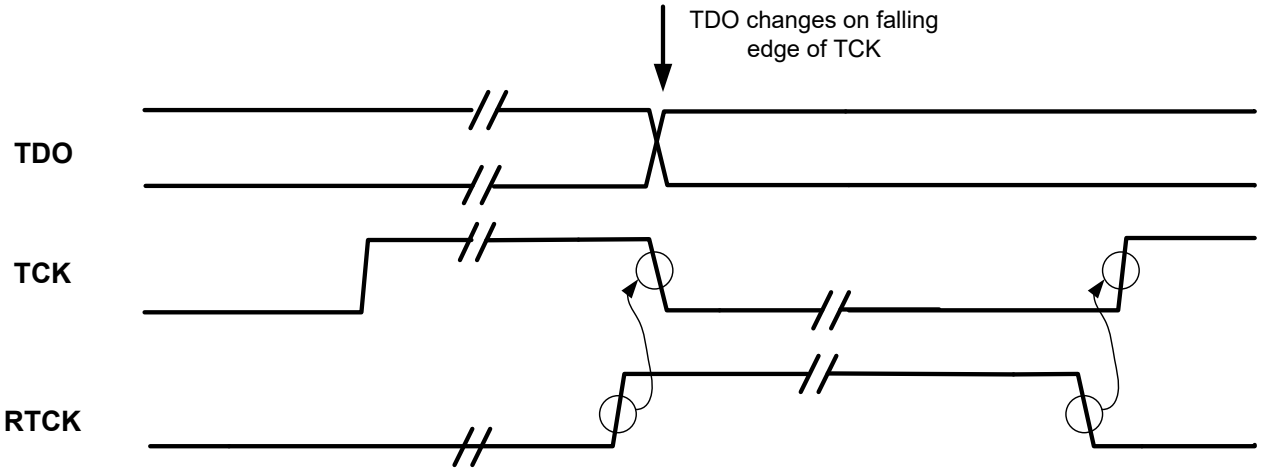


Figure 9 - Adaptive Clocking Waveform

Adaptive clocking is not enabled by default.

See application note AN_108 Command Processor for MPSSE and MCU Host Bus Emulation Modes. for more details.

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4.5 Synchronous and Asynchronous Bit-Bang Interface Mode Description

The FT4233HP/FT4232HP channel A, B, C, or channel D can be configured as a bit-bang interface. There are two types of bit-bang modes: synchronous and asynchronous.

4.5.1 Asynchronous Bit-Bang Mode

Asynchronous Bit-Bang mode is the same as BM-style Bit-Bang mode. On any channel configured in asynchronous bit-bang mode, data written to the device in the normal manner will be self-clocked onto the parallel I/O data pins (those which have been configured as outputs). Each I/O pin can be independently set as an input or an output. The rate that the data is clocked out at is controlled by the baud rate generator.

For the data to change there has to be new data written, and the baud rate clock has to tick. If no new data is written to the channel, the pins will hold the last value written.

4.5.2 Synchronous Bit-Bang Mode

The synchronous Bit-Bang mode will only update the output parallel I/O port pins whenever data is sent from the USB interface to the parallel interface. When this is done, data is read from the USB Rx FIFO buffer and written out on the pins. Data can only be received from the parallel pins (to the USB Tx FIFO interface) when the parallel interface has been written to.

With Synchronous Bit-Bang mode, data will only be sent out by the FT4233HP/FT4232HP if there is space in the FT4233HP/FT4232HP USB TXFIFO for data to be read from the parallel interface pins. This Synchronous Bit-Bang mode will read the data bus parallel I/O pins first before it transmits data from the USB RxFIFO. It is therefore 1 byte behind the output, and so to read the inputs for the byte that you have just sent, another byte must be sent.

For example:

(1) Pins start at 0xFF
Send 0x55, 0xAA
Pins go to 0x55 and then to 0xAA
Data read = 0xFF, 0x55

(2) Pins start at 0xFF
Send 0x55, 0xAA, 0xAA
(Repeat the last byte sent)
Pins go to 0x55 and then to 0xAA

Data read = 0xFF, 0x55, 0xAA

Synchronous Bit-Bang Mode differs from Asynchronous Bit-Bang mode in that the device parallel output is only read when the parallel output is written to by the USB interface. This makes it easier for the controlling program to measure the response to a USB output stimulus as the data returned to the USB interface is synchronous to the output data.

Asynchronous Bit-Bang mode is enabled using Set Bit Bang Mode driver command. A hex value of 1 will enable Asynchronous Bit-Bang mode.

Synchronous Bit-Bang mode is enabled using Set Bit Bang Mode driver command. A hex value of 4 will enable Synchronous Bit-Bang mode.

See application note AN2232-02 Bit Mode Functions for the FT2232 for more details and examples of using the bit-bang modes.

An example of the synchronous bi-bang mode timing is shown in **Figure 10** and **Table 11.**

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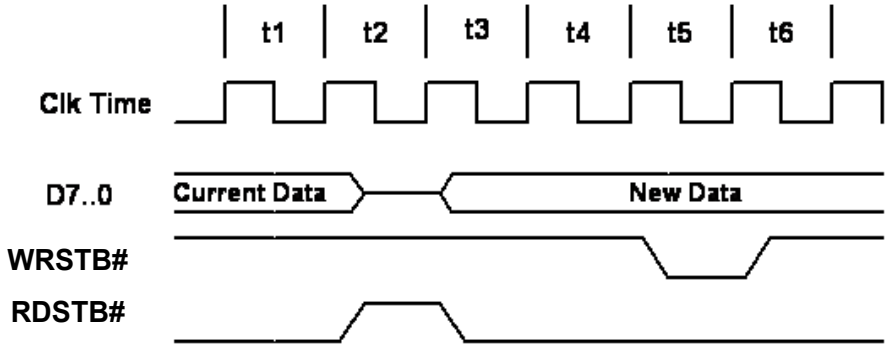


Figure 10 - Synchronous Bit-Bang Mode Timing Interface Example

It should be noted that the FT4233HP/FT4232HP do not output the WRSTB# or RDSTB# signals when configured in bit-bang mode.

Figure 10 shows these signals for illustration purposes only.

Name	Description
t1	Current pin state is read.
t2	RDSTB# is set inactive and data on the parallel I/O pin is read and sent to the USB host.
t3	RDSTB# is set active again, and any pins that are output will change to their new data.
t4	1 clock cycle to allow for data setup
t5	WRSTB# goes active. This indicates that the host PC has written new data to the I/O parallel data.
t6	WRSTB# goes inactive.

Table 11 - Synchronous Bit-Bang Mode Timing Interface Example

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4.6 USB Type-C/PD Controller

4.6.1 PD controller description

The FT4233HP/FT4232HP have a Type-C/PD controller that fully supports the latest USB Type-C and Power Delivery (PD) 3.0 standards enabling support for power negotiation with the ability to sink or source current to a USB host device. There are two PD ports in the device (FT4233HPQ only), one port supports legacy USB 2.0 data transfer as well as providing power sink or source capability, and the other port is standalone PD port as a sink which is used to connect to PD power source. Power Delivery function is designed to meet PD2.0/3.0 specification. If the device is configured to be operated in legacy USB2.0 mode it will be backward compatible to FT4232H in terms of USB2.0 and its peripheral IOs functions.

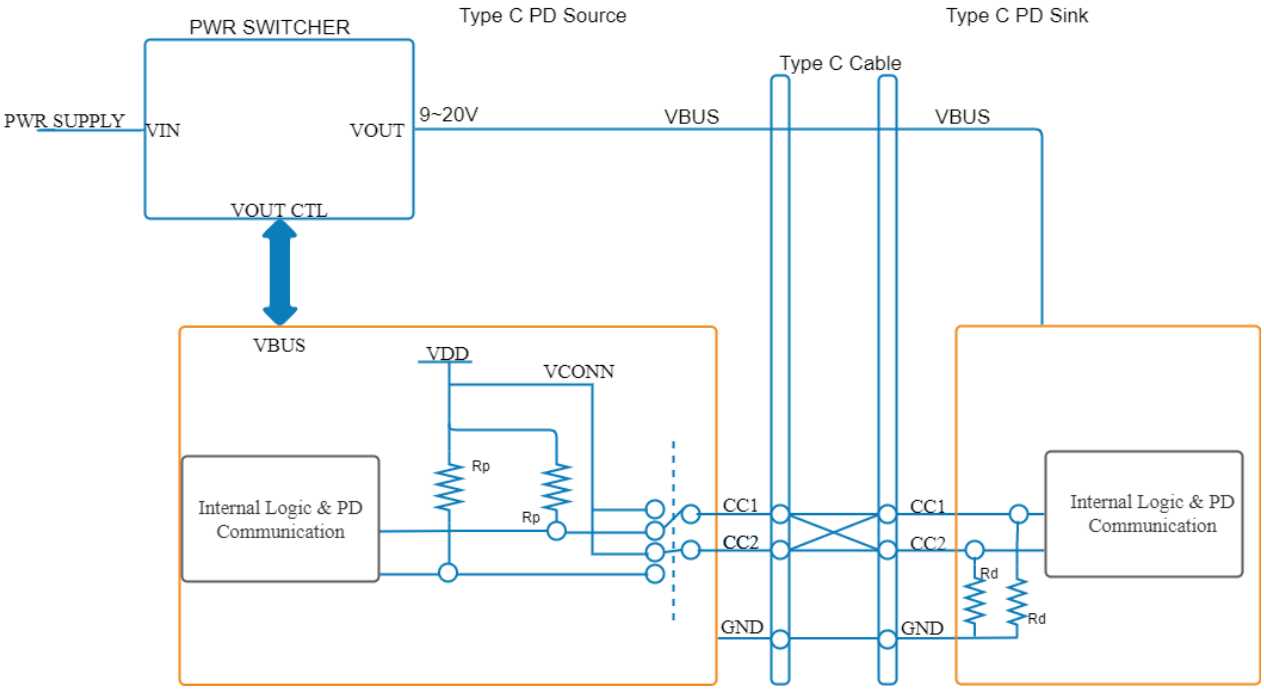


Figure 11 - General PD Working Diagram

4.6.2 Features

- PD 3.0 Compliant
- Physical layer and Policy Engine
- Initial Sink, with Dual Role Power (Power Role Swap)
- Multiple Configurable Power Profiles
- Supports up to 20V3A power profile as a source and up to 20V5A as a sink
- Supports Fast Role Swap to switch from source to sink so that VBUS will be uninterruptible
- Supports dead battery mode for sink devices to be powered from dead battery state through external source
- Charge through Support
- Cable Attach and Orientation Detection
- Supports 1.5 A and 3 A cables in Type-C legacy mode (NON-PD Mode)
- Profile Selection indication through GPIOs when operating In Sink Mode
- Supports External MCU to take over the control of PD policy engine from internal MCU
- 8 bit register interface for a low speed processor, or optional I2C port
- Integrated Chapter 6 protocol reduces required MPU response time to 10 ms
- K code recognition/coding, preamble, CRC, etc offloaded from processor
- VCONN 35 mA protected driver switches
- Single 12 MHz clock + 32 KHz low power clock
- Slew rate limited driving of CC cable lines drive to 1.1 V and 300 ns linear transition time

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4.6.3 AC timing on GPIO pins

Best case transition time with 5pF load		Worst case transition time with 15pF load	
Rise(ns)	Fall(ns)	Rise(ns)	Fall(ns)
1.2	1.1	6.0	6.5

Table 12 - AC Timing on GPIO

4.6.4 GPIO Timing for PD Operation

GPIOs are used as a power profile indicator as well as power supply controllers.

When operating as a Sink, GPIO pins are used for LOAD_EN and ISET.
Note that these cannot be used as GPIO to be controlled by an application

Depending on the kind of profile negotiated, the appropriate ISET GPIO will go high followed by LOAD_EN pin.

The timing between this ISET going high to LOAD_EN can be as high as 12.5 µS.

When operating as a Source, GPIO pins are used as power supply controller. During Source operation, initial voltage will be 5 V and then depending on the profile setting, the PD controller can negotiate a higher voltage. The switching from 5 V to higher Voltage or vice versa is by switching GPIOs. 5 V could be controlled by one Pin whereas each higher Voltage is controlled by a different pin.

For example:

Table 13 shows a sample GPIO states for 3 different voltage cases.

	5 V	9 V	20 V
PS_EN	HIGH	HIGH	HIGH
GPIO_9v	LOW	HIGH	LOW
GPIO_20v	LOW	LOW	HIGH

Table 13 - Example GPIO States for Power Control

In this case 5 V to 9 V or 5 V to 20 V is just an additional GPIO pin going high. In this case the timing does not matter.

However, in the scenario when the profile changes from 9 V to 20 V, there is one GPIO going Low whereas another one going high. In this case, the delay between one pin going low to another pin going high can be as high as 12.5 µS.

4.6.5 Voltage parameters

Based on USB Type-C specification, during initialization when Source connects to Sink, both are in the unattached state. Source firstly detects the Sink's pull down on CC then enters attached state, Source turns on VBUS and VCONN. So USB Type-C specification requests voltage parameters shown below:

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable / adapter(vRa)	0.00 V	0.15 V	0.20 V
Sink(vRd)	0.25 V	1.50 V	1.60 V
No connect (vOPEN)	1.65 V		

Table 14 - CC Voltage on Source Side - Default USB

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable / adapter(vRa)	0.00 V	0.35 V	0.40 V

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Sink(vRd)	0.45 V	1.50 V	1.60 V
No connect (vOPEN)	1.65 V		

Table 15 - CC Voltage on Source Side - 1.5 A @ 5 V

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable / adapter(vRa)	0.00 V	0.75 V	0.80 V
Sink(vRd)	0.85 V	2.45 V	2.60 V
No connect (vOPEN)	2.75 V		

Table 16 - CC Voltage on Source Side – 3 A @ 5 V

To better achieve USB Type-C specification requests, we suggest to use a Schottky Diode to isolate DCDC power from Vcc_PD and PD1_Vconn of FT4233HP/FT4232HP in order to guarantee the expected voltage parameters. The capacitance between Vcc_PD/PD1_Vconn and ground should not be more than 1 µF to avoid the slow rise up of CC line due to the leakage through Vcc_PD and PD1_Vconn to the capacitor. The equivalent circuit is shown in **Figure 12**.

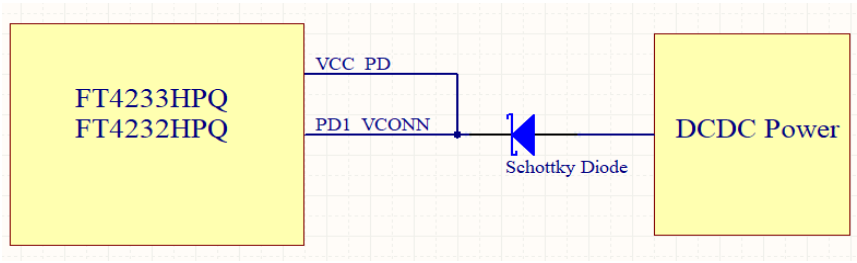


Figure 12 - Schottky Diode Equivalent Circuit

Recommended Schottky Diode parameters:

V(R)	IF	VF (Forward Voltage)
-30 V (max)	≤ 5 A	≤ 0.3 V

Table 17 - Schottky Diode Recommended Characteristics

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5 Devices Characteristics and Ratings

5.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT4233HP/FT4232HP devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these values may cause permanent damage to the device.

Parameter	Value	Unit
Storage Temperature	-65°C to 150°C	Degrees C
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168 Hours (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)*	Hours
Ambient Operating Temperature (Power Applied)	-40°C to 85°C	Degrees C
MTTF/MTBF FT4233HP/FT4232HP	6,719,851	Hours (60% Confidence Level FIT = 148.81)
VCORE Supply Voltage	-0.3 to +2.0	V
VCCIO IO Voltage	-0.3 to +4.0	V
DC Input Voltage – USBDP and USBDM	-0.5 to +3.63	V
DC Input Voltage – High Impedance Bi-directional (powered from VCCIO)	-0.3 to +5.8	V
DC Input Voltage – PD1_CC1, PD1_VCONN, PD1_SVBUS, PD1_CC2, PD2_CC1, PD2_SVBUS, PD2_CC2	-0.5 to (VCC_PD + 0.5)	V
DC Input Voltage - VPP	-0.5 to 1.85	V
DC Input Voltage - FSOURCE	-0.5 to 3.7	V
DC Output Current – Outputs	16	mA

Table 18 - Absolute Maximum Ratings

* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of +125°C and baked for up to 17 hours.

5.2 DC Characteristics

DC Characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCORE	VCC Core Operating Supply Voltage	1.08	1.20	1.32	V	
VCCIO*	VCCIO Operating Supply Voltage	2.97	3.30	3.63	V	
VREGIN	VREGIN Voltage regulator Input	3.00	3.30	3.60	V	
VREGOUT	Voltage regulator Output	1.08	1.2	1.32	V	
Ireg	Regulator Current		21.11	150	mA	VREGIN +3.3 V and data transfer with 12 Mbps
Icc1s	VREGIN Suspend Supply Current		1.64		mA	USB Suspend
I_vccio	VCC_IO operating supply current		0.87		mA	UART Data transfer at 12 Mbps

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Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
I_vcc_pd	VCC_PD suspend supply current		209		µA	PD suspend

Table 19 - Operating Voltage and Current

Note: Failure to connect all VCCIO pins will result in failure of the device.
The I/O pins are +3.3 V cells, which are +5 V tolerant (except the USB PHY pins).

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.4	3.26	VCCIO	V	Ioh = +/-2 mA I/O Drive strength* = 4 mA
		2.4	3.28	VCCIO	V	I/O Drive strength* = 8 mA
		2.4	3.285	VCCIO	V	I/O Drive strength* = 12 mA
		2.4	3.29	VCCIO	V	I/O Drive strength* = 16 mA
Vol	Output Voltage Low		0.1	0.4	V	Iol = +/-2 mA I/O Drive strength* = 4 mA
			0.05		V	I/O Drive strength* = 8 mA
			0.04		V	I/O Drive strength* = 12 mA
			0.03		V	I/O Drive strength* = 16 mA
Vil	Input low Switching Threshold		-	0.80	V	LVTTL
Vih	Input High Switching Threshold	2.0	-		V	LVTTL
Vt	Switching Threshold		1.50		V	LVTTL
Vt-	Schmitt trigger negative going threshold voltage	0.80	1.10	-	V	
Vt+	Schmitt trigger positive going threshold voltage		1.60	2.0	V	
Rpu	Input pull-up resistance**	40	75	190	kΩ	Vin = 0
Rpd	Input pull-down resistance	40	75	190	kΩ	Vin =VCCIO
Iin	Input Leakage Current	-10	+/-1	10	µA	Vin = 0
Ioz	Tri-state output leakage current	-10	+/-1	10	µA	Vin = 5.5 V or 0

Table 20 - I/O Pin Characteristics (except USB PHY Pins)

*The I/O drive strength and slow slew-rate are configurable in the EEPROM.
**The voltage pulled up to is VCCIO-0.9 V in the worst case.

DC Characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCC_USB	PHY Operating Supply Voltage	3.0	3.3	3.6	V	3.3 V I/O

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Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
I_vcc_usb	PHY Operating Supply Current	---	22.7	---	mA	UART Data transfer at 12 Mbps
I_vcc_usb (susp)	PHY Suspend Supply Current	---	0.2	---	mA	USB Suspend

Table 21 - PHY Operating Voltage and Current

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
USB2.0 Transceiver (HS)						
VHSOI	High-speed idle level output voltage (Differential)	-10		10	mV	
VHSOL	High-speed low level output voltage (Differential)	-10		10	mV	
VHSOH	High-speed high level output voltage (Differential)	-360		400	mV	
VCHIRPJ	Chirp-J output voltage (Differential)	700		1100	mV	
VCHIRPK	Chirp-K output voltage (Differential)	-900		-500	mV	
USB 1.1 Transceiver (FS)						
Voh	Output Voltage High	2.8	-	3.6	V	
Vol	Output Voltage Low	0	-	0.3	V	
Vil	Input low Switching Threshold		-	0.8	V	
Vih	Input High Switching Threshold	2.0	-		V	

Table 22 - PHY I/O Pin Characteristics

5.3 ESD Tolerance

ESD protection for FT4233HP/FT4232HP IO's.

Parameter	Reference	Minimum	Typical	Maximum	Units
Human Body Model (HBM)	ANSI/ESDA/JEDEC JS-001 Class 2		±2 kV		kV
Machine Mode (MM)	JEDEC EIA/JESD22-A115-C, Class B		±200 V		V
Charge Device Model (CDM)	ANSI/ESDA/JEDEC JS-002, JEDEC JESD22-C101-D Class-III		±500 V		V
Latch-up	JEDEC STANDARD EIA/JESD78, Trigger Class-II		±200 mA		mA

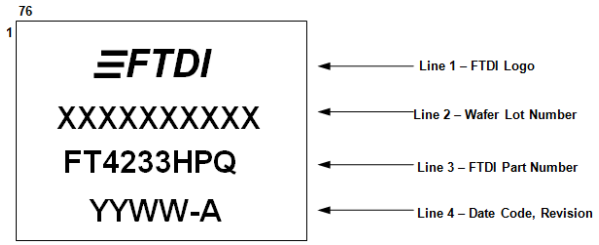
Table 23 - ESD Tolerance

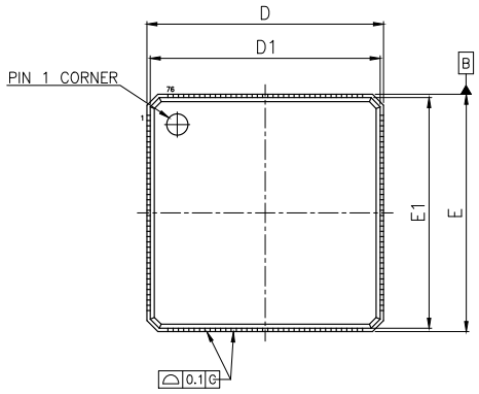
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6 Package Parameters

The FT4233HP/FT4232HP are available in two different packages. The FT4233HPQ is the QFN-76 package option and the FT4232HPQ is the QFN-68 package option. See technical note TN_166 FTDI Example IC Footprints for PCB footprint guidelines.

6.1 FT4233HPQ, QFN-76 Package Dimensions





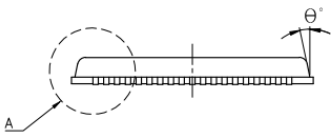
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.65 REF.	
A3		0.20 REF.	
b	0.15	0.20	0.25
c	0.24	0.42	0.60
D	8.90	9.00	9.10
D1	8.65	8.75	8.85
E	8.90	9.00	9.10
E1	8.65	8.75	8.85
e		0.40 BSC.	
K	0.20	—	—
θ°	0.00	—	12.00

UNIT : mm

UNIT : mm	EXPOSED PAD						L		
	D2			E2					
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
245X26* MIL	5.56	5.81	6.06	6.06	6.31	6.56	0.30	0.40	0.50

2 "*"表示汎用字元,此汎用字元可能被其它不同字元所取代,實際的字元請參照bonding diagram所示.
2 "*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

NOTES :
1. JEDEC : N/A.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (0.012 INCHES MAXIMUM).
3. DIMENSION "b" APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. THE PIN #1 IDENTIFIER EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
7. DIMENSION "A1" APPLIED ONLY TO TERMINALS.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.



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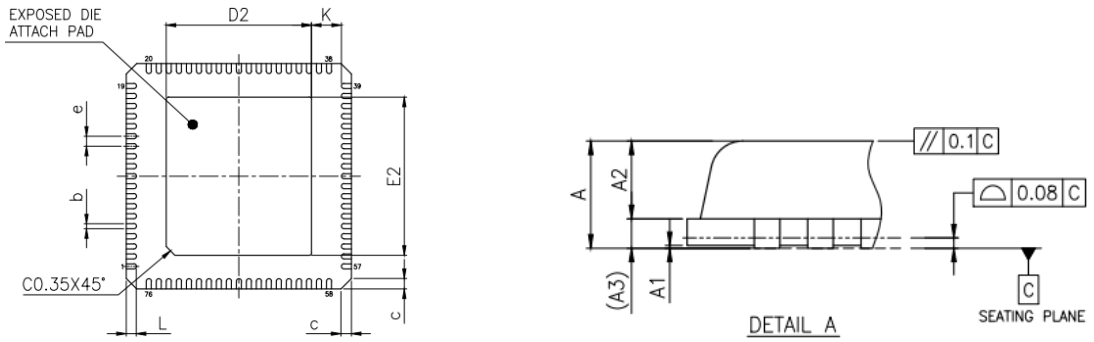
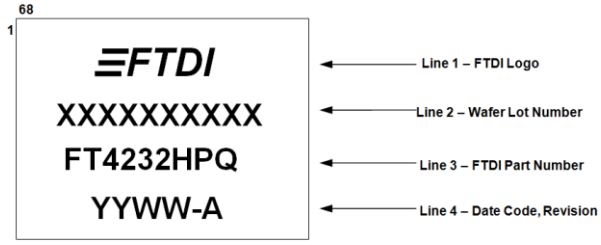
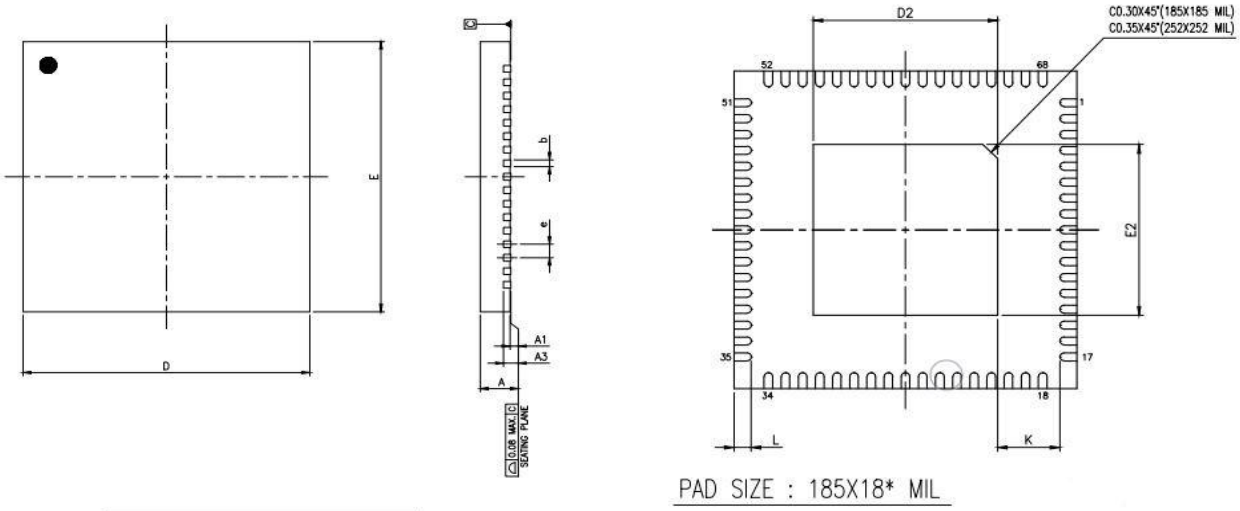


Figure 13 - 76 Pin QFN Package Details

Note: The bottom side central solder pad must be connected to the ground of the system.

6.2 FT4232HPQ, QFN-68 Package Dimensions





	PACKAGE TYPE		
JEDEC OUTLINE	MO-220		
PKG CODE	VQFN(Y868)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	8.00 BSC		
E	8.00 BSC		
e	0.40 BSC		
L	0.35	0.40	0.45
K	0.20	—	—

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
185X18* MIL	4.25	4.30	4.35	4.25	4.30	4.35	V	X	N/A

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 14 - 68 Pin QFN Package Details

Note: The bottom side central solder pad must be connected to the ground of the system.

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7 FT4233HP/FT4232HP Configuration

7.1 Oscillator Configuration

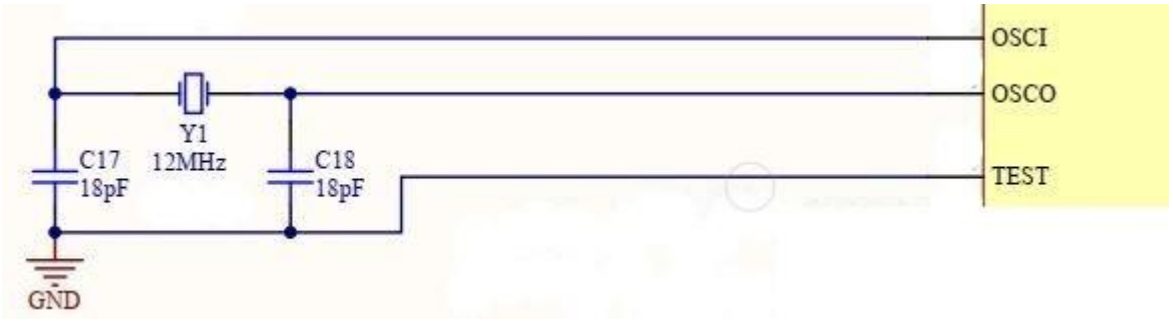


Figure 15 - Recommended FT4233HP/FT4232HP Crystal Oscillator Configuration

Figure 15 illustrates how to connect the FT4233HP/FT4232HP with a 12 MHz ± 0.003% crystal. In this case loading capacitors should be added between OSCI, OSCO and GND as shown. A value of 18 pF is shown as the capacitor in the example – this will be good for many crystals, but it is recommended to select the loading capacitor value based on the manufacturer's recommendations wherever possible. It is recommended to use a parallel cut type crystal.

It is also possible to use a 12 MHz oscillator with the FT4233HP/FT4232HP. In this case the output of the oscillator would drive OSCI, and OSCO should be left unconnected. The oscillator must have a CMOS output drive capability.

Item / Type	7B
Frequency Tolerance (at 25 ℃)	± 30 ppm
Frequency Stability Over Operating Temperature Range	± 30 ppm
Shunt Capacitance (C0)	7 pF Max
Drive Level	100 µW Max
Load Capacitance	18 pF

Table 24 - Crystal Characteristics

7.2 4 Channel Transmit and Receiver LED Indication Example

Figure 16 illustrates how a 74HC595 can be used to decode the EEDATA data to indicate Tx and Rx on each of the channels. The associated LED will light when the Channel is transmitting or receiving data.

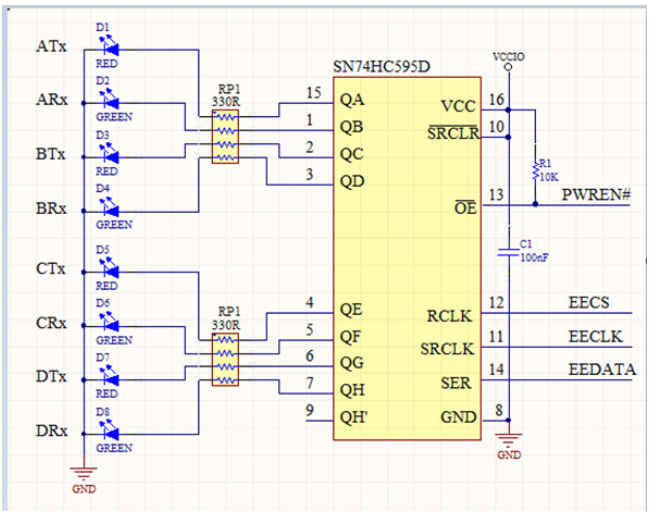


Figure 16 - Using 74HC595 to indicate Tx and Rx Data

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In this configuration, the LEDs will flash when the EEPROM is accessed e.g., during enumeration.

Under normal operation, the EECS is held low to disable access to the EEPROM. In this special case, the EECLK (frequency = 1.56µS) will clock the EEDATA into the 74HC595 shift register (with EECS low, therefore EEPROM ignores the EEDATA). Then EECS will pulse high. The rising edge of the EECS latches the data into a storage register of the 74HC595 which drives the LEDs.

Please refer to the 74HC595 datasheet for further explanation.

7.3 PD Configuration

Figure 17 illustrates the application example of bus power configuration for PD. The device gets the power either from PD1 or PD2. In this application, the FT4233HP requires that the VBUS is regulated down to +3.46V (using LDO) to supply VCCIO, VCC_USB and VREGIN.

VREGIN is the +3.46 V input to the on chip +1.2 V regulator. The output of the on chip LDO regulator drive the FT4233HP core supply (Vcore).

Schottky diode is added between +3.46 V and VCC_PD/PD1_VCONN to prevent CC leakage during the initial attach when the chip is not yet fully powered up.

The GPIOs are used to drive the load switch as well as controlling power level of the voltage regulator according to the negotiated PD profiles.

Please refer to the UMFT4233HPEV Evaluation Module Datasheet for more details on the PD configuration in various user scenario.

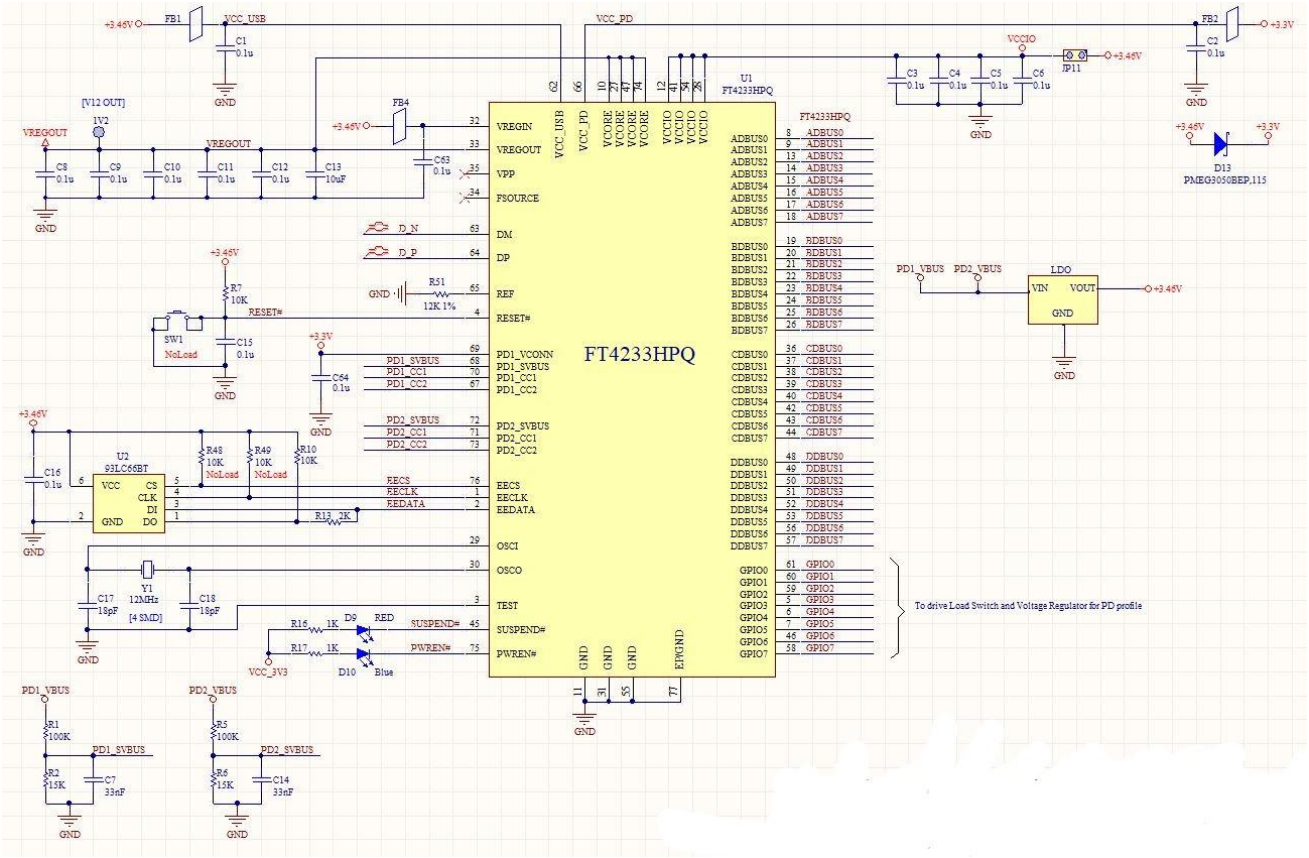


Figure 17 - Bus Power PD Configuration Diagram

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8 EEPROM Configuration

If an external EEPROM is fitted (eg 93LC66) it can be programmed over USB using FT_PROG. The EEPROM must be 16 bits wide and capable of working at a VCC supply of +3.0 to +3.6 volts and have a minimum size of 4Kb.

Adding an external EEPROM allows selecting the TXDEN for RS485 mode when asynchronous serial interface has been selected.

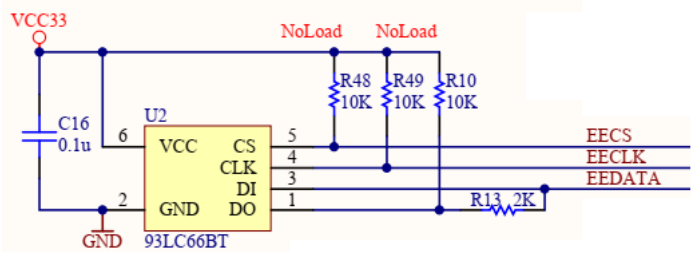


Figure 18 - EEPROM Interface

The external EEPROM can also be used to customise the USB VID, PID, Serial Number, Product Description Strings and Power Descriptor value of the FT4233HP/FT4232HP for OEM applications. Other parameters controlled by the EEPROM include Remote Wake Up, Soft Pull Down on Power-Off, I/O pin drive strength and TXDEN selection.

If no EEPROM is connected (or the EEPROM is blank), the FT4233HP/FT4232HP uses its built-in default VID (0403), PID (6041/6043) Product Description and Power Descriptor Value. In this case, the device will not have a serial number as part of the USB descriptor.

8.1 Default EEPROM Configuration

The external EEPROM (if it is fitted) can be programmed over USB using FT_PROG. This allows a blank part to be soldered onto the PCB and programmed as part of the manufacturing and test process. Users who do not have their own USB Vendor ID but who would like to use a unique Product ID in their design can apply to FTDI for a free block of unique PIDs.

See technical note TN_100 USB Vendor ID/Product ID Guidelines for more information.

Parameter	Value	Notes
USB Vendor ID (VID)	0403h	FTDI default VID (hex)
USB Product ID (PID)	6041h 6043h	FTDI default PID (hex) for FT4233HP FTDI default PID (hex) for FT4232HP
bcd Device	0x2900 0x3100	For FT4233HP For FT4232HP
Serial Number Enabled?	Yes	
Serial Number	None	
Pull down I/O Pins in USB Suspend	Disabled	Enabling this option will make the device pull down on the UART interface lines when in USB suspend mode (PWREN# is high).
Manufacturer Name	FTDI	
Product Description	Quad RS232-HS	
Max Bus Power Current	500 mA	5V/3000mA is negotiated when plugged into Type-C host controller
Power Source	Bus Powered	
Device Type	FT4233HP FT4232HP	For FT4233HP For FT4232HP
USB Version	0200h	Returns USB 2.0 device description to the host.
Remote Wake Up	Disabled	Taking RI# low will wake up the USB host controller from suspend in approximately 20 ms. If enabled.

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Parameter	Value	Notes
RI RS485	Disabled	Enables TXDEN signal for RS485 buses.
High Current I/Os	Disabled	Enables the high drive level on the UART and ACBUS I/O pins.
IO Slew	Disabled	Slow slew rate if enabled
Schmitt Trigger for Input pin	Normal trigger	Schmitt trigger for input pin if enabled
Load VCP Driver	Enabled	Makes the device load the VCP driver interface for the device.

Table 25 - Default Configuration with a blank/no EEPROM

8.2 PD Configuration and Default values

Refer to application note AN_448 FT4233HP/FT2233HP/FT233HP Configuration Guide for FT4233HP Power Delivery configuration and Default values.

Refer to application note AN_551 FT4232HP/FT2232HP/FT232HP Configuration Guide for FT4232HP Power Delivery configuration and Default values.

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9 Contact Information

Europe, Middle East, Africa

Future Technology Devices International Limited (UK)
Unit 1, 2 Seaward Place, Centurion Business Park
Glasgow G41 1HH
United Kingdom
Tel: +44 (0) 141 429 2777

E-mail (Sales) sales1@ftdichip.com
E-mail (Technical Support) support1@ftdichip.com

Americas

Future Technology Devices International Limited (USA)
7130 SW Fir Loop
Tigard, OR 97223-8160
USA
Tel: +1 (503) 547 0988

E-mail (Sales) us.sales@ftdichip.com
E-mail (Technical Support) us.support@ftdichip.com

Asia Pacific

Future Technology Devices International Limited (Singapore)
1 Tai Seng Avenue, Tower A #03-06
Singapore 536464
Tel: (+65) 6841 1174
Tel (Technical Support): +886 (0) 2 8797 1330

E-mail (Sales) tw.sales1@ftdichip.com
E-mail (Technical Support) tw.support1@ftdichip.com

China

Future Technology Devices International Limited (China)
Room 1103, No. 666 West Huaihai Road,
Shanghai, 200052
China
Tel: +86 21 62351596

E-mail (Sales) cn.sales@ftdichip.com
E-mail (Technical Support) cn.support@ftdichip.com

Web Site

https://ftdichip.com/

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Appendix A – References

Document References

AN_108 Command Processor for MPSSE and MCU Host Bus Emulation Modes
AN_110 Programmer's Guide for High-Speed FTCJTAG DLL
AN_113 Interfacing FT2232H Hi-Speed Devices to I2C Bus
AN_114 Interfacing FT2232H Hi-Speed Devices to SPI Bus
AN_135 MPSSE Basics
AN_177 User Guide for LibMPSSE-I2C
AN_178 User Guide for LibMPSSE-SPI
AN_411 FTX232H MPSSE I2C Master Example in C#
AN_448 FT4233HP/FT2233HP/FT233HP Configuration Guide
AN_449 FT4233HP/FT2233HP/FT4232HP/FT2232HP DCDC Power Delivery
AN_551 FT4232HP/FT2232HP/FT232HP Configuration Guide
AN2232-02 Bit Mode Functions for the FT2232

TN_100 USB Vendor ID/Product ID Guidelines
TN_104 Guide to Debugging Customer's Failed Driver Installation
TN_166 FTDI Example IC Footprints
TN_180 FT4233HP/FT2233HP/FT233HP Errata Technical Note

74HC595 datasheet
UMFT4233HPEV Evaluation Module Datasheet
FT_PROG - EEPROM Programming Utility

Acronyms and Abbreviations

Terms	Description
DRP	Dual Role Power
EEPROM	Electrically Erasable Programmable Read-Only Memory
FIFO	First In First Out
FPGA	Field-Programmable Gate Array
IC	Integrated Circuit
I2C	Inter Integrated Circuit
JTAG	Joint Test Action Group
LDO	Low Drop Out
LED	Light Emitting Diode
MCU	Microcontroller Unit
MPSSE	Multi-Protocol Synchronous Serial Engine
PD	Power Delivery
PDO	Power Data Object
PLD	Programmable Logic Device
QFN	Quad Flat No-Lead
SPI	Serial Peripheral Interface
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver/Transmitter
UTMI	Universal Transceiver Macrocell Interface
VCP	Virtual COM Ports

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Appendix C – Revision History

Document Title: FT4233HP/FT4232HP Datasheet

Document Reference No.: FT_001473

Clearance No.: FTDI#555

Product Page: https://ftdichip.com/product-category/products/

Document Feedback: Send Feedback

Revision	Changes	Date
Draft	Initial Release	03-06-2020
1.0	Update the Figure #12 caption Updated terms in section 4.6.2 and 4.6.4	02-07-2020
1.1	Updated the following: - Packing details for reel and tray in section 1.2 - vConn power in section 4.2 - vConn swap support has been removed in section 4.6.2 - circuit diagram and description in section 4.6.5 - Tables in section 5.2 - Table 15 in Section 5.3 with latest spec - Latency Timer description in Section 4.1 - Added new Chapter 7 for EEPROM configuration - Document References section	14-05-2020
1.2	Updated Release – Removed Thermal Characteristics; Removed Solder Reflow; Updated Fig 12; Corrected 20v5A to 20V3A; Updated package dimension for QFN68; Update tables in section 5; Added section 7 to cover configuration	21-11-2021
1.3	Updated the datasheet to address the internal and external feedback.	22-06-2022
1.4	Updated Table 20 VOL spec and removed 500uA current requirement in suspend.	22-02-2023
1.5	Added 20V/5A sink support. Added Fast Role Swap support from sink to source. Updated Package Dimensions. Removed references to HPL package. Removed first bullet in section 1 "(source and devices)"	27-09-2023
1.6	Updated VCONN power support. Added note on central solder pad grounding. Added note on GPIO0 and GPIO1 when the EEPROM is blank or there is no EEPROM fitted.	19-06-2024
1.7	Updated MTTF value.	06-09-2024
1.8	Removed the text for VREGIN to be connected to VREGOUT as VREGIN is not a 1.2V supply, section 4.2 LDO Regulator. Added the minimum EEPROM size to be 4Kb in sections 8 EEPROM Configuration and 4.2 EEPROM Interface. Added support for dead battery mode in page 1 and section 4.6.2. Added MTBF acronym to Table 18 and added FIT value. Updated Figure 7 (CLKOUT to TCK) Updated t6 in Table 10 to be a maximum rather than minimum. Added comment to 'Max Bus Power Current' in Table 25.	15-09-2025

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Revision	Changes	Date
	Added PDO to Acronymns table. Updated contact information.	

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