

MOSFET – Power, Single N-Channel Logic Level, DPAK

60 V, 54 A, 17 mΩ

NVD5484NL

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- High Current Capability
- Avalanche Energy Specified
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current $R_{\theta JC}$ (Notes 1 & 3)	$T_C = 25^\circ\text{C}$ 54 $T_C = 100^\circ\text{C}$ 38	A
P_D	Power Dissipation $R_{\theta JC}$ (Note 1)	$T_C = 25^\circ\text{C}$ 100 $T_C = 100^\circ\text{C}$ 50	W
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2 & 3)	$T_A = 25^\circ\text{C}$ 10.7 $T_A = 100^\circ\text{C}$ 7.6	A
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)	$T_A = 25^\circ\text{C}$ 3.9 $T_A = 100^\circ\text{C}$ 2.0	W
I_{DM}	Pulsed Drain Current	$T_A = 25^\circ\text{C}$, $t_p = 10 \mu\text{s}$ 305	A
I_{Dmaxpk}	Current Limited by Package (Note 3)	$T_A = 25^\circ\text{C}$ 60	A
T_J, T_{stg}	Operating Junction and Storage Temperature	-55 to +175	$^\circ\text{C}$
I_S	Source Current (Body Diode)	83	A
E_{AS}	Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}$, $V_{DD} = 50 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_L(pk) = 50 \text{ A}$, $L = 0.1 \text{ mH}$, $R_G = 25 \Omega$)	125	mJ
T_L	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	260	$^\circ\text{C}$

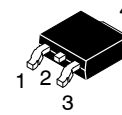
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

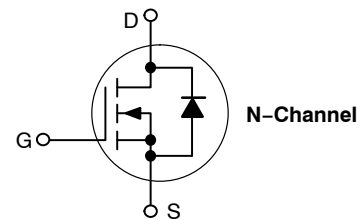
Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State (Drain)	1.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 2)	38	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

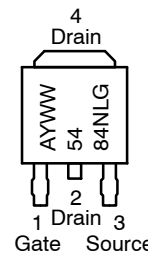
$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
60 V	17 mΩ @ 10 V 23 mΩ @ 4.5 V	54 A



DPAK
CASE 369AA
STYLE 2



MARKING DIAGRAMS & PIN ASSIGNMENT



A = Assembly Location*
Y = Year
WW = Work Week
5484NL = Device Code
G = Pb-Free Package

* The Assembly Location Code (A) is front side optional. In cases where the Assembly Location is stamped in the package bottom (molding ejector pin), the front side assembly code may be blank.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60	–	–	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}$	$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$	– –	1.0 10	μA
I_{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	–		± 100	nA

ON CHARACTERISTICS (Note 4)

$V_{GS(TH)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.5	1.9	2.5	V
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 25\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 25\text{ A}$	– –	13.5 18	17 23	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$	–	41	–	S

CHARGES AND CAPACITANCES

C_{iss}	Input Capacitance	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 25\text{ V}$	–	1410	–	pF
C_{oss}	Output Capacitance		–	315	–	
C_{rss}	Reverse Transfer Capacitance		–	135	–	
$Q_{G(TOT)}$	Total Gate Charge	$V_{DS} = 48\text{ V}, I_D = 23\text{ A}$	$V_{GS} = 4.5\text{ V}$ $V_{GS} = 10\text{ V}$	– –	27 48	nC
$Q_{G(TH)}$	Threshold Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V}, I_D = 23\text{ A}$	–	0.9	–	
Q_{GS}	Gate-to-Source Charge		–	4.4	–	
Q_{GD}	Gate-to-Drain Charge		–	19	–	
R_G	Gate Resistance		–	8.5		Ω

SWITCHING CHARACTERISTICS (Note 5)

$t_{d(on)}$	Turn-On Delay Time	$V_{GS} = 4.5\text{ V}, V_{DS} = 48\text{ V}, I_D = 23\text{ A}, R_G = 10\text{ }\Omega$	–	18	–	ns
t_r	Rise Time		–	160	–	
$t_{d(off)}$	Turn-Off Delay Time		–	100	–	
t_f	Fall Time		–	110	–	
$t_{d(on)}$	Turn-On Delay Time	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V}, I_D = 23\text{ A}, R_G = 10\text{ }\Omega$	–	7.8	–	
t_r	Rise Time		–	45	–	
$t_{d(off)}$	Turn-Off Delay Time		–	152	–	
t_f	Fall Time		–	113	–	

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Forward Diode Voltage	V _{GS} = 0 V, I _S = 25 A	T _J = 25°C	–	0.9	1.2	V
			T _J = 125°C	–	0.8	–	
t _{RR}	Reverse Recovery Time	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 23 A		–	64	–	ns
t _a	Charge Time			–	33	–	
t _b	Discharge Time			–	31	–	
Q _{RR}	Reverse Recovery Charge			–	118	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures.



TYPICAL CHARACTERISTICS

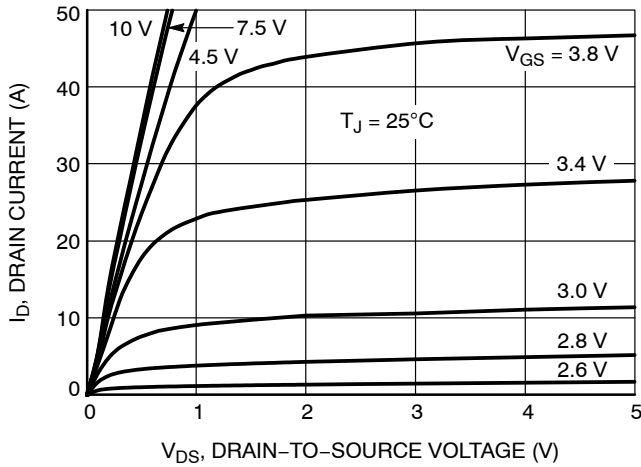


Figure 1. On-Region Characteristics

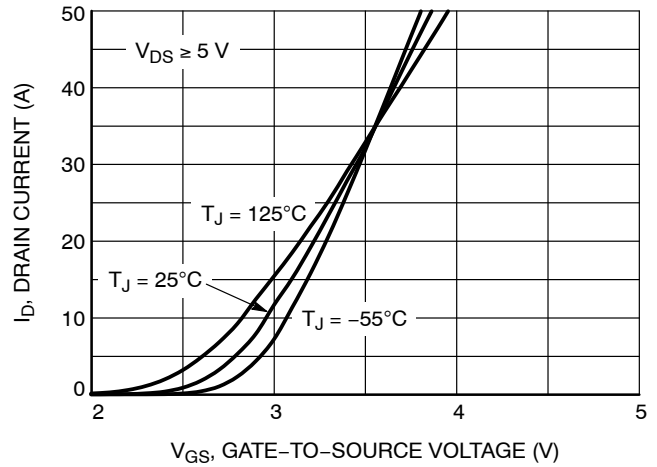


Figure 2. Transfer Characteristics

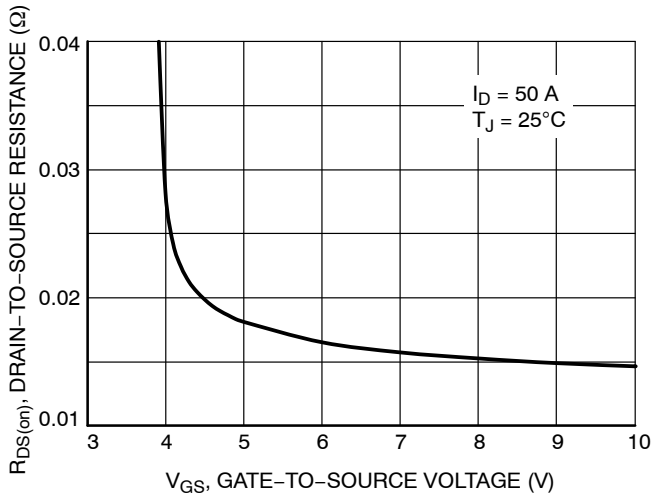


Figure 3. On-Resistance vs. Gate-to-Source Voltage

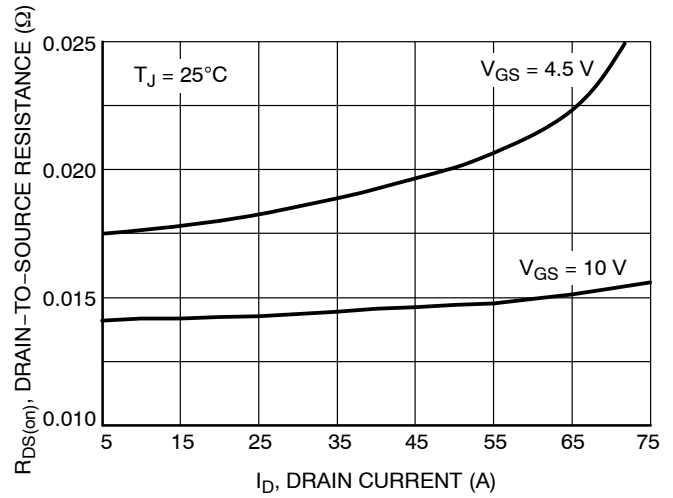


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

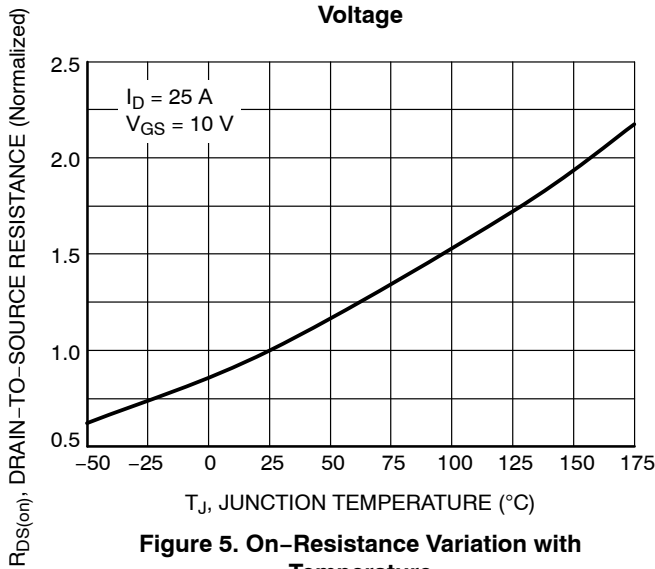


Figure 5. On-Resistance Variation with Temperature

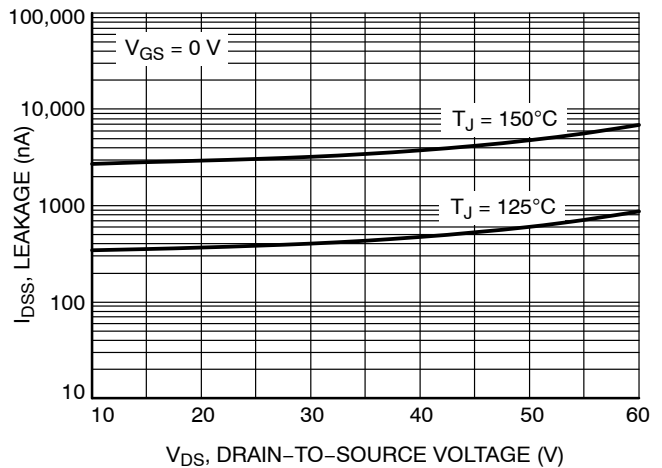


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS (continued)

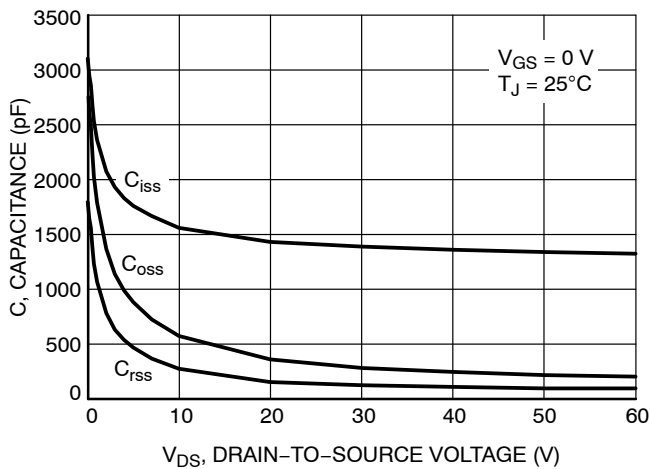


Figure 7. Capacitance Variation

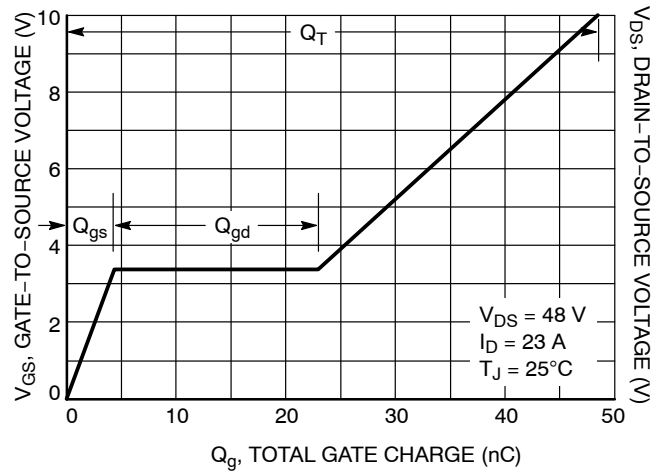


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

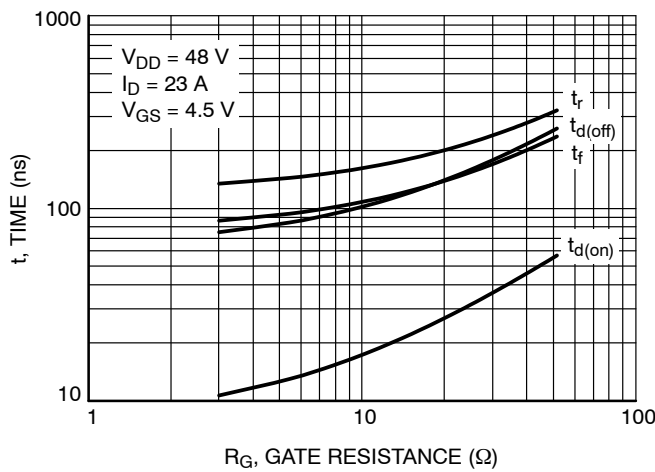


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

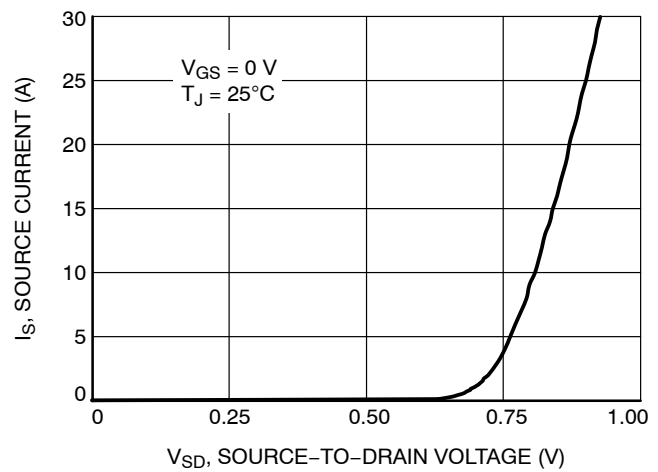


Figure 10. Diode Forward Voltage vs. Current

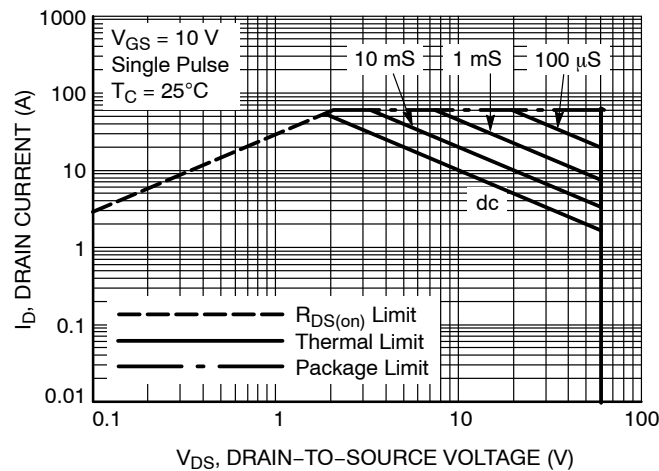


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS (continued)

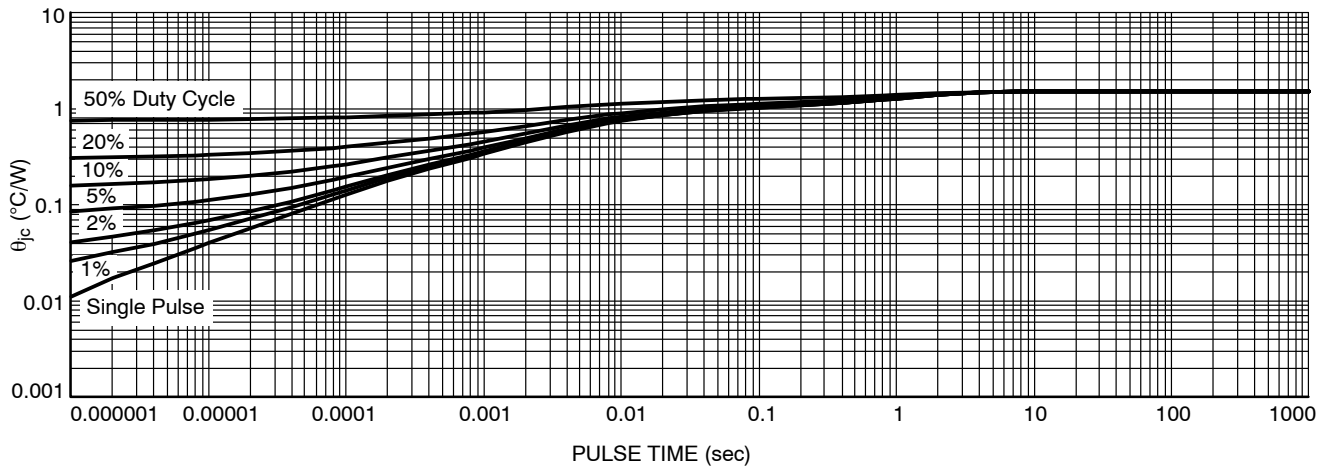


Figure 12. Thermal Response

ORDERING INFORMATION

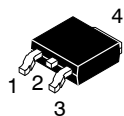
Order Number	Package	Shipping [†]
NVD5484NLT4G-VF01	DPAK (Pb-Free)	2500 / Tape & Reel

DISCONTINUED (Note 6)

NVD5484NLT4G	DPAK (Pb-Free)	2500 / Tape & Reel
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[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

6. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.



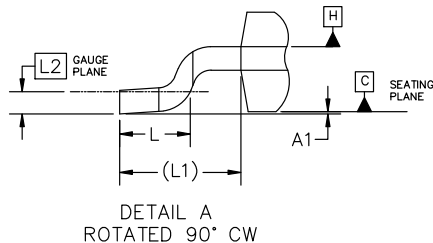
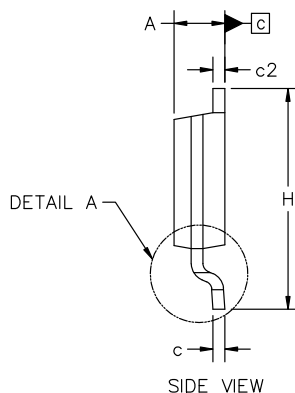
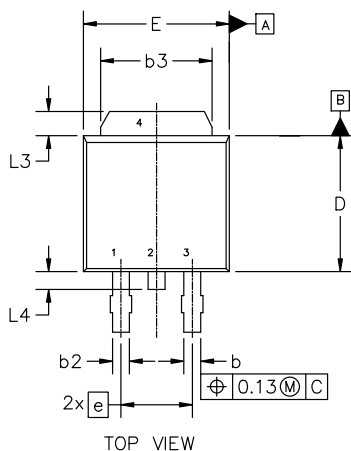
SCALE 1:1

DPAK-3 6.10x6.54x2.28, 2.29P
CASE 369AA
ISSUE C

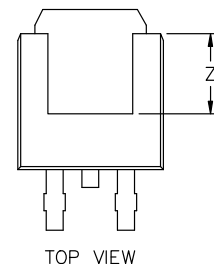
DATE 14 MAY 2026

NOTES

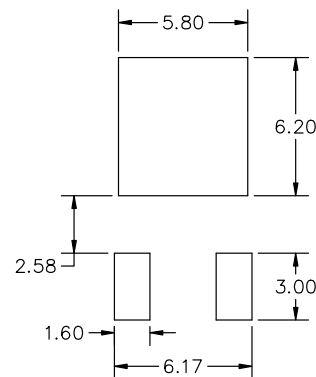
1. DIMENSION AND TOLERANCING PER ASME Y14.5 2018
2. CONTROLLING DIMENSION: MILLIMETERS
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION b3, L3, AND Z
4. DIMENSION D AND E DO NOT INCLUDED MOLD FLASH, PROTRUSION, OR BURRS.
5. DIMENSION D AND E ARE DETERMINED AT OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H



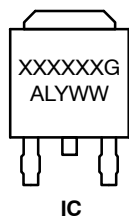
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.76	0.95	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.74 REF		
L2	0.51 BSC		
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---



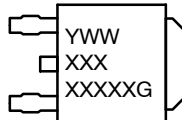
RECOMMENDED
MOUNTING FOOTPRINT



GENERIC
MARKING DIAGRAM*



IC



Discrete

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	DPAK-3 6.10x6.54x2.28, 2.29P	PAGE 1 OF 1

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