SN74LV4052A Dual 4-Channel Analog Multiplexers and Demultiplexers

1 Features

- 1.65V to 5.5V V_{CC} operation
- Fast switching
- High on-off output-voltage ratio
- Low crosstalk between switches
- Extremely low input current
- Latch-up performance exceeds 100mA per JESD 78, class II
- ESD protection exceeds JESD 22:
  - 2000V human-body model (A114-A)
  - 1000V charged-device model (C101)

2 Applications

- Telecommunications
- Infotainment
- Signal gating and isolation
- Home appliances
- Programmable logic circuits
- Modulation and demodulation

3 Description

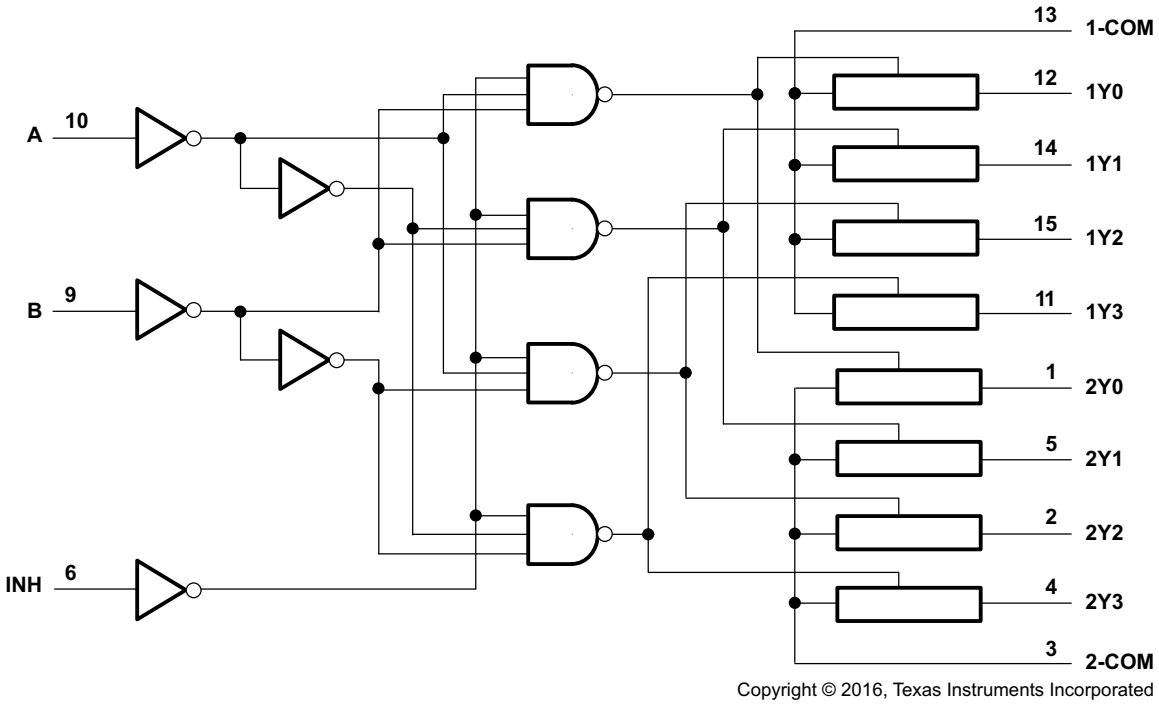
The SNx4LV4052A device is a dual, 4-channel CMOS analog multiplexer and demultiplexer that is designed for 1.65V to 5.5V V_{CC} operation.

The SNx4LV4052A device handles both analog and digital signals. Each channel permits signals with amplitudes up to 5.5V (peak) to be transmitted in either direction.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE (2)
SNx4LV4052A	D (SOIC, 16)	9.9mm × 6mm
	PW (TSSOP, 16)	5mm × 6.4mm
	RGY (VQFN, 16)	4mm × 3.5mm
	DYY (SOT-23-THIN, 16)	4.2mm x 3.26mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)

Table of Contents

4 Pin Configuration and Functions

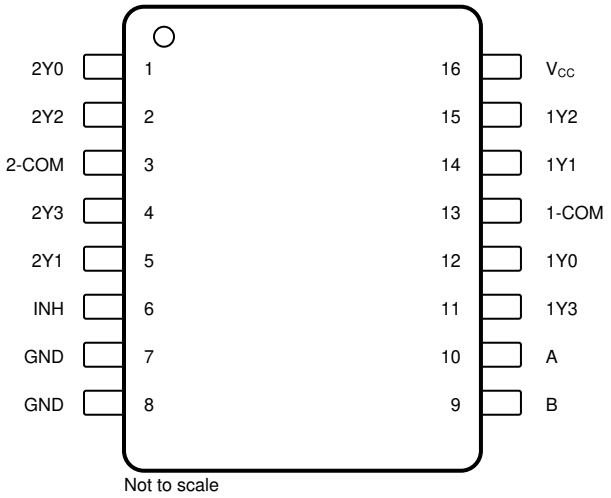


Figure 4-1. D, PW, or DYY Packages, 16-Pin SOIC, TSSOP, or SOT-23-THIN (Top View)

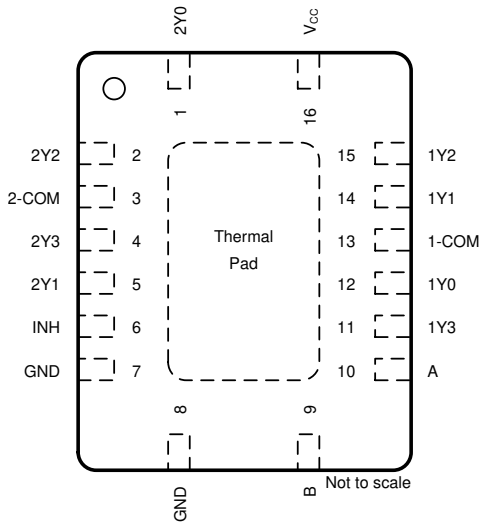


Figure 4-2. RGY Package, 16-Pin VQFN With Thermal Pad (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
2Y0	1	I/O	Port 2 channel 0
2Y2	2	I/O	Port 2 channel 2
2-COM	3	I/O	Port 2 common channel
2Y3	4	I/O	Port 2 channel 3
2Y1	5	I/O	Port 2 channel 1
INH	6	I	Inhibit input
GND	7	—	Device ground
GND	8	—	Device ground
B	9	I	Logic input selector B
A	10	I	Logic input selector A
1Y3	11	I/O	Port 1 channel 3
1Y0	12	I/O	Port 1 channel 0
1-COM	13	I/O	Port 1 common channel
1Y1	14	I/O	Port 1 channel 1
1Y2	15	I/O	Port 1 channel 2
V_{CC}	16	—	Device power

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7.0	V
V_I	Logic input voltage range		–0.5	7.0	V
V_{IO}	Switch I/O voltage range(2) (3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0	–20		mA
I_{IOK}	Switch IO diode clamp current	V_{IO} < 0 or V_{IO} > V_{CC}	–50	50	mA
I_T	Switch continuous current	V_{IO} = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(3) This value is limited to 5.5 V maximum

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	All pins	±4000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±2000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Thermal Information: SN74LV4052A

THERMAL METRIC (1)		SN74LV4052A D (SOIC) 16 PINS	SN74LV4052A PW (TSSOP) 16 PINS	SN74LV4052A RGY (VQFN) 16 PINS	SN74LV4052A DYY (SOT) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.2	140.2	89.4	199.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75.0	72.6	89.7	121.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	76.6	98.7	65.4	129.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	31.3	13.4	25.0	24.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	75.7	97.3	65.2	126.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	48.9	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		1(2)		5.5	V
V_{IH}	High-level input voltage, logic control inputs	V_{CC} = 1.65	1.2		5.5	V
		V_{CC} = 2 V	1.5		5.5	
		V_{CC} = 2.3 V to 2.7 V	V_{CC} x 0.7		5.5	
		V_{CC} = 3 V to 3.6 V	V_{CC} x 0.7		5.5	
		V_{CC} = 4.5 V to 5.5 V	V_{CC} x 0.7		5.5	
V_{IL}	Low-level input voltage, logic control inputs	V_{CC} = 1.65	0		0.4	V
		V_{CC} = 2 V	0		0.5	
		V_{CC} = 2.3 V to 2.7 V	0		V_{CC} x 0.3	
		V_{CC} = 3 V to 3.6 V	0		V_{CC} x 0.3	
		V_{CC} = 4.5 V to 5.5 V	0		V_{CC} x 0.3	
V_I	Logic control input voltage		0		5.5	V
V_{IO}	Switch input or output voltage		0		V_{CC}	V
Δt/ΔV	Logic input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V			200	ns/V
		V_{CC} = 3 V to 3.6 V			100	
		V_{CC} = 4.5 V to 5.5 V			20	
T_A	Ambient temperature		–40		125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, SCBA004.
(2) When using a V_{CC} of ≤1.2 V, it is recommended to use these devices only for transmitting digital signals. When supply voltage is near 1.2 V the analog switch ON resistance becomes very non-linear

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		Condition	T_A	V_{CC}	MIN	TYP	MAX	UNIT
r_{ON}	ON-state switch resistance	I_T = 2 mA, V_I = V_{CC} or GND, V_{INH} = V_{IL}	25°C	1.65 V		60	150	Ω
r_{ON}	ON-state switch resistance	I_T = 2 mA, V_I = V_{CC} or GND, V_{INH} = V_{IL}	–40°C to 85°C	1.65 V			225	Ω
r_{ON}	ON-state switch resistance	I_T = 2 mA, V_I = V_{CC} or GND, V_{INH} = V_{IL}	–40°C to 125°C	1.65 V			225	Ω
r_{ON}	ON-state switch resistance	I_T = 2 mA, V_I = V_{CC} or GND, V_{INH} = V_{IL}	25°C	2.3 V		38	180	Ω
			–40°C to 85°C				225	
			–40°C to 125°C				225	
			25°C	3 V		30	150	Ω
			–40°C to 85°C				190	
			–40°C to 125°C				190	
			25°C	4.5 V		22	75	Ω
			–40°C to 85°C				100	
			–40°C to 125°C				100	
$r_{ON(p)}$	Peak ON-state resistance	I_T = 2 mA, V_I = GND to V_{CC}, V_{INH} = V_{IL}	25°C	1.65 V		220	600	Ω

5.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		Condition	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$r_{ON(p)}$	Peak ON-state resistance	I_T = 2 mA, V_I = GND to V_{CC}, V_{INH} = V_{IL}	–40°C to 85°C	1.65 V			700	Ω
$r_{ON(p)}$	Peak ON-state resistance	I_T = 2 mA, V_I = GND to V_{CC}, V_{INH} = V_{IL}	–40°C to 125°C	1.65 V			700	Ω
$r_{ON(p)}$	Peak ON-state resistance	I_T = 2 mA, V_I = GND to V_{CC}, V_{INH} = V_{IL}	25°C	2.3 V		113	500	Ω
			–40°C to 85°C				600	
			–40°C to 125°C				600	
			25°C	3 V		54	180	Ω
			–40°C to 85°C				225	
			–40°C to 125°C				225	
			25°C	4.5 V		31	100	Ω
			–40°C to 85°C				125	
			–40°C to 125°C				125	
Δr_{ON}	Difference in ON-state resistance between switches	I_T = 2 mA, V_I = GND to V_{CC}, V_{INH} = V_{IL}	25°C	1.65 V		3	40	Ω
Δr_{ON}	Difference in ON-state resistance between switches	I_T = 2 mA, V_I = GND to V_{CC}, V_{INH} = V_{IL}	–40°C to 85°C	1.65 V			50	Ω
Δr_{ON}	Difference in ON-state resistance between switches	I_T = 2 mA, V_I = GND to V_{CC}, V_{INH} = V_{IL}	–40°C to 85°C	1.65 V			50	Ω
Δr_{ON}	Difference in ON-state resistance between switches	I_T = 2 mA, V_I = GND to V_{CC}, V_{INH} = V_{IL}	25°C	2.3 V		2.1	30	Ω
			–40°C to 85°C				40	
			–40°C to 125°C				40	
			25°C	3 V		1.4	20	Ω
			–40°C to 85°C				30	
			–40°C to 125°C				30	
			25°C	4.5 V		1.3	15	Ω
			–40°C to 85°C				20	
			–40°C to 125°C				20	
I_{IH} I_{IL}	Control input current	V_I = 5.5 V or GND	25°C	0 to 5.5 V			0.1	μA
			–40°C to 85°C				1	
			–40°C to 125°C				2	
$I_{S(off)}$	OFF-state switch leakage current	V_I = V_{CC} and V_O = GND, or V_I = GND and V_O = V_{CC}, V_{INH} = V_{IH}	25°C	5.5 V			0.1	μA
			–40°C to 85°C				1	
			–40°C to 125°C				2	
$I_{S(on)}$	ON-state switch leakage current	V_I = V_{CC} or GND, V_{INH} = V_{IL} (see Figure4)	25°C	5.5 V			0.1	μA
			–40°C to 85°C				1	
			–40°C to 125°C				2	
I_{CC}	Supply current	V_I = V_{CC} or GND V_{INH} = 0 V	25°C	5.5 V		0.01		μA
			–40°C to 85°C				20	
			–40°C to 125°C				40	
C_{IC}	Control input capacitance	f = 10 MHz	25°C	3.3 V		2		pF

5.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		Condition	T_A	V_{CC}	MIN	TYP	MAX	UNIT
C_{OS}	Switch terminal capacitance	f = 10 MHz	25°C	3.3 V		5		pF
C_{IS}	Common ternminal capacitance	f = 10 MHz	25°C	3.3 V		23		pF
$C_{OS(on)}$	Common ternminal ON-capacitance	f = 10 MHz	25°C	3.3 V		23		pF
C_F	Feedthrough capacitance	f = 10 MHz	25°C	3.3 V		0.5		pF
C_{PD}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	25°C	3.3 V		6		pF

5.6 Timing Characteristics V_{CC} = 2.5 V ± 0.2 V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 15 pF	25°C		1.9	10	ns
					–40°C to 85°C			16	
					–40°C to 125°C			18	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 15 pF	25°C		6.6	18	ns
					–40°C to 85°C			23	
					–40°C to 125°C			25	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 15 pF	25°C		7.4	18	ns
					–40°C to 85°C			23	
					–40°C to 125°C			25	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50 pF	25°C		3.8	12	ns
					–40°C to 85°C			18	
					–40°C to 125°C			20	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50 pF	25°C		7.8	28	ns
					–40°C to 85°C			35	
					–40°C to 125°C			35	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50 pF	25°C		11.5	28	ns
					–40°C to 85°C			35	
					–40°C to 125°C			35	

5.7 Timing Characteristics V_{CC} = 3.3 V ± 0.3 V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 15 pF	25°C		1.2	6	ns
					–40°C to 85°C			10	
					–40°C to 125°C			12	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 15 pF	25°C		4.7	12	ns
					–40°C to 85°C			15	
					–40°C to 125°C			18	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 15 pF	25°C		5.7	12	ns
					–40°C to 85°C			15	
					–40°C to 125°C			18	

5.7 Timing Characteristics V_{CC} = 3.3 V ± 0.3 V (continued)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50 pF	25°C		2.5	9	ns
					–40°C to 85°C			12	
					–40°C to 125°C			14	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50 pF	25°C		5.5	20	ns
					–40°C to 85°C			25	
					–40°C to 125°C			25	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50 pF	25°C		8.8	20	ns
					–40°C to 85°C			25	
					–40°C to 125°C			25	

5.8 Timing Characteristics V_{CC} = 5 V ± 0.5 V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 15 pF	25°C		0.6	4	ns
					–40°C to 85°C			7	
					–40°C to 125°C			10	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 15 pF	25°C		3.5	8	ns
					–40°C to 85°C			10	
					–40°C to 125°C			12	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 15 pF	25°C		4.4	10	ns
					–40°C to 85°C			11	
					–40°C to 125°C			12	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50 pF	25°C		1.5	6	ns
					–40°C to 85°C			8	
					–40°C to 125°C			10	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50 pF	25°C		4	14	ns
					–40°C to 85°C			18	
					–40°C to 125°C			18	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50 pF	25°C		6.2	14	ns
					–40°C to 85°C			18	
					–40°C to 125°C			18	

5.9 AC Characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Device	CONDITIONS		MIN	TYP	MAX	UNIT
Frequency response (switch on)	COM or Yn	Yn or COM	SN74LV4052	C_L = 50 pF, R_L = 600 Ω, F_{in} = 1 MHz (sine wave) see Figure 7)(1)	V_{CC} = 2.3 V		30		MHz
					V_{CC} = 3 V		35		
					V_{CC} = 4.5 V		50		
Charge Injection (control input to signal output)	INH	COM or Yn		C_L = 50 pF, R_L = 600 Ω, F_{in} = 1 MHz (sine wave) (see Figure 9)	V_{CC} = 2.3 V		20		mV
					V_{CC} = 3 V		35		
					V_{CC} = 4.5 V		60		

5.9 AC Characteristics (continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Device	CONDITIONS		MIN	TYP	MAX	UNIT
Feedthrough attenuation (switch off)	COM or Yn	Yn or COM		C_L = 50 pF, R_L = 600 Ω, F_{in} = 1 MHz (sine wave) (see Figure 10) (2)	V_{CC} = 2.3 V		–45		dB
					V_{CC} = 3 V		–45		
					V_{CC} = 4.5 V		–45		
Crosstalk (between any switches)	COM or Yn	Yn or COM		C_L = 50 pF, R_L = 600 Ω, F_{in} = 1 MHz (sine wave) (see Figure 8)(2)	V_{CC} = 2.3 V		–45		dB
					V_{CC} = 3 V		–45		
					V_{CC} = 4.5 V		–45		
Sine-wave distortion	COM or Yn	Yn or COM		C_L = 50 pF, R_L = 10 kΩ, F_{in} = 1 kHz (sine wave) (see Figure 11)	V_I = 2 V_{p-p} V_{CC} = 2.3 V		0.1		%
					V_I = 2.5 V_{p-p} V_{CC} = 3 V		0.1		
					V_I = 4 V_{p-p} V_{CC} = 4.5 V		0.1		

5.10 Typical Characteristics

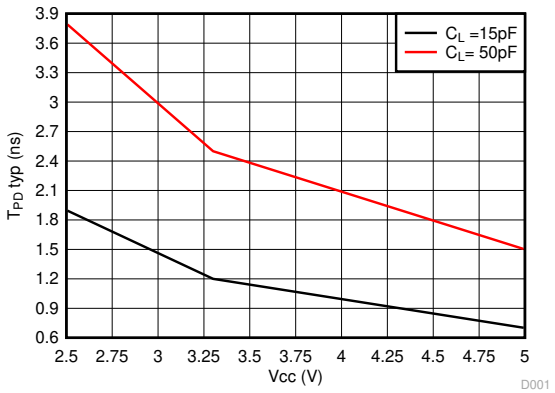


Figure 5-1. Typical Propagation Delay vs V_{cc}

6 Parameter Measurement Information

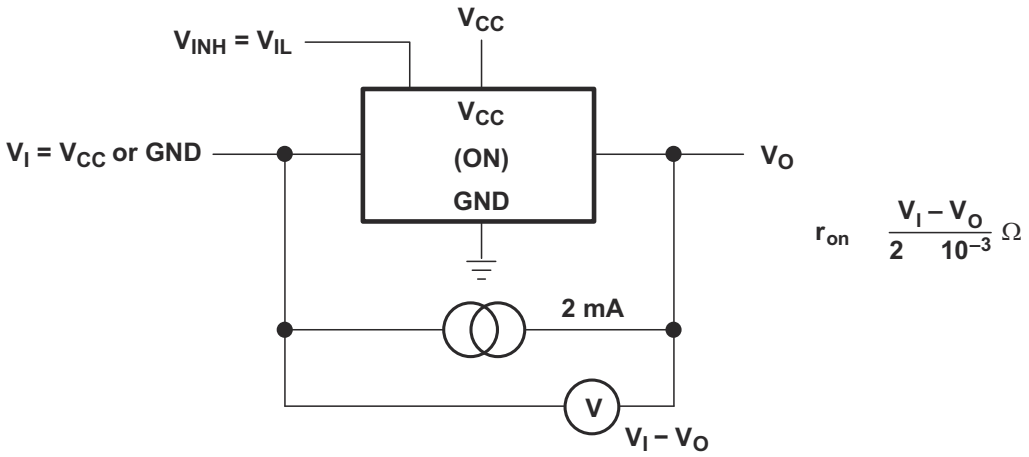
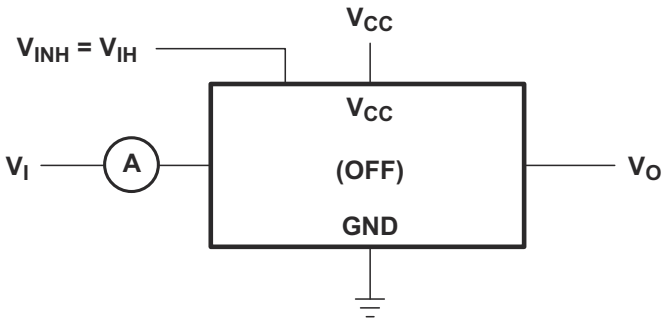


Figure 6-1. ON-State Resistance Test Circuit



Condition 1: $V_I = 0$, $V_O = V_{CC}$
Condition 2: $V_I = V_{CC}$, $V_O = 0$

Figure 6-2. OFF-State Switch Leakage-Current Test Circuit

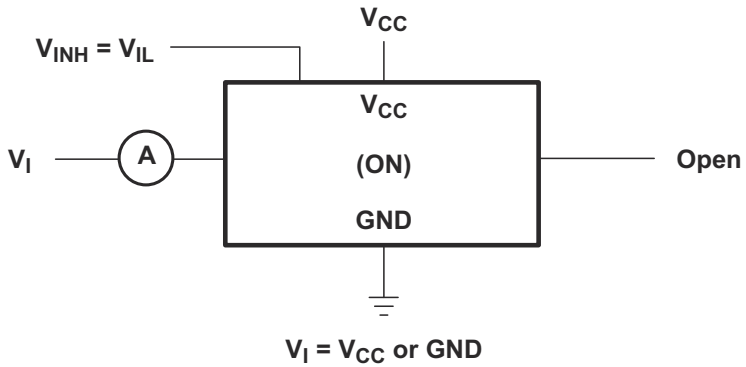


Figure 6-3. ON-State Switch Leakage-Current Test Circuit

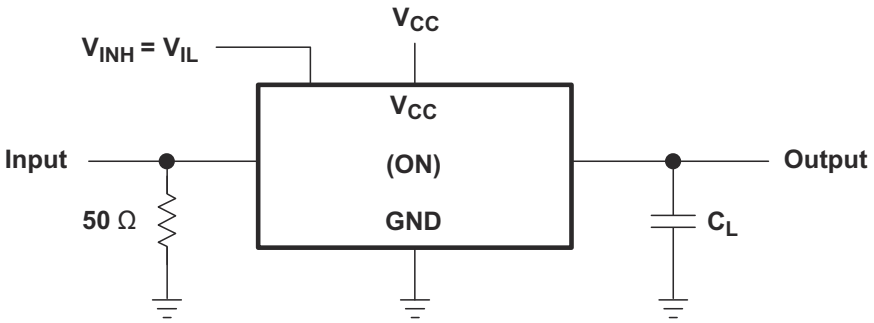
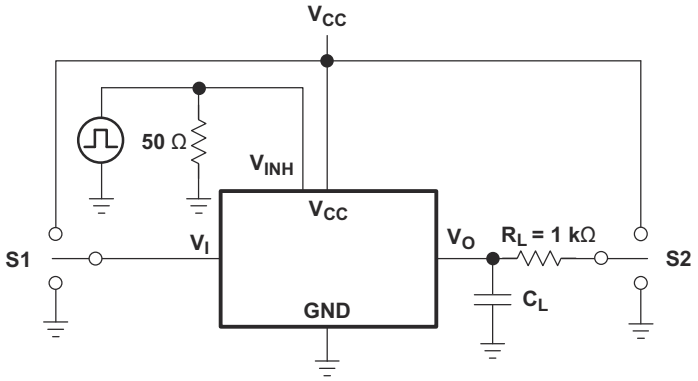
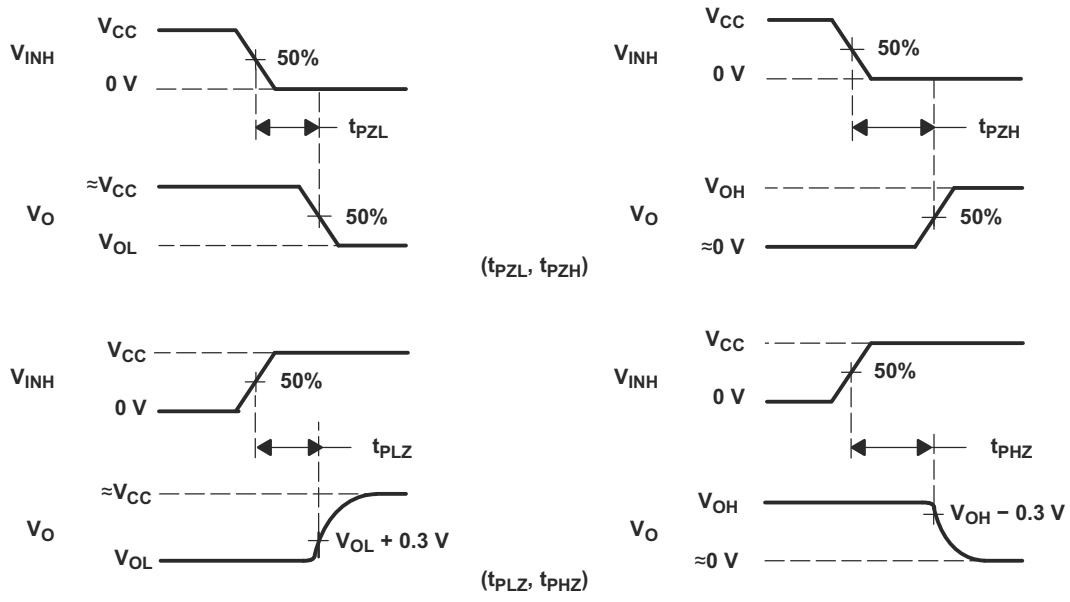


Figure 6-4. Propagation Delay Time, Signal Input to Signal Output



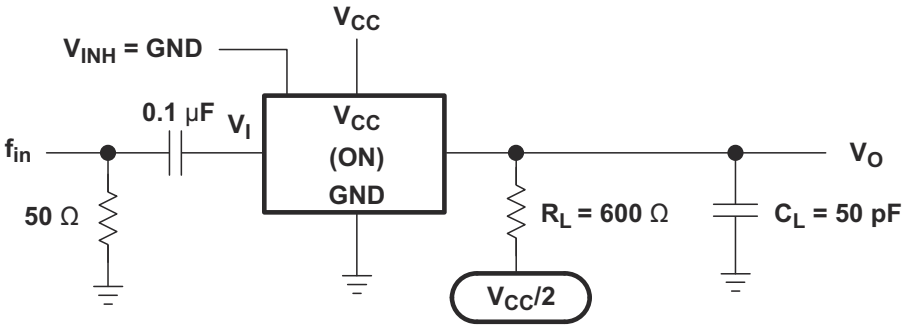
TEST	S1	S2
t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	GND V_{CC}	V_{CC} GND

TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 6-5. Switching Time (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), Control to Signal Output



NOTE A: f_{in} is a sine wave.

Figure 6-6. Frequency Response (Switch ON)

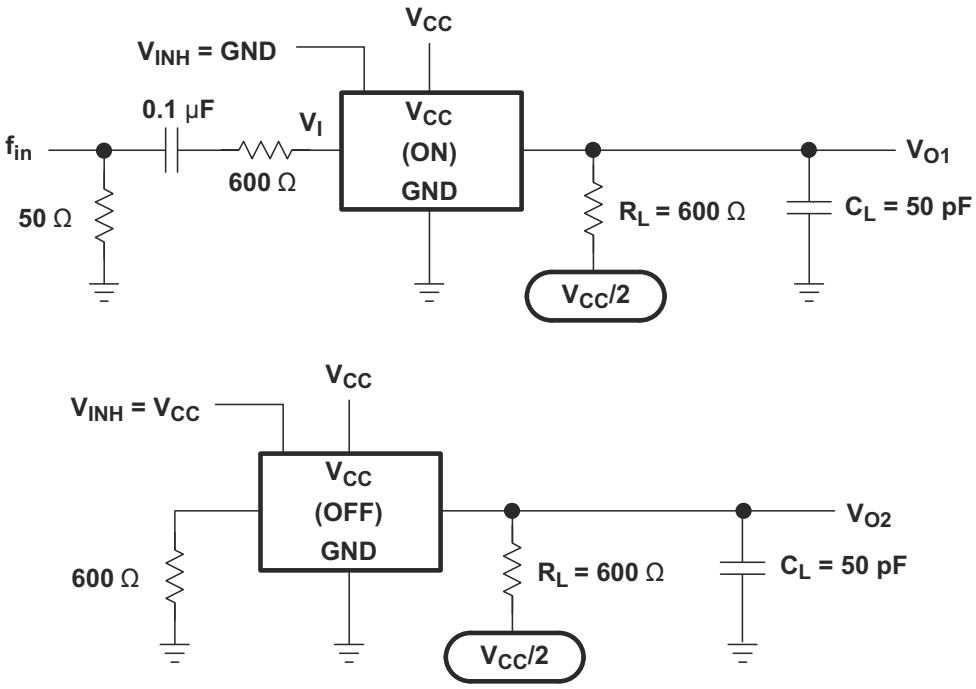


Figure 6-7. Crosstalk Between Any Two Switches

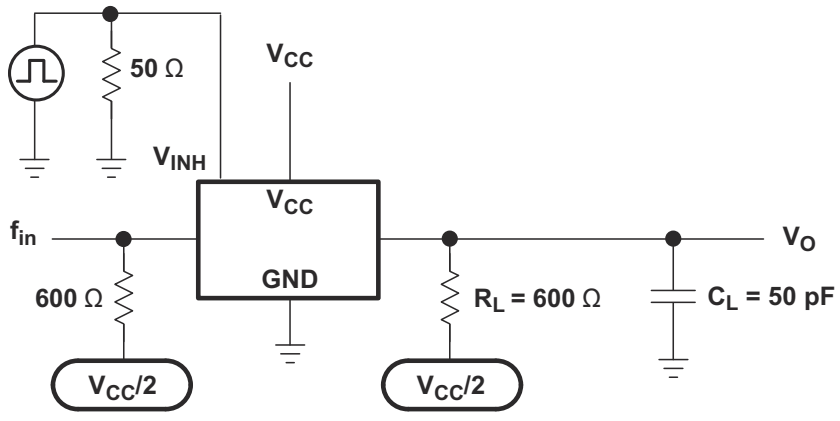


Figure 6-8. Crosstalk Between Control Input and Switch Output

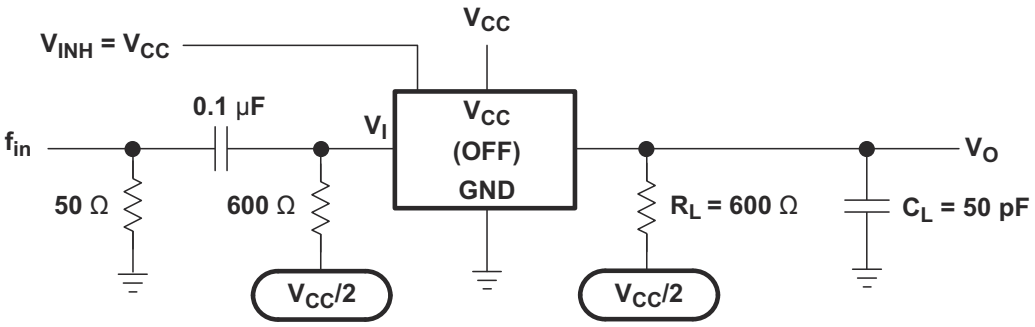


Figure 6-9. Feedthrough Attenuation (Switch OFF)

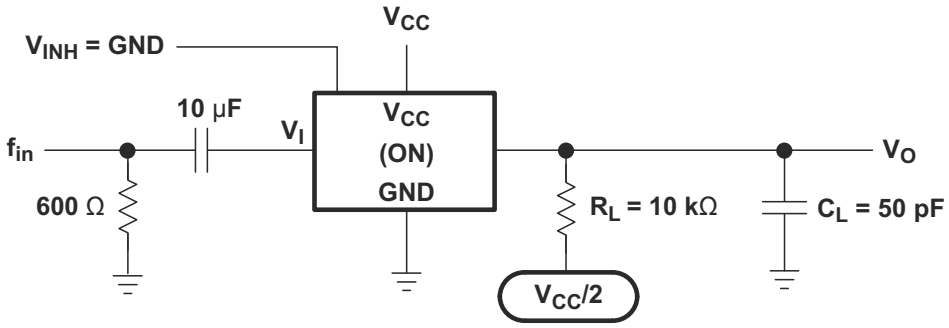


Figure 6-10. Sine-Wave Distortion

7 Detailed Description

7.1 Overview

The SNx4LV4052A device is a dual, 4-channel CMOS analog multiplexer and demultiplexer that is designed for 2V to 5.5V V_{CC} operation. It has low input current consumption at the digital input pins and low crosstalk between switches. The active low Inhibit (INH) tri-state all the channels when high and when low, depending on the A and B inputs, one of the four independent input/outputs (nY0 - nY3) connects to the COM channel. The SNx4LV4052A is available in multiple package options including TSSOP (PW), SOIC (D), DYY (SOT-23-THIN) and QFN (RGY).

7.2 Functional Block Diagram

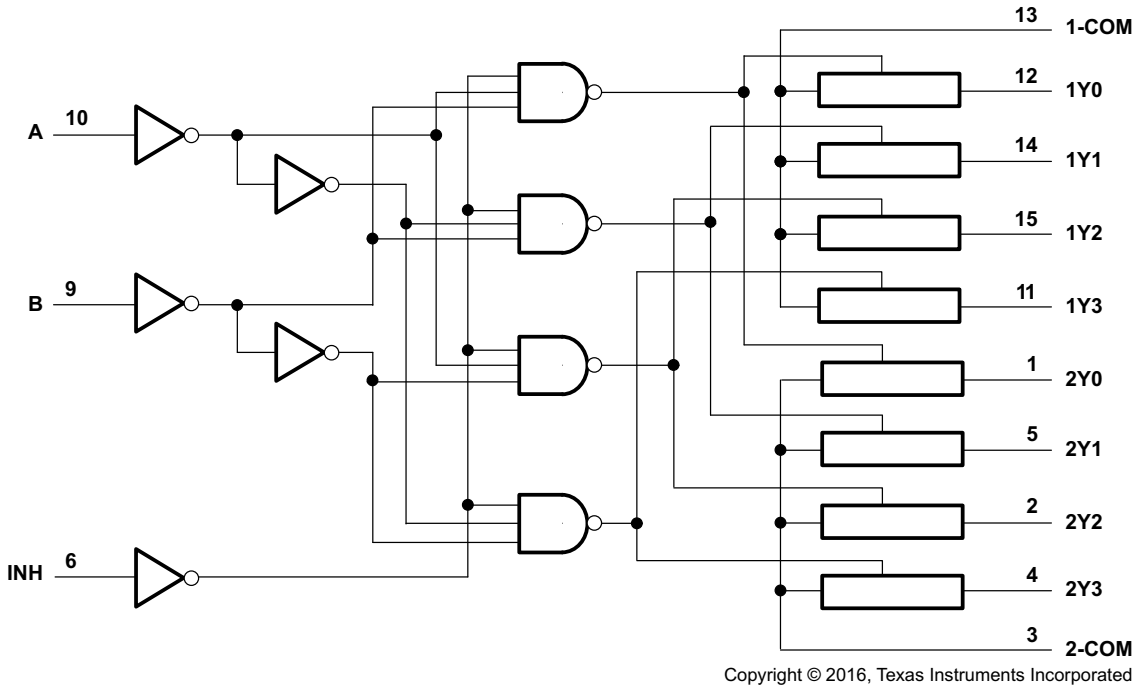


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

- The SNx4LV4052A operates from 2V to 5.5V V_{CC} with extremely low input current consumption at the CMOS input pins of A, B and INH.
- The SNx4LV4052A enables fast switching with low crosstalk between the switches. 5.5V peak level bidirectional transmission allowed with the either analog or digital signals.

7.4 Device Functional Modes

Table 7-1 lists the functional modes of SNx4LV4052A.

Table 7-1. Function Table

INPUTS			ON CHANNELS
INH	B	A	
L	L	L	1Y0, 2Y0
L	L	H	1Y1, 2Y1
L	H	L	1Y2, 2Y2
L	H	H	1Y3, 2Y3
H	X	X	None

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

Typical applications for the SNx4LV4052A include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

8.2 Typical Application

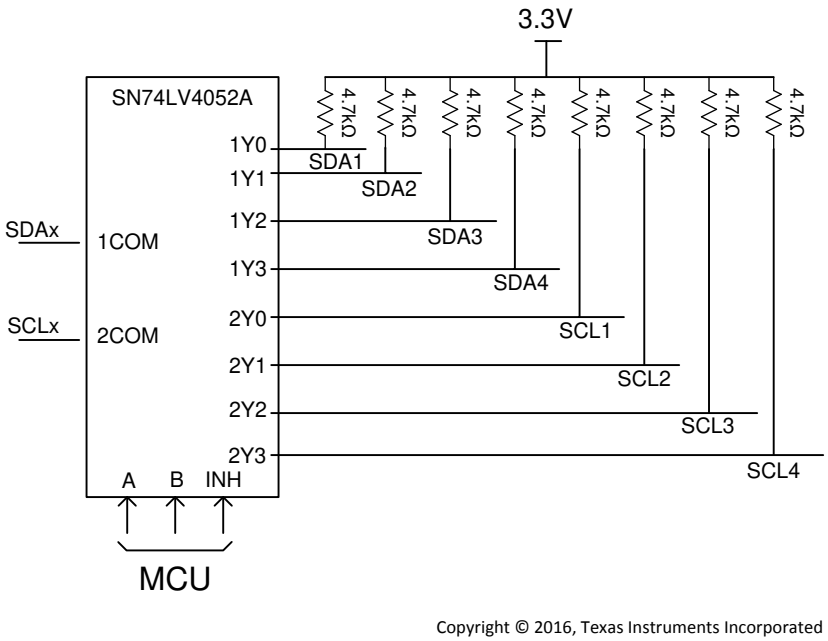


Figure 8-1. Typical I²C Multiplexing Application

8.2.1 Design Requirements

Designing with the SNx4LV4052A device requires a stable input voltage between 2V and 5.5V (see *Recommended Operating Conditions* for details). Another important design consideration are the characteristics of the signal being multiplexed—ensure no important information is lost due to timing or incompatibility with this device.

8.2.2 Detailed Design Procedure

The SNx4LV4052A dual 1- to 4-channel multiplexer is an excellent choice for I²C selection. The I²C data and clock lines are selected using A,B select lines from the MCU. The pullup resistors are selected based on the capability of the driver. Low pullup resistor results in faster rise time; however, it generates additional current during the low state into the driver. See the *Recommended Operating Conditions* for the input transition rates (V_{IH} and V_{IL}) of the CMOS inputs.

8.2.3 Application Curve

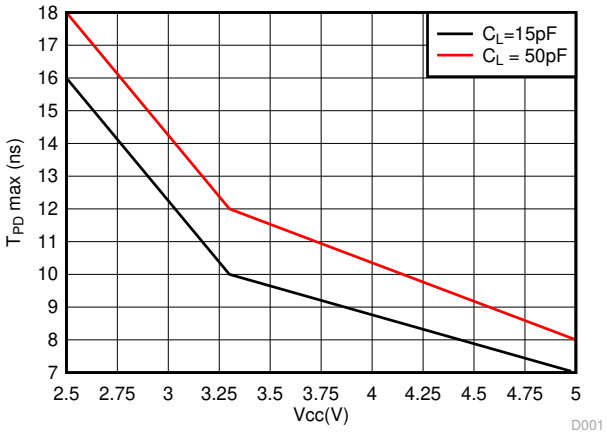


Figure 8-2. Maximum Propagation Delay vs V_{cc}

8.3 Power Supply Recommendations

Most systems have a common 3.3V or 5V rail that can supply the V_{CC} pin of this device. If this rail is not available, a switched-mode power supply (SMPS) or a low dropout regulator (LDO) can supply this device from a higher-voltage rail.

See the *Recommended Operating Conditions* for operating voltage range for this device. Having bypass capacitors of 0.1µF is highly recommended.

8.4 Layout

8.4.1 Layout Guidelines

TI recommends keeping the signal lines as short and as straight as possible (see Figure 8-3). Incorporation of microstrip or stripline techniques are also recommended when signal lines are more than 1 in. long. These traces must be designed with a characteristic impedance of either 50Ω or 75Ω as required by the application.

Do not place this device too close to high-voltage switching components because they may cause interference. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 8-4 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

8.4.2 Layout Example

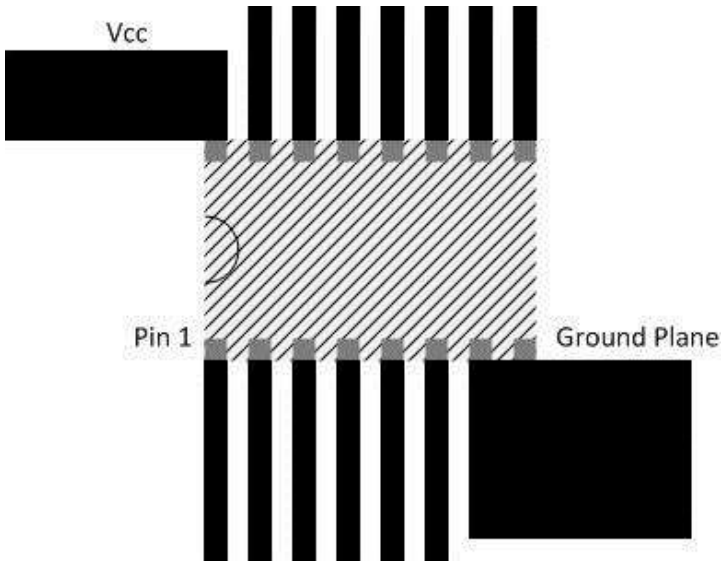


Figure 8-3. Layout Schematic

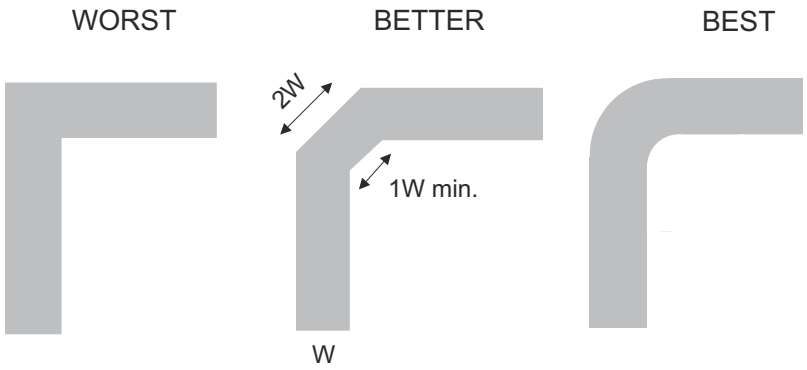


Figure 8-4. Trace Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision M (September 2024) to Revision N (September 2024)	Page
• Added DYY package and size	1
• Added DYY package	3
• Added DYY package	4
• Added DYY package	4

Changes from Revision L (June 2024) to Revision M (September 2024)	Page
• Updated ESD Ratings CDM from +/-1500V to +/-2000V	4

Changes from Revision K (November 2016) to Revision L (June 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added new VIH and VIL Specifications at 1.65V Vcc	5
• Increased max ambient temperature max to 125C	5
• Added Ron, Ron Peak, and Delta Ron Specifications at 1.65V Vcc	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV4052AD	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 85	LV4052A
SN74LV4052ADBR	NRND	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A
SN74LV4052ADBR.A	NRND	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A
SN74LV4052ADBRE4	NRND	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A
SN74LV4052ADGVR	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A
SN74LV4052ADGVR.A	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A
SN74LV4052ADR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4052A
SN74LV4052ADR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4052A
SN74LV4052ADYYR	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4052
SN74LV4052ADYYR.A	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4052
SN74LV4052AN	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74LV4052AN
SN74LV4052AN.A	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74LV4052AN
SN74LV4052ANSR	NRND	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4052A
SN74LV4052ANSR.A	NRND	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4052A
SN74LV4052APWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A
SN74LV4052APWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A
SN74LV4052APWRG4	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	LW052A
SN74LV4052APWT	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	LW052A
SN74LV4052ARGYR	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A
SN74LV4052ARGYR.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74LV4052A :

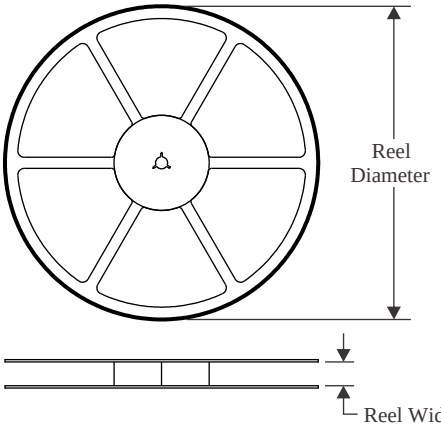
- Automotive : SN74LV4052A-Q1
- Enhanced Product : SN74LV4052A-EP

NOTE: Qualified Version Definitions:

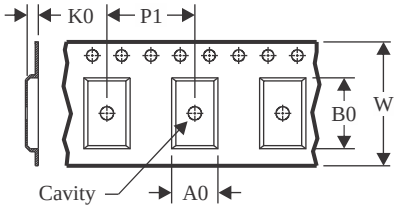
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

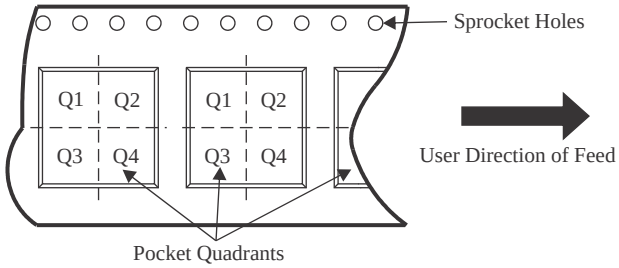


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

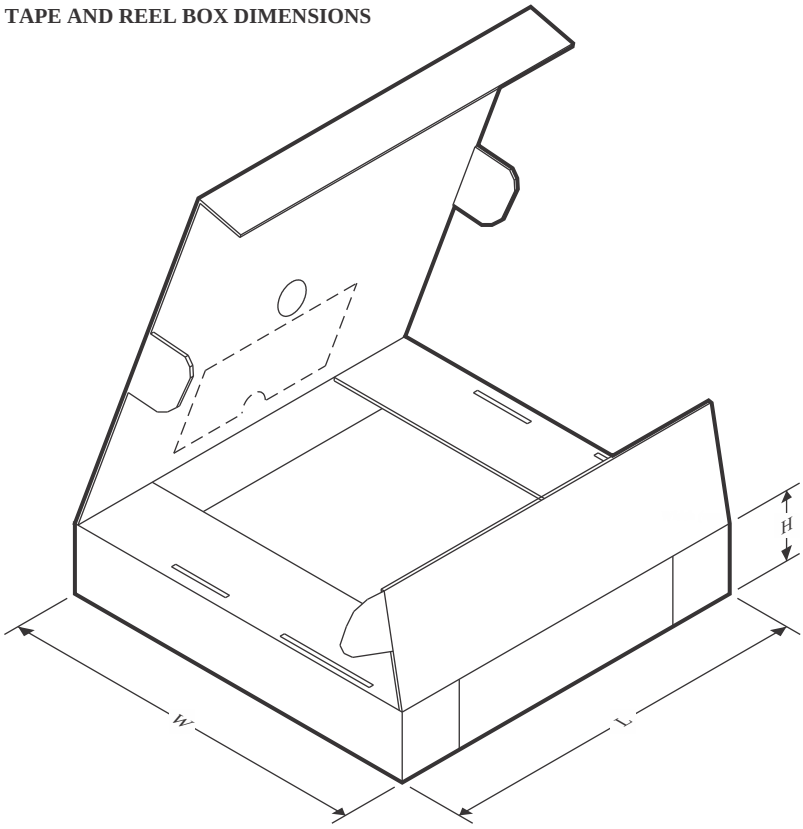
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV4052ADBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV4052ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV4052ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV4052ADYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
SN74LV4052ANSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LV4052APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4052APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4052ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

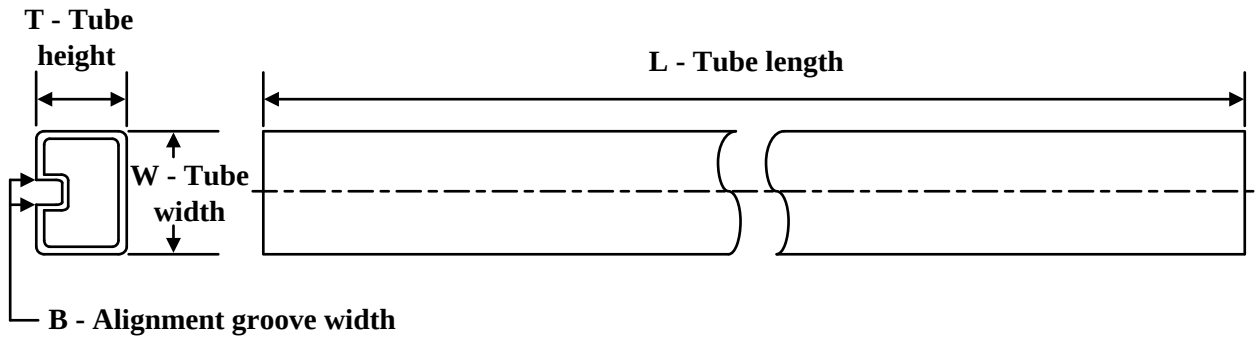
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV4052ADBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74LV4052ADGVR	TVSOP	DGV	16	2000	356.0	356.0	35.0
SN74LV4052ADR	SOIC	D	16	2500	353.0	353.0	32.0
SN74LV4052ADYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
SN74LV4052ANSR	SOP	NS	16	2000	356.0	356.0	35.0
SN74LV4052APWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74LV4052APWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74LV4052ARGYR	VQFN	RGY	16	3000	360.0	360.0	36.0

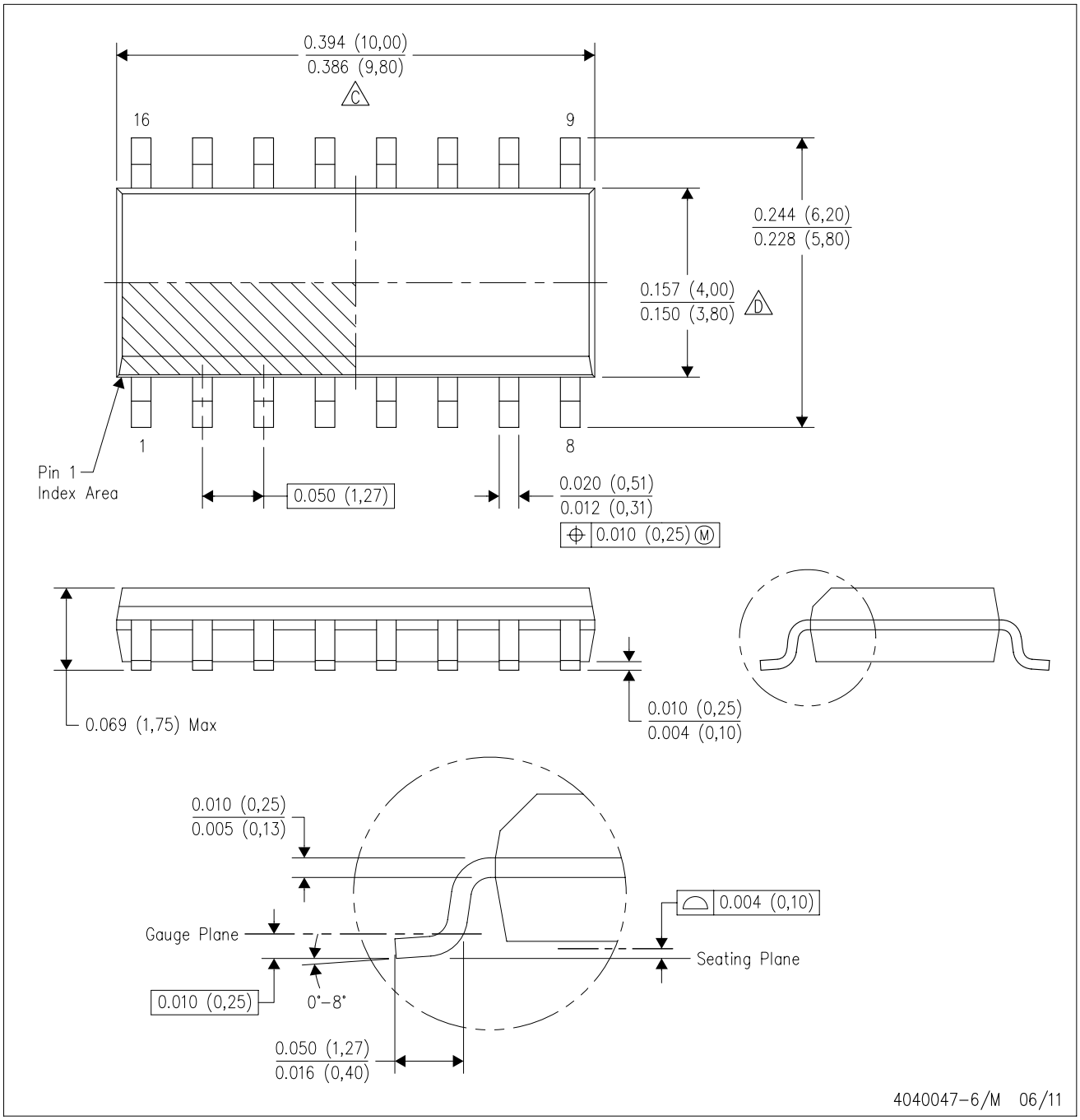
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LV4052AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LV4052AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LV4052AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LV4052AN.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



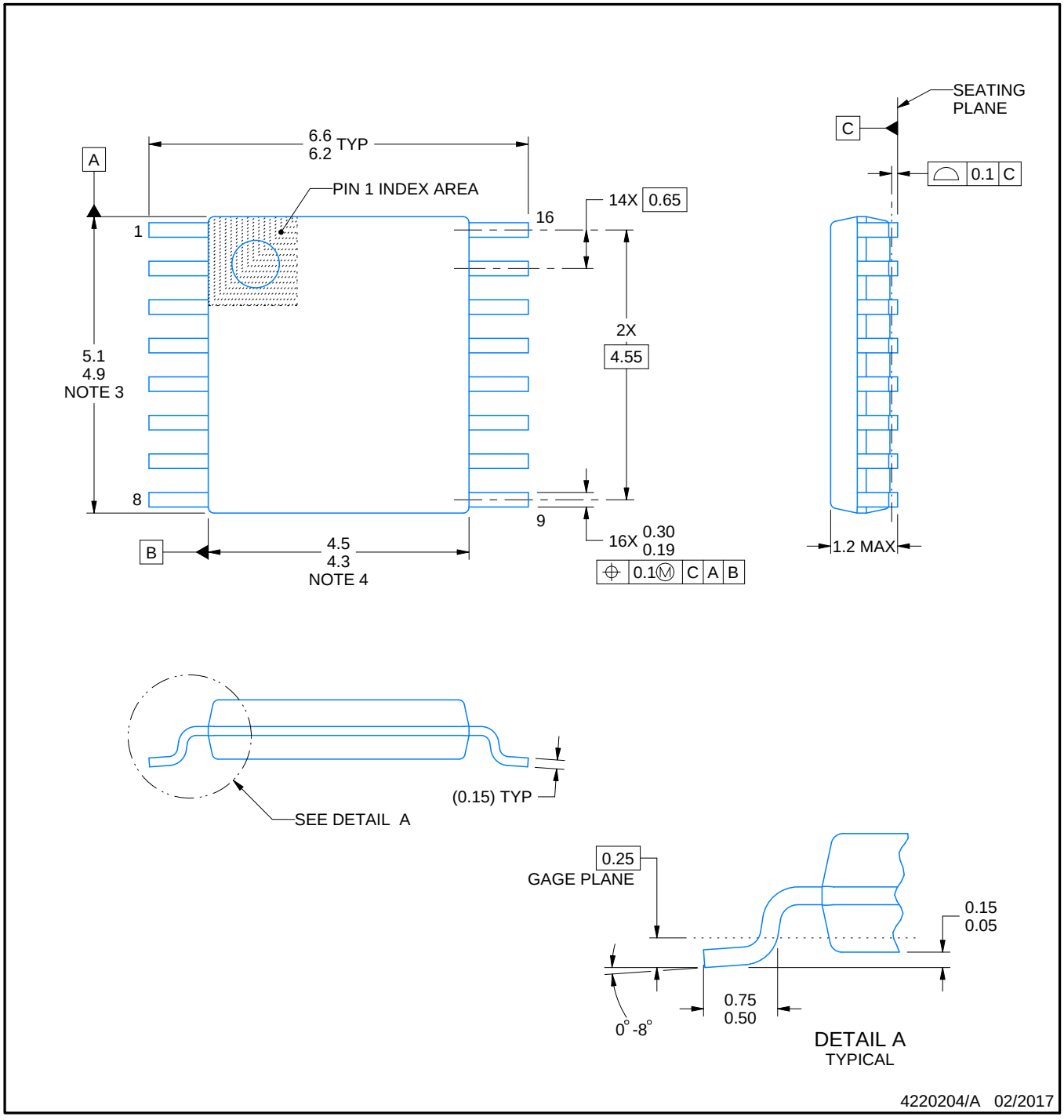
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

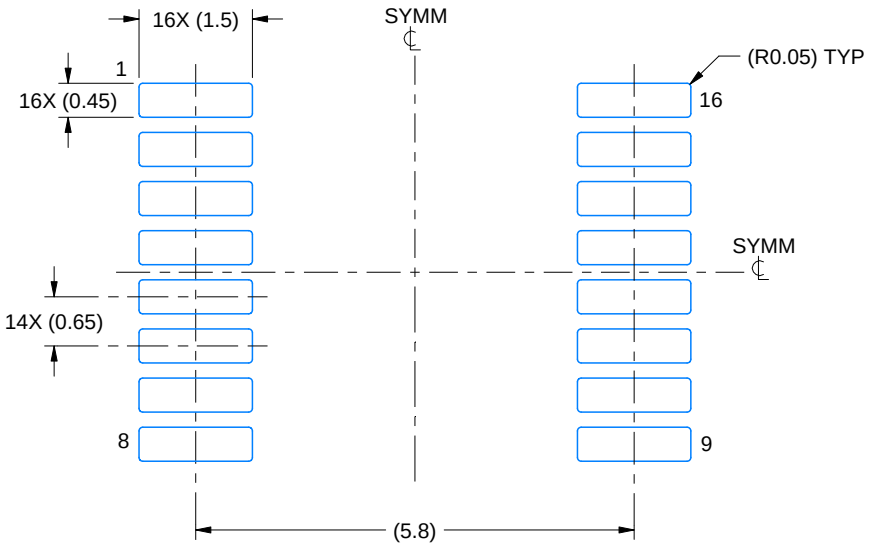
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



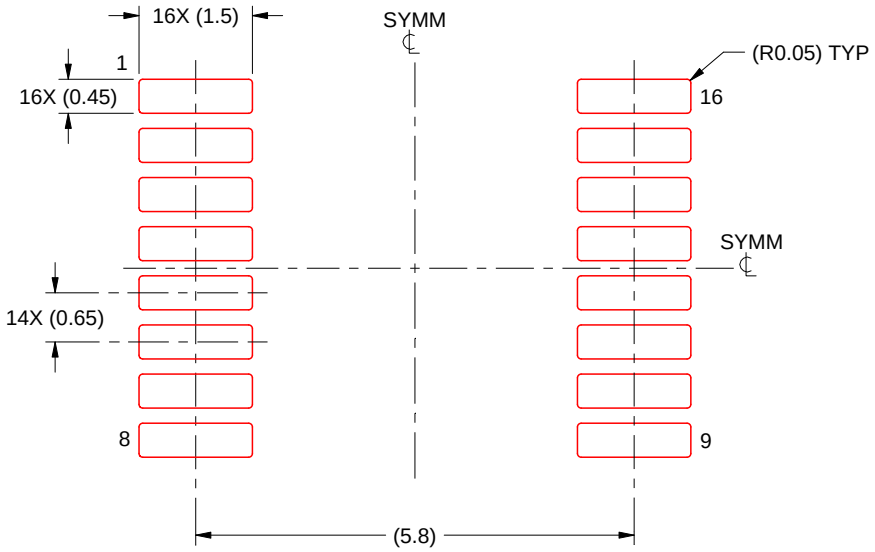
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

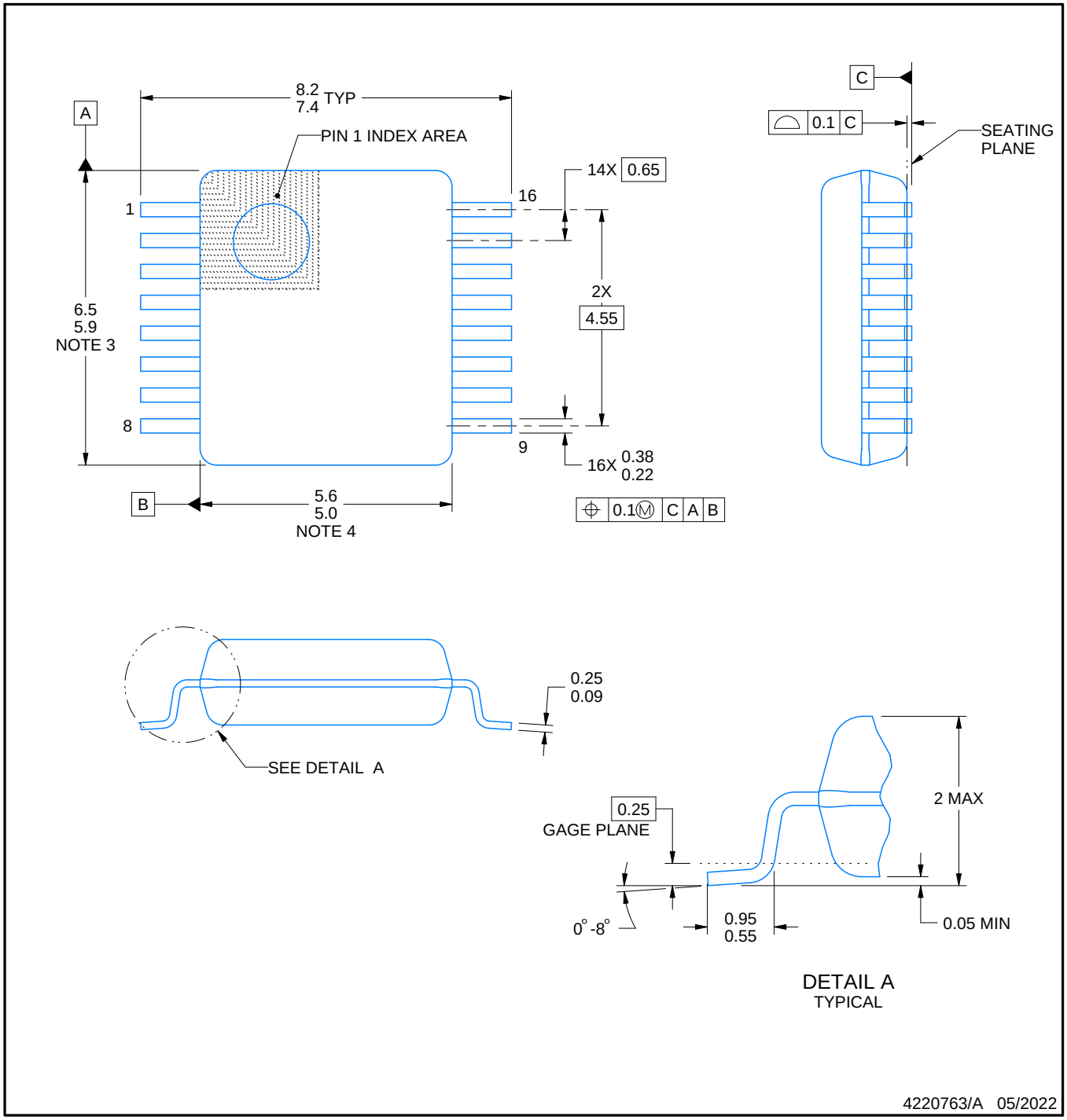
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DB0016A

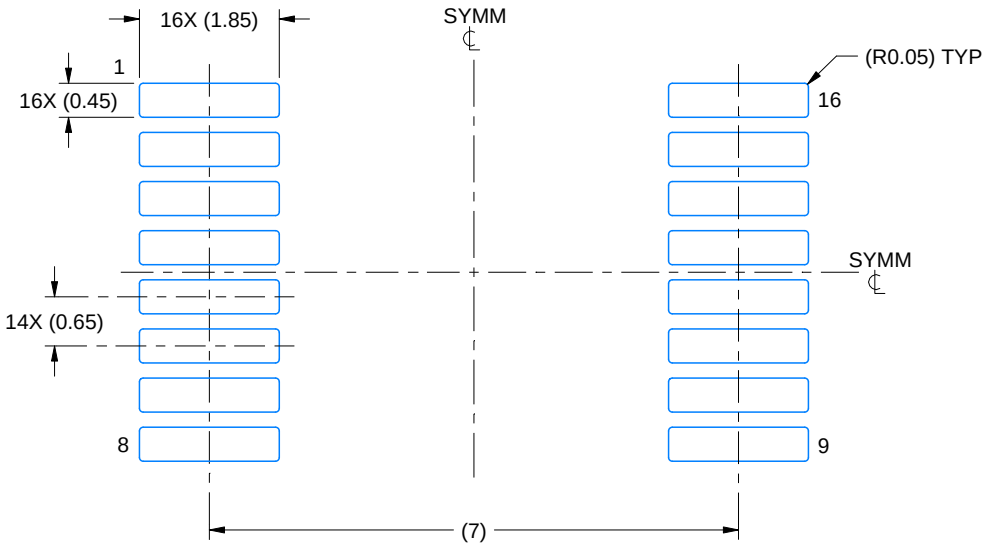
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

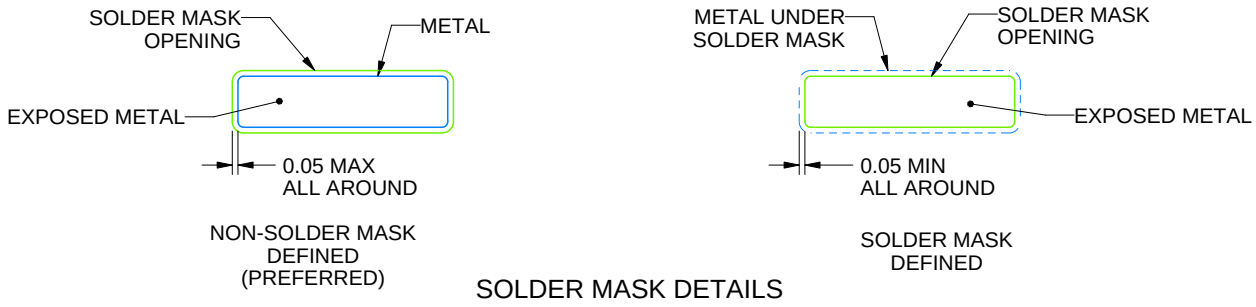


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

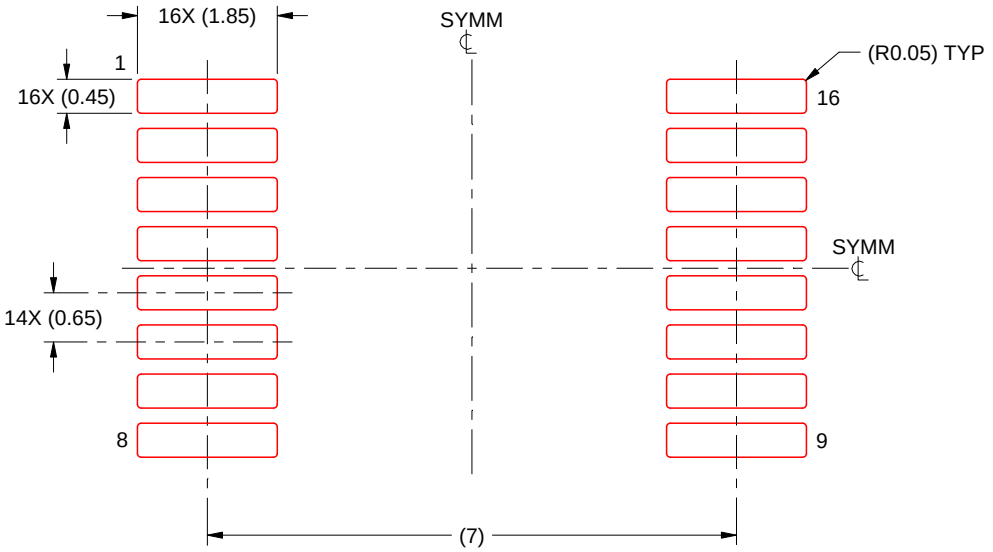


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

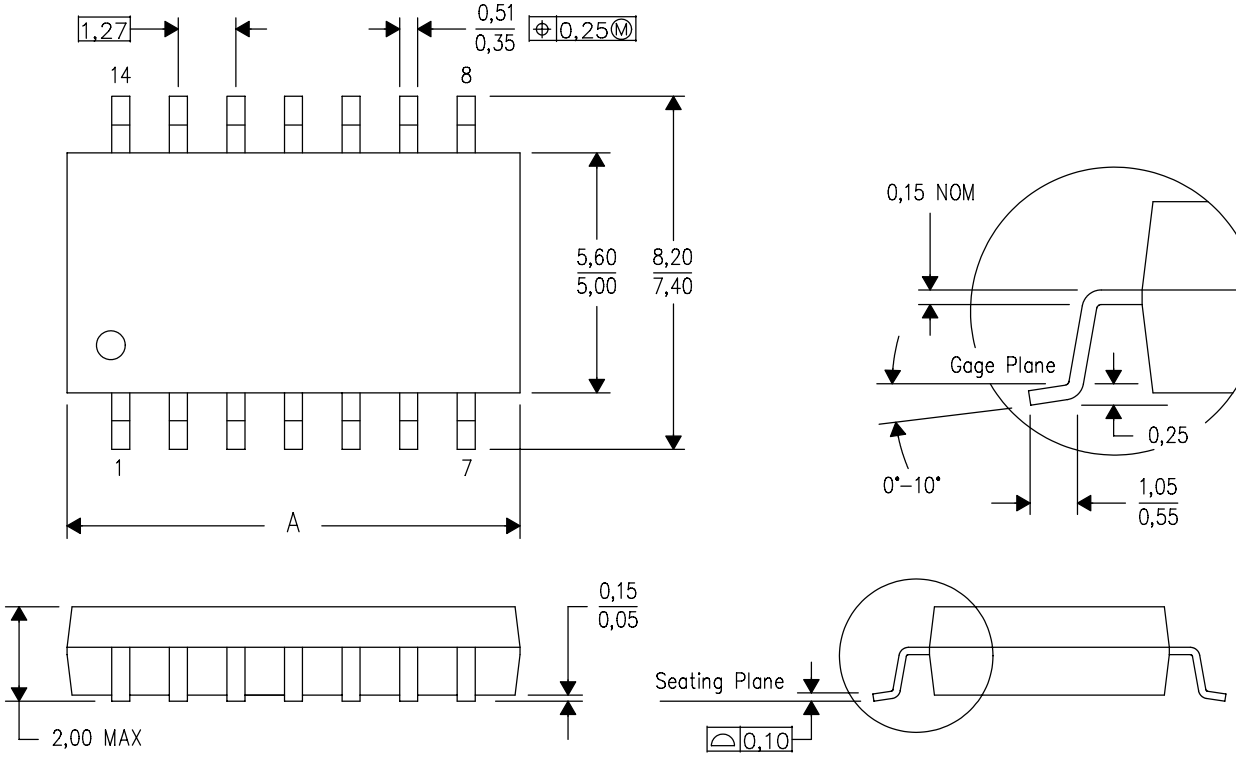
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

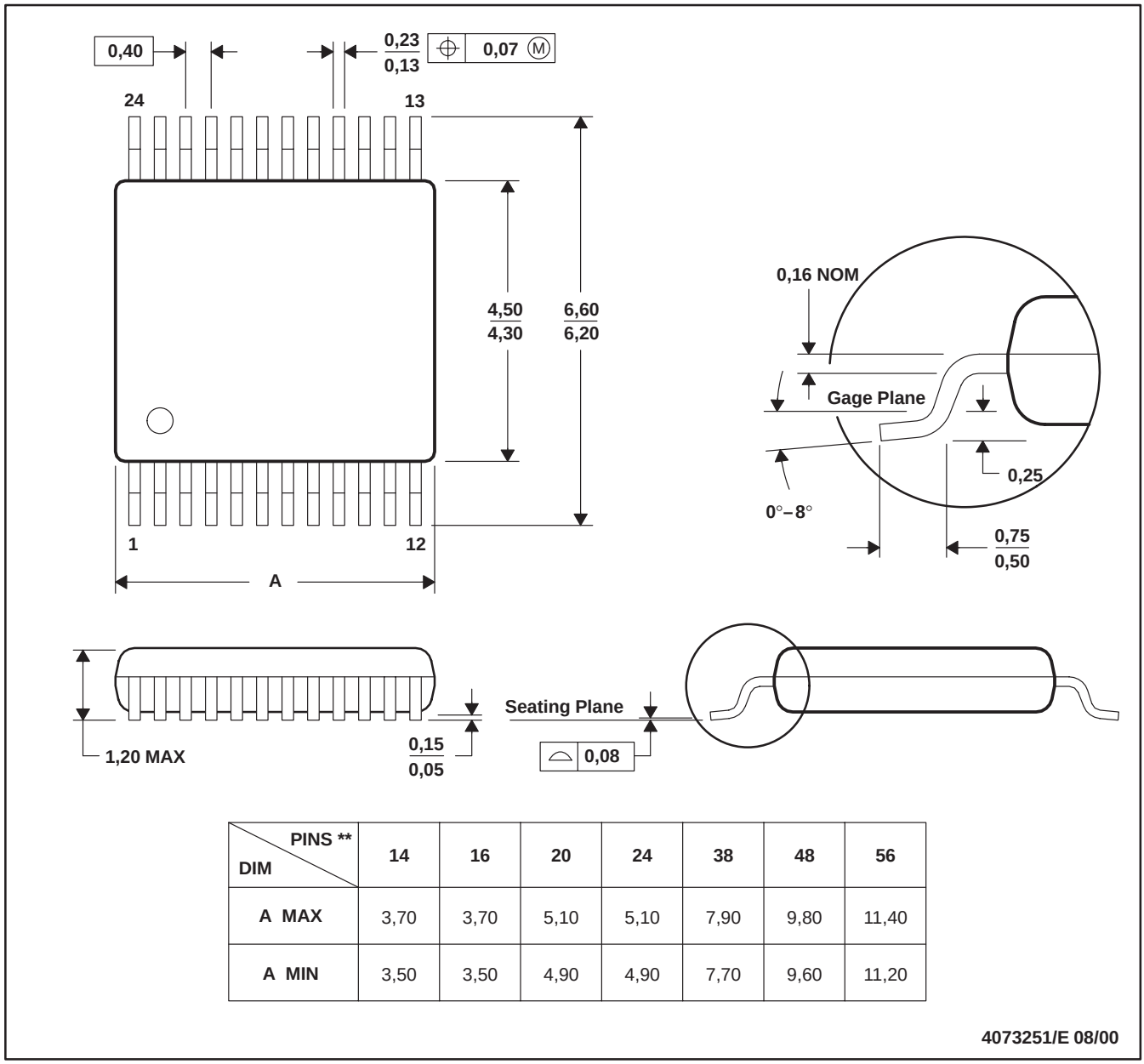
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MPDS006C – FEBRUARY 1996 – REVISED AUGUST 2000

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

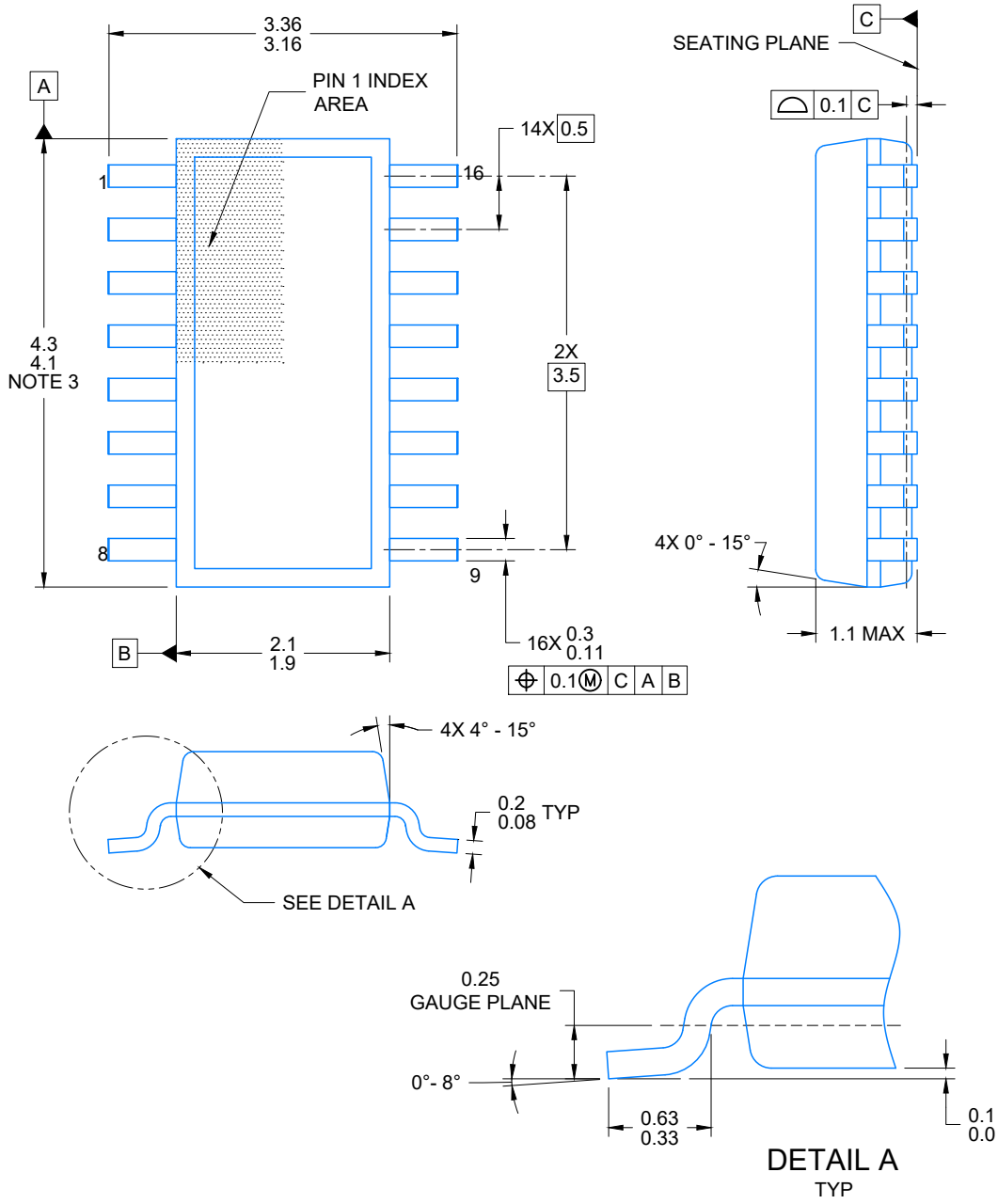
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

PACKAGE OUTLINE

DYY0016A

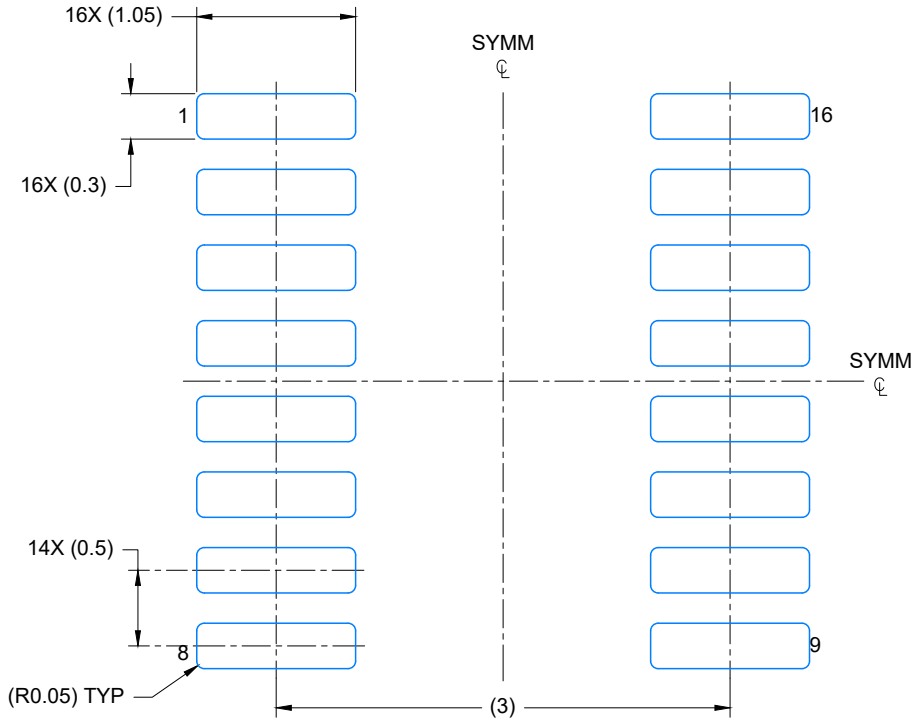
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

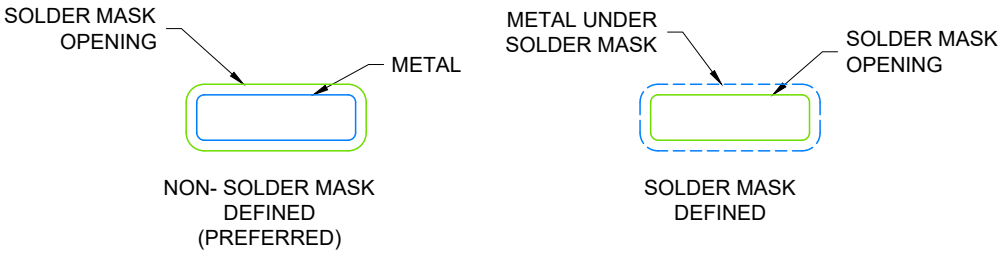


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224642/D 07/2024

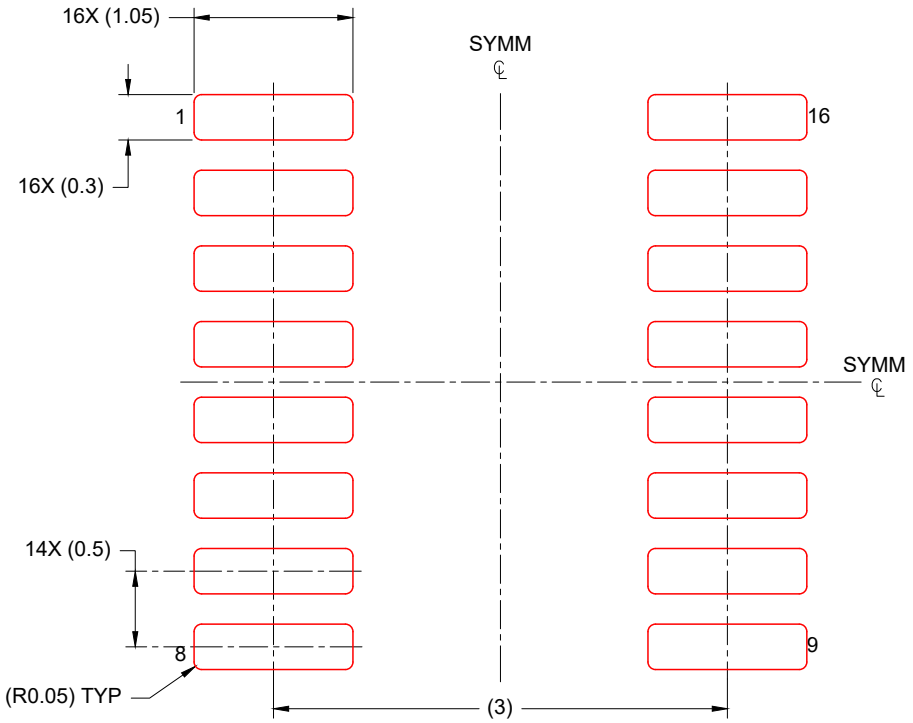
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

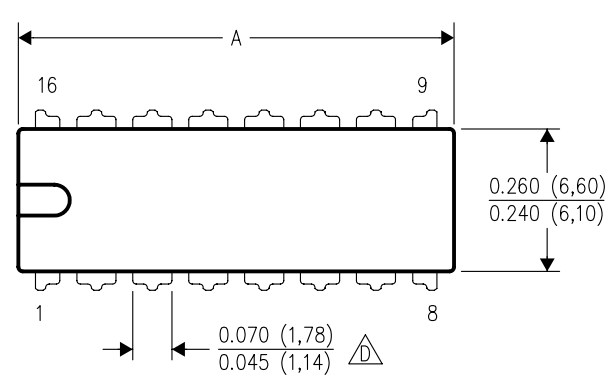
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

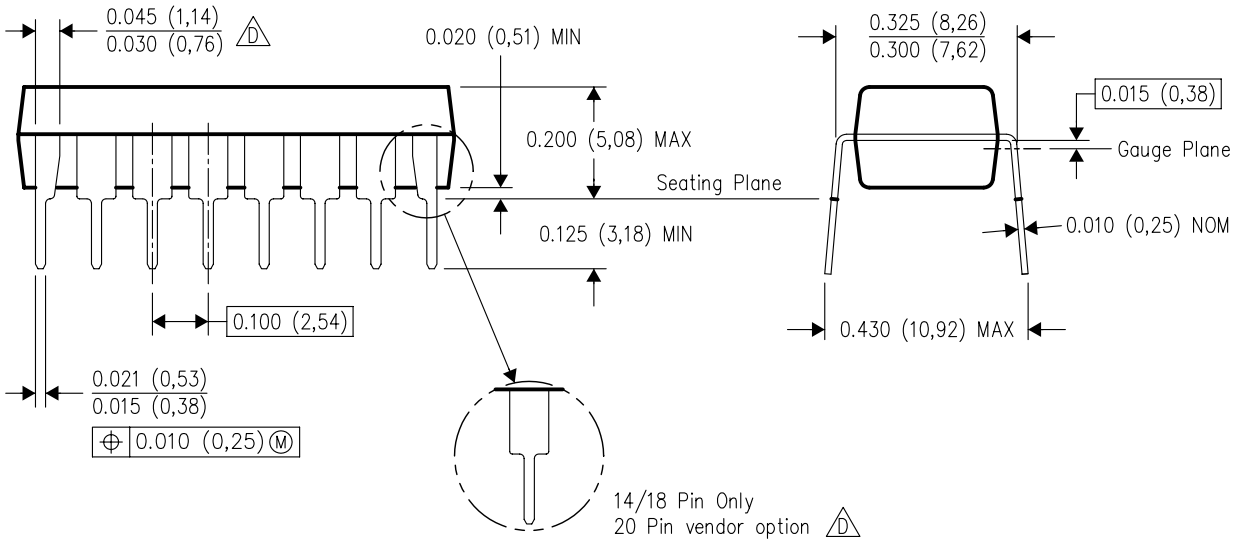
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



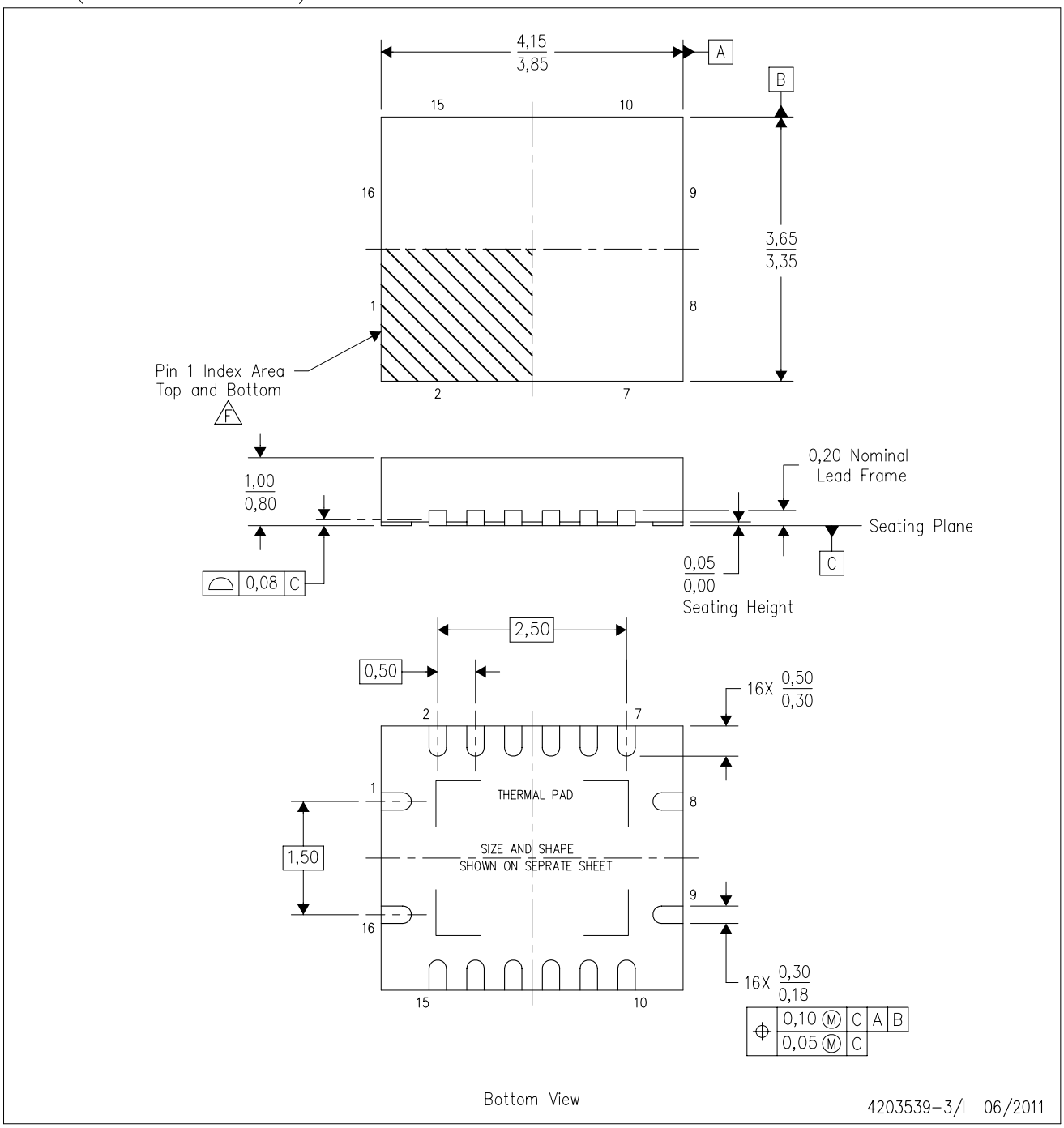
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



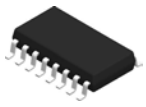
4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

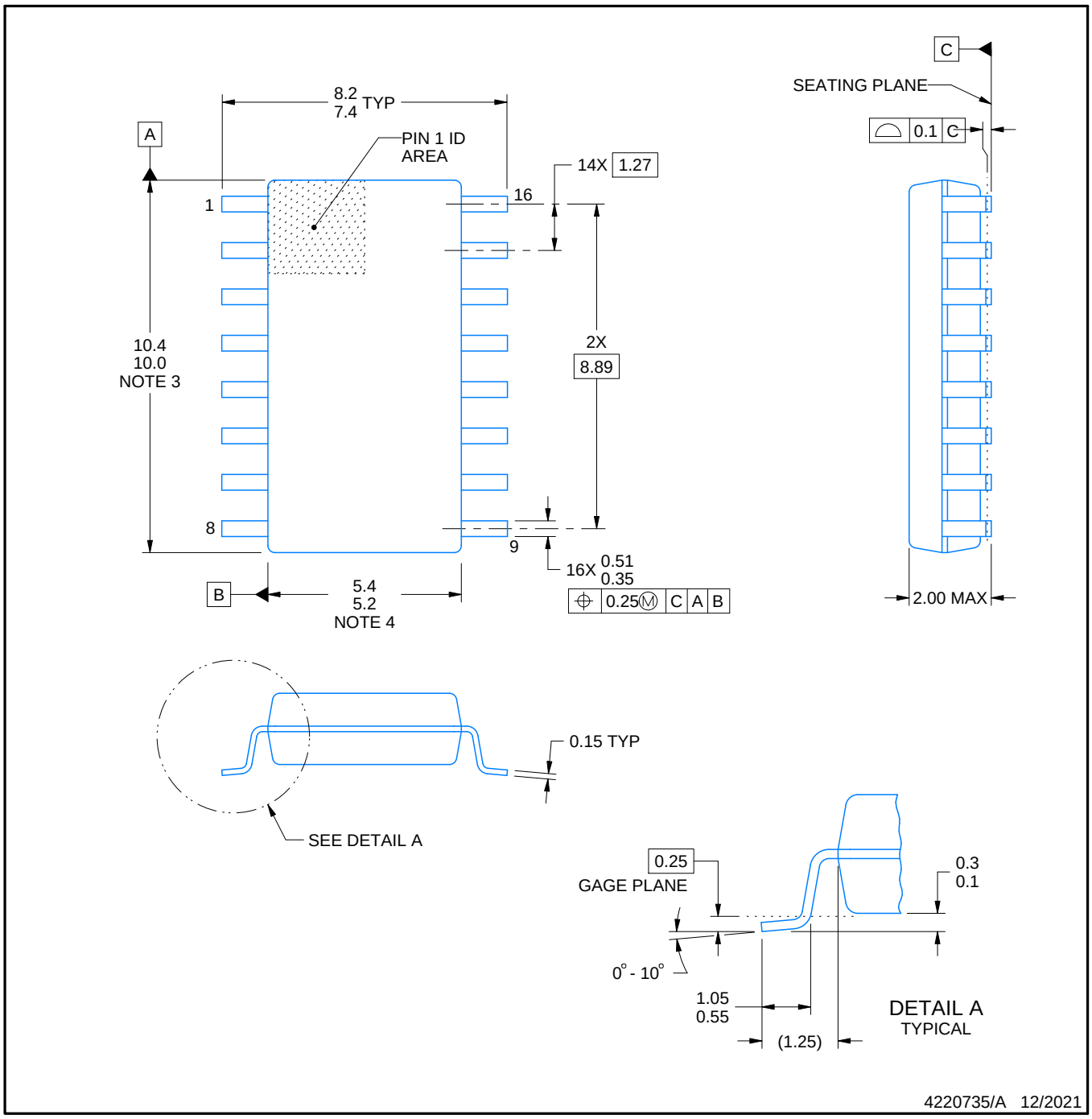


PACKAGE OUTLINE

NS0016A

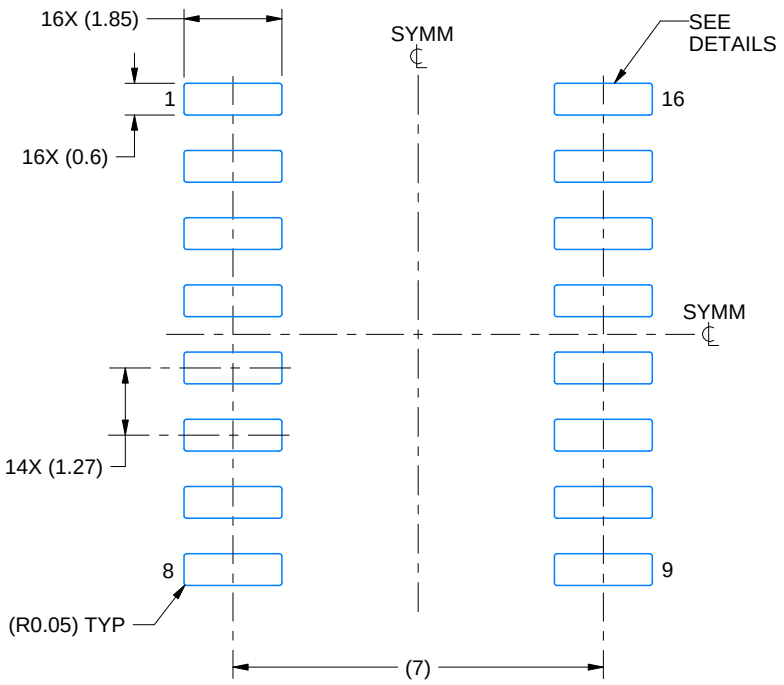
SOP - 2.00 mm max height

SOP

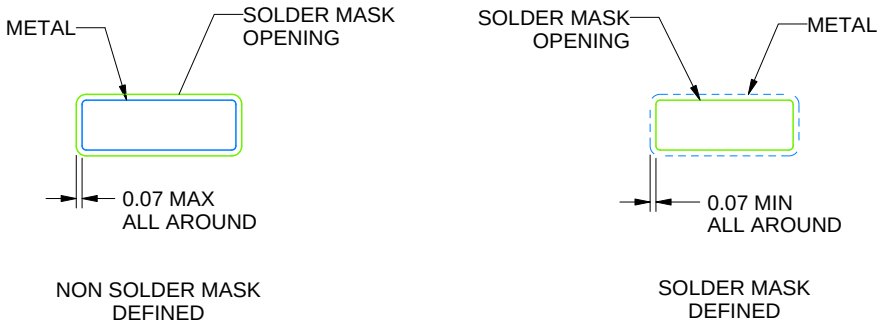


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X

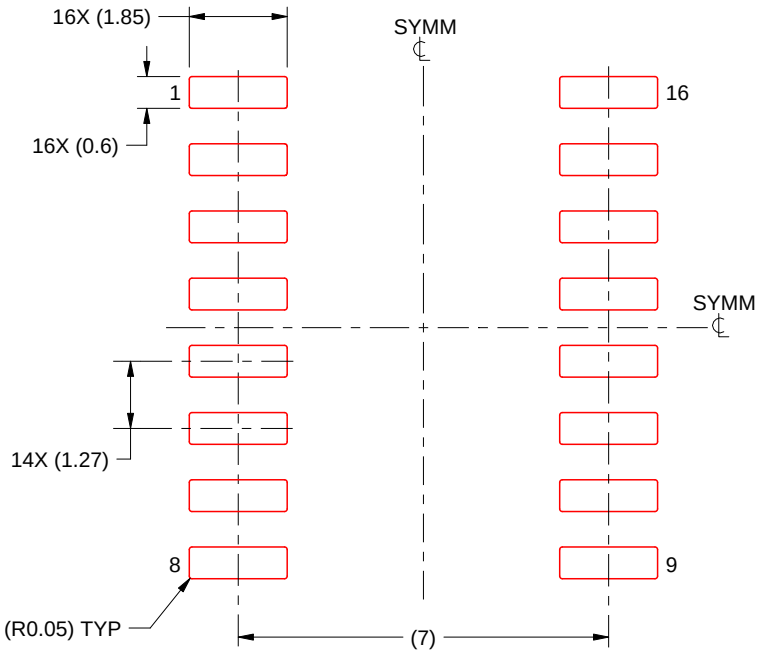


SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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