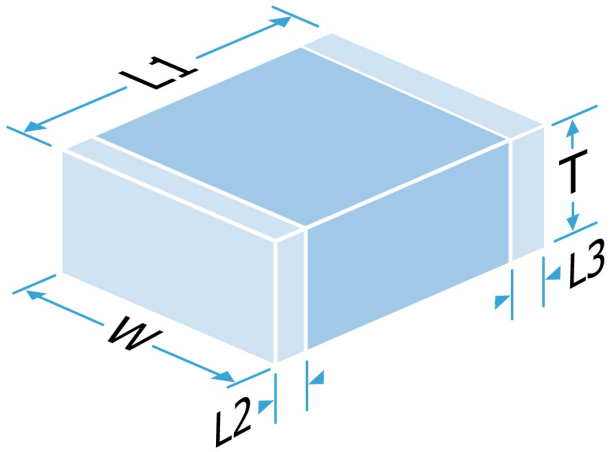
Multilayer Ceramic Chip Capacitor

Part Number: 111122K01P80BQTAF9LM

Description: 1111 2000Vdc 1.8pF ±0.10pF C0G - Hi Q/Low ESR Non-Mag (PME)

Ultra stable HighQ Low ESR multi-layer ceramic capacitors offering very stable 0±30ppm/°C, 0±15ppm/°C or +90±20ppm/°C High Q material systems that provide excellent low loss performance and guaranteed non-magnetic / relative permeability of 1.000 for critical applications such as NMR / MRI. Optimised for the lowest possible ESR and with maximised voltage ratings, this range provides the best possible conduction of high power RF signals.



Mechanical Specification

Size Code	1111
Length (L1) in mm (")	2.79 +0.51/-0.25 (0.11 +0.02/-0.01)
Width (W) in mm (")	2.79 ± 0.38 (0.113 ± 0.015)
Thickness (T) in mm (")	2.0 ± 0.2 (0.08 ± 0.008)
Minimum Termination Band (L2,L3) in mm (")	0.13 (0.005)
Maximum Termination Band (L2,L3) in mm (")	0.63 (0.025)
Termination Material	Copper Barrier, Sn Plated Solder (Non-Mag., RoHS compliant)
Solderability	IEC-60068-2-58
Packaging	7" Reel Horizontal Orientation, 1000 per reel

General Electrical Specification

Rated Voltage	2000Vdc
Nominal Capacitance Value	1.8pF
Capacitance Tolerance	±0.10pF
Tangent of Loss Angle (Tan δ)	≤0.0014
Capacitance and Tan δ Test Conditions	1.0Vrms @ 1MHz
Voltage Proof (Voltage applied for 5 secs max. @ 50mA max. charge current)	2400Vdc
Min Insulation Resistance (IR)	100.00GOhm @ 100Vdc
Dielectric Classification	C0G - Hi Q/Low ESR Non-Mag (PME)
Rated Temperature Range	-55°C / +125°C
Maximum Capacitance Change over Temperature Range	No DC Voltage 0±30ppm/°C Rated DC Voltage -
Climatic Category (IEC)	55/125/56
Ageing Characteristic	Zero

Knowles Precision Devices - Sales
Europe: KPD-Europe-sales@knowles.com
Asia: KPD-Asia-sales@knowles.com
USA: KPD-NA-sales@knowles.com
www.knowlescapacitors.com

This datasheet is for a standard item and is confirmed valid on the date generated, the latest published data for this part may differ and is available at http://www.knowlescapacitors.com or by contacting us.

Data is correct to the best of our knowledge, errors and omissions excepted.

Date: Sunday, February 06, 2022

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Environmental

RoHS Compliant to 2011/65/EC as amended by 2015/863/EU	Compliant
REACH Compliant	219 compliant
California Proposition 65	No exposure risk

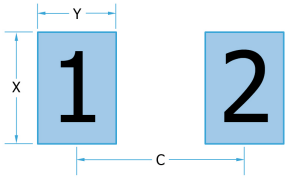
Board Layout

Knowles' conventional 2-terminal chip capacitors can generally be mounted using pad designs in accordance with international specification IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should be considered.

Some high voltage parts may require modifications to the board layout and/or the addition of a conformal coating to prevent flashover. Refer to application note AN0043 for further information.

IPC-7351 pad design

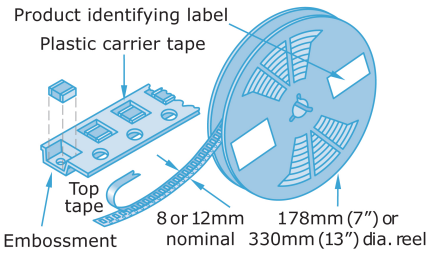
	1111	
C	2.80mm	0.110"
Y	1.20mm	0.047"
X	3.20mm	0.126"



Packaging

Tape packaging information for tape-and-reel parts:

Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.



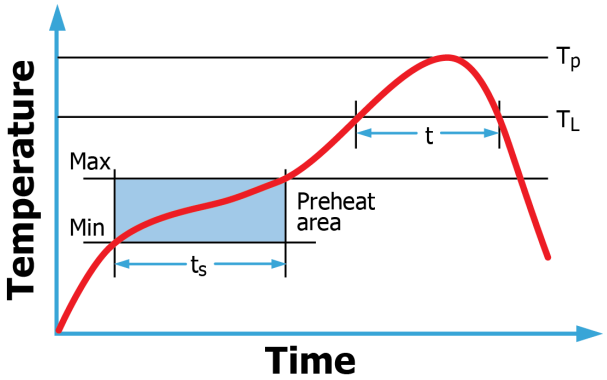
Soldering

Reflow solder in accordance with IPC-A-610. Recommended reflow profile as laid down in IPC/JEDEC J-STD-020.

Wave soldering is also possible, but care must be taken for case sizes 1210 and larger and component thickness >1.0mm. Trials are encouraged.

Hand soldering is not recommended and can lead to component damage through thermal shock.

PdAg terminations are primarily intended for conductive epoxy attachment - they may be suitable for soldering but trials are recommended.



Application notes with mounting and handling guidance are available on request.

Compex DLI Johanson MFG Novacap Syfer Voltronics

Knowles Precision Devices - Sales

Europe: KPD-Europe-sales@knowles.com

Asia: KPD-Asia-sales@knowles.com

USA: KPD-NA-sales@knowles.com

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