

PerFET™ Power Transistor

FEATURES

- Excellent FOM
- AEC-Q101 Qualified
- Wettable Flank leads for Enhanced AOI
- 100% UIS and Rg tested
- 175°C Operating Junction Temperature
- RoHS Compliant
- Halogen-Free

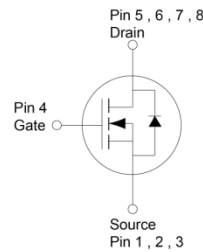
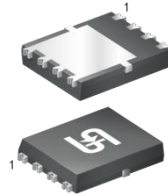
APPLICATIONS

- Automotive Applications
- Solenoid and Motor Drivers
- DC-DC Converters

PRODUCT SUMMARY			
PARAMETER		VALUE	UNIT
V_{DS}		40	V
$R_{DS(on)}$ (max)	$V_{GS} = 10V$	7	mΩ
	$V_{GS} = 4.5V$	9.8	
Q_g	$V_{GS} = 4.5V$	11	nC



PDFN56U



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 16	V
Continuous Drain Current, Silicon limited	$T_C = 25^\circ\text{C}$	I_D	70	A
Continuous Drain Current (Note 1)	$T_C = 25^\circ\text{C}$	I_D	54	A
	$T_C = 100^\circ\text{C}$		50	
	$T_A = 25^\circ\text{C}$		16	
Pulsed Drain Current (Note 2)		I_{DM}	216	A
Single Pulse Avalanche Current (Note 3)		I_{AS}	18.2	A
Single Pulse Avalanche Energy (Note 3)		E_{AS}	49.9	mJ
Total Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	46.8	W
	$T_C = 125^\circ\text{C}$		15.6	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +175	$^\circ\text{C}$

THERMAL RESISTANCE

PARAMETER	SYMBOL	MAXIMUM	UNIT
Thermal Resistance – Junction to Case	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$
Thermal Resistance – Junction to Ambient (Note 4)	$R_{\theta JA}$	50	$^\circ\text{C/W}$

NOTE:

1. Package current limit.
2. Pulse Width $\leq 100\mu\text{s}$.
3. $L = 0.3\text{mH}$, $V_{GS} = 10V$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.
4. Device on a PCB FR4 with 1 in² (single layer, 2 oz thick) copper area for drain connection.

ELECTRICAL CHARACTERISTICS (T _A = 25°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 1mA	BV _{DSS}	40	--	--	V
Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 250μA	V _{GS(TH)}	1.4	1.8	2.2	V
Gate-Source Leakage Current	V _{GS} = ±16V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Drain-Source Leakage Current	V _{GS} = 0V, V _{DS} = 40V	I _{DSS}	--	--	1	μA
	V _{GS} = 0V, V _{DS} = 40V T _J = 125°C		--	--	100	
Drain-Source On-State Resistance (Note 5)	V _{GS} = 10V, I _D = 27A	R _{DS(on)}	--	5.6	7	mΩ
	V _{GS} = 4.5V, I _D = 27A		--	7.5	9.8	
Forward Transconductance (Note 5)	V _{DS} = 10V, I _D = 7A	g _{fs}	--	60	--	S
Dynamic (Note 6)						
Total Gate Charge	V _{GS} = 4.5V, V _{DS} = 20V, I _D = 16A	Q _g	--	11	16.5	nC
Total Gate Charge	V _{GS} = 10V, V _{DS} = 20V, I _D = 16A	Q _g	--	23	34.5	
Gate-Source Charge		Q _{gs}	--	4.3	8.6	
Gate-Drain Charge		Q _{gd}	--	3.5	7	
Input Capacitance	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz	C _{iss}	--	1446	2169	pF
Output Capacitance		C _{oss}	--	229	458	
Reverse Transfer Capacitance		C _{rss}	--	34	68	
Gate Resistance	f = 1.0MHz	R _g	--	1.4	--	Ω
Switching (Note 7)						
Turn-On Delay Time	V _{GS} = 10V, V _{DS} = 20V, I _D = 16A, R _G = 3.3Ω	t _{d(on)}	--	7.2	--	ns
Rise Time		t _r	--	50.8	--	
Turn-Off Delay Time		t _{d(off)}	--	23.2	--	
Fall Time		t _f	--	5.7	--	
Source-Drain Diode						
Diode Forward Voltage (Note 5)	V _{GS} = 0V, I _S = 27A	V _{SD}	--	--	1.1	V
Reverse Recovery Time	I _S = 16A,	t _{rr}	--	32	--	ns
Reverse Recovery Charge	di/dt = 100A/μs	Q _{rr}	--	26	--	nC

Notes:

- Pulse test: Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$.
- Defined by design. Not subject to production test.
- Switching time is essentially independent of operating temperature.

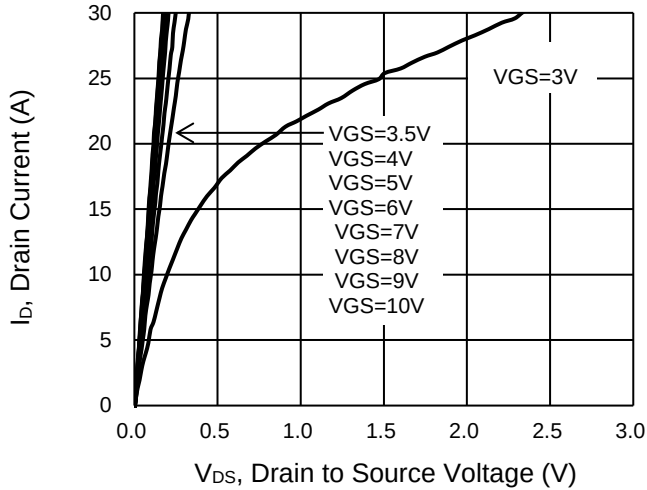
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TQM070NH04LCR RLG	PDFN56U	2,500pcs / 13" Reel

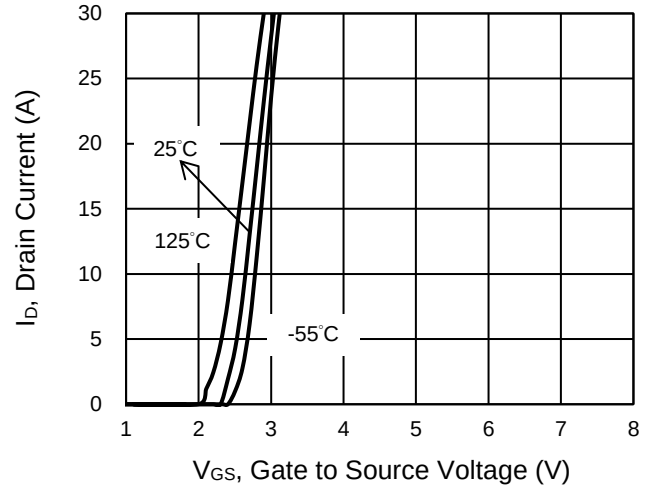
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

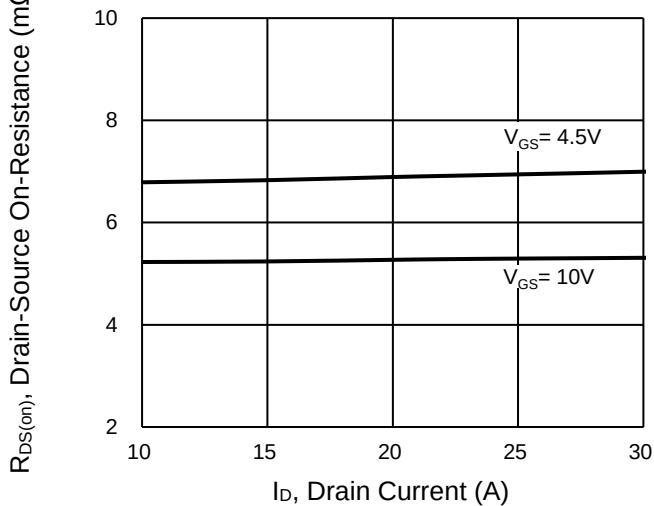
Output Characteristics



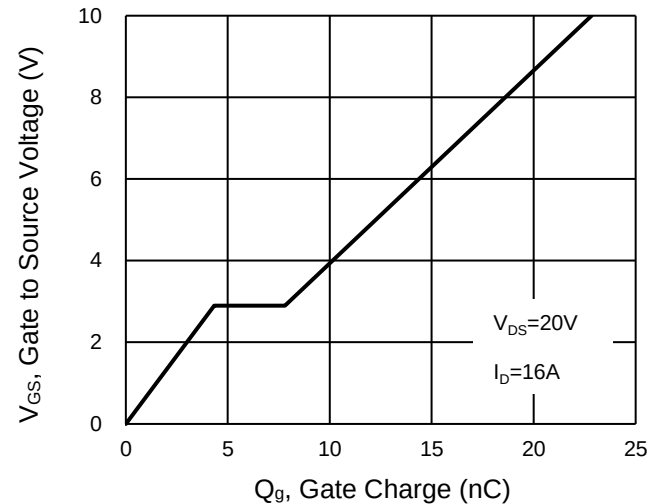
Transfer Characteristics



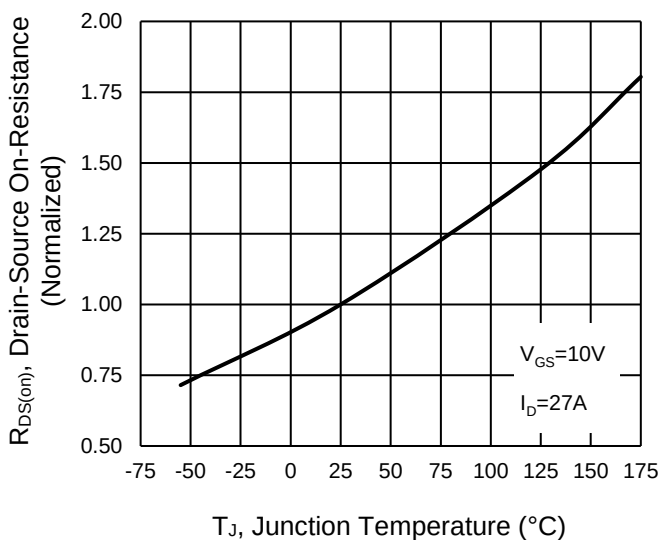
On-Resistance vs. Drain Current



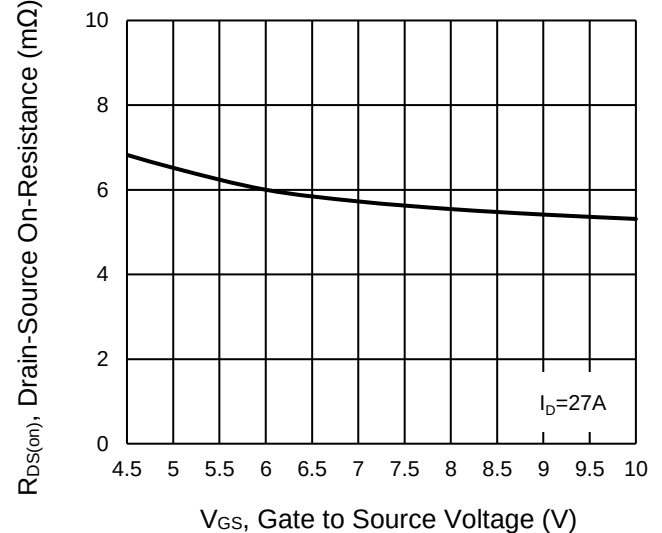
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature

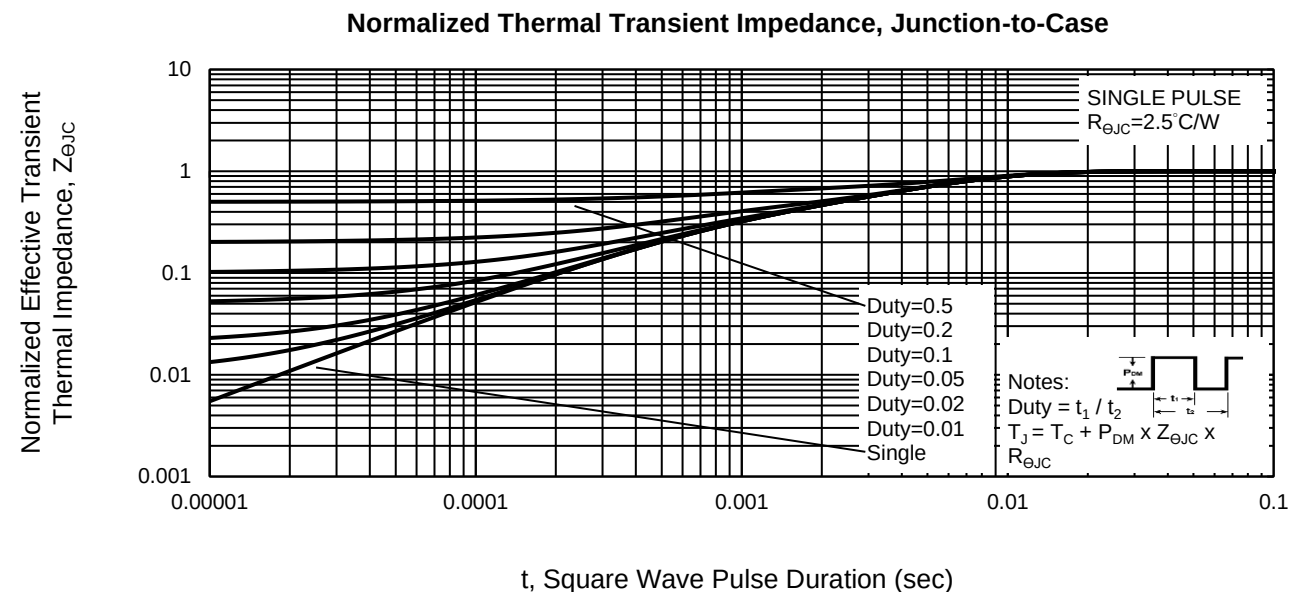
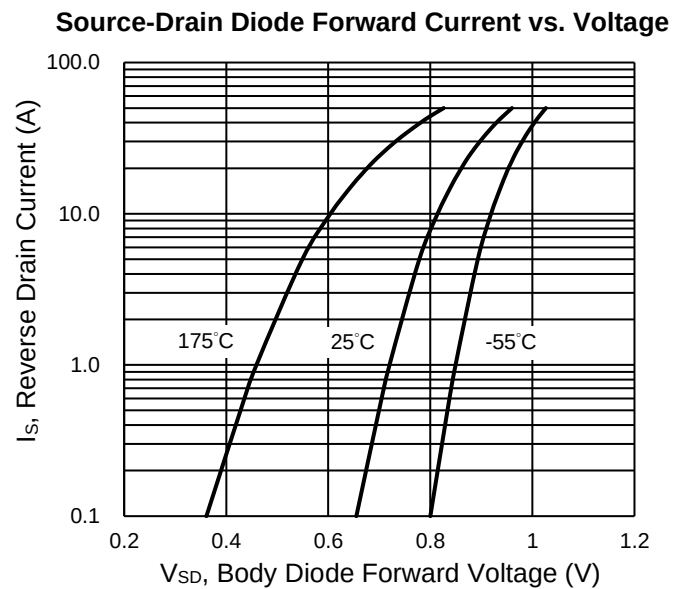
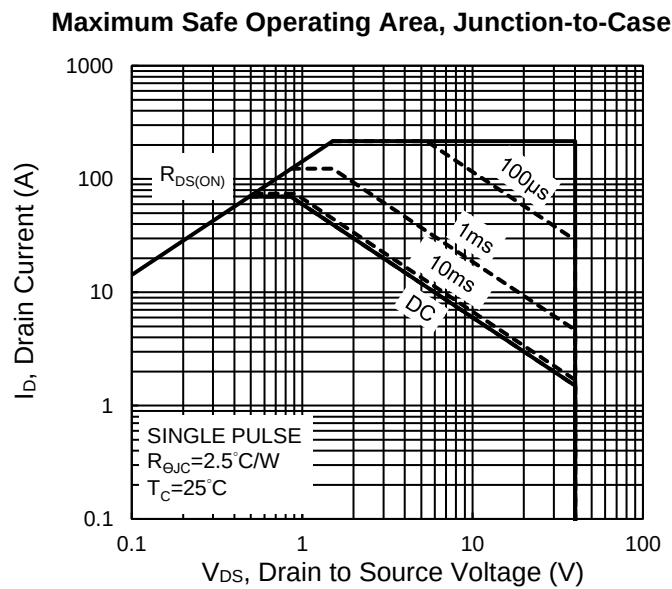
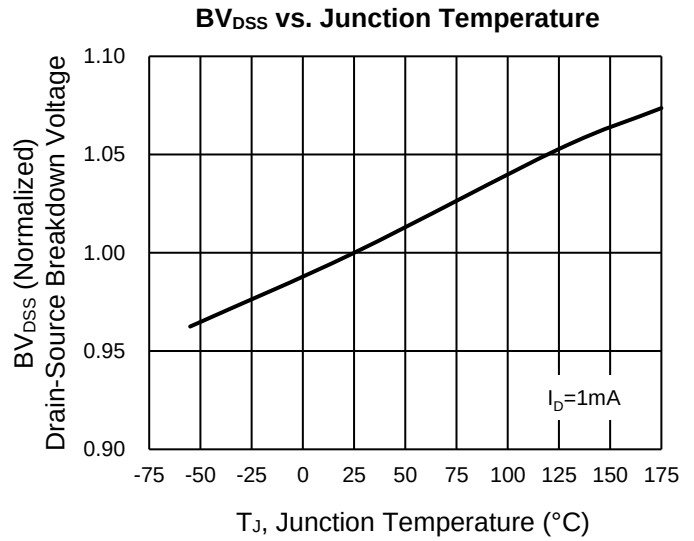
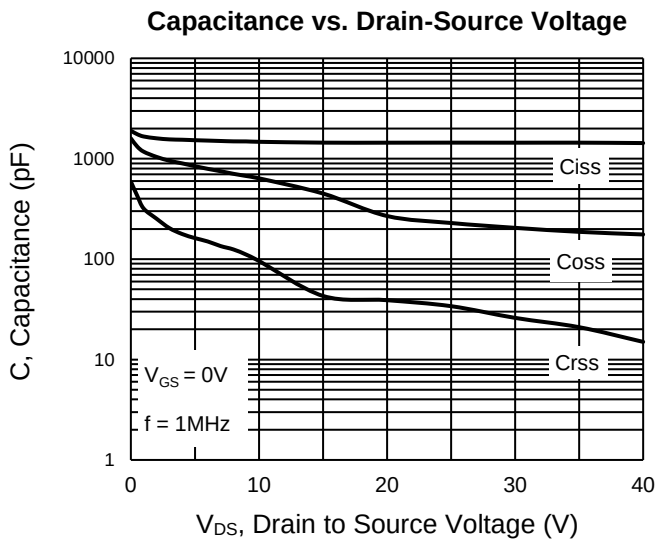


On-Resistance vs. Gate-Source Voltage



CHARACTERISTICS CURVES

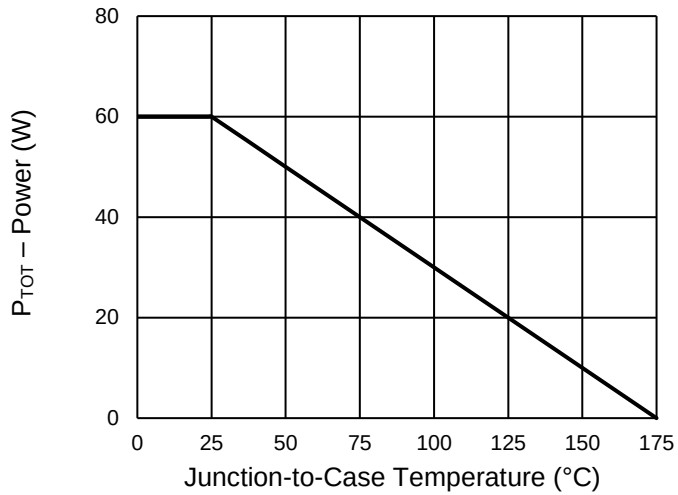
($T_A = 25^\circ\text{C}$ unless otherwise noted)



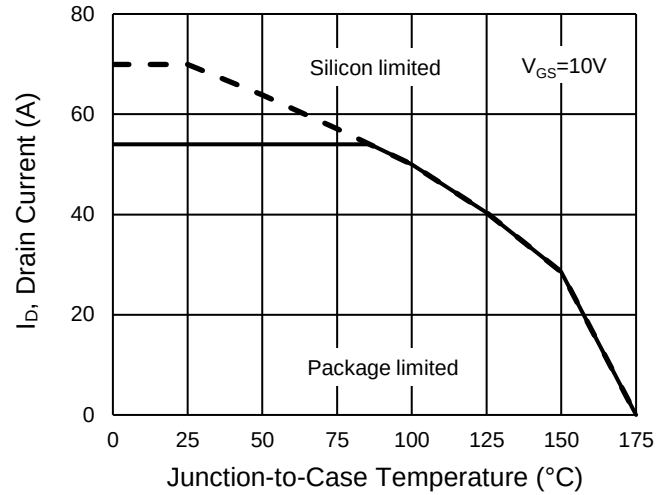
CHARACTERISTICS CURVES

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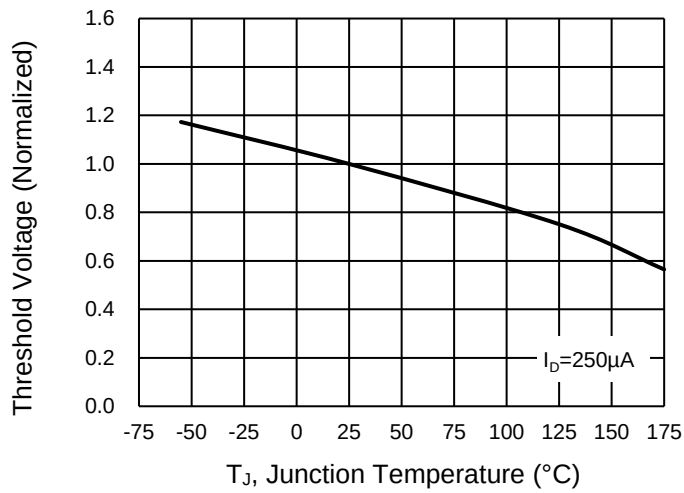
Power Dissipation



Drain Current

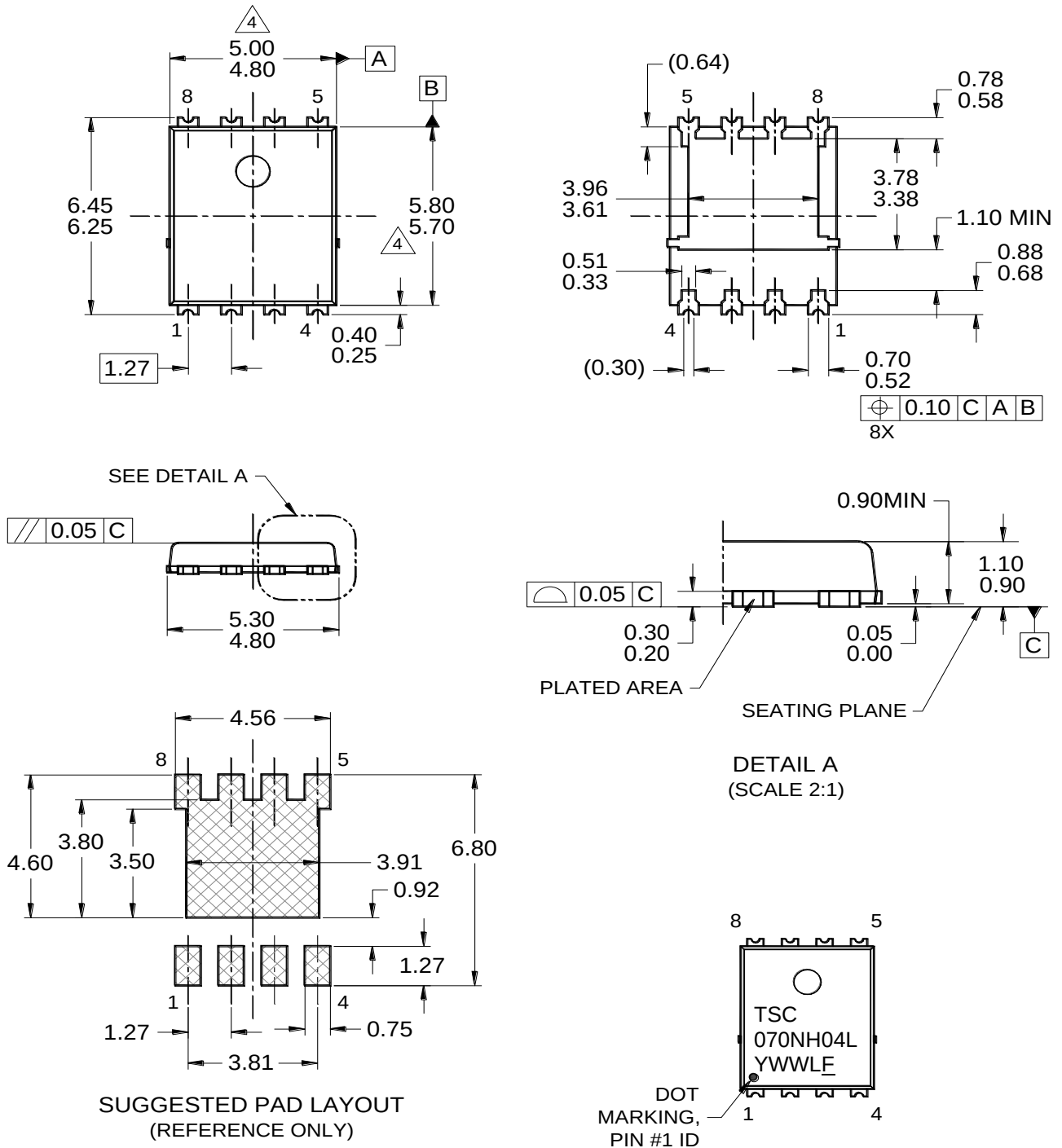


Normalized gate threshold voltage vs Temperature



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

PDFN56U



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: JEITA ED-7500B, EIAJ SC-111BB.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DWG NO. REF: HQ2SD07-PDFN56U-023 REV B.

Y = YEAR CODE
WW = WEEK CODE (01~52)
L = LOT CODE (1~9, A~Z)
F = FACTORY CODE
- = AEC-Q101 QUALIFIED

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