

# 1.1nV/ $\sqrt{\text{Hz}}$ Noise, Low Power, Precision Operational Amplifier in Small DFN-8 Package

## FEATURES

- **LOW VOLTAGE NOISE:** 1.1nV/ $\sqrt{\text{Hz}}$  at 1kHz
- **INPUT VOLTAGE NOISE:** 80nV<sub>PP</sub> (0.1Hz to 10Hz)
- **THD+N:** –136dB (G = 1, f = 1kHz)
- **OFFSET VOLTAGE:** 125 $\mu\text{V}$  (max)
- **OFFSET VOLTAGE DRIFT:** 0.35 $\mu\text{V}/^\circ\text{C}$  (typ)
- **LOW SUPPLY CURRENT:** 3.6mA/Ch (typ)
- **UNITY-GAIN STABLE**
- **GAIN BANDWIDTH PRODUCT:** 80MHz (G = 100)  
45MHz (G = 1)
- **SLEW RATE:** 27V/ $\mu\text{s}$
- **16-BIT SETTLING:** 700ns
- **WIDE SUPPLY RANGE:**  $\pm 2.25\text{V}$  to  $\pm 18\text{V}$ , +4.5V to +36V
- **RAIL-TO-RAIL OUTPUT**
- **OUTPUT CURRENT:** 30mA
- **DFN-8 (3mm  $\times$  3mm), MSOP-8, AND SO-8**

## APPLICATIONS

- **PLL LOOP FILTER**
- **LOW-NOISE, LOW-POWER SIGNAL PROCESSING**
- **16-BIT ADC DRIVERS**
- **DAC OUTPUT AMPLIFIERS**
- **ACTIVE FILTERS**
- **LOW-NOISE INSTRUMENTATION AMPS**
- **ULTRASOUND AMPLIFIERS**
- **PROFESSIONAL AUDIO PREAMPLIFIERS**
- **LOW-NOISE FREQUENCY SYNTHESIZERS**
- **INFRARED DETECTOR AMPLIFIERS**
- **HYDROPHONE AMPLIFIERS**
- **GEOPHONE AMPLIFIERS**
- **MEDICAL**

## DESCRIPTION

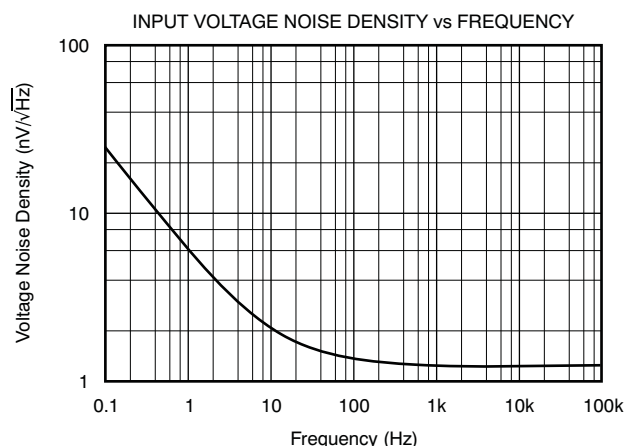
The OPA211 series of precision operational amplifiers achieves very low 1.1nV/ $\sqrt{\text{Hz}}$  noise density with a supply current of only 3.6mA. This series also offers rail-to-rail output swing, which maximizes dynamic range.

The extremely low voltage and low current noise, high speed, and wide output swing of the OPA211 series make these devices an excellent choice as a loop filter amplifier in PLL applications.

In precision data acquisition applications, the OPA211 series of op amps provides 700ns settling time to 16-bit accuracy throughout 10V output swings. This ac performance, combined with only 125 $\mu\text{V}$  of offset and 0.35 $\mu\text{V}/^\circ\text{C}$  of drift over temperature, makes the OPA211 ideal for driving high-precision 16-bit analog-to-digital converters (ADCs) or buffering the output of high-resolution digital-to-analog converters (DACs).

The OPA211 series is specified over a wide dual-power supply range of  $\pm 2.25\text{V}$  to  $\pm 18\text{V}$ , or for single-supply operation from +4.5V to +36V.

The OPA211 is available in the small DFN-8 (3mm  $\times$  3mm), MSOP-8, and SO-8 packages. A dual version, the OPA2211, is available in the DFN-8 (3mm  $\times$  3mm) or an SO-8 PowerPAD™ package. This series of op amps is specified from  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ .



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range (unless otherwise noted).

		VALUE	UNIT
Supply Voltage	$V_S = (V+) - (V-)$	40	V
Input Voltage		$(V-) - 0.5$ to $(V+) + 0.5$	V
Input Current (Any pin except power-supply pins)		±10	mA
Output Short-Circuit <sup>(2)</sup>		Continuous	
Operating Temperature	(T <sub>A</sub> )	–55 to +150	°C
Storage Temperature	(T <sub>A</sub> )	–65 to +150	°C
Junction Temperature	(T <sub>J</sub> )	200	°C
ESD Ratings	Human Body Model (HBM)	3000	V
	Charged Device Model (CDM)	1000	V

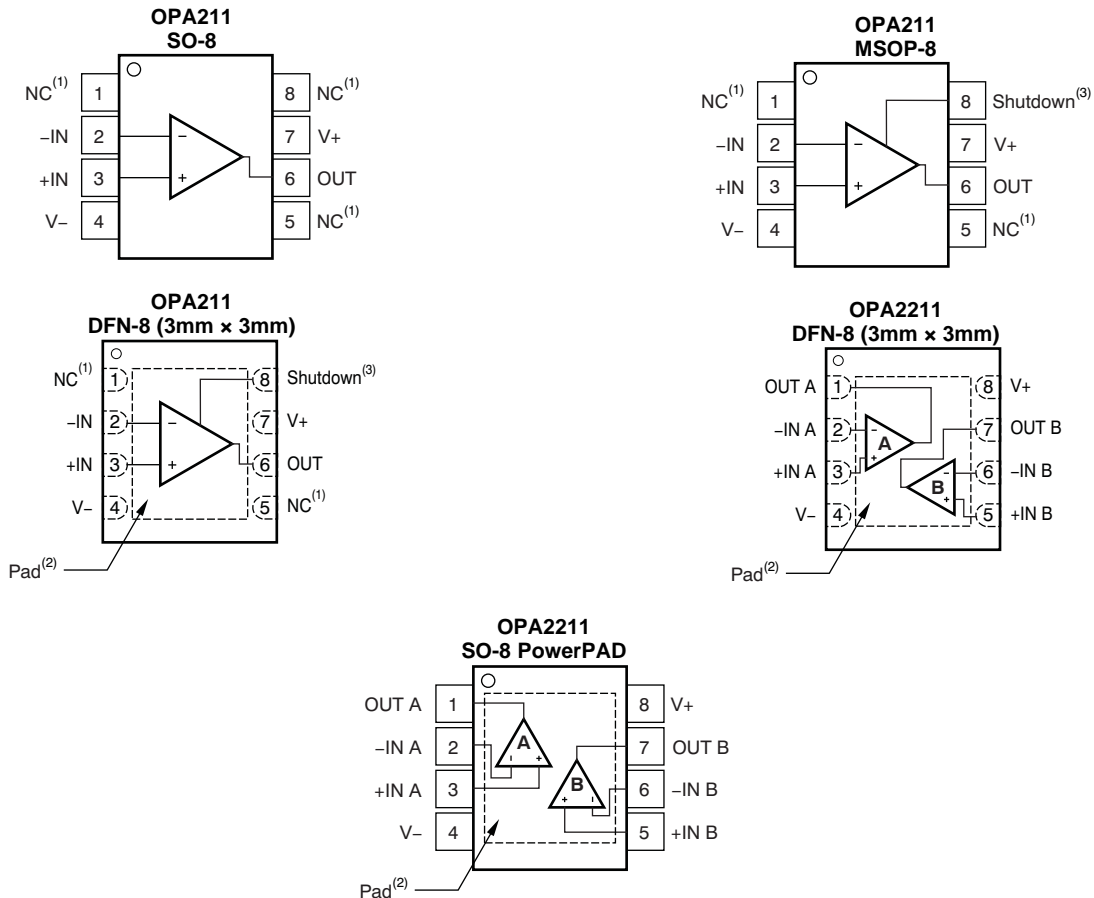
- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
- (2) Short-circuit to  $V_S/2$  (ground in symmetrical dual supply setups), one amplifier per package.

## PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	PACKAGE-LEAD	SINGLE	SHUTDOWN	DUAL	PACKAGE DESIGNATOR	PACKAGE MARKING
<b>Standard Grade</b>						
OPA211AI	DFN-8 (3mm × 3mm)	✓	✓		DRG	OBDQ
	MSOP-8	✓	✓		DGK	OBCQ
	SO-8	✓			D	A TI OPA 211
OPA2211AI	DFN-8 (3mm × 3mm)			✓	DRG	OBHQ
	SO-8 PowerPAD			✓	DDA	A TI OPA 2211
<b>High Grade</b>						
OPA211I	DFN-8 (3mm × 3mm)	✓	✓		DRG	OBDQ
	MSOP-8	✓	✓		DGK	OBCQ
	SO-8	✓			D	TI OPA 211

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

## PIN CONFIGURATIONS



- (1) NC denotes no internal connection.
- (2) Exposed thermal die pad on underside; connect thermal die pad to V-. Soldering the thermal pad improves heat dissipation and provides specified performance.
- (3) Shutdown function:
  - Device enabled:  $(V-) \leq V_{\text{SHUTDOWN}} \leq (V+) - 3V$
  - Device disabled:  $V_{\text{SHUTDOWN}} \geq (V+) - 0.35V$

## ELECTRICAL CHARACTERISTICS: $V_S = \pm 2.25V$ to $\pm 18V$

**BOLDFACE** limits apply over the specified temperature range,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

At  $T_A = +25^\circ\text{C}$ ,  $R_L = 10\text{k}\Omega$  connected to midsupply,  $V_{CM} = V_{OUT} = \text{midsupply}$ , unless otherwise noted.

PARAMETER		CONDITIONS	Standard Grade OPA211AI, OPA2211AI			High Grade OPA211I <sup>(1)</sup>			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE									
Input Offset Voltage	V <sub>OS</sub>								
OPA211		V <sub>S</sub> = ±15V		±30	±125		±20	±50	μV
OPA2211		V <sub>S</sub> = ±15V		±50	±150				μV
Drift	dV <sub>OS</sub> /dT			0.35	1.5		0.15	0.85	μV/°C
vs Power Supply	PSRR	V <sub>S</sub> = ±2.25V to ±18V		0.1	1		0.1	0.5	μV/V
Over Temperature					3			3	μV/V
INPUT BIAS CURRENT									
Input Bias Current	I <sub>B</sub>	V <sub>CM</sub> = 0V		±60	±175		±50	±125	nA
Over Temperature									
OPA211					±200			±200	nA
OPA2211					±250				nA
Offset Current	I <sub>OS</sub>	V <sub>CM</sub> = 0V		±25	±100		±20	±75	nA
Over Temperature					±150			±150	nA
NOISE									
Input Voltage Noise	e <sub>n</sub>	f = 0.1Hz to 10Hz		80			80		nV <sub>PP</sub>
Input Voltage Noise Density		f = 10Hz		2			2		nV/√Hz
		f = 100Hz		1.4			1.4		nV/√Hz
		f = 1kHz		1.1			1.1		nV/√Hz
Input Current Noise Density	i <sub>n</sub>	f = 10Hz		3.2			3.2		pA/√Hz
		f = 1kHz		1.7			1.7		pA/√Hz
INPUT VOLTAGE RANGE									
Common-Mode Voltage Range	V <sub>CM</sub>	V <sub>S</sub> ≥ ±5V V <sub>S</sub> < ±5V	(V-) + 1.8 (V-) + 2		(V+) - 1.4 (V+) - 1.4	(V-) + 1.8 (V-) + 2		(V+) - 1.4 (V+) - 1.4	V V
Common-Mode Rejection Ratio	CMRR	V <sub>S</sub> ≥ ±5V, (V-) + 2V ≤ V <sub>CM</sub> ≤ (V+) - 2V V <sub>S</sub> < ±5V, (V-) + 2V ≤ V <sub>CM</sub> ≤ (V+) - 2V	114 110	120 120		114 110	120 120		dB dB
INPUT IMPEDANCE									
Differential				20k    8			20k    8		Ω    pF
Common-Mode				10 <sup>9</sup>    2			10 <sup>9</sup>    2		Ω    pF
OPEN-LOOP GAIN									
Open-Loop Voltage Gain	A <sub>OL</sub>	(V-) + 0.2V ≤ V <sub>O</sub> ≤ (V+) - 0.2V, R <sub>L</sub> = 10kΩ	114	130		114	130		dB
	A <sub>OL</sub>	(V-) + 0.6V ≤ V <sub>O</sub> ≤ (V+) - 0.6V, R <sub>L</sub> = 600Ω	110	114		110	114		dB
Over Temperature									
OPA211	A <sub>OL</sub>	(V-) + 0.6V ≤ V <sub>O</sub> ≤ (V+) - 0.6V, I <sub>O</sub> ≤ 15mA	110			110			dB
OPA211	A <sub>OL</sub>	(V-) + 0.6V ≤ V <sub>O</sub> ≤ (V+) - 0.6V, 15mA ≤ I <sub>O</sub> ≤ 30mA	103			103			dB
OPA2211 (per channel)	A <sub>OL</sub>	(V-) + 0.6V ≤ V <sub>O</sub> ≤ (V+)-0.6V, I <sub>O</sub> ≤ 15mA	100						dB
FREQUENCY RESPONSE									
Gain-Bandwidth Product	GBW	G = 100 G = 1		80 45			80 45		MHz MHz
Slew Rate	SR			27			27		V/μs
Settling Time, 0.01%	t <sub>s</sub>	V <sub>S</sub> = ±15V, G = -1, 10V Step, C <sub>L</sub> = 100pF		400			400		ns
0.0015% (16-bit)		V <sub>S</sub> = ±15V, G = -1, 10V Step, C <sub>L</sub> = 100pF		700			700		ns
Overload Recovery Time		G = -10		500			500		ns
Total Harmonic Distortion + Noise	THD+N	G = +1, f = 1kHz, V <sub>O</sub> = 3V <sub>RMS</sub> , R <sub>L</sub> = 600Ω		0.000015			0.000015		%
				-136			-136		dB

(1) Shaded cells indicate different specifications from standard-grade version of device.

**ELECTRICAL CHARACTERISTICS:  $V_S = \pm 2.25V$  to  $\pm 18V$  (continued)**
**BOLDFACE** limits apply over the specified temperature range,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ .

At  $T_A = +25^{\circ}C$ ,  $R_L = 10k\Omega$  connected to midsupply,  $V_{CM} = V_{OUT} =$  midsupply, unless otherwise noted.

PARAMETER	CONDITIONS	Standard Grade OPA211AI, OPA2211AI			High Grade OPA211I <sup>(1)</sup>			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>OUTPUT</b>								
<b>Voltage Output</b> $V_{OUT}$	$R_L = 10k\Omega$ , $A_{OL} \geq 114dB$ $R_L = 600\Omega$ , $A_{OL} \geq 110dB$ $I_O < 15mA$ , $A_{OL} \geq 110dB$	<b>(V-) + 0.2</b> (V-) + 0.6 <b>(V-) + 0.6</b>		<b>(V+) – 0.2</b> (V+) – 0.6 <b>(V+) – 0.6</b>	<b>(V-) + 0.2</b> (V-) + 0.6 <b>(V-) + 0.6</b>		<b>(V+) – 0.2</b> (V+) – 0.6 <b>(V+) – 0.6</b>	<b>V</b> V <b>V</b>
Short-Circuit Current $I_{SC}$			+30/–45			+30/–45		mA
Capacitive Load Drive $C_{LOAD}$		See <a href="#">Typical Characteristics</a>			See <a href="#">Typical Characteristics</a>			pF
Open-Loop Output Impedance $Z_O$	$f = 1MHz$		5			5		$\Omega$
<b>SHUTDOWN</b>								
Shutdown Pin Input Voltage <sup>(2)</sup>	Device disabled (shutdown) Device enabled	(V+) – 0.35		(V+) – 3	(V+) – 0.35		(V+) – 3	V V
Shutdown Pin Leakage Current			1			1		$\mu A$
Turn-On Time <sup>(3)</sup>			2			2		$\mu s$
Turn-Off Time <sup>(3)</sup>			3			3		$\mu s$
Shutdown Current	Shutdown (disabled)		1	20		1	20	$\mu A$
<b>POWER SUPPLY</b>								
Specified Voltage $V_S$		$\pm 2.25$		$\pm 18$	$\pm 2.25$		$\pm 18$	V
Quiescent Current (per channel) $I_Q$	$I_{OUT} = 0A$		3.6	4.5		3.6	4.5	mA
<b>Over Temperature (per channel)</b>				<b>6</b>			<b>6</b>	<b>mA</b>
<b>TEMPERATURE RANGE</b>								
Specified Range $T_A$		–40		+125	–40		+125	$^{\circ}C$
Operating Range $T_A$		–55		+150	–55		+150	$^{\circ}C$
Thermal Resistance								
OPA211								
SO-8 $\theta_{JA}$			150			150		$^{\circ}C/W$
MSOP-8 $\theta_{JA}$			200			200		$^{\circ}C/W$
DFN-8 (3mm x 3mm) $\theta_{JA}$ <sup>(4)</sup>			65			65		$^{\circ}C/W$
$\theta_{JP}$			20			20		$^{\circ}C/W$
OPA2211								
SO-8 PowerPAD $\theta_{JA}$ <sup>(4)</sup>			52			52		$^{\circ}C/W$
$\theta_{JP}$			2			2		$^{\circ}C/W$
DFN-8 (3mm x 3mm) $\theta_{JA}$ <sup>(4)</sup>			65			65		$^{\circ}C/W$
$\theta_{JP}$			10			10		$^{\circ}C/W$

(2) When disabled, the output assumes a high-impedance state.

(3) See [Typical Characteristic](#) graphs, [Figure 41](#) through [Figure 43](#).

(4) Typical  $\theta_{JA}$  specification is based on the use of a high-k board.

## TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 18\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.

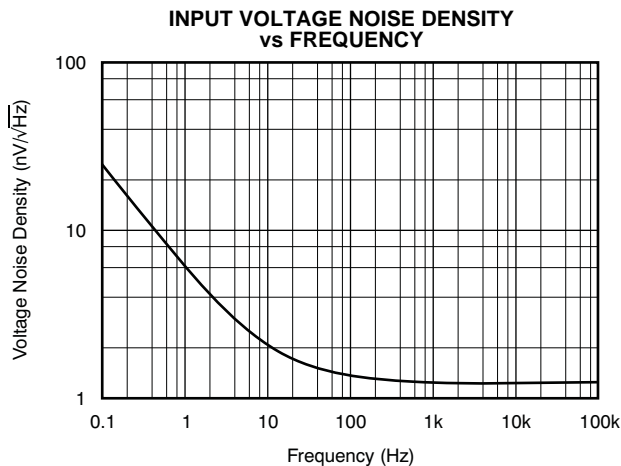


Figure 1.

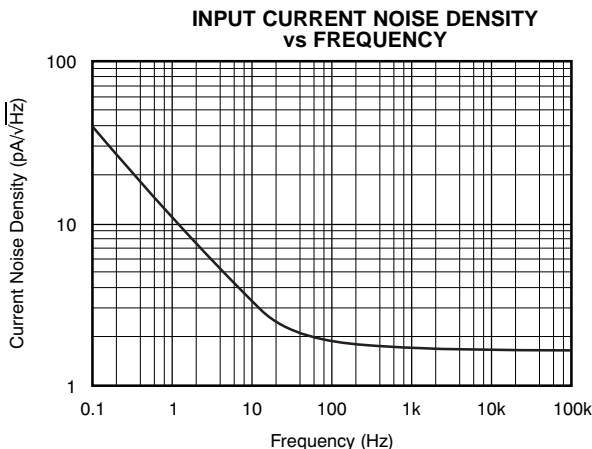


Figure 2.

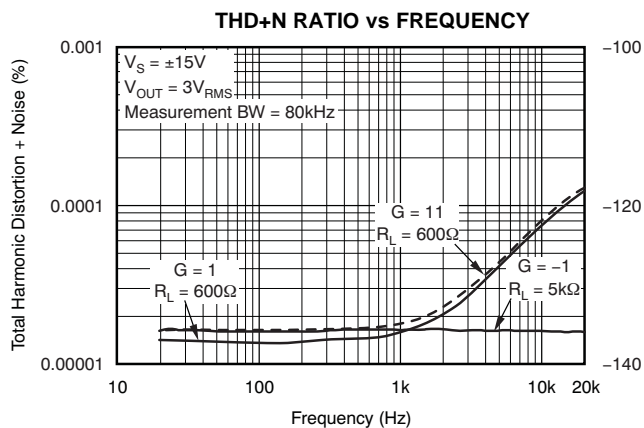


Figure 3.

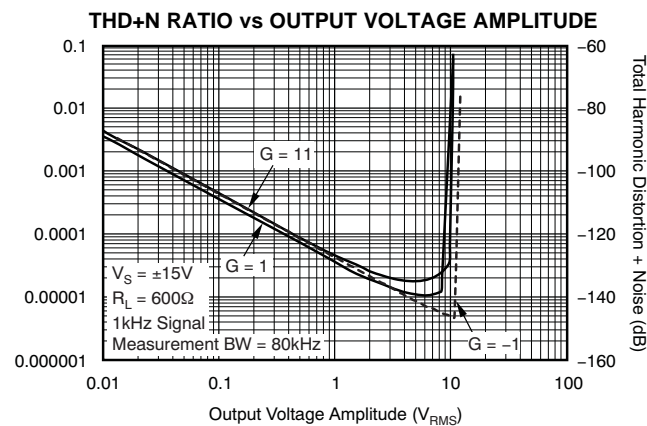


Figure 4.

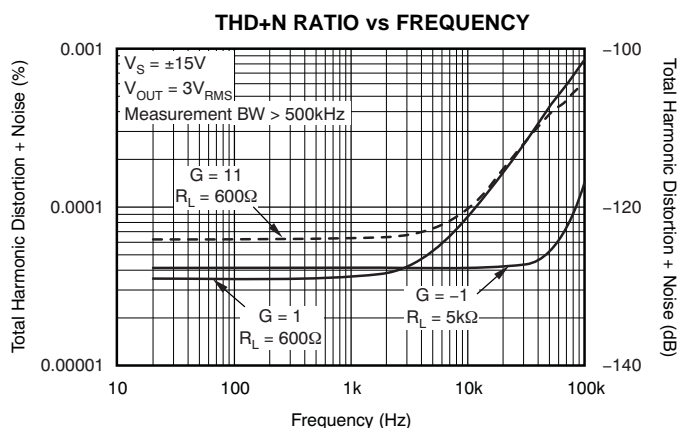


Figure 5.

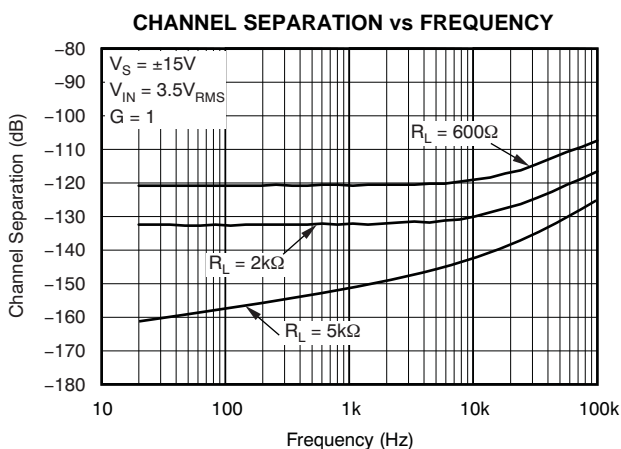


Figure 6.

## TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 18\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.

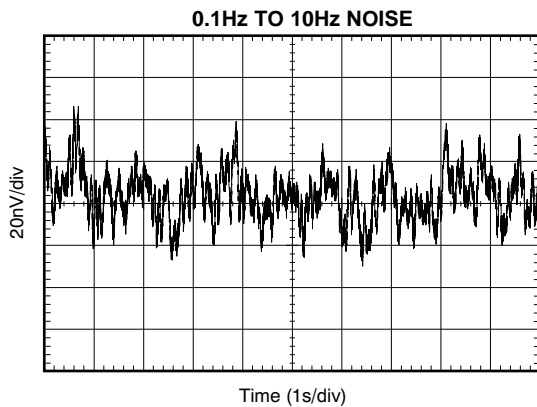


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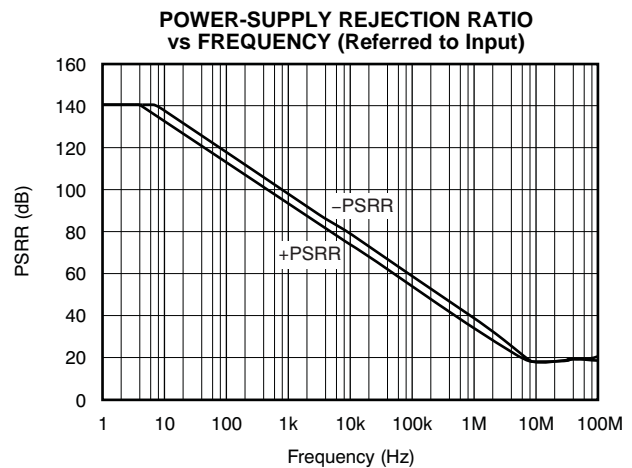


Figure 8.

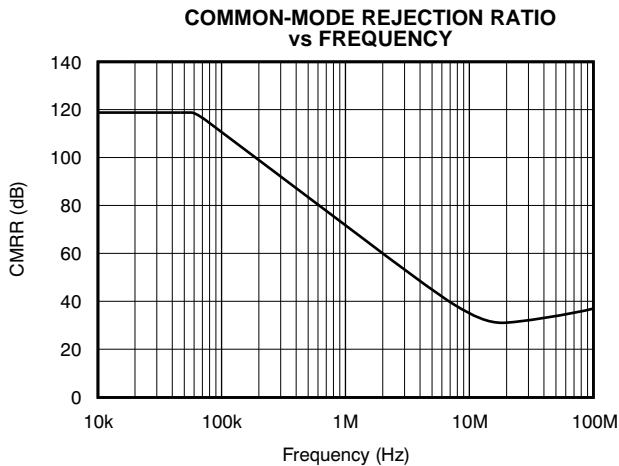


Figure 9.

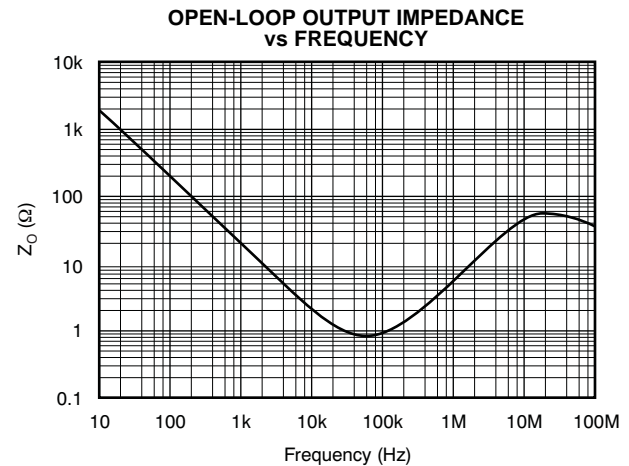


Figure 10.

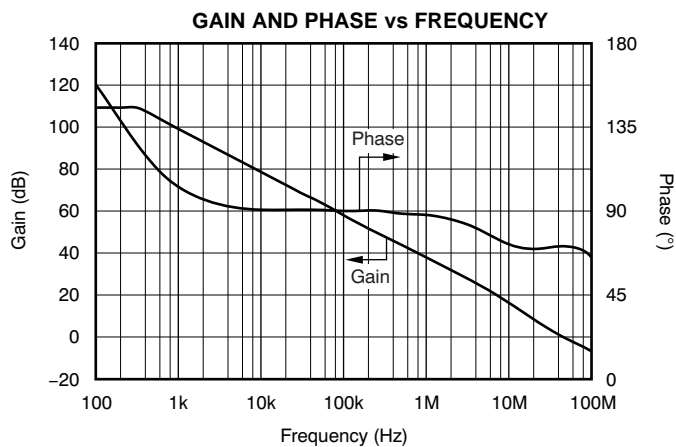


Figure 11.

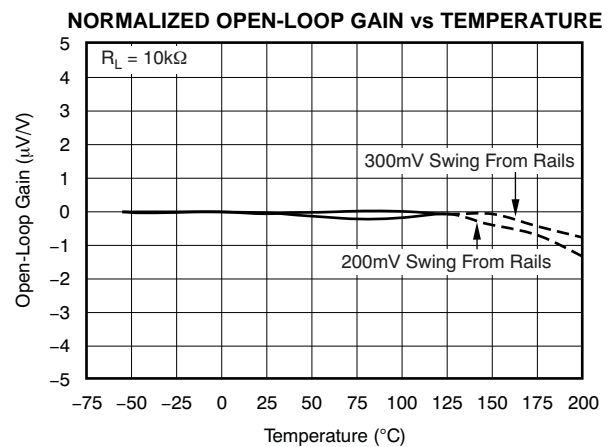


Figure 12.

## TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 18\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

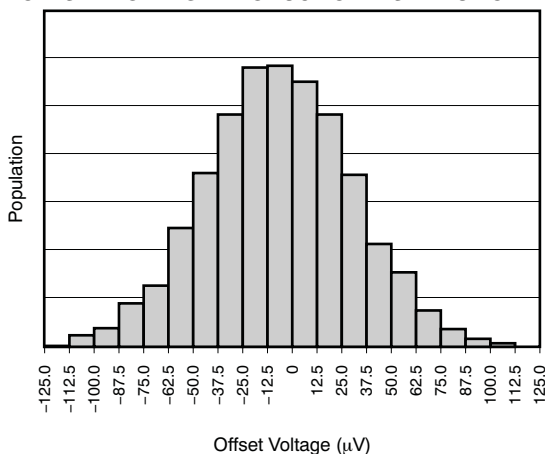


Figure 13.

OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION

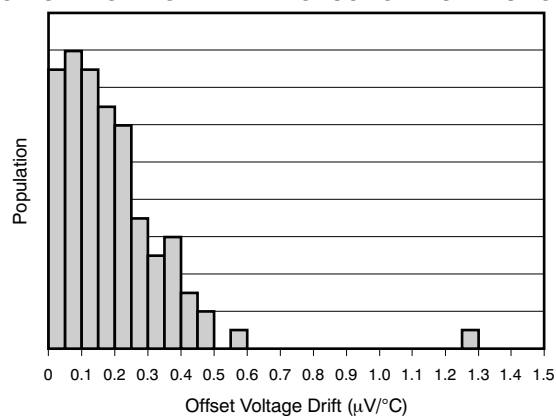


Figure 14.

$I_B$  AND  $I_{OS}$  CURRENT vs TEMPERATURE

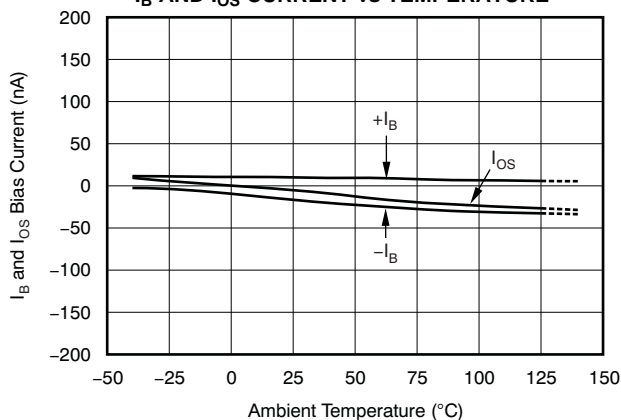


Figure 15.

OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

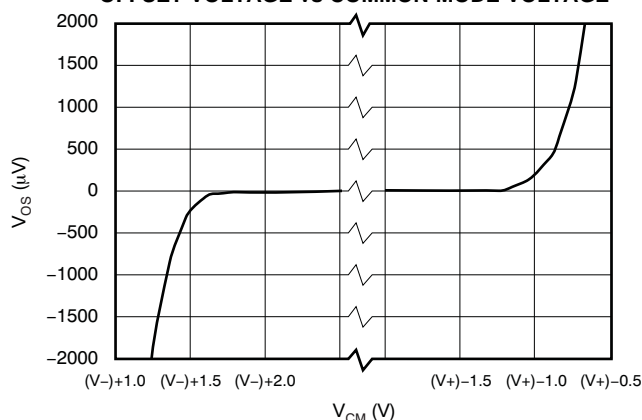


Figure 16.

$V_{OS}$  WARMUP

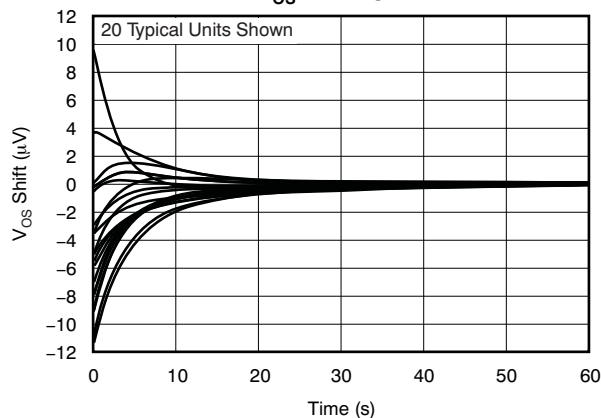


Figure 17.

INPUT OFFSET CURRENT vs SUPPLY VOLTAGE

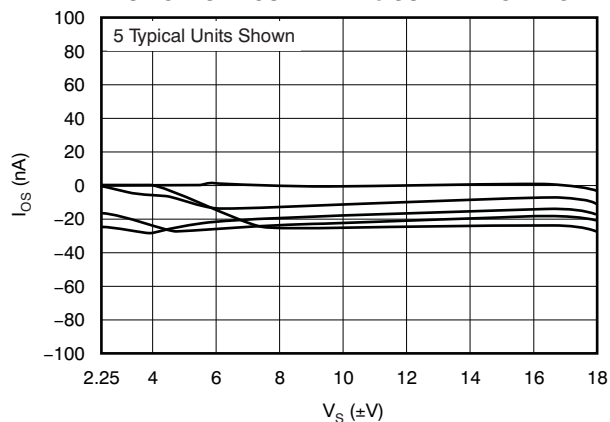


Figure 18.



## TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 18\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.

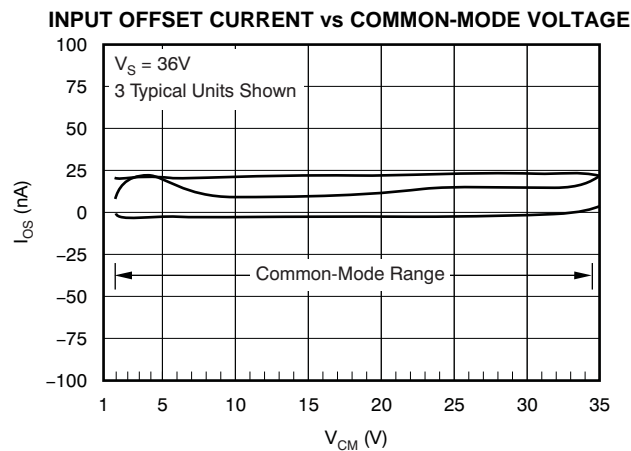


Figure 19.

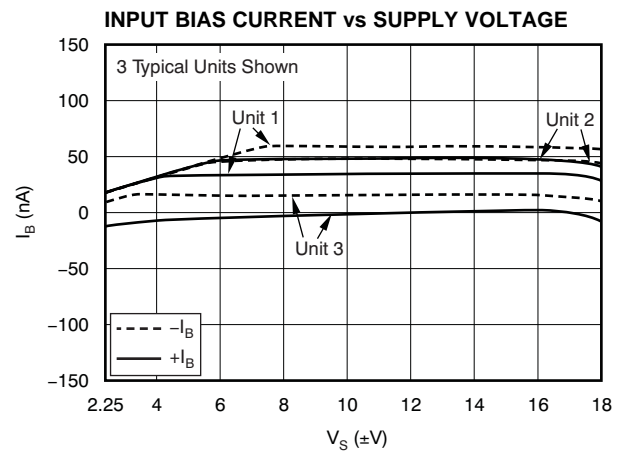


Figure 20.

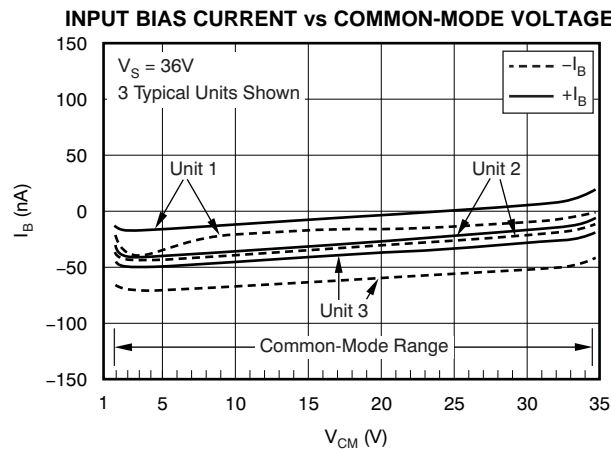


Figure 21.

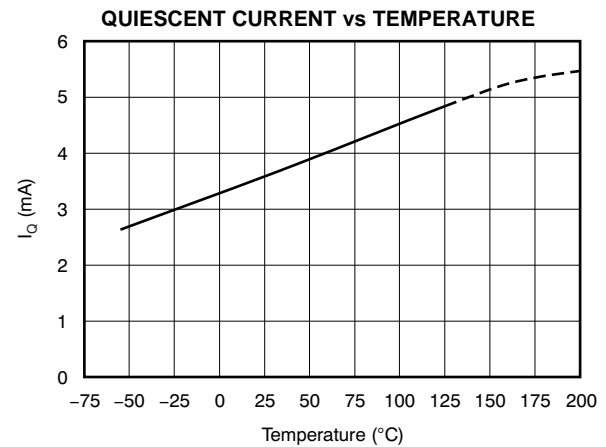


Figure 22.

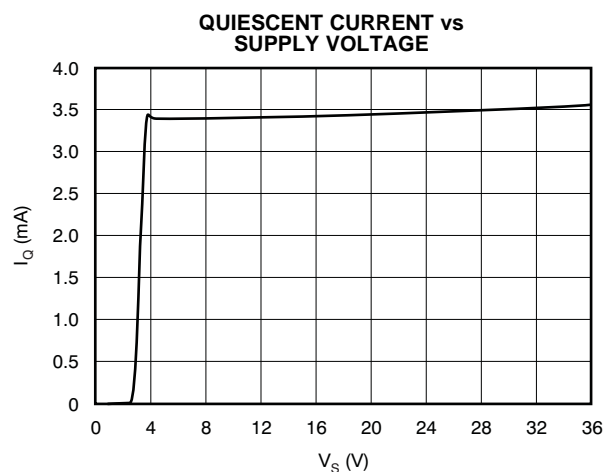


Figure 23.

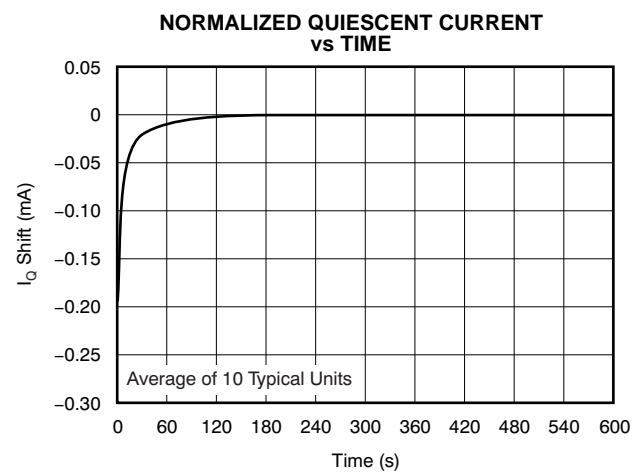


Figure 24.

## TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 18\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.

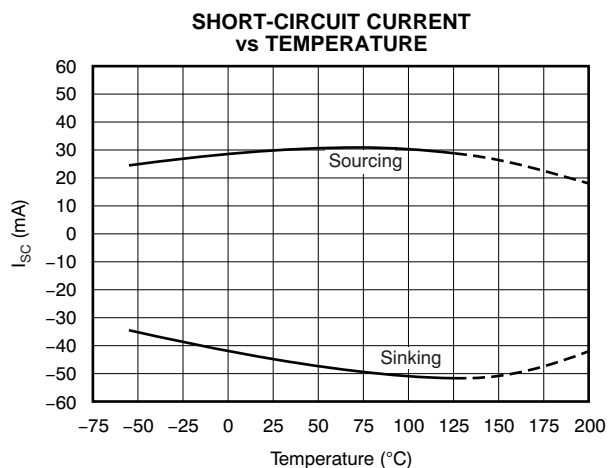


Figure 25.

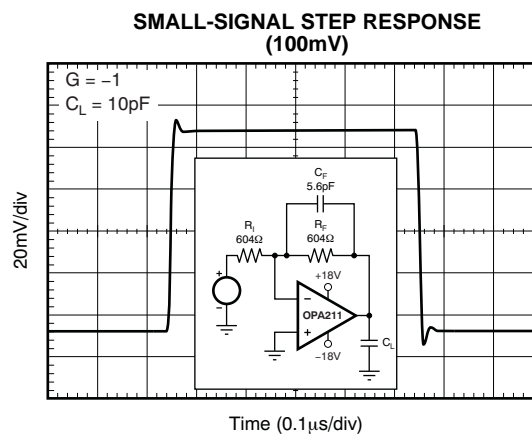


Figure 26.

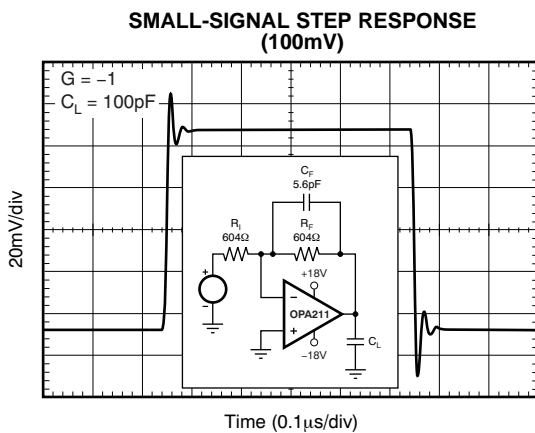


Figure 27.

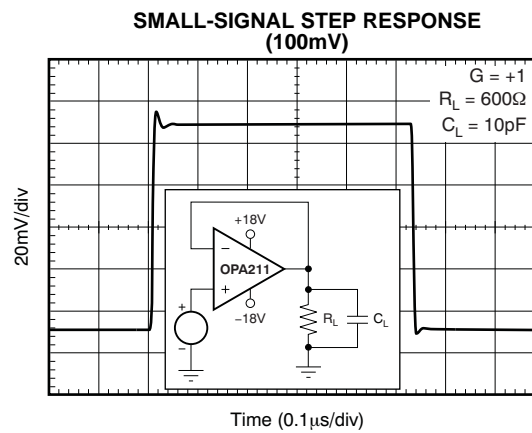


Figure 28.

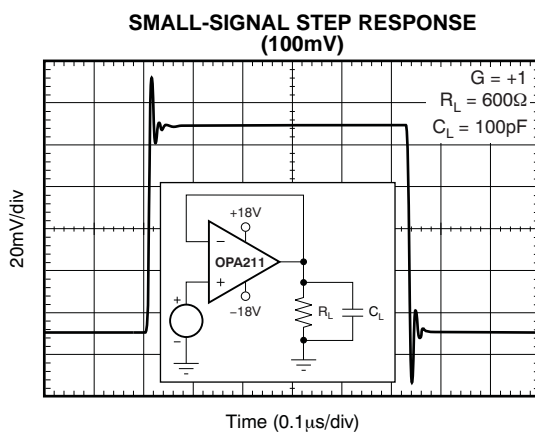


Figure 29.

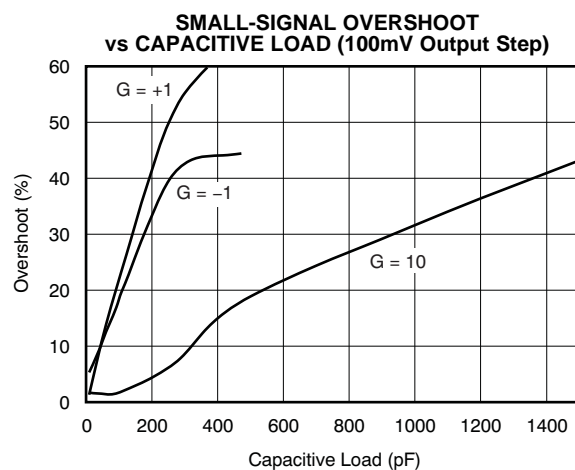


Figure 30.

## TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 18\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.

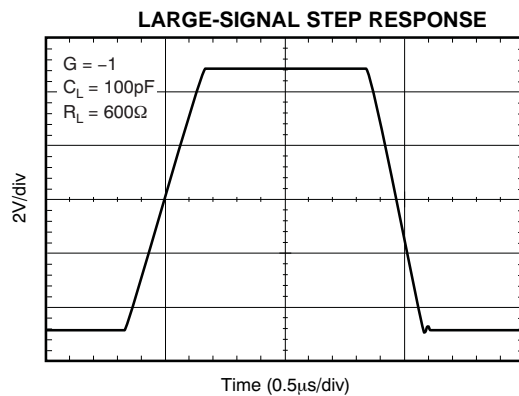


Figure 31.

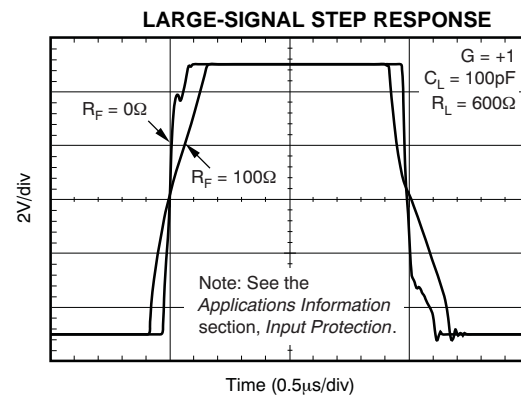


Figure 32.

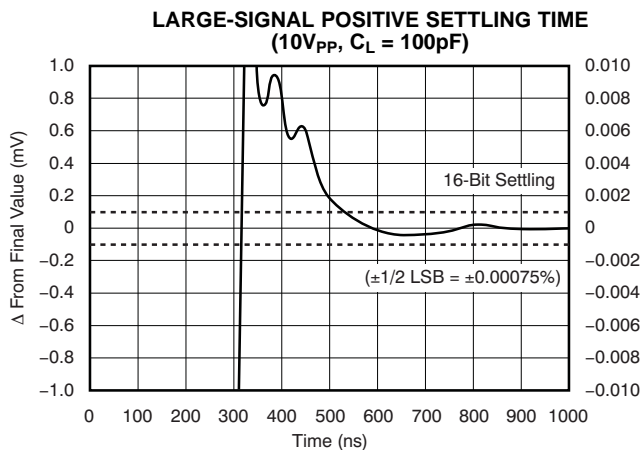


Figure 33.

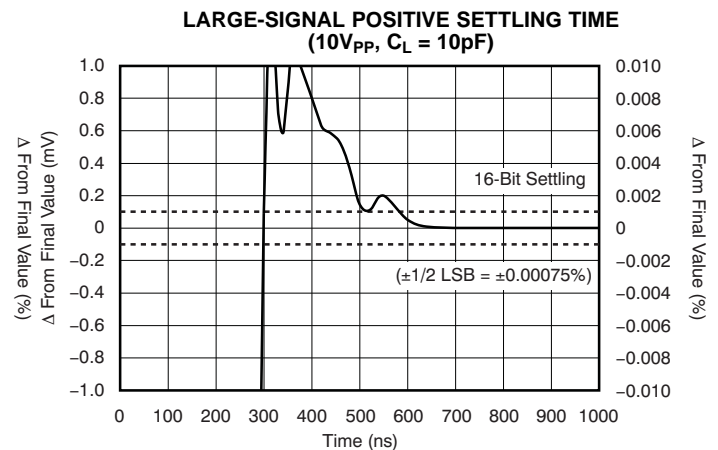


Figure 34.

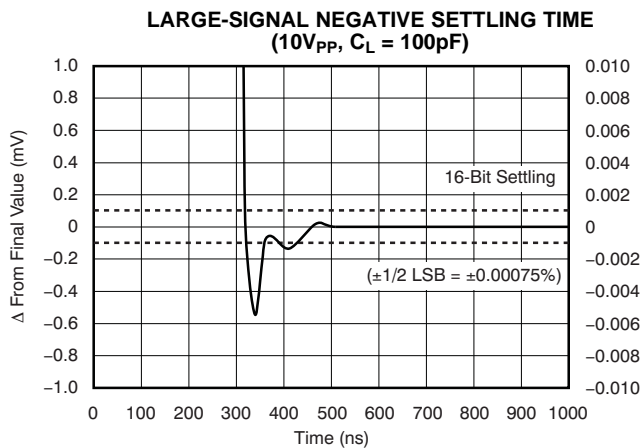


Figure 35.

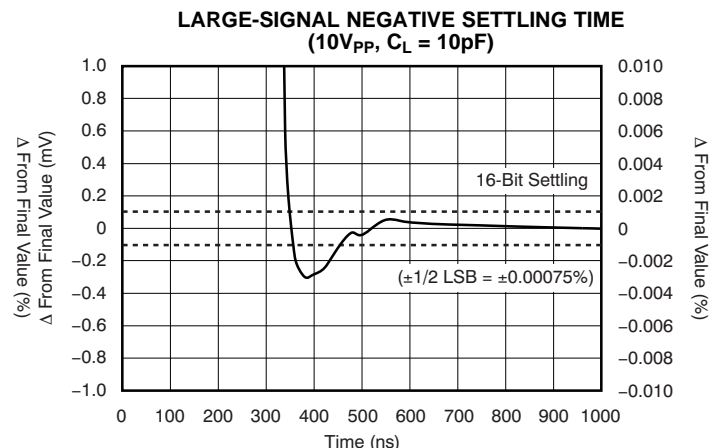
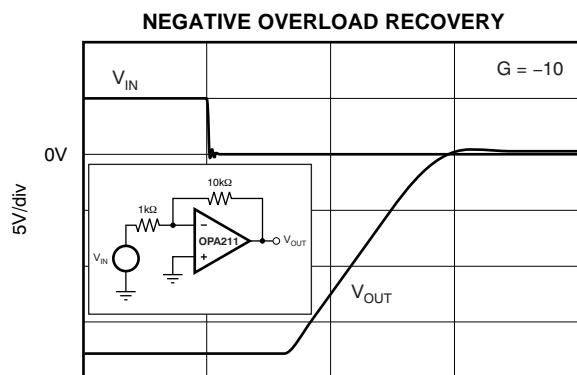


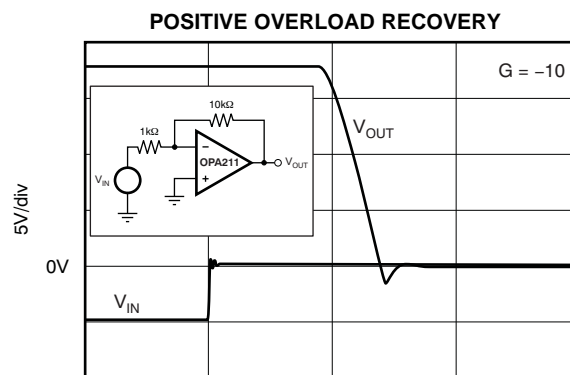
Figure 36.

## TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 18\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.



Time (0.5μs/div)  
Figure 37.



Time (0.5μs/div)  
Figure 38.

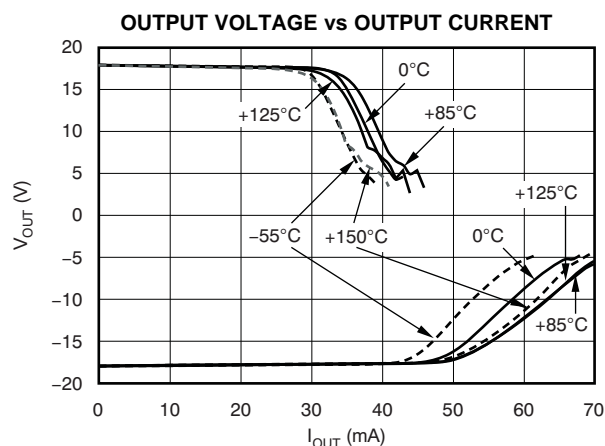


Figure 39.

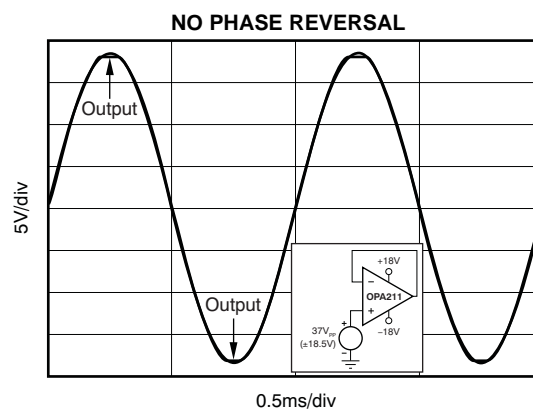


Figure 40.

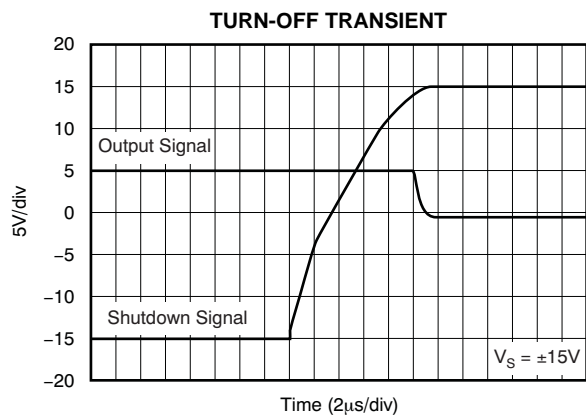


Figure 41.

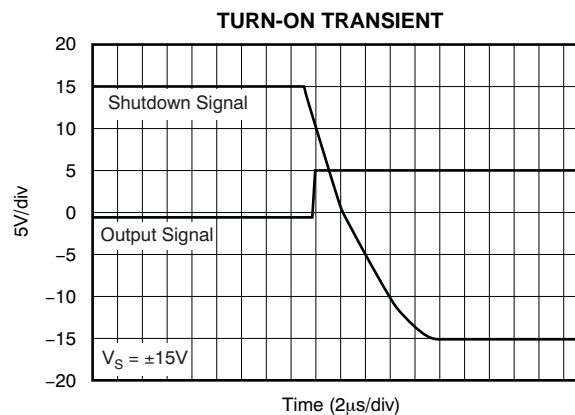
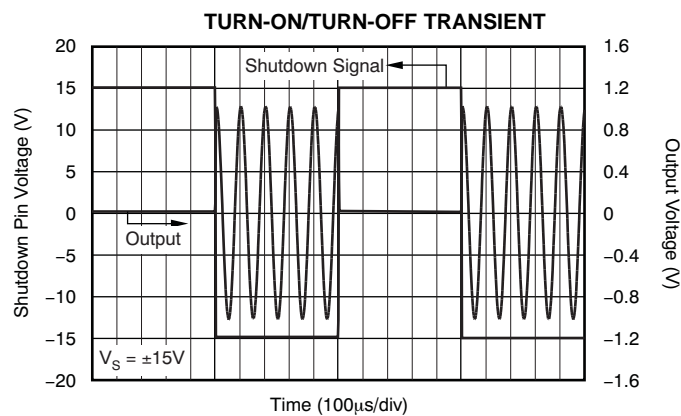


Figure 42.

## TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 18\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.



**Figure 43.**

## APPLICATION INFORMATION

The OPA211 and OPA2211 are unity-gain stable, precision op amps with very low noise. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1 $\mu$ F capacitors are adequate. [Figure 44](#) shows a simplified schematic of the OPA211. This die uses a SiGe bipolar process and contains 180 transistors.

### OPERATING VOLTAGE

OPA211 series op amps operate from  $\pm 2.25$ V to  $\pm 18$ V supplies while maintaining excellent performance. The OPA211 series can operate with as little as +4.5V between the supplies and with up to +36V between the supplies. However, some applications do not require equal positive and

negative output voltage swing. With the OPA211 series, power-supply voltages do not need to be equal. For example, the positive supply could be set to +25V with the negative supply at -5V or vice-versa.

The common-mode voltage must be maintained within the specified range. In addition, key parameters are assured over the specified temperature range,  $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . Parameters that vary significantly with operating voltage or temperature are shown in the [Typical Characteristics](#).

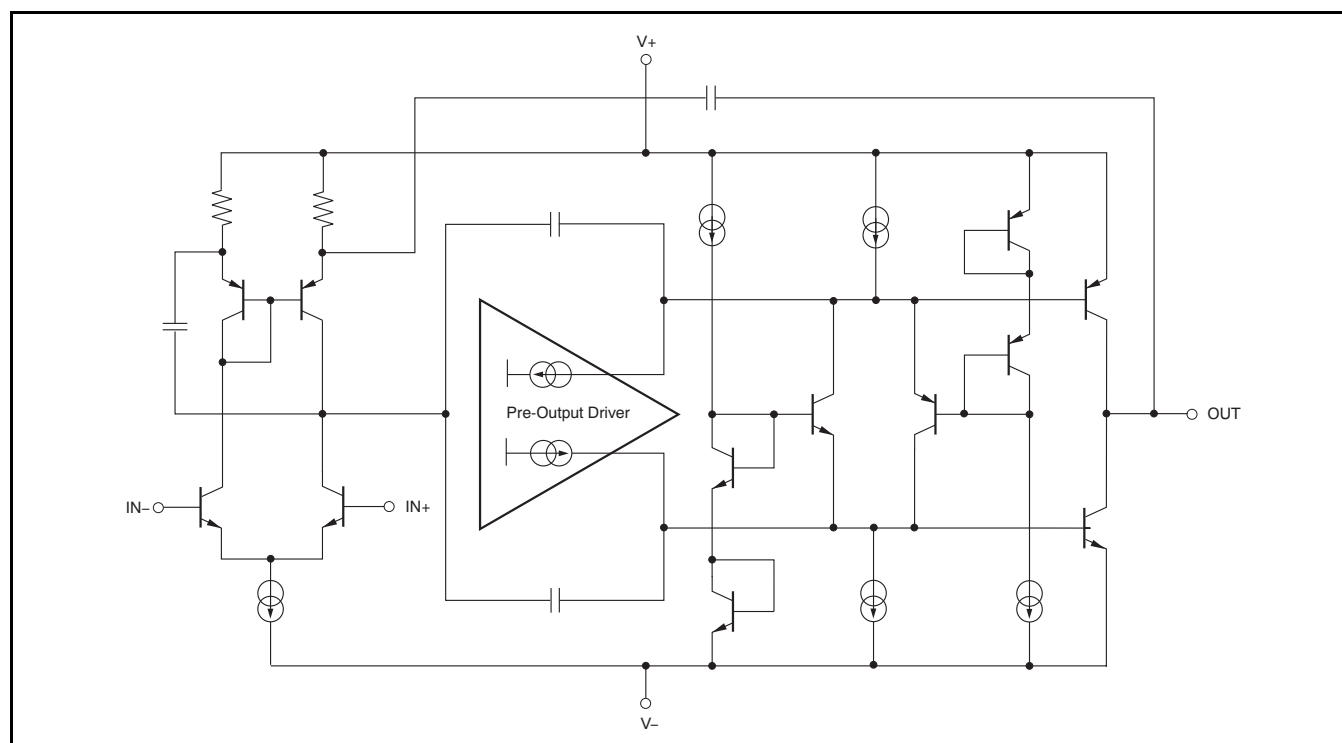


Figure 44. OPA211 Simplified Schematic

## INPUT PROTECTION

The input terminals of the OPA211 are protected from excessive differential voltage with back-to-back diodes, as shown in Figure 45. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or  $G = 1$  circuits, fast ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. This effect is illustrated in Figure 32 of the Typical Characteristics. If the input signal is fast enough to create this forward bias condition, the input signal current must be limited to 10mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPA211, and is discussed in the Noise Performance section of this data sheet. Figure 45 shows an example implementing a current-limiting feedback resistor.

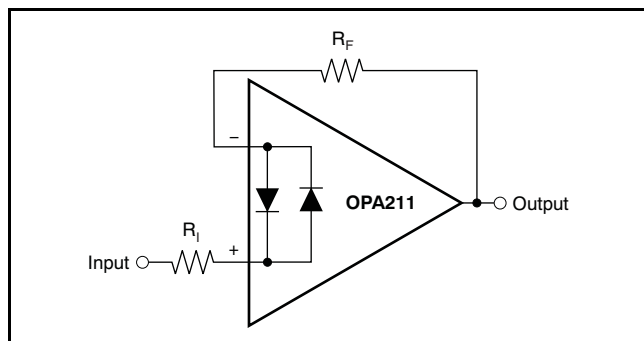


Figure 45. Pulsed Operation

## SHUTDOWN

The shutdown (enable) function of the OPA211 is referenced to the positive supply voltage of the operational amplifier. A valid high disables the op amp. A valid high is defined as  $(V+) - 0.35V$  of the positive supply applied to the shutdown pin. A valid low is defined as  $(V+) - 3V$  below the positive supply pin. For example, with  $V_{CC}$  at  $\pm 15V$ , the device is enabled at or below 12V. The device is disabled at or above 14.65V. If dual or split power supplies are used, care should be taken to ensure the valid high or valid low input signals are properly referred to the positive supply voltage. This pin must be connected to a valid high or low voltage or driven, and not left open-circuit. The enable and disable times are provided in the Typical Characteristics section (see Figure 41 through Figure 43). When disabled, the output assumes a high-impedance state.

## NOISE PERFORMANCE

Figure 46 shows total circuit noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). Two different op amps are shown with total circuit noise calculated. The OPA211 has very low voltage noise, making it ideal for low source impedances (less than 2k $\Omega$ ). A similar precision op amp, the OPA227, has somewhat higher voltage noise but lower current noise. It provides excellent noise performance at moderate source impedance (10k $\Omega$  to 100k $\Omega$ ). Above 100k $\Omega$ , a FET-input op amp such as the OPA132 (very low current noise) may provide improved performance. The equation in Figure 46 is shown for the calculation of the total circuit noise. Note that  $e_n$  = voltage noise,  $i_n$  = current noise,  $R_S$  = source impedance,  $k$  = Boltzmann's constant =  $1.38 \times 10^{-23}$  J/K, and  $T$  is temperature in degrees Kelvin.

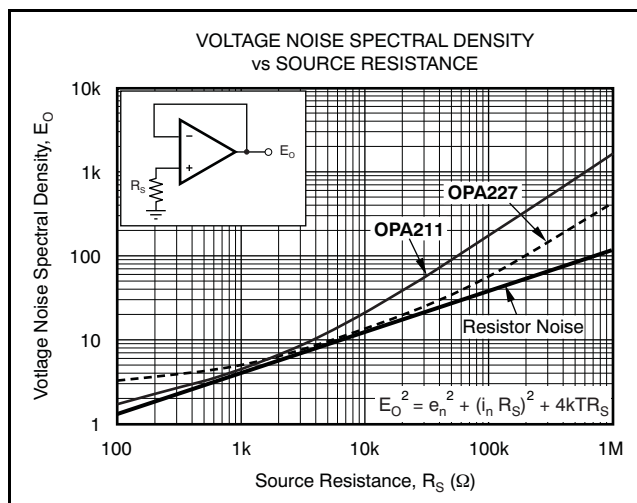


Figure 46. Noise Performance of the OPA211 and OPA227 in Unity-Gain Buffer Configuration

## BASIC NOISE CALCULATIONS

Design of low-noise op amp circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the op amp, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in Figure 46. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 46 depicts total noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). The operational amplifier itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise.

Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible and voltage noise generally dominates. For high source impedance, current noise may dominate.

Figure 47 illustrates both inverting and noninverting op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the op amp reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

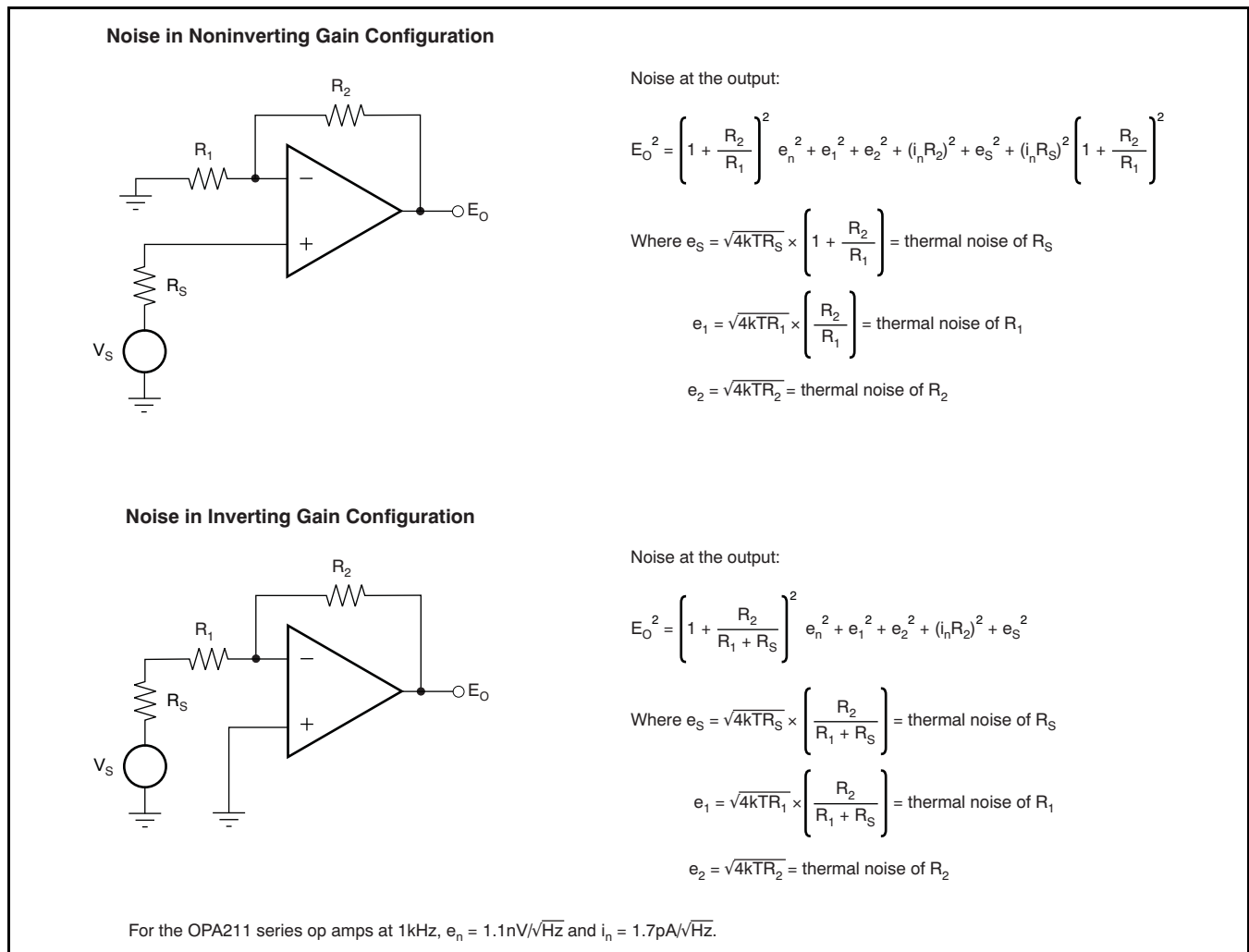


Figure 47. Noise Calculation in Gain Configurations



## TOTAL HARMONIC DISTORTION MEASUREMENTS

OPA211 series op amps have excellent distortion characteristics. THD + Noise is below 0.0002% ( $G = +1$ ,  $V_{OUT} = 3V_{RMS}$ ) throughout the audio frequency range, 20Hz to 20kHz, with a 600Ω load.

The distortion produced by OPA211 series op amps is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit illustrated in Figure 48 can be used to extend the measurement capabilities.

Op amp distortion can be considered an internal error source that can be referred to the input. Figure 48 shows a circuit that causes the op amp distortion to be 101 times greater than that normally produced by the op amp. The addition of  $R_3$  to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101, thus extending the resolution by 101. Note that the input signal and load applied to the op amp are the same as with conventional feedback without  $R_3$ . The value of  $R_3$  should be kept small to minimize its effect on the distortion measurements.

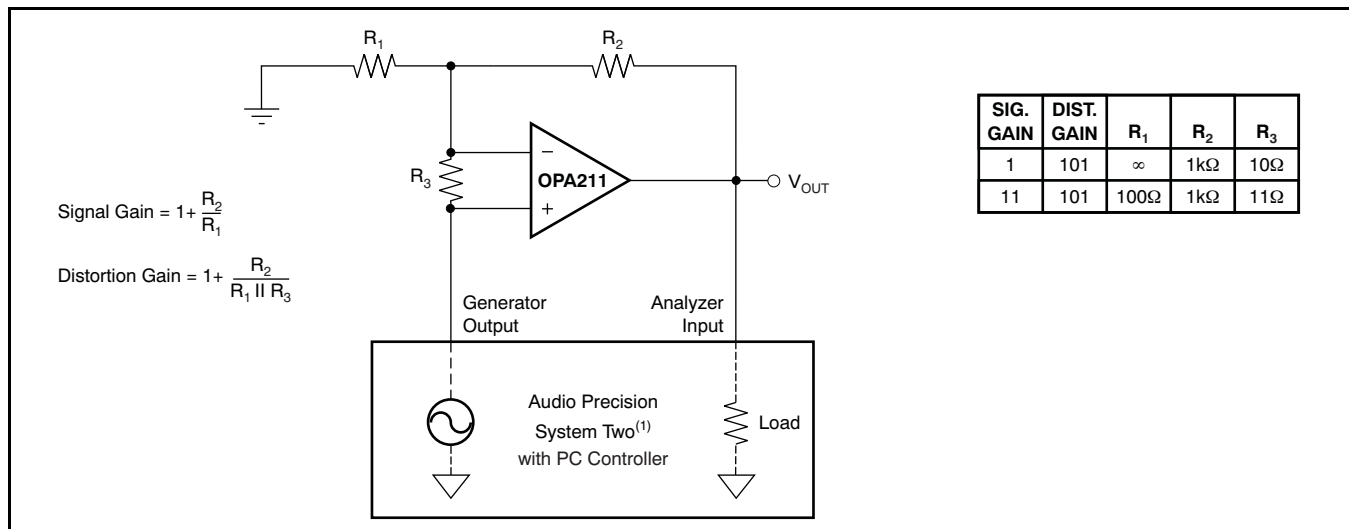
Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an

Audio Precision System Two distortion/noise analyzer, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

## ELECTRICAL OVERSTRESS

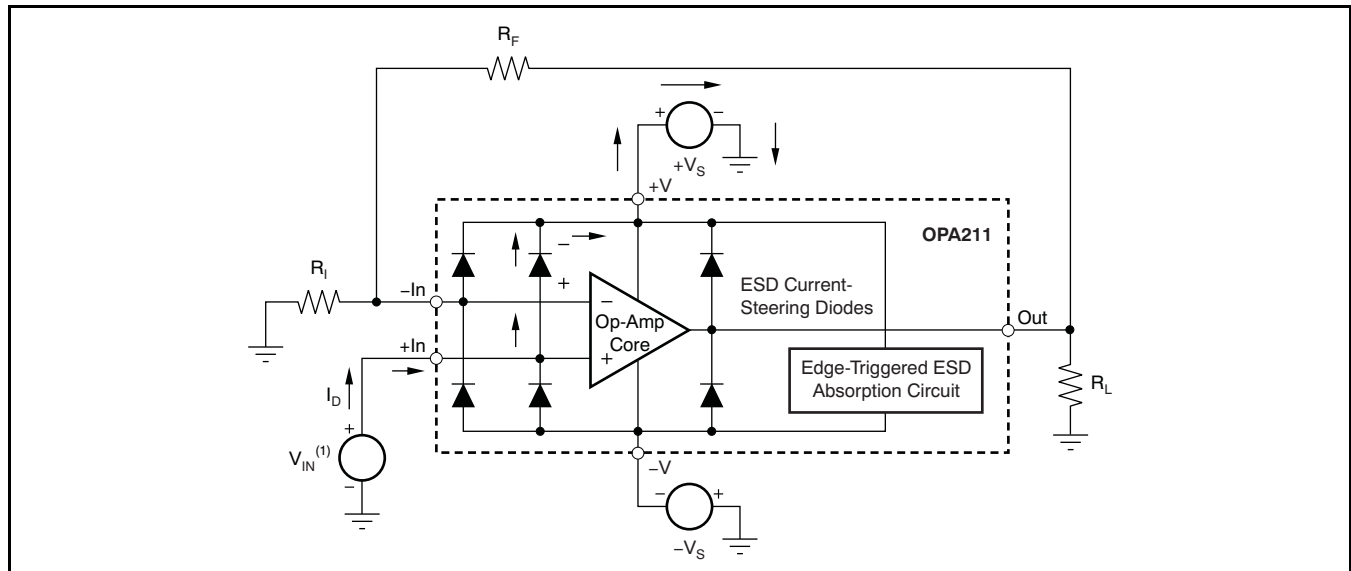
Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. See Figure 49 for an illustration of the ESD circuits contained in the OPA211 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.



(1) For measurement bandwidth, see Figure 3, Figure 4, and Figure 5.

**Figure 48. Distortion Test Circuit**



(1)  $V_{IN} = +V_S + 500\text{mV}$ .

**Figure 49. Equivalent Internal ESD Circuitry and Its Relation to a Typical Circuit Application**

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA211 but below the device breakdown voltage level. Once this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit such as that illustrated in Figure 49, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

Figure 49 depicts a specific example where the input voltage,  $V_{IN}$ , exceeds the positive supply voltage ( $+V_S$ ) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If  $+V_S$  can sink the current, one of the upper input steering diodes conducts and directs current to  $+V_S$ . Excessively high current levels can flow with increasingly higher  $V_{IN}$ . As a result, the datasheet specifications recommend that applications limit the input current to 10mA.

If the supply is not capable of sinking the current,  $V_{IN}$  may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings. In extreme but rare cases, the absorption device triggers on while  $+V_S$  and  $-V_S$  are applied. If this event happens, a direct current path is established between the  $+V_S$  and  $-V_S$  supplies. The power dissipation of the absorption device is quickly exceeded, and the extreme internal heating destroys the operational amplifier.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies  $+V_S$  and/or  $-V_S$  are at 0V. Again, it depends on the supply characteristic while at 0V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source via the current steering diodes. This state is not a normal bias condition; the amplifier

most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

## THERMAL CONSIDERATIONS

A primary issue with all semiconductor devices is junction temperature ( $T_J$ ). The most obvious consideration is assuring that  $T_J$  never exceeds the absolute maximum rating specified for the device. However, addressing device thermal dissipation has benefits beyond protecting the device from damage. Even modest increases in junction temperature can decrease op amp performance, and temperature-related errors can accumulate. Understanding the power generated by the device within the specific application and assessing the thermal effects on the error tolerance lead to a better understanding of system performance and thermal-dissipation needs. For dual-channel products, the worst-case power resulting from both channels must be determined. Products with a thermal pad (DFN and PowerPAD devices) provide the best thermal conduction away from the junction; see the *Thermal Resistance from Junction to Pad* parameter ( $\theta_{JP}$ ) in the [Electrical Characteristics](#) section. The use of packages with a thermal pad improves thermal dissipation. The device achieves its optimal performance through careful board and system design that considers characteristics such as board thickness, metal layers, component spacing, airflow, and board orientation. Refer to these application notes (available for download at [www.ti.com](http://www.ti.com)) for additional details: [SZZA017A](#), [SCBA017](#), and [SPRA953A](#). For unusual loads and signals, see [SBOA022](#).

## DFN PACKAGE

The OPA211 is offered in an DFN-8 package (also known as SON). The DFN package is a QFN package with lead contacts on only two sides of the bottom of the package. This leadless package maximizes board space and enhances thermal and electrical characteristics through an exposed pad.

DFN packages are physically small, and have a smaller routing area, improved thermal performance, and improved electrical parasitics. Additionally, the absence of external leads eliminates bent-lead issues.

The DFN package can be easily mounted using standard printed circuit board (PCB) assembly techniques. See Application Note *QFN/SON PCB Attachment* ([SLUA271](#)) and Application Report *Quad Flatpack No-Lead Logic Packages* ([SCBA017](#)), both available for download at [www.ti.com](http://www.ti.com).

**The exposed leadframe die pad on the bottom of the package must be connected to V-. Soldering the thermal pad improves heat dissipation and enables specified device performance.**

## DFN LAYOUT GUIDELINES

The exposed leadframe die pad on the DFN package should be soldered to a thermal pad on the PCB. A mechanical drawing showing an example layout is attached at the end of this data sheet. Refinements to this layout may be necessary based on assembly process requirements. Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad. The five holes in the landing pattern are optional, and are intended for use with thermal vias that connect the leadframe die pad to the heatsink area on the PCB.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

## GENERAL POWERPAD DESIGN CONSIDERATIONS

The OPA2211 is available in a thermally-enhanced SO-8 PowerPAD package. This package is constructed using a downset leadframe upon which the die is mounted, as [Figure 50\(a\)](#) and [Figure 50\(b\)](#) illustrate. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package, as shown in [Figure 50\(c\)](#). This thermal pad has direct thermal contact with the die; thus, excellent thermal performance is achieved by providing a good thermal path away from the thermal pad.

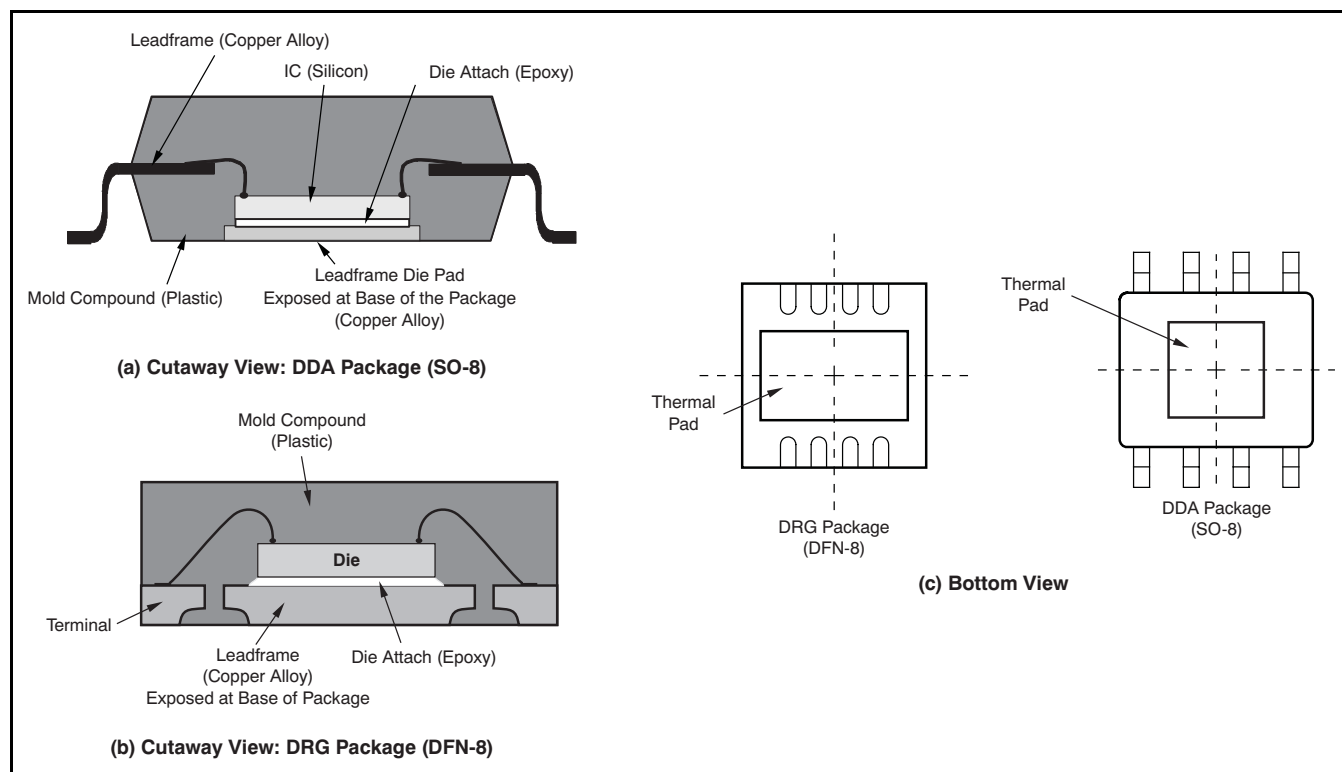
The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. Soldering the PowerPAD to the printed circuit board (PCB) is always required, even with applications that have low power dissipation. This technique provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

The PowerPAD must be connected to the most negative supply voltage on the device (V<sub>-</sub>).

1. Prepare the PCB with a top-side etch pattern. There should be etching for the leads as well as etch for the thermal pad.
2. Place recommended holes in the area of the thermal pad. Ideal thermal land size and thermal via patterns for the SO-8 DDA package can be seen in the technical brief, *PowerPAD Thermally-Enhanced Package* ([SLMA002](#)), available for download at [www.ti.com](http://www.ti.com). These holes should be 13 mils (0,33mm) in diameter. Keep them small, so that solder wicking through the holes is not a problem during reflow. An

example thermal land pattern mechanical drawing is attached to the end of this data sheet.

3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area to help dissipate the heat generated by the OPA2211 SO-8. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered; thus, wicking is not a problem.
4. Connect all holes to the internal plane that is at the same voltage potential as the V<sub>-</sub> pin.
5. When connecting these holes to the internal plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This configuration makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the OPA2211 PowerPAD package should make their connection to the internal plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its six holes exposed. The bottom-side solder mask should cover the holes of the thermal pad area. This masking prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, simply place the OPA2211 SO-8 IC in position and run the chip through the solder reflow operation as any standard surface-mount component. This preparation results in a properly installed part.



**Figure 50. Views of Thermally-Enhanced SO-8 and DFN-8 Packages**

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (November, 2008) to Revision G	Page
• Changed orderable status of OPA2211 device packages to <i>released</i> from <i>product preview</i> throughout document .....	2
• Revised description of NC pin .....	3
• Added <i>Input Offset Voltage</i> , <i>Input Bias Current</i> , <i>Open-Loop Gain</i> , and <i>Thermal Resistance</i> specifications to indicate performance for OPA2211 device .....	4
• Corrected Temperature Range parametric symbol location for specified and operating range specifications .....	5
• Added footnote (4) to <i>Electrical Characteristics</i> table .....	5
• Updated <a href="#">Figure 3</a> .....	6
• Added information to legend in <a href="#">Figure 4</a> .....	6
• Added <a href="#">Figure 5</a> .....	6
• Added <a href="#">Figure 6</a> .....	6
• Changed title of <a href="#">Figure 12</a> for clarification .....	7
• Corrected circuit drawing in <a href="#">Figure 26</a> .....	10
• Corrected circuit drawing in <a href="#">Figure 27</a> .....	10
• Changed first paragraph of <i>Total Harmonic Distortion Measurements</i> section .....	17
• Updated <a href="#">Figure 48</a> .....	17
• Added <i>Thermal Considerations</i> section .....	19
• Added <i>General PowerPAD Design Considerations</i> section .....	20

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA211AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 211 A	<a href="#">Samples</a>
OPA211AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 211 A	<a href="#">Samples</a>
OPA211AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   Call TI	Level-2-260C-1 YEAR	-40 to 125	OBCQ	<a href="#">Samples</a>
OPA211AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU   Call TI	Level-2-260C-1 YEAR	-40 to 125	OBCQ	<a href="#">Samples</a>
OPA211AIDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBCQ	<a href="#">Samples</a>
OPA211AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 211 A	<a href="#">Samples</a>
OPA211AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 211 A	<a href="#">Samples</a>
OPA211AIDRGR	ACTIVE	SON	DRG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBDQ	<a href="#">Samples</a>
OPA211AIDRGT	ACTIVE	SON	DRG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBDQ	<a href="#">Samples</a>
OPA211AIDRGTG4	ACTIVE	SON	DRG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBDQ	<a href="#">Samples</a>
OPA211ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 211	<a href="#">Samples</a>
OPA211IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   Call TI	Level-2-260C-1 YEAR	-40 to 125	OBCQ	<a href="#">Samples</a>
OPA211IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU   Call TI	Level-2-260C-1 YEAR	-40 to 125	OBCQ	<a href="#">Samples</a>
OPA211IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 211	<a href="#">Samples</a>
OPA211IDRGR	ACTIVE	SON	DRG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBDQ	<a href="#">Samples</a>



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA211IDRGT	ACTIVE	SON	DRG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBDQ	<a href="#">Samples</a>
OPA2211AIDDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA 2211 A	<a href="#">Samples</a>
OPA2211AIDDA	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA 2211 A	<a href="#">Samples</a>
OPA2211AIDRGR	ACTIVE	SON	DRG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBHQ	<a href="#">Samples</a>
OPA2211AIDRGT	ACTIVE	SON	DRG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBHQ	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF OPA211 :**

- Enhanced Product: [OPA211-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA211AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA211AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA211AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA211AIDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA211AIDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA211IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA211IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA211IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA211IDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA211IDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2211AIDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2211AIDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2211AIDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA211AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA211AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA211AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA211AIDRGR	SON	DRG	8	3000	367.0	367.0	35.0
OPA211AIDRGT	SON	DRG	8	250	210.0	185.0	35.0
OPA211IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA211IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA211IDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA211IDRGR	SON	DRG	8	3000	367.0	367.0	35.0
OPA211IDRGT	SON	DRG	8	250	210.0	185.0	35.0
OPA2211AIDAR	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
OPA2211AIDRGR	SON	DRG	8	3000	367.0	367.0	35.0
OPA2211AIDRGT	SON	DRG	8	250	210.0	185.0	35.0

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - This package complies to JEDEC MS-012 variation BA

PowerPAD is a trademark of Texas Instruments.

DDA (R-PDSO-G8)

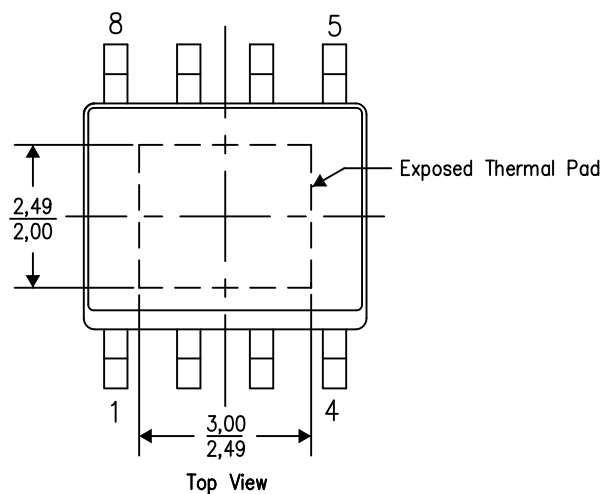
PowerPAD™ PLASTIC SMALL OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

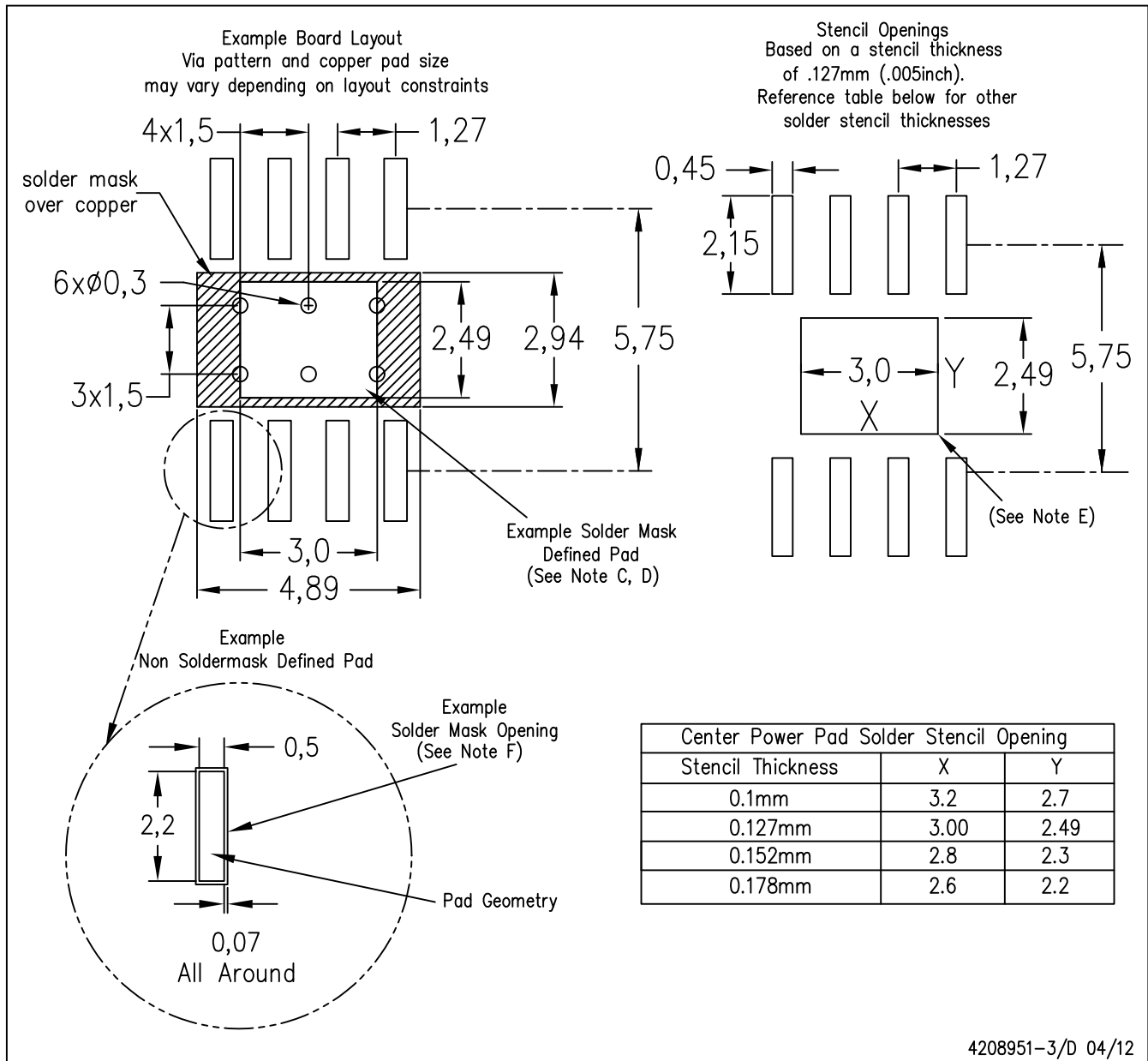
4206322-3/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



## DGK (S-PDSO-G8)

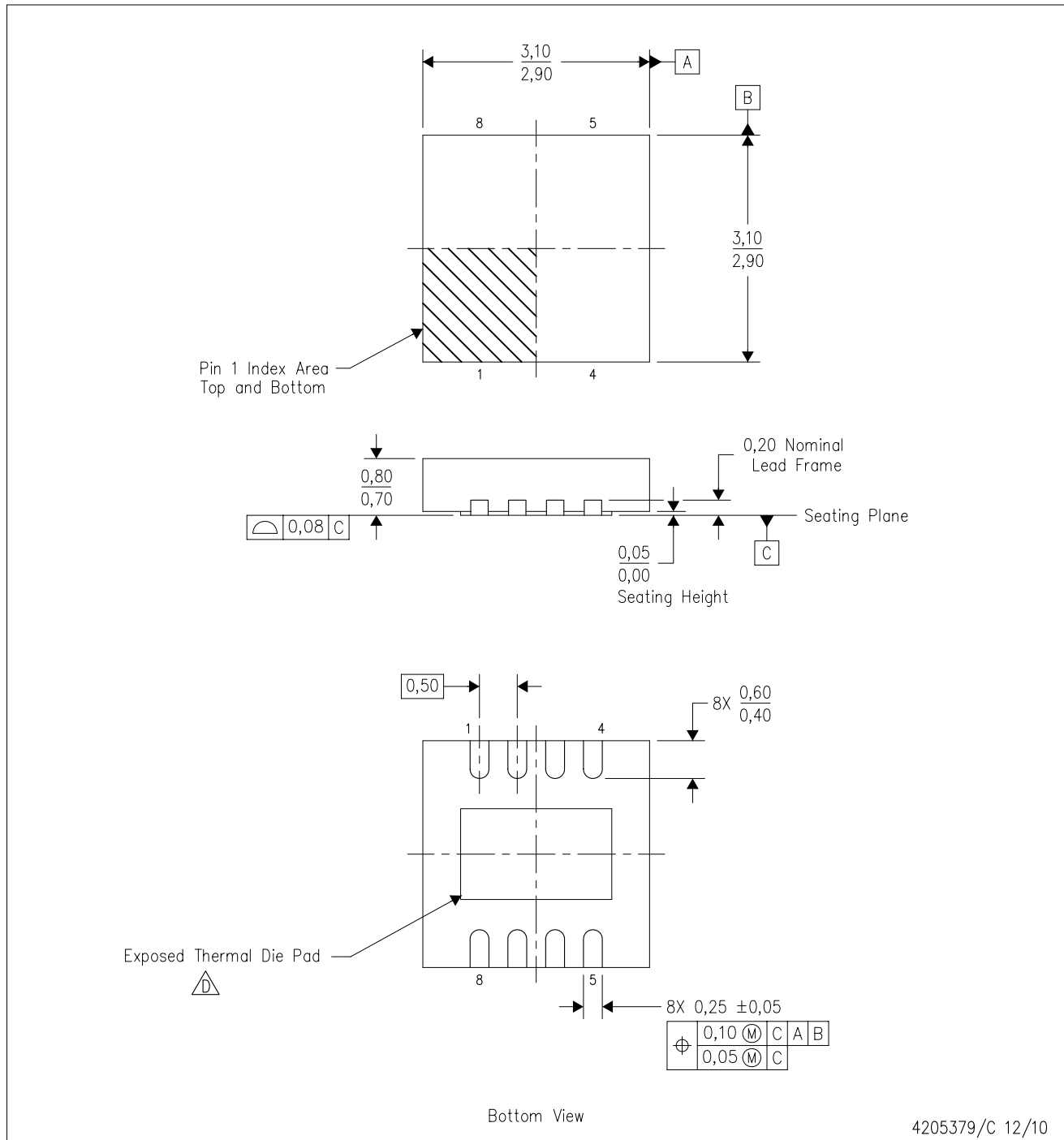
## PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DRG (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. SON (Small Outline No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. JEDEC MO-229 package registration pending.

DRG (S-PWSON-N8)

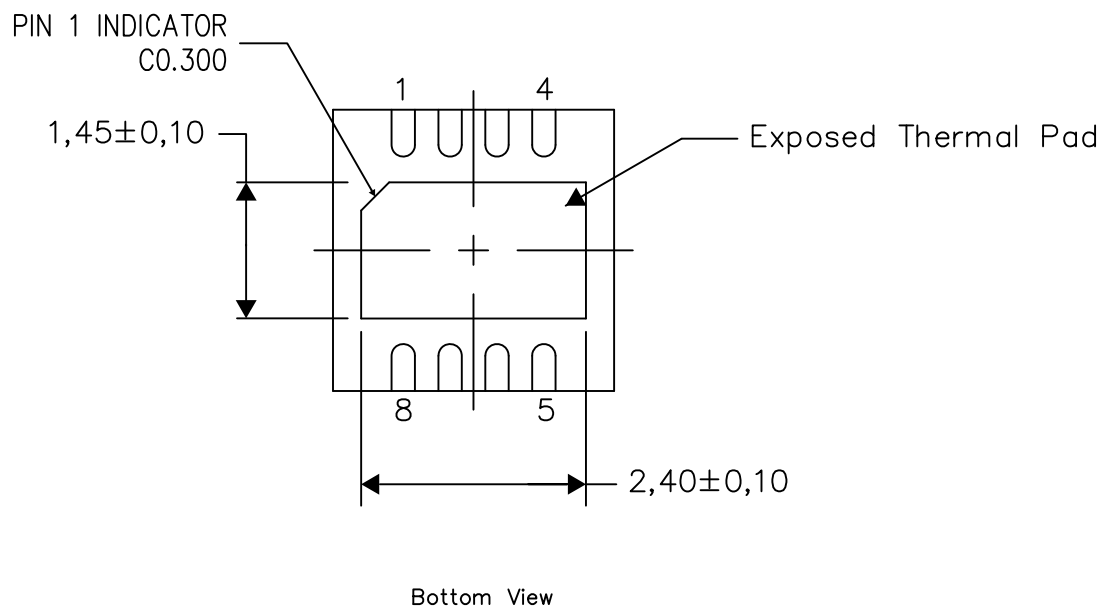
PLASTIC SMALL OUTLINE NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



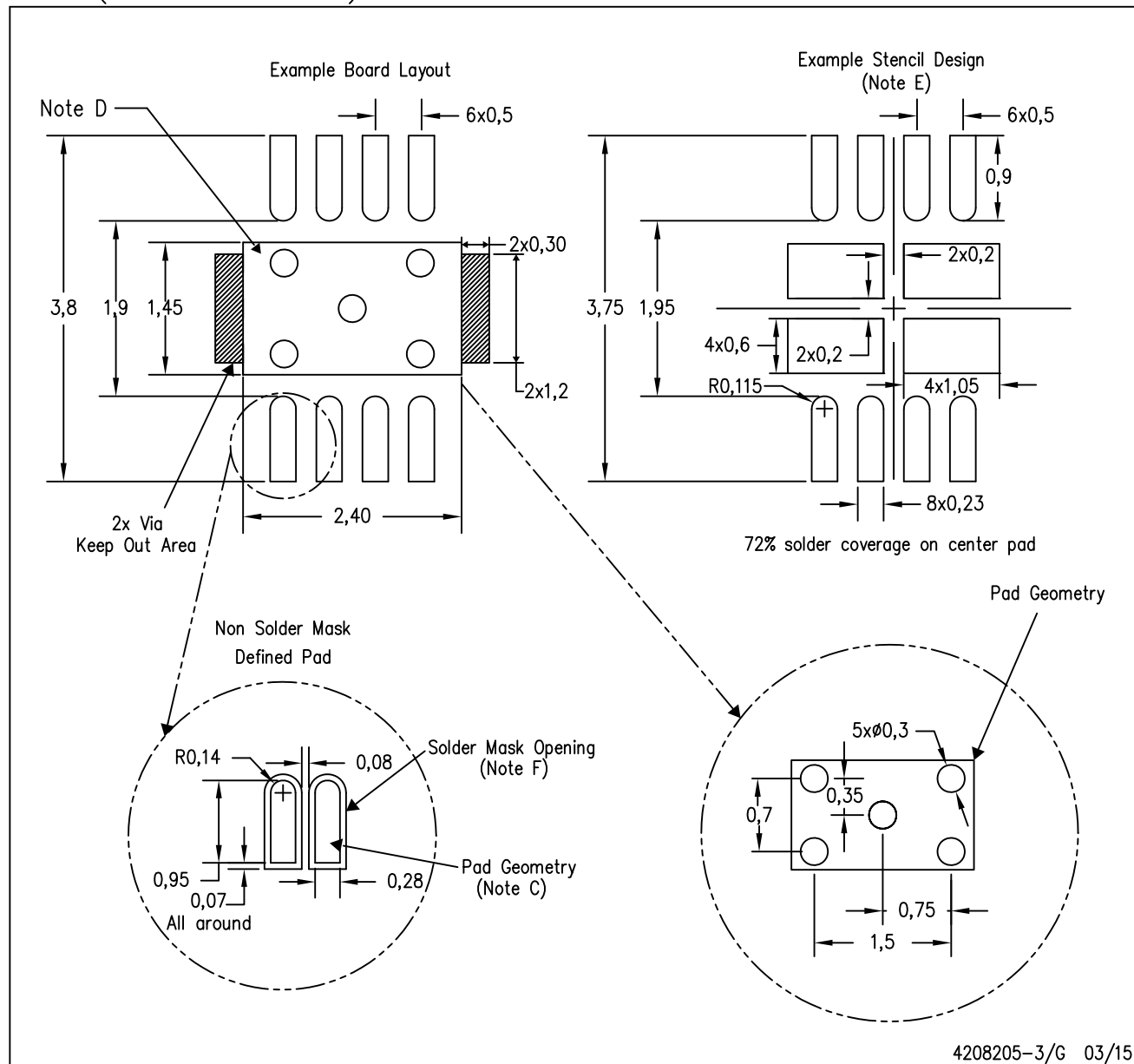
Exposed Thermal Pad Dimensions

4206881-3/I 03/15

NOTE: All linear dimensions are in millimeters

DRG (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-SM-782 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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