

Features

- RoHS compliant*
- Halogen free**
- ESD protection >15 kV
- Protects Vcc and two data lines

Applications

- Ethernet - 10/100/1000 Base T
- Firewire and USB
- Portable electronics
- Video/graphic cards

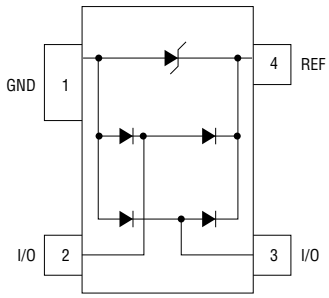
BOURNS®

CD143A-SR05LC - Steering/TVS Diode Array Series

General Information

The Bourns® Model CD143A-SR05LC device provides ESD, EFT and surge protection for the external ports of portable electronic devices such as cellphones, handheld electronics and personal computers.

The ESD protection provided by the component enables a data port to withstand a minimum ±8 KV Contact / ±15 KV Air Discharge per the ESD test method specified in IEC 61000-4-2. The device measures 2.80 mm x 1.20 mm and is available in a SOT-143 package intended to be mounted directly onto an FR4 printed circuit board.The Bourns® device will meet IEC 61000-4-2 (ESD), IEC 61000-4-4 (EFT) and IEC 61000-4-5 (Surge) requirements.



Additional Information

Click these links for more information:

PRODUCT SELECTOR | TECHNICAL LIBRARY | INVENTORY | SAMPLES | CONTACT

Absolute Maximum Ratings (@ T_A = 25 °C Unless Otherwise Noted)

Parameter	Symbol	Value	Unit
Peak Pulse Current (t_p= 8/20 μs)	I_{PP}	13	A
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C
Forward Voltage (I_f= 15 mA, Pin 1-4)	V_f	1	V

Electrical and Thermal Characteristics (@ T_A = 25 °C Unless Otherwise Noted)

Parameter	Symbol	Value	Unit
Breakdown Voltage Minimum @ 2 mA [1]	V_{BR}	6.1	V
Working Peak Voltage [1]	V_{WM}	5.0	V
Clamping Voltage Maximum @ I_P = 5 A [2,4]	V_C	9.0	V
Clamping Voltage Maximum @ I_{PP} [2,4]	V_C	12.5 @ 13 A	V
Leakage Current @ V_{WM} [1]	I_D	1.0	μA
Capacitance Maximum between I/O Pins and Ground @ V_R = 0 V, f = 1 MHz [3]	C_{IN}	3	pF

Notes:
1. From Pin 4 to Pin 1.
2. See Pulse Wave Form.
3. Pin 1 (GND) connected to Ground, Pin 4 (REF) connected to 5 V.
4. I/O to GND, REF connected to 5 V and GND connected to Ground.

WARNING Cancer and Reproductive Harm - www.P65Warnings.ca.gov

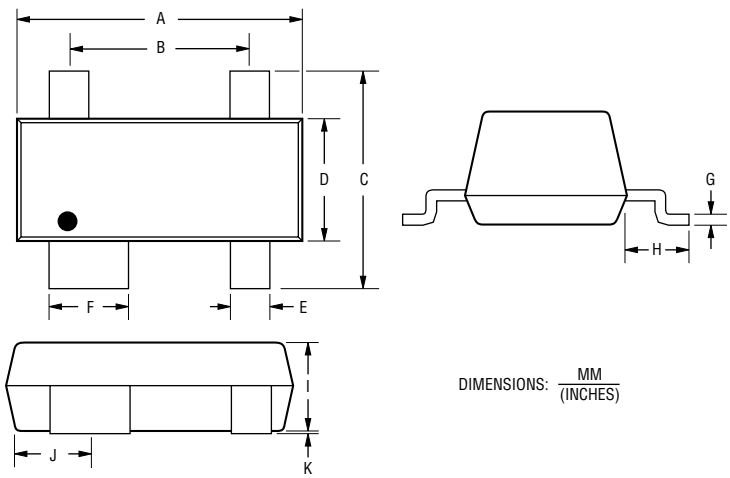
* RoHS Directive 2015/863, Mar 31, 2015 and Annex.
** Bourns considers a product to be "halogen free" if (a) the Bromine (Br) content is 900 ppm or less; (b) the Chlorine (Cl) content is 900 ppm or less; and (c) the total Bromine (Br) and Chlorine (Cl) content is 1500 ppm or less.

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Users should verify actual device performance in their specific applications.
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Product Dimensions

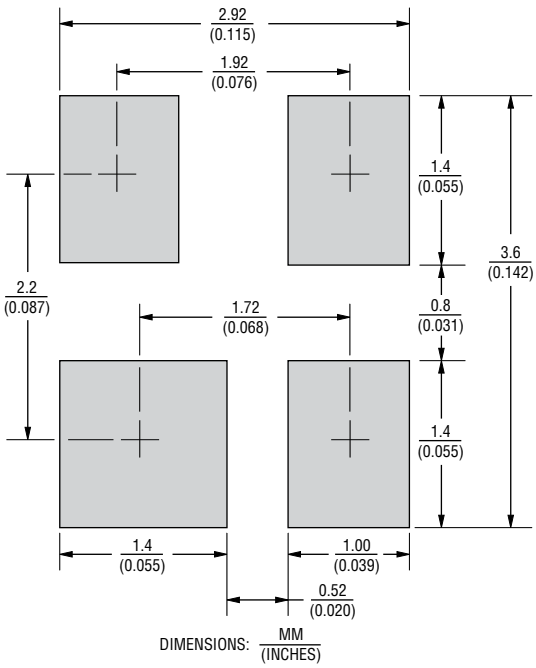
This is a molded JEDEC SOT-143 device. It has a flammability rating of UL 94V-0.
The dimensions for the packaged device are shown below.



Dimensions	
A	2.80 - 3.04 (0.110 - 0.12)
B	1.78 - 2.03 (0.070 - 0.080)
C	2.11 - 2.55 (0.083 - 0.100)
D	1.2 - 1.4 (0.047 - 0.055)
E	0.35 - 0.5 (0.014 - 0.020)
F	0.76 - 0.93 (0.030 - 0.037)
G	0.08 - 0.18 (0.003 - 0.007)
H	0.46 - 0.60 (0.018 - 0.024)
I	0.84 - 1.14 (0.033 - 0.045)
J	0.72 - 0.83 (0.028 - 0.033)
K	0.013 - 0.10 (0.0005 - 0.004)

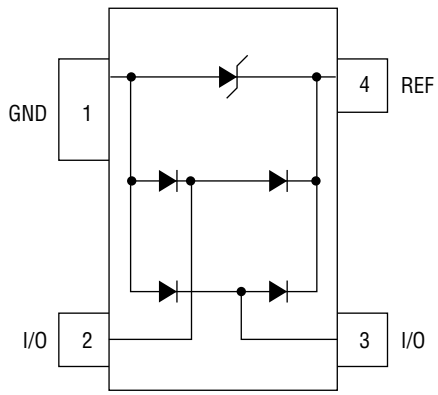
Recommended Pad Layout

This is the footprint recommended for this SOT-143 device.



Block Diagram

The device block diagram below includes the pin names and basic electrical connections associated with each channel.



Typical Part Marking

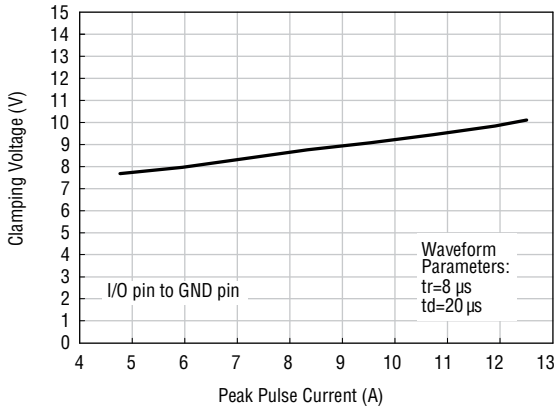
CD143A-SR05LC 5LC

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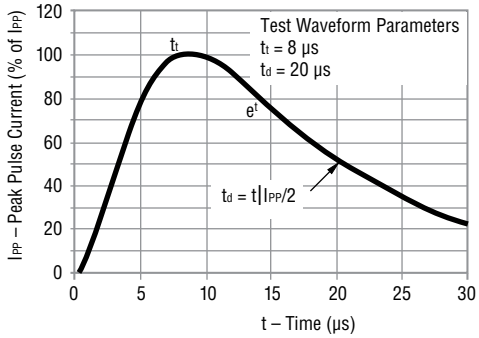
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Performance Graphs

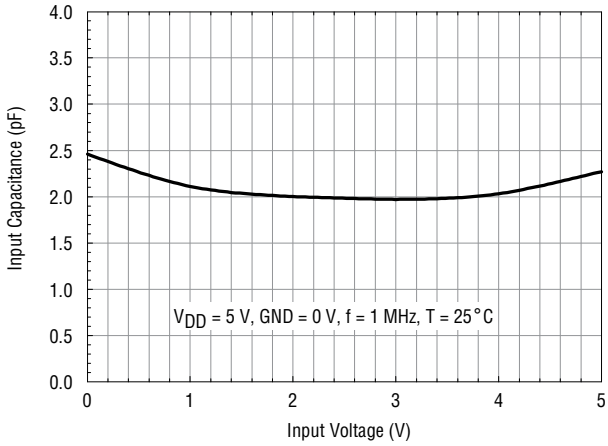
Typical Clamping Voltage vs. Peak Pulse Current



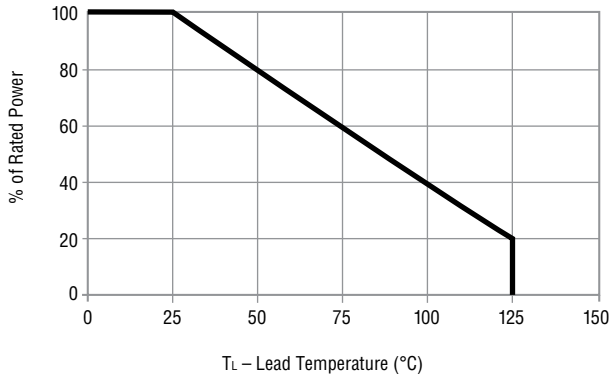
Pulse Wave Form



Typical Capacitance vs. Reverse Voltage



Power Derating Curve



How to Order

CD 143A - SR 05 LC

Common Code
Chip Diode

Package
143A = SOT-143

Model
SR = Steering Diode Array

Workint Peak Voltage
05 = 5.0 V_{WM} (Volts)

Capacitance
LC = Low Capacitance

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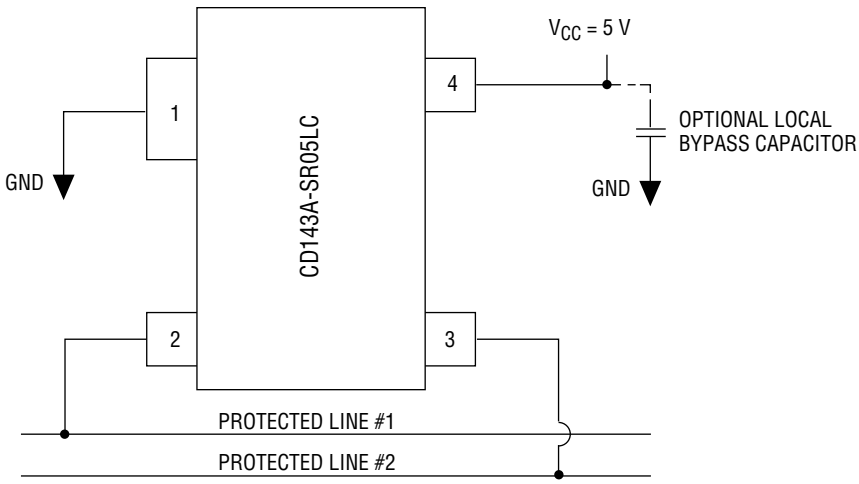
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Application Information

The Model CD143A-SR05LC is designed to protect two data lines against transient overvoltage events, as well as to limit the transient voltage on the 5 V supply line of the protected device.

Pin 1 must be connected to the local Ground used by the protected device and Pin 4 must be connected to the 5 V supply rail used by the protected device, as shown in the figure below. Under no circumstances should Pins 1 and 4 be left unconnected (floating).

To optimize the performance of the protection design, connections to the CD143A-SR05LC should be as short as possible. This will minimize the parasitic inductance of the printed circuit board traces. An optional 0.1 μF bypass chip capacitor can be added from Pin 4 to Ground to enhance the ESD performance of the design when the nearest bypass capacitor is a significant distance from the Model CD143A-SR05LC.

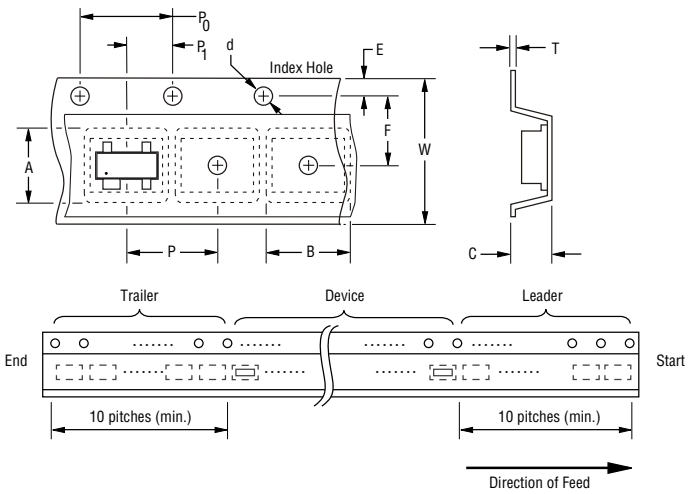


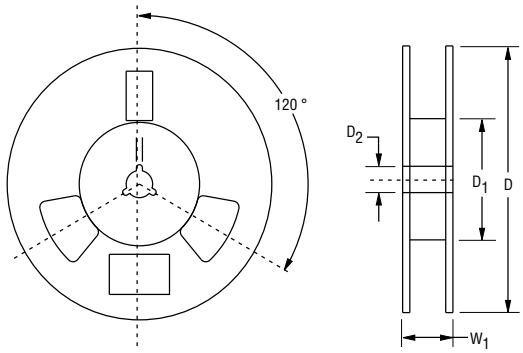
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Packaging Information

The surface mount product is packaged in an 8 mm x 4 mm tape and reel format per EIA-481 standard.





DIMENSIONS: MM / (INCHES)

Item	Symbol	SOT-143
Carrier Width	A	2.80 ± 0.15 (0.110 ± 0.006)
Carrier Length	B	3.25 ± 0.15 (0.128 ± 0.006)
Carrier Depth	C	1.25 ± 0.15 (0.049 ± 0.006)
Sprocket Hole	d	1.50 ± 0.10 (0.059 ± 0.004)
Reel Outside Diameter	D	178 ± 2 (7.008 ± 0.079)
Reel Inner Diameter	D_1	50.0 (1.969) MIN.
Feed Hole Diameter	D_2	13.0 ± 0.20 (0.512 ± 0.008)
Sprocket Hole Position	E	1.75 ± 0.10 (0.069 ± 0.004)
Punch Hole Position	F	3.50 ± 0.10 (0.138 ± 0.004)
Punch Hole Pitch	P	4.00 ± 0.10 (0.157 ± 0.004)
Sprocket Hole Pitch	P_0	4.00 ± 0.20 (0.157 ± 0.008)
Embossment Center	P_1	2.00 ± 0.10 (0.079 ± 0.004)
Overall Tape Thickness	T	0.20 ± 0.10 (0.008 ± 0.004)
Tape Width	W	8.00 ± 0.20 (0.315 ± 0.008)
Reel Width	W_1	14.4 (0.567) MAX.
Quantity per Reel	--	3,000

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